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High-Gain Coupled-Inductor Boost Converters Using Voltage-Doubling and Continuous Input Current Design

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Abstract

This paper proposes a family of high-efficiency DC-DC boost converters employing voltage-doubling coupled-inductor technology with a low component count. By varying the homonymous winding connections of the coupled inductor, three topologies are developed: parallel (PWCDVD-CLBC), series (SWCDVD-CLBC), and flipped-parallel (FPWCDVD-CLBC). These converters achieve high-voltage gain, continuous input current, and low-voltage stress across components. The PWCDVD-CLBC and FPWCDVD-CLBC configurations exhibit voltage gains proportional to the turn ratio, while the SWCDVD-CLBC shows an inverse relation, enabling reduced turn ratios. Detailed operational principles, mathematical analysis, and performance advantages are presented. A comparative evaluation demonstrates a higher voltage gain, realizes continuous input current, and has lower voltage stresses. The experimental results validate the theoretical analysis and confirm the feasibility and efficiency of the proposed designs.

Keywords: magnetically boost structure; high-voltage gain; continuous input current; low component count

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1. Introduction

Wireless charging systems have been extensively applied to electric vehicle batteries due to their contactless nature, safety, and convenience. Various DC/DC converter topologies have been developed to meet the demands of high-voltage gain and improved efficiency in renewable energy and electric vehicle applications [1]. However, conventional boost converters suffer from limited voltage gain and high-voltage stress on switching devices, which restricts their applicability in high step-up scenarios.

To address these limitations, Z-source converters (ZSCs) and Y-source were introduced, offering an impedance network capable of boosting voltage [2–4]. However, ZSCs typically suffer from discontinuous input current and limited gain, which has led to the development of quasi-Z-source (QZSC) and enhanced Z-source networks [5–8]. While these offer better performance, they often involve increased component count and complexity.

By introducing switched-inductor cells to realize four inductors' parallel charging and serial discharging, the converter [9] largely improves boost ability. By adding switched-impedance networks, an enhanced Z-source structure is presented in [10] to increase boost ability, which results in larger device counts and system losses. Therefore, converters based on coupled-inductor boost technology are presented for a higher voltage gain but utilizing a lesser component count. Magnetically coupled structures have gained attention due to their ability to combine multiple inductors and achieve a higher voltage gain. The

Δ-source converter [11] realizes high-voltage gain by utilizing a three-winding magnetically structured, two capacitors, and two diodes. Different from converters [11], Γ-source and flipped Γ-source converters [12,13] have an inversely proportional relation; namely, a low turn ratio can help produce a high boost ability. A Y-source converter with a three-winding coupled-inductor cell is reported in [14], which has more freedom in winding matches.

Figure 1 shows the topologies of the Δ-source, Γ-source, and Y-source converters. The Δ-source, Γ-source, and Y-source converters utilize multi-winding coupled-inductor cells to achieve enhanced performance [11–14], though many of them still suffer from discontinuous input current and parasitic-induced losses. Subsequently, a three-winding Π-source converter [15] realizes a stronger boost ability, but its voltage gain is heavily affected by the parasitic resistances on passive components and switching devices. Although the converters above enhance the output performance of systems, input currents are discontinuous, which is not beneficial to the input power source, and is sensitive to passive component parasitics.

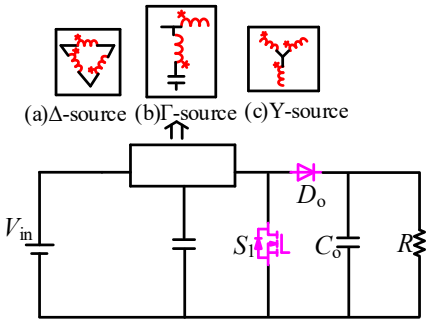


Figure 1. Δ-source, Γ-source, and Y-source converters. (* represents the homonymous end of the coupling inductance).

Through varying the charging and discharging paths of the Z-source converter, quasi-Z-source converters (QZSCs) [5] realize the continuous input current. Subsequently, enhanced QZSCs [6–8] are reported to produce a higher voltage gain by introducing multiple parallel charging paths. Next, some high-performance coupled-inductor converters, such as the T-source [16], LCCT-Z-source [17], quasi-Y-source [18], modified-Y-source [19], quasi-Γ-source [20], and switched-coupled-inductor converters [21], are presented to further optimize the topology performance. Figure 2 shows the topologies of the switched-inductor and the quasi-switched-inductor converters. However, these converters use multiple diodes, one individual inductor, one coupled-inductor cell, and two capacitors, which will increase system losses to a great degree. Quasi-switched-boost impedance networks are discussed in references [22–26] and have been proposed to further improve gain and continuity of the input current; however, these approaches often introduce multiple diodes, additional switches, and complex control requirements, thereby increasing overall system loss and design costs. The corresponding comparison is shown in Table 1.

In summary, there remains a need for converter topologies that simultaneously achieve a high-voltage gain, continuous input current, reduced component count, and low-voltage stress. In response, this paper introduces a novel family of voltage-doubling coupled-inductor boost converters with simplified structures and enhanced performance, addressing the limitations found in prior designs. By utilizing different winding homonymous end connections of coupled-inductor cells, three converters are formed and have these performance advantages at the same time. Regarding some differences for the proposed topologies, the voltage gain and turn ratio of the PWCDVD-CLBC and FPWCDVD-CLBC have proportional relations, and yet the SWCDVD-CLBC has inversely proportional relations.

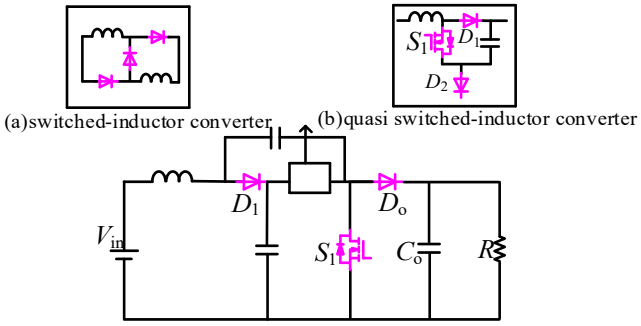


Figure 2. Switched-inductor converter and quasi-switched-inductor converter.

Table 1. Comparison table of converters.

Topology	G	Component Count	Input Current
Z-source converter	$\frac{1}{1-2D}$	4	Discontinuous
Quasi-switched boost converter	$\frac{1}{1-3D}$	11	Continuous
Modified-Y-source network	$\frac{1+KD}{1-D}$	12	Continuous
Δ-Source network	$\frac{1}{1-K_{\triangle}D}$	9	Discontinuous
Y-source impedance network	$\frac{1}{1-K_{Y}D}$	8	Discontinuous
Extended Z-source	$\frac{1+KD}{1-(1+n_{TZ})D}$	10	Discontinuous
Π-source impedance network	$\frac{1}{1-K_{\Pi}D}$	7	Discontinuous
extended boost trans-Z-source inverter	$\frac{1}{(1-2D)(1-D)^2}$	9	Continuous
Switched-inductor-Z-source	$\frac{1+D}{1-3D}$	13	Continuous
L-Z-source inverter	$\frac{1+D}{1-D}$	5	Continuous
Trans-switched boost inverters	$\frac{1+n_S D}{1-(2+n_S)D}$	6	Discontinuous
Quasi-Y-source inverter	$\frac{1}{1-\delta D}$	7	Continuous
LCCT Z-source	$\frac{m+1}{2-2\left(1+\frac{n_2}{n_3}\right)D}$	8	Continuous
Improved trans-Z-source inverter	$\frac{1}{1-(2+n)D}$	6	Continuous
Three-winding switched-coupled inductor (PSCL)	$\frac{\frac{1+n_1}{n_1}}{1-\left(1+\frac{1+n_1+n_2}{n_1}\right)D}$	9	Continuous

2. Proposed Topologies and Analysis

2.1. Proposed Topologies

Figure 3 provides the topology of the ZSC. It can be seen that the ZSC can realize a boosted performance by the X-source impedance network. When the switch is on, two capacitors charge two inductors. When the switch is off, the two inductors and the input source discharge to loads and capacitors. However, the input source is lower than the capacitor voltage and results in discontinuous input current when the switch is on.

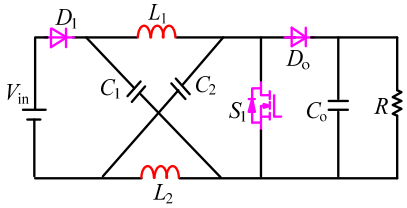


Figure 3. Z-source converter.

Inspired by the operation principle of the ZSC and combining magnetically boost technology, a family of voltage-double coupled-inductor boost DC/DC converters is proposed

in Figure 4. The proposed converters directly utilize the input source to charge the coupled-inductor cell and construct a voltage-double circuit path with diode-winding-capacitor technology. The proposed three converters realize a continuous input current, have a lower component count, and obtain a higher boost ability. Different winding homonymous end connections form different topologies, respectively, called PWCDVD-CLBC in Figure 4a, FPWCDVD-CLBC in Figure 4b, and SWCDVD-CLBC in Figure 4c. The voltage gain and turn ratio of the PWCDVD-CLBC and FPWCDVD-CLBC exhibit a proportional relation, and yet the SWCDVD-CLBC has an inversely proportional relation. Therefore, the proposed three converters must produce different outcomes. (* represents the homonymous end of the coupling inductance).

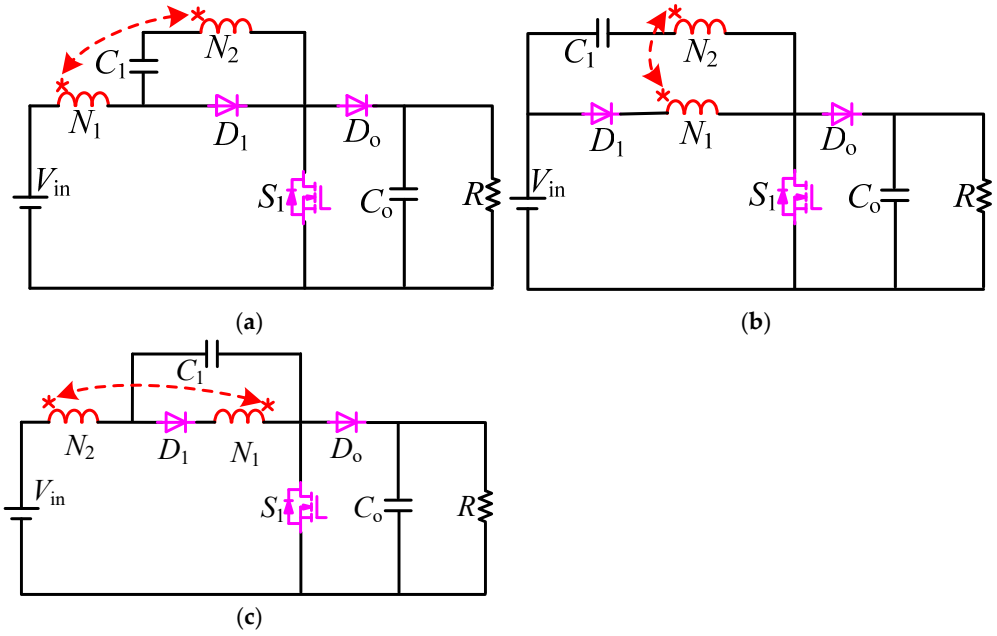


Figure 4. Proposed converters: (**a**) PWCDVD-CLBC, (**b**) FPWCDVD-CLBC, and (**c**) SWCDVD-CLBC.

In this section, the operational status of the three proposed converters will be analyzed individually. Figure 5 shows the theoretical waveforms of the related components in one cycle of the topology in Figure 4, and Figure 5 shows the equivalent circuits when the switch is on or off.

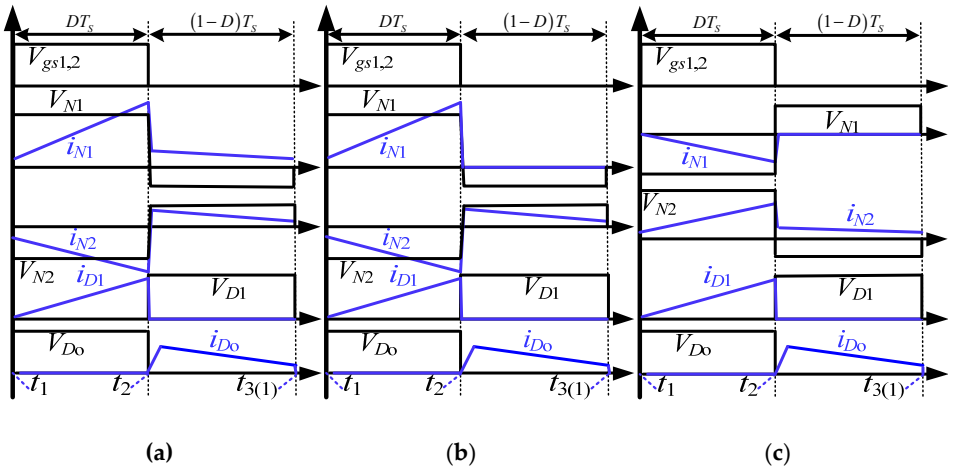


Figure 5. Theoretical waveforms: (**a**) PWCDVD-CLBC, (**b**) FPWCDVD-CLBC, and (**c**) SWCDVD-CLBC. (V_{gs} is the switch pulse trigger signal, V_{N1}/I_{N1} is the primary side of the coupling inductance voltage/current, V_{N2}/I_{N2} is the secondary side of the coupling inductance voltage/current, V_{D1}/I_{D1} is the diode voltage/current, and V_{Do}/I_{Do} is the diode voltage/current.).

2.1.1. PWCDVD-CLBC

As described in Figure 6a, the input source supplies power for the windings N_1, magnetizing inductance L_M, and the leakage inductance L_k by diode D_1 and switch S_1 when the switch is on. Meanwhile, wind N_2 charges the capacitor C_1 through diode D_1. As described in Figure 6b, the input source V_{in}, the whole coupled-inductor structure, and capacitor C_1 supply the power for the loads when switch S_1 is off.

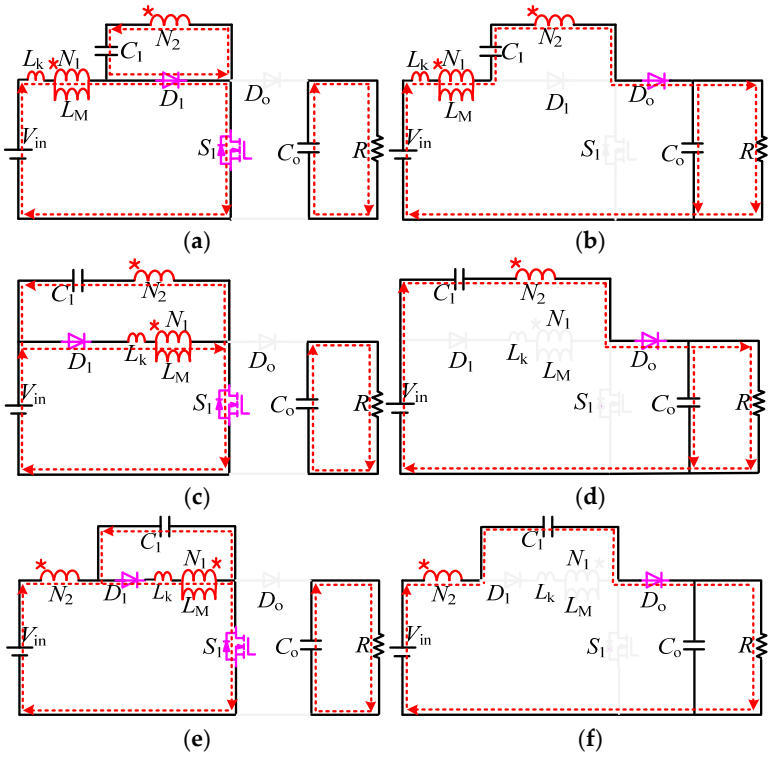


Figure 6. Equivalent circuits of different operation states: (**a**,**c**,**e**) switch is on and (**b**,**d**,**f**) switch is off. (* represents the homonymous end of the coupling inductance).

2.1.2. FPWCDVD-CLBC

As described in Figure 6c, the input source supplies power for windings N_1, magnetizing inductance L_M, and leakage inductance L_k by diode D_1 and switch S_1 when the switch is on. Meanwhile, the whole coupled-inductor structure charges capacitor C_1 through diode D_1. As described in Figure 6d, the input source V_{in}, winding N_2, and capacitor C_1 supply the power for the loads when switch S_1 is off. The relevant parameters and symbols are shown in Table 2.

Table 2. Parameters and symbols.

Symbol	Description	Unit
V_{in}	Input voltage	V
C_o	Output capacitor voltage	V
D_1	Diode	-
L_K	Leakage inductance	H
L_M	Magnetizing inductance	H
C_1	Intermediate capacitor	F
R	Load resistance	Ω
$N_{1/2}$	Primary/secondary edge	-
S_1	Switch	-

2.1.3. SWCDVD-CLBC

As described in Figure 6e, the input source supplies power for the whole coupled-inductor structure through the diode D_1 and switch S_1 when the switch is on. Meanwhile, the wind N_1 and leakage inductance L_k thus charge capacitor C_1 through diode D_1. As described in Figure 6f, the input source V_{in}, winding N_2, and capacitor C_1 supply the power for the loads when switch S_1 is off.

In summary, the proposed converters can achieve continuous input current. Additionally, by forming a voltage-doubling circuit, these topologies can significantly enhance the voltage gain with a low component count.

2.2. Math Derivation and Performance Analysis

The detailed math derivation and performance analysis will be given out as follows. The following definitions are given out. Leakage inductance L_k and magnetizing inductance L_M have the following expressions:

$$g = L_M/(L_M + L_k) \tag{1}$$

where V_{in} is the input voltage, D is the shoot-through duty ratio, n is the turn ratio of the coupling inductance, V_{C1} is the voltage of capacitor C_1, and V_o is the output voltage. V_{N1S}, V_{N1N}, V_{N2S}, V_{N2N}, V_{LkS}, and V_{LkN} are, respectively, the voltages of the windings (N_1 and N_2) and leakage inductance when the switch is on or off.

2.2.1. PWCDVD-CLBC

When the switch is on, the following theoretical relations can be obtained.

$$V_{in} - V_{LkS} - V_{N1S} = 0 \tag{2}$$

$$V_{N2S} = nV_{N1S} \tag{3}$$

$$V_{C1} = V_{N2S} \tag{4}$$

When the switch is off, the following theoretical relations can be obtained.

$$V_{in} - V_{LkN} - V_{N1N} - V_{N2N} + V_{C1} = V_o \tag{5}$$

$$V_{N2N} = nV_{N1N} = ngV_{LkN}/(1-g) \tag{6}$$

$$V_{D1} = V_{C1} - V_{N2N} \tag{7}$$

Therefore, the output voltage is provided as follows.

$$V_o = \frac{(ng+1)V_{in}}{(1-D)} \tag{8}$$

When g = 1, the voltage gain and voltage stresses of diode D_1 and capacitor C_1 are provided as follows.

$$\begin{cases} G = \frac{n+1}{1-D} \\ V_{C1} = nV_{in} \\ V_{D1} = \frac{nV_{in}}{1-D} \end{cases} \tag{9}$$

2.2.2. FPWCDVD-CLBC

When the switch is on, the following theoretical relations can be obtained.

$$V_{in} - V_{N1S} - V_{LkS} = 0 \tag{10}$$

$$V_{N2S} = nV_{N1S} \tag{11}$$

$$V_{C1} = V_{N2S} - V_{N1S} - V_{LkS} \tag{12}$$

When the switch is off, the following theoretical relations can be obtained.

$$V_{\text{in}} + V_{C1} - V_{N2N} = V_{\text{o}} \tag{13}$$

$$V_{N2N} = nV_{N1N} = nV_{LkS}g/(1-g) \tag{14}$$

Therefore, the output voltage is provided as follows.

$$V_{\text{o}} = \frac{Dng^2 + (1-D)(ng+g-1)}{(1-D)g} V_{\text{in}} \tag{15}$$

When g = 1, the voltage gain and voltage stresses of diode D_1 and capacitor C_1 are provided as follows.

$$\begin{cases} G = \frac{n}{1-D} \\ V_{C1} = (n-1)V_{\text{in}} \\ V_{D1} = \frac{(n-1)V_{\text{in}}}{1-D} \end{cases} \tag{16}$$

2.2.3. SWCDVC-CLBC

When the switch is on, the following theoretical relations can be obtained.

$$V_{\text{in}} - V_{N2S} + V_{N1S} + V_{LkS} = 0 \tag{17}$$

$$V_{N2S} = nV_{N1S} \tag{18}$$

$$V_{C1} = V_{N1S} \tag{19}$$

When the switch is off, the following theoretical relations can be obtained.

$$V_{\text{in}} + V_{C1} - V_{N2N} - V_{LkN} = V_{\text{o}} \tag{20}$$

$$V_{N2N} = nV_{N1N} = nV_{LkN}g/(1-g) \tag{21}$$

$$V_{D1} = V_{C1} - V_{N1N} \tag{22}$$

Therefore, the output voltage is given out.

$$V_{\text{o}} = \frac{V_{\text{in}} n(1-D+Dg)}{(1-2g+n)(1-D)} \tag{23}$$

When g = 1, the voltage gain and voltage stresses of diode D_1 and capacitor C_1 are provided as follows.

$$\begin{cases} G = \frac{n}{(n-1)(1-D)} \\ V_{C1} = \frac{V_{\text{in}}}{n-1} \\ V_{D1} = \frac{V_{\text{in}}}{(n-1)(1-D)} \end{cases} \tag{24}$$

Figure 7a,b illustrates the voltage gain curves that consider various coupling coefficients and turn ratios for the proposed three topologies. As described in Figure 7a,b, the voltage gain can be regulated by varying the switch-duty ratio, and it rises as the coupling coefficient rises. Voltage gains of the PWCDVD-CLBC and FPWCDVD-CLBC are directly proportional to the turn ratio, yet the SWCDVD-CLBC is inversely proportional to the turn ratio. Figure 7c,d, respectively, describes the normalized voltage stresses of capacitor C_1 and diode D_1 under various turn ratios for the proposed three converters.

As described in Figure 7c,d, the normalized voltage stresses of capacitor C_1 and diode D_1 of the PWCDVD-CLBC and FPWCDVD-CLBC have a proportional relation with the turn ratio, and then the normalized voltage stresses of capacitor C_1 and diode D_1 of the SWCDVD-CLBC have an inversely proportional relation with the turn ratio.

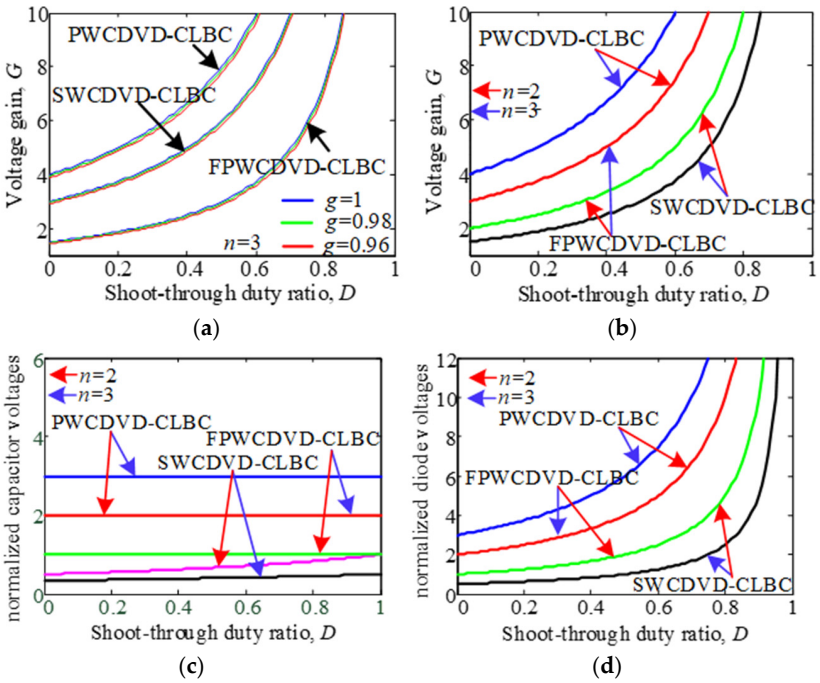


Figure 7. Performance analysis: (**a**) voltage gain with various coupling coefficients, (**b**) voltage gain with various turn ratios, (**c**) diode voltage, and (**d**) capacitor voltage.

2.3. Parameter Design and Performance Comparison

The following part shows the design of the coupled-inductor cell and capacitors for the proposed three topologies. Inductor values of primary and secondary winding are typically designed based on the principle that input power equals output power.

$$P_{\text{in}} = V_{\text{in}}\bar{i}_{\text{in}} = GV_{\text{in}}\bar{i}_{\text{out}} = P_{\text{out}} \tag{25}$$

where i_{in} is the average input current, the equation for primary and secondary windings, input voltage, shoot-through duty ratio, and switch frequency is given. i_{out} is the average output current; this is the equation for voltage gain and loads.

The voltage fluctuation of the capacitors is mainly caused by the charging and discharging currents.

$$C\frac{dV}{dt} = i \tag{26}$$

where C is the capacitor value, i is the current across the capacitor C, and dV is the voltage fluctuation of the capacitor in this interval dt.

The coupled-inductor cell and capacitors of the proposed three topologies can be designed separately, as follows.

2.3.1. PWCDVD-CLBC

According to the operation states in Figure 6a,b, i_{in} and i_{out} are provided as follows.

$$\begin{cases} \bar{i}_{\text{in}} = \frac{V_{\text{in}}DT_s(1-D+nD)}{2nL_{N1}} \\ \bar{i}_{\text{o}} = \frac{V_{\text{in}}(1+n)}{(1-D)R} \end{cases} \tag{27}$$

where R is the load, and T_s is the switch cycle. Therefore, the inductor values of the primary and secondary windings are provided as follows.

$$L_{N1} = \frac{D(1-D)^2(1-D+nD)RT_s}{2(1+n)^2 n} \tag{28}$$

$$L_{N2} = \frac{nD(1-D)^2(1-D+nD)RT_s}{2(1+n)^2} \tag{29}$$

The capacitor C_1 is designed according to Equation (30).

$$\frac{V_{\text{in}}D^2T_s^2}{nL_{N1}\Delta V_{C1}} \leq C_1 \tag{30}$$

where C_1 is the value of capacitor C_1, and Δv_{C_1} is the permitted voltage ripple of capacitors C_1.

2.3.2. FPWCDVD-CLBC

According to the operation states in Figure 6c,d, $\bar{i}_{\text{in}}$ and $\bar{i}_{\text{out}}$ are provided as follows.

$$\begin{cases} \bar{i}_{\text{in}} = \frac{V_{\text{in}}D^2T_s}{2L_{N1}} \\ \bar{i}_{\text{o}} = \frac{nV_{\text{in}}}{(1-D)R} \end{cases} \tag{31}$$

Therefore, the inductor values of the primary and secondary windings are provided as follows.

$$L_{N1} = \frac{D^2T_s(1-D)^2R}{2n^2} \tag{32}$$

$$L_{N2} = \frac{D^2T_s(1-D)^2R}{2} \tag{33}$$

The capacitor C_1 is designed according to the Equation (34).

$$\frac{V_{\text{in}}D^2T_s^2}{nL_{N1}\Delta V_{C1}} \leq C_1 \tag{34}$$

2.3.3. SWCDVD-CLBC

According to the operation states in Figure 6e,f, $\bar{i}_{\text{in}}$ and $\bar{i}_{\text{out}}$ are provided as follows.

$$\begin{cases} \bar{i}_{\text{in}} = \frac{V_{\text{in}}DT_s(n-1+D)}{2(n-1)n^2L_{N1}} \\ \bar{i}_{\text{o}} = \frac{nV_{\text{in}}}{(n-1)(1-D)R} \end{cases} \tag{35}$$

Therefore, the inductor values of the primary and secondary windings are provided as follows.

$$L_{N1} = \frac{DT_s(n-1+D)(n-1)(1-D)^2R}{2n^4} \tag{36}$$

$$L_{N1} = \frac{DT_s(n-1+D)(n-1)(1-D)^2R}{2n^2} \tag{37}$$

The capacitor C_1 is designed according to the Equation (38).

$$\frac{V_{\text{in}}D^2T_s^2}{(n-1)L_{N1}\Delta V_{C1}} \leq C_1 \tag{38}$$

2.4. Comparative Analysis

A comparative analysis was performed among the Δ-source [11], modified-Y-source [19], high-gain quasi-switched [24], and the proposed three converters. The voltage gain, maximum capacitor voltage, maximum diode voltage, shoot-through peak current, component count, and input current state of the converters above are listed in Table 3.

The proposed converters use a lower component count than other converters [11,19,24]. As we can see, their input currents are continuous. In addition, the proposed impedance structure can achieve a high boost effect with a small switch-duty ratio. The specific parameters for comparison are shown below.

The input current of the converter [11] is discontinuous. Still, the converter [19] is continuous, and the converter [24] and the proposed converters are also continuous. The proposed topologies utilize the fewest components while maintaining continuous input current, which is in contrast to other converters [11,19,24].

Parameter comparisons among the converters [11,19,24] and the proposed converters are made. The comparison of voltage gain is shown in Figure 8a. Figure 8a demonstrates that the proposed three converters achieve a higher voltage gain. Voltage gains of the proposed PWCDVD-CLBC and FPWCDVD-CLBC have a positively proportional relationship with the turn ratio, yet the proposed SWCDVD-CLBC has an inversely proportional relationship.

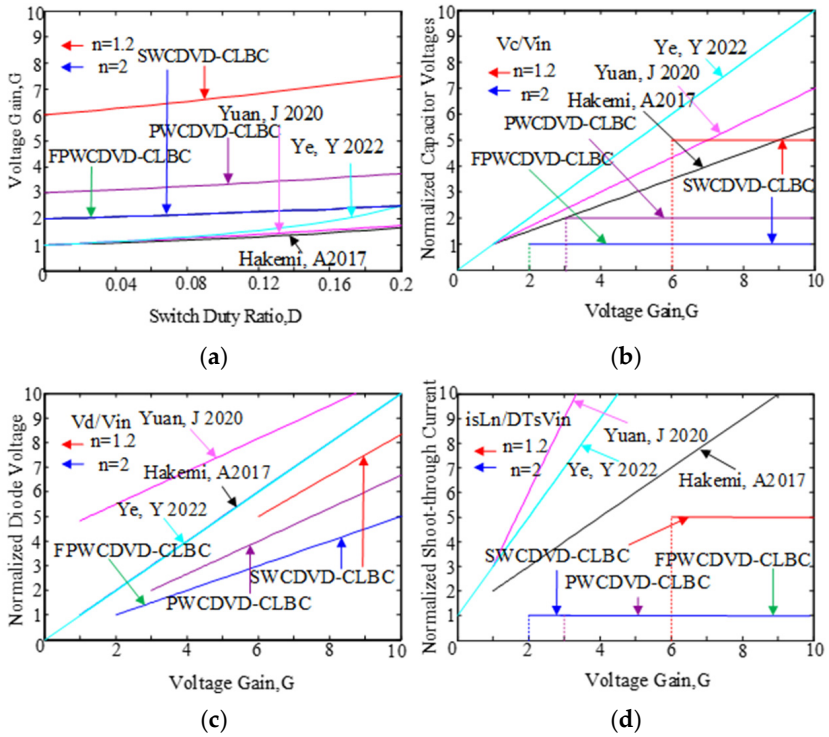


Figure 8. Comparative curves of boost ability, device voltages, and current: (**a**) voltage gain, (**b**) capacitors, (**c**) diode voltage, and (**d**) shoot-through currents [11,19,24].

Figure 8b provides comparative curves of normalized capacitor voltage stress. The proposed three converters have the lowest voltage stress across capacitors when the turn ratio is 2, compared to other converters [11,19,24]. When the turn ratio is 1.2, the capacitor voltage of the proposed SWCDVD-CLBC is lower than the converters [24] and higher than converters [11,19]. However, as the voltage gain gradually increases, when the voltage gain reaches 7, we can see that the SWCDVD-CLBC is lower than converters [19,24].

Figure 8c illustrates the comparative curves of the normalized diode voltage. It is clear that the diode voltage stresses for the proposed converters are lower than those of converters [11,19,24]. The comparison of normalized shoot-through current is shown in

Figure 8d. The proposed impedance networks have a lower shoot-through current than those of the impedance networks [11,19,24].

Table 3. Parameter comparisons.

Parameters	Δ-Source Network [11]	Modified-Y-Source Network [19]	Quasi-Switched Network [24]	PWCDVD-CLBC	FPWCDVD-CLBC	SWCDVD-CLBC
G	$\frac{1}{1-K_{\triangle}D}$	$\frac{1+KD}{1-D}$	$\frac{1}{1-3D}$	$\frac{n+1}{1-D}$	$\frac{n}{1-D}$	$\frac{n}{(n-1)(1-D)}$
$V_{C\text{-max}}$	$\frac{(1-D)V_{in}}{1-K_{\triangle}D}$	$\frac{(1+KD-D)Vin}{1-D}$	$\frac{V_{in}}{1-3D}$	nV_{in}	$(n-1)V_{in}$	$\frac{V_{in}}{n-1}$
$V_{D\text{-max}}$	$\frac{(K_{\triangle}-1)V_{in}}{1-K_{\triangle}D}$	$\frac{(K+G)V_{in}}{(1+K)}$	$\frac{V_{in}}{1-3D}$	$\frac{nV_{in}}{1-D}$	$\frac{(n-1)V_{in}}{1-D}$	$\frac{V_{in}}{(n-1)(1-D)}$
Shoot-through peak current	$\frac{(1-D)K_{\triangle}DT_sV_{in}}{(1-K_{\triangle}D)L_m}$	$\frac{(2KG-K+1)DT_sV_{in}}{\left(\frac{N_3}{N_2}-1\right)L_{N2}}$	$\frac{(3-3D)DT_sV_{in}}{(1-3D)L_1}$	$\frac{DT_sV_{in}}{L_{N1}}$	$\frac{DT_sV_{in}}{L_{N1}}$	$\frac{DT_sV_{in}}{(n-1)L_{N1}}$
Component count	9	12	11	5	5	5
Input current	Discontinuous	Continuous	Continuous	Continuous	Continuous	Continuous
Cost	Medium	High	Medium	Low	Low	Low

Based on the above comparison, the three proposed impedance networks can achieve a higher voltage gain with fewer components while exhibiting lower voltage stress in a smaller range through the switch-duty ratio, thereby reducing energy loss.

2.5. Voltage Gain Analysis

2.5.1. PWCDVD-CLBC

The influence of inductance resistance on the voltage gain of the PWCDVD-CLBC is analyzed as follows in Figure 9. R_{N1} and R_{N2} represent the conduction resistances of the windings (N_1 and N_2, * represents the homonymous end of the coupling inductance).

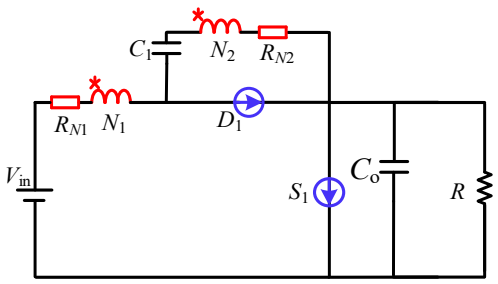


Figure 9. Simplified analysis of PWCDVD-CLBC inductance resistance.

From the above circuit diagram analysis, we have:

$$\begin{gathered} V_{in} - \bar{i}_{in}R_{N1} - V_{N1S} = 0 \\ V_{N2S} = nV_{N1S} \\ V_{C1} + \bar{i}_{in}R_{N2} - V_{N2S} = 0 \end{gathered} \tag{39}$$

$$\begin{gathered} V_{in} - \bar{i}_{in}(R_{N1} + R_{N2}) + V_{C1} - V_{N1N} - V_{N2N} = V_O \\ V_{N2N} = nV_{N1N} \end{gathered} \tag{40}$$

Due to the existence of inductance resistance, there is a voltage drop in the actual value of V_{N1}. At the same time, there is also a voltage drop between V_{N2} and V_{C1} due to electromagnetic induction. Therefore, from this, we obtain the following image in Figure 10.

2.5.2. FPWCDVD-CLBC

The influence of inductance resistance on the voltage gain of the FPWCDVD-CLBC is analyzed as follows in Figure 11. R_{N1} and R_{N2} represent the conduction resistances of the windings (N_1 and N_2, * represents the homonymous end of the coupling inductance).

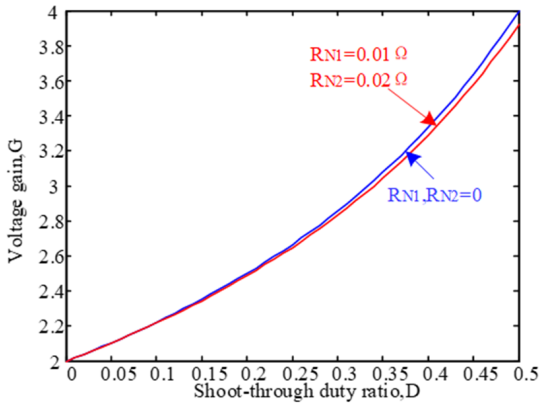


Figure 10. Influence of inductance resistance on PWCDVD-CLBC voltage gain.

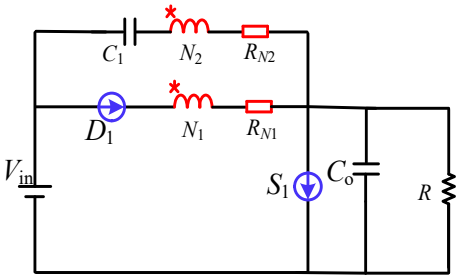


Figure 11. Simplified analysis of FPWCDVD-CLBC inductance resistance.

From the above circuit diagram analysis, we have:

$$\begin{gathered} V_{in} - \bar{i}_{in} R_{N1} - V_{N1S} = 0 \\ V_{N2S} = n V_{N1S} \\ V_{C1} = V_{N2S} - \bar{i}_{in}(R_{N1} + R_{N2}) - V_{N1S} \end{gathered} \tag{41}$$

$$\begin{gathered} V_{\text{in}} + V_{C1} - V_{N2N} - \bar{i}_{in} R_{N2} = V_{\text{o}} \\ V_{N2N} = n V_{N1N} \end{gathered} \tag{42}$$

Due to the existence of inductance resistance, when the switch is on, because of the inductive impedance on N_1, the current of N_1 decreases. The induced electromotive force of N_2 is generated due to electromagnetic induction. At the same time, the energy stored in C_1 is reduced due to the impedance of N_2, resulting in a decrease in voltage gain. The simulation is shown in Figure 12.

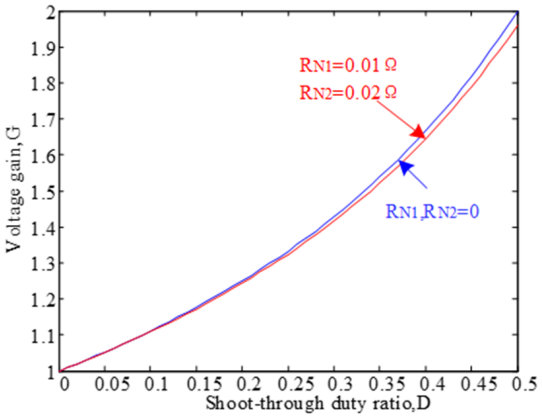


Figure 12. Influence of inductance resistance on FPWCDVD-CLBC voltage gain.

2.5.3. SWCDVD-CLBC

The influence of inductance resistance on the voltage gain of the SWCDVD-CLBC is analyzed as follows in Figure 13. R_{N1} and R_{N2} represent the conduction resistances of the windings (N_1 and N_2, * represents the homonymous end of the coupling inductance).

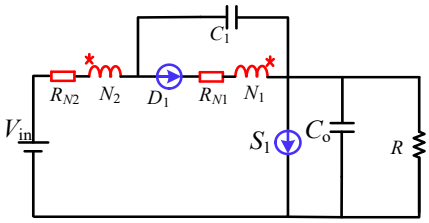


Figure 13. Simplified analysis of SWCDVD-CLBC inductance resistance.

From the above circuit diagram analysis, we have:

$$\begin{gathered} V_{\text{in}} - V_{N2S} + V_{N1S} - i_{N1}R_{N1} - i_{N2}R_{N2} = 0 \\ V_{N2S} = nV_{N1S} \\ V_{C1} = V_{N1S} - i_{N1}R_{N1} \end{gathered} \tag{43}$$

$$\begin{gathered} V_{\text{in}} + V_{C1} - V_{N2N} - i_{\text{N2}}R_{N2} = V_{\text{o}} \\ V_{N2N} = nV_{N1N} \end{gathered} \tag{44}$$

When the switch is on, due to the existence of inductance resistance, the inductive impedance on L_{N1} and L_{N2} will consume some energy, resulting in a voltage drop. At the same time, when the switch is off—because the inductance impedance on N_2 causes the current to drop—the stored energy of the C_1 capacitor will drop, and then the voltage gain will drop. The simulation is shown in Figure 14.

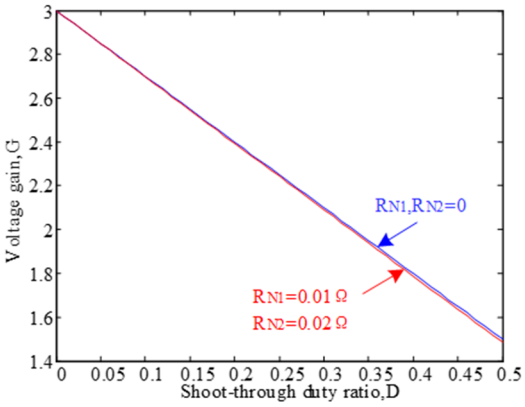


Figure 14. Influence of inductance resistance on SWCDVD-CLBC voltage gain.

2.6. Efficiency Calculation

Loss models for the proposed three converters are, respectively, described in Figure 15. The relevant efficiency calculation is given as follows. R_{N1}, $R_{N2,}$ and R_{C1} represent the conduction resistances of the windings (N_1 and N_2) and capacitor C_1. V_{SD} represents the conduction voltage drop of diode D_1 and switch S_1.

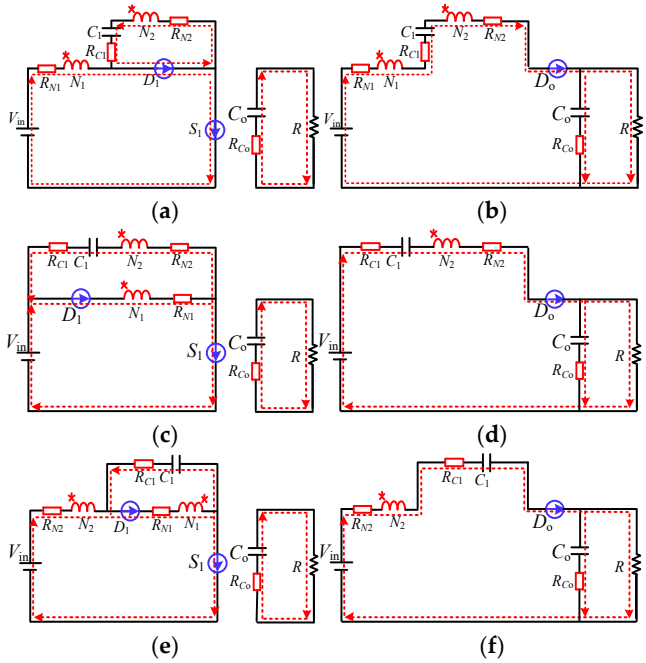


Figure 15. Loss models for proposed converters: (**a**,**b**) PWCDVD-CLBC, (**c**,**d**) FPWCDVD-CLBC, and (**e**,**f**) SWCDVD-CLBC. (* represents the homonymous end of the coupling inductance).

2.6.1. PWCDVD-CLBC

The losses of the capacitor C_1, switch S_1, diode D_1, and coupled-inductor cell are provided as follows.

$$P_{C-loss} = I_{C1}^2 R_{C1} = \frac{V_{\text{in}}^2 D^2 T_s^2 [1-(n+1)D]^2 R_{C1}}{n^2 L_{N1}^2} \tag{45}$$

$$P_{S-loss} = I_S V_{SD} = \frac{D^2 T_s V_{\text{in}} V_{SD}}{2L_{N1}} \tag{46}$$

$$P_{D-loss} = I_{D1}\, V_{SD} = \frac{V_{\text{in}} D T_s (1-D+nD) V_{SD}}{2nL_{N1}} \tag{47}$$

$$\begin{aligned} P_{CL-loss} &= I_{N1}^2 R_{N1} + I_{N2}^2\, R_{N2} \\ &= \frac{V_{\text{in}}^2 D^2 T_s^2 [(1-D+nD)^2 R_{N1} + 4(1-nD-D)^2 R_{N2}]}{4n^2 L_{N1}^2} \end{aligned} \tag{48}$$

Therefore, efficiency is provided as follows.

$$\eta = \frac{P_{\text{in}} - P_{C-loss} - P_{S-loss} - P_{D-loss} - P_{CL-loss}}{P_{\text{in}}} \tag{49}$$

where P_{in} is input power, calculated as follows.

$$P_{\text{in}} = \frac{V_{\text{in}}^2 D T_s (1-D+nD)}{2nL_{N1}} \tag{50}$$

2.6.2. FPWCDVD-CLBC

The losses of the capacitor C_1, switch S_1, diode D_1, and coupled-inductor cell are provided as follows.

$$P_{C-loss} = I_{C1}^2 R_{C1} = \frac{V_{\text{in}}^2 D^4 T_s^2 R_{C1}}{L_{N1}^2} \tag{51}$$

$$P_{S-loss} = I_S V_{SD} = \frac{V_{\text{in}} D^2 T_s V_{SD}}{2L_{N1}} \tag{52}$$

$$P_{D-loss} = I_{D1}\, V_{SD} = \frac{V_{\text{in}} D^2 T_s V_{SD}}{2L_{N1}} \tag{53}$$

$$P_{CL-loss} = I_{N1}^2 R_{N1} + I_{N2}^2\, R_{N2} = \frac{V_{\text{in}}^2 D^4 T_s^2 (R_{N1} + 4R_{N2})}{4L_{N1}^2} \tag{54}$$

Therefore, efficiency is provided as follows.

$$\eta = \frac{P_{\text{in}} - P_{C-loss} - P_{S-loss} - P_{D-loss} - P_{CL-loss}}{P_{\text{in}}} \tag{55}$$

where P_{in} is input power, calculated as follows.

$$P_{\text{in}} = \frac{V_{\text{in}}^2 D^2 T_s}{2L_{N1}} \tag{56}$$

2.6.3. SWCDVD-CLBC

The losses of the capacitor C_1, switch S_1, diode D_1, and coupled-inductor cell are provided as follows.

$$P_{C-loss} = I_{C1}^2 R_{C1} = \frac{V_{\text{in}}^2 D^2 T_s^2 (n-1)^2 (1-D)^2 R_{C1}}{(n-1)^2 n^4 L_{N1}^2} \tag{57}$$

$$P_{S-loss} = I_S V_{SD} = \frac{D^2 T_s V_{\text{in}} V_{SD}}{2(n-1)L_{N1}} \tag{58}$$

$$P_{D-loss} = I_{D1}\, V_{SD} = \frac{V_{\text{in}} D T_s (n-1+D) V_{SD}}{2(n-1)n^2 L_{N1}} \tag{59}$$

$$P_{CL-loss} = I_{N1}^2 R_{N1} + I_{N2}^2\, R_{N2} = \frac{V_{\text{in}}^2 D^2 T_s^2 (n-1+D)^2 (R_{N1} + R_{N2})}{4(n-1)n^4 L_{N1}^2} \tag{60}$$

Therefore, efficiency is provided as follows.

$$\eta = \frac{P_{\text{in}} - P_{C-loss} - P_{S-loss} - P_{D-loss} - P_{CL-loss}}{P_{\text{in}}} \tag{61}$$

where P_{in} is input power, calculated as follows.

$$P_{\text{in}} = \frac{V_{\text{in}}^2 D T_s (n-1+D)}{2(n-1)n^2 L_{N1}} \tag{62}$$

3. Results

The hardware structure of the proposed three converters is established and displayed in Figure 16, and their detailed device specifications are given in Table 4.

Figure 17 displays the experimental waveforms of the proposed PWCDVD-CLBC. Figure 17a shows the experimental waveforms of the voltages of the capacitors (*Co* and C_1). The experimental values of the parameters mentioned above are approximately 292 V and 156 V. Figure 17b describes the experimental waveforms of the windings (N_1 and N_2), and these waveforms are consistent with the theoretical operational status shown in Figure 6a,b. As described in Figure 17b, the current ranges of windings (N_1 and N_2), respectively, vary from 1 A to 13 A and −5 A to 2 A. Figure 17c shows the experimental waveforms of the voltages of the diodes (*Do* and D_1), whose experimental peak values are about 291 V and 196 V. Figure 17d–f shows the theoretical waveforms.

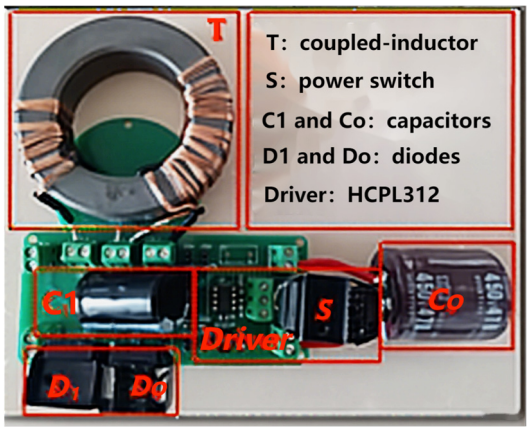


Figure 16. Experiment prototype.

Table 4. Experiment device's specifications.

Parameter	Description	Experiment/Value
Input Voltage	V_{in}	80 V
Output Voltage	V_o	300 V, 200 V, 200 V
Switch frequency	f	50 kHZ
Duty ratio	D	0.2
Output power	P	300 W
Capacitor	C_1	240 uF
Capacitor	C_o	440 uF
Magnetic core material	/	PC40
Maximum magnetic flux density	B_s	0.4 T
Hysteresis loss coefficient	C_h	1×10^{-7}/mT
Effective permeability	μ_e	$2400 \pm 20\%$
Turn ratio	n	16:8
Diode	D_1	SF1005G (10 A/300 V)
Diode	D_o	MUR1070 (1.5 A/700 V)
Switch	S_1	IPW65R019C7
MOSFET driver	/	HCPL3120

Figure 18 displays the experimental waveforms of the proposed SWCDVD-CLBC. Figure 18a shows the experimental waveforms of the voltages of the capacitors (C_o and C_1), whose experimental values are about 195 V and 77 V. Figure 18b shows the experimental waveforms of the windings (N_1 and N_2); the waveforms align with the theoretical operational status shown in Figure 6c,d. Its current ranges of windings (N_1 and N_2), respectively, vary from 0 A to 18 A and 1.5 to 12 A. Figure 18c shows the experimental waveforms of the voltages of the diodes (D_o and D_1), whose experimental peak values are about 194 V and 97 V. Figure 18d–f shows the theoretical waveforms.

Figure 19 displays the experimental waveforms of the proposed FPWCDVD-CLBC. Figure 19a shows the experimental waveforms of the voltages of the capacitors (C_o and C_1), whose experimental values are about 196 V and 78 V. Figure 19b provides the experimental waveforms of the windings (N_1 and N_2), and these waveforms are consistent with the theoretical operational status shown in Figure 6e,f. Its current ranges of windings (N_1 and N_2), respectively, vary from 0 A to 17 A and -2 to 7 A. Figure 19c shows the experimental waveforms of the voltages of the diodes (D_o and D_1), whose experimental peak values are about 195 V and 98 V. Figure 19d–f shows the theoretical waveforms.

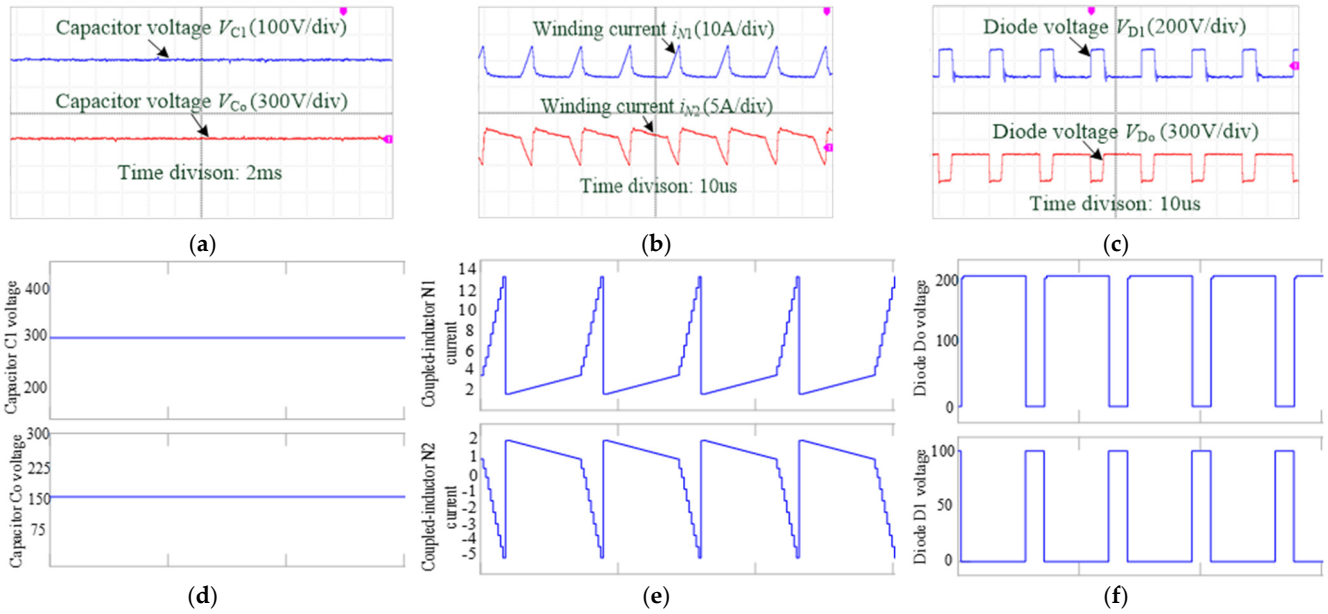


Figure 17. The experimental results of the proposed PWCDVD-CLBC's (**a**) voltages of capacitors (C1 and Co), (**b**) currents of windings (N1 and N2), and (**c**) voltages of diodes (D1 and Do). The theoretical results of the proposed PWCDVD-CLBC's (**d**) voltages of capacitors (C1 and Co), (**e**) currents of windings (N1 and N2), and (**f**) voltages of diodes (D1 and Do).

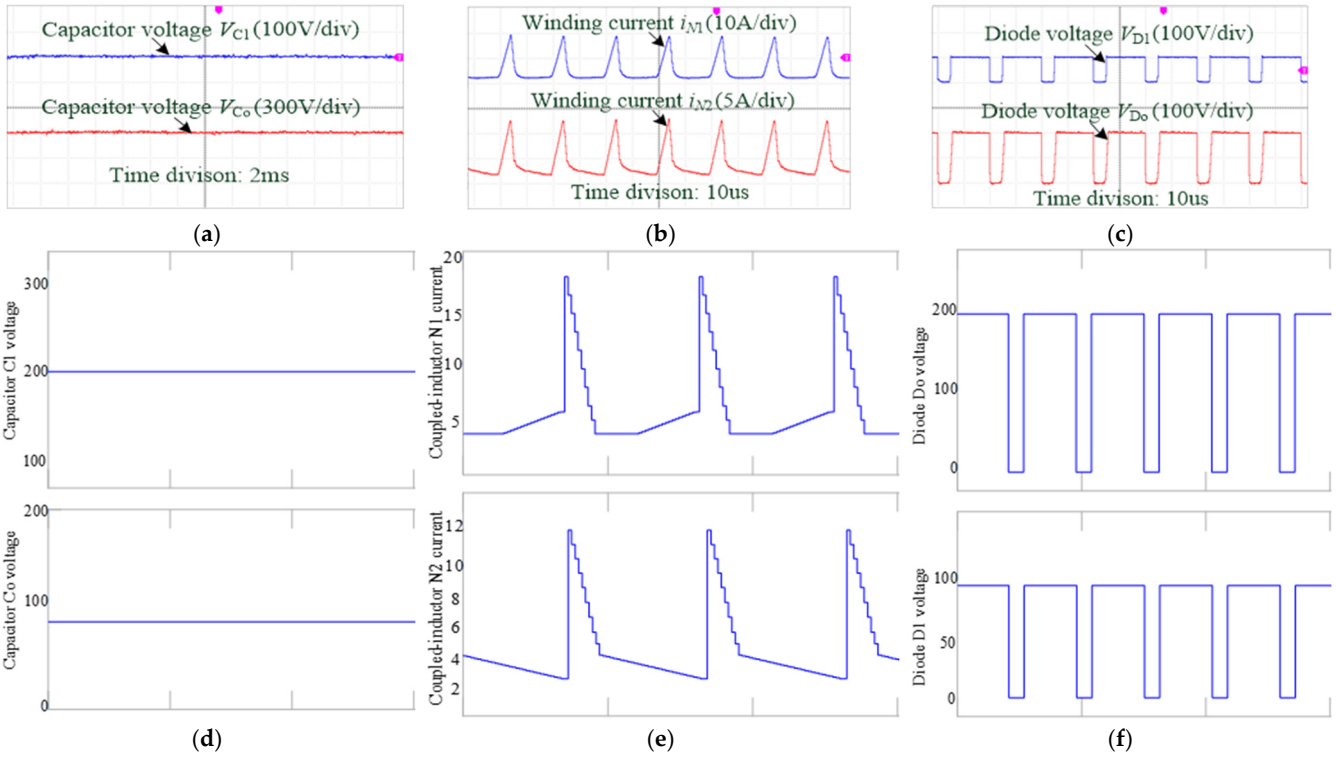


Figure 18. The experimental results of the proposed SWCDVD-CLBC's (**a**) voltages of capacitors (C_1 and C_o), (**b**) currents of windings (N_1 and N_2), and (**c**) voltages of diodes (D_1 and D_o). The theoretical results of the proposed PWCDVD-CLBC's (**d**) voltages of capacitors (C1 and Co), (**e**) currents of windings (N1 and N2), and (**f**) voltages of diodes (D1 and Do).

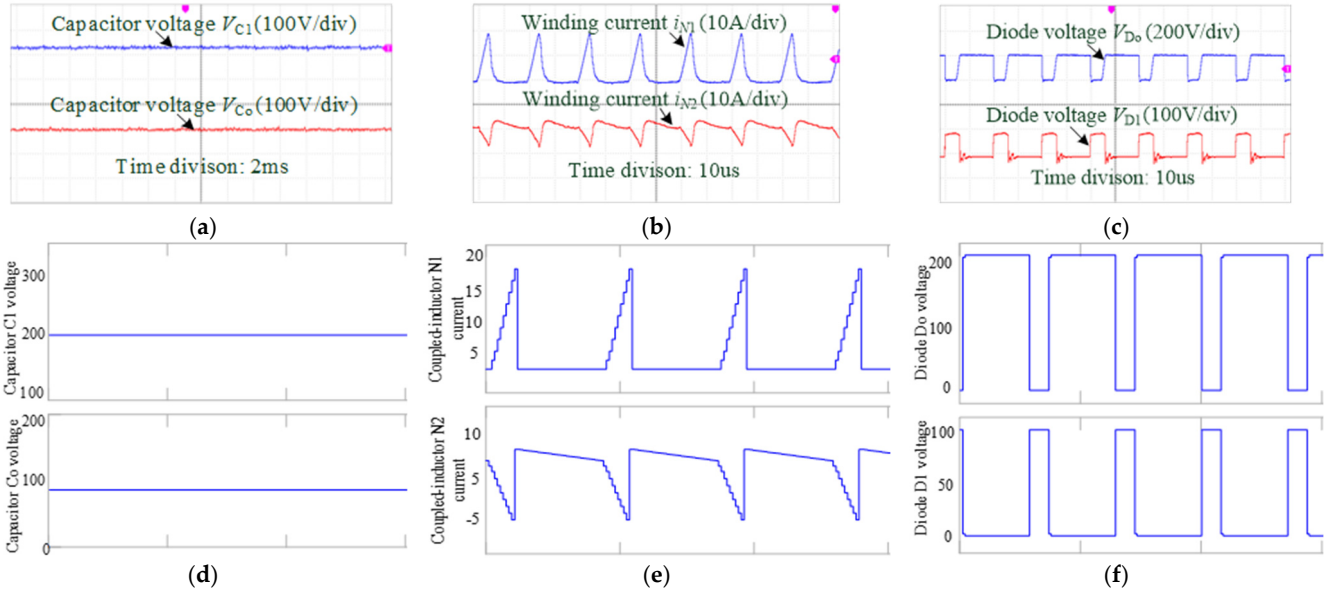


Figure 19. The experimental results of the proposed FPWCDVD-CLBC's (**a**) voltages of capacitors (C_1 and C_o), (**b**) currents of windings (N_1 and N_2), and (**c**) voltages of diodes (D_1 and D_o) The theoretical results of the proposed PWCDVD-CLBC's (**d**) voltages of capacitors (C1 and Co), (**e**) currents of windings (N1 and N2), and (**f**) voltages of diodes (D1 and Do).

In summary, the experimental results are very close to the theoretical values and confirm the performance and feasibility of the proposed topologies.

An efficiency test for the proposed three converters was conducted, whose turn ratios are 2 and 1.5. The corresponding power range is between 50 W and 350 W. Figure 20 shows the efficiency curves of theoretical efficiency and experimental efficiency. In Figure 20, the experimental efficiency value is slightly higher and close to the theoretical efficiency value. All proposed converters can obtain a higher efficiency since their topologies utilize a lower component count. The magnetizing inductance L_M and leakage inductance L_k are crucial to energy transfer in the coupled-inductor cells. If the core saturates, the inductance values will drop significantly, and the inductor cannot store or transfer the expected energy, which results in a reduced voltage gain and lower output voltage than designed. The paper's efficiency calculations (Equations (49), (55) and (61)) assume linear inductance behavior. Once core saturation sets in, effective inductance drops. The current increases to maintain power, causing higher conduction and switching losses.

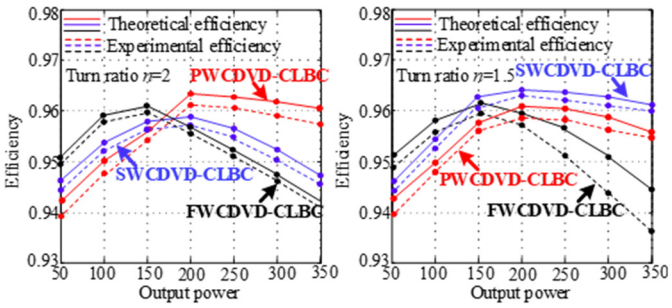


Figure 20. Efficiency (**a**) n = 2 and (**b**) n = 1.5.

4. Discussion

By moving the switch device of the proposed converters forward and keeping the original charging and discharging path invariant, the topology extension of the proposed three converters is shown in Figure 21, which lowers the switch voltage stresses to a large degree and maintains the same voltage gain. The generalized structure variation is described in Figure 22. (* represents the homonymous end of the coupling inductance).

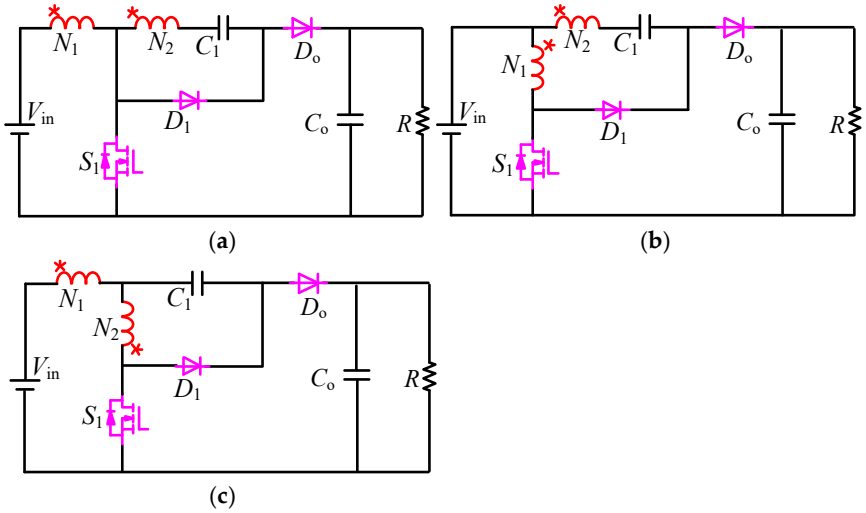


Figure 21. Topology extension: (**a**) PWCDVD-CLBC, (**b**) SWCDVD-CLBC, and (**c**) FPWCDVD-CLBC.

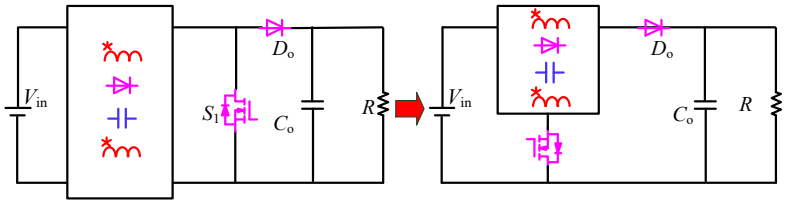


Figure 22. Generalized structure variation.

5. Conclusions

This paper proposes a family of voltage-doubling coupled-inductor boost converters—PWCDVD-CLBC, FPWCDVD-CLBC, and SWCDVD-CLBC—where the voltage gains and turn ratios for the PWCDVD-CLBC and FPWCDVD-CLBC have proportional relations, and the SWCDVD-CLBC has an inversely proportional relation, which was designed for high-voltage gains, continuous input current, and a reduced component count. By exploiting different winding configurations, the proposed topologies demonstrate superior performance in terms of efficiency, voltage stress, and shoot-through current, as validated through theoretical analyses, simulations, and experimental results. The practical implications are significant for applications requiring compact and efficient DC/DC conversion, such as renewable energy systems and electric vehicle charging infrastructures. Also, different topologies have varying efficiencies under different output power ranges when the turn ratio is adjusted. Finally, the experimental results of the proposed converters verify the correctness of the theoretical analysis.

Author Contributions: Conceptualization, Y.J. and S.J.; methodology, Y.L.; software, Y.J.; validation, Y.J., S.J. and Y.L.; formal analysis, Y.J., S.J. and Y.L.; writing—original draft preparation, Y.J.; writing—review and editing, Y.J. and S.J.; funding acquisition, Y.L. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflicts of interest.

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