

## Article

# Buck Converter with Improved Efficiency and Wide Load Range Enabled by Negative Level Shifter and Low-Power Adaptive On-Time Controller

Xuan Thanh Pham <sup>1</sup>, Minh Tan Nguyen <sup>1</sup>, Cong-Kha Pham <sup>2</sup> and Kieu-Xuan Thuc <sup>1,\*</sup>

<sup>1</sup> School of Electrical and Electronic Engineering, Hanoi University of Industry, Hanoi 100000, Vietnam; thanhpx@haui.edu.vn (X.T.P.); minhntanbg2001@gmail.com (M.T.N.)

<sup>2</sup> Department of Information and Network Engineering, The University of Electro-Communications (UEC), Tokyo 182-8585, Japan; phamck@uec.ac.jp

\* Correspondence: thuckx@haui.edu.vn

**Abstract:** This paper introduces a high-efficiency buck converter designed for a wide load range, targeting low-power applications in medical devices, smart homes, wearables, IoT, and technology utilizing WiFi and Bluetooth. To achieve high efficiency across varying loads, the proposed converter employs a low-power adaptive on-time (AOT) controller that ensures output voltage stability and seamless mode transitions. An adaptive comparator (ACP) with variable output impedance is introduced, offering a variable DC gain and bandwidth to be suitable for different load conditions. A negative-level shifter (NLS) circuit, with its swing ranging from  $-0.5$  V to the battery voltage ( $V_{BAT}$ ), is proposed to control the smaller power p-MOS transistors. By using an NLS, the chip area, which is mostly occupied by power CMOS transistors, is reduced while the power efficiency is improved, particularly under a heavy load. A status time detector (STD) block which provides control signals to the ACP and NLS for optimized power consumption is added to identify load conditions (heavy, light, ultra-light). By employing a 180 nm CMOS technology, the active chip area occupies about  $0.31$  mm<sup>2</sup>. With an input voltage range of 2.8–3.3 V, the controller's current consumption ranges from 1.2  $\mu$ A to 16  $\mu$ A, corresponding to the output load current varying from 12  $\mu$ A to 120 mA. Although the output load can vary, the output voltage is regulated at 1.2 V with a ripple between 3 and 12 mV. The proposed design achieves a peak efficiency of 96.2% under a heavy load with a switching frequency of 1.3 MHz.

**Keywords:** adaptive on-time (AOT) control; quiescent current; low-power control; high efficiency; low-power applications



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## 1. Introduction

System-on-Chip (SoC) technology is crucial for low-power devices such as smart-watches, implantable medical devices, and IoT applications [1–4], which exhibit dynamic power demands as shown in Figure 1. These devices consume microwatts power in standby for tasks such as notification checks and low-power wireless communication, enabling rapid wake-up. During active processing, power consumption can range from milliwatts to hundreds of milliwatts depending on the executed functions. Buck converters in these low-power devices are employed with the controller blocks using ultra-low current to maximize battery life and efficiency, especially during standby [5,6]. DC-DC converters are not only needed to maintain a stable output voltage over a wide input voltage range due

to fluctuations in battery charge, but also for handling significant load current variations during operation [7,8]. Therefore, minimizing power consumption, maximizing efficiency across a wide load range, and optimizing device dimensions are critical for prolonged device operation and reduced recharging frequency [9–11].

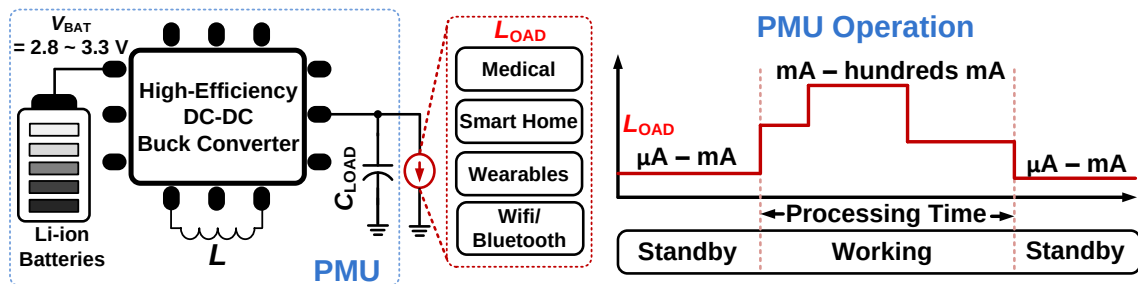


**Figure 1.** Diagram of lithium-ion battery of DC-DC converter in low-power device application.

Recently, several power management units (PMUs) [12,13] often utilize multiple control modes with switching frequencies tailored to specific load conditions. However, the seamless mode conversions can be challenging due to decision making and mode-switching delays [14,15]. The pulse width modulation (PWM) [16] for high and medium loads and the pulse frequency modulation (PFM) [17] for light loads are used to reduce switching losses. However, such approaches can complicate the controller design, potentially increasing current consumption and output ripple in PFM mode [18,19]. Single-controller approaches such as a single bounded hysteresis control (SBHC) [20] and a dynamic on/off time (DOOT) control [21] are used for a high efficiency across a wide load range. However, due to fixed low-bias current comparators, the designs [20,21] suffer from a slow response and poor regulation under heavy loads [22,23]. Consequently, combining controllers with adaptive bias current comparators is necessary for high efficiency across a wide load range [24].

In order to respond to heavy output load, the large power transistor switches (PTSs) are needed for a high current throughput, which causes the chip area to increase. For instance, the design in [25] uses a PMOS and NMOS PTS occupying 2.7 and 1.7  $\text{mm}^2$ , respectively, along with the high-power gate drivers. The level shifting (LS) techniques used in [26] can increase the gate-source voltage ( $V_{GS}$ ) of CMOS transistors, enabling smaller PTS for high current throughput. However, these designs [25,26] still occupied significant areas about 7  $\text{mm}^2$  and 0.78  $\text{mm}^2$ , respectively. Other approaches [27–29] using both a PMOS and NMOS PTS with level shifters and bootstrap configurations are used to reduce PMOS on-resistance ( $R_{ON}$ ) and PTS sizing, but still result in relatively large active areas (0.75, 1.4, and 1.404  $\text{mm}^2$ ). To achieve high performance with low fabrication costs, low current consumption, small chip size, while maintaining efficiency across variable loads, is a big challenge during the design DC-DC converter [30].

This paper presents a proposed buck converter with low power consumption and high efficiency across a wide output current load range (12  $\mu\text{A}$  to 120 mA). A negative level shifter (NLS) with its output swing from a negative voltage ( $V_{NEG}$ ) to  $V_{BAT}$  is proposed to reduce the PMOS PTS on-resistance ( $R_{ON}$ ) without increasing its size. By employing an adaptive on-time (AOT) controller, a novel adaptive comparator (ACP) operating with dual-mode currents, and NLS, the proposed DC-DC buck converter achieves a high efficiency higher than 90% and 65% to approximate 90% with the output current load of from 40 to 120 mA and lower than 40 mA, respectively. Simulated in 180 nm CMOS technology, the proposed design occupies a small chip area of 0.31  $\text{mm}^2$ . With an input voltage range of 2.8–3.3 V, the low-power AOT controller consumes 1.2 to 16  $\mu\text{A}$  as the output current load changes from 12  $\mu\text{A}$  to 120 mA. The output voltage is regulated at 1.2 V with the voltage ripple varying from 3 to 12 mV across different output loads. The subsequent sections of

this paper detail the AOT control buck converter architecture and circuit implementations (Section 2), the simulation results (Section 3), and the conclusions (Section 4).

## 2. The AOT Control Buck Converter Architecture and Circuit Implementations

### 2.1. The Operating Mechanism of the Architecture

Figure 2 shows the block diagram of the proposed buck converter using AOT and NLS. In order to achieve low power consumption and high efficiency, a control block operating at a supply voltage  $V_{DD} = 1.2$  V is designed to drive the PTS ( $S_1, S_2, S_3, S_4$ ). The bandgap reference 1,2 (BGR1,2) blocks are utilized to produce the reference bias voltages to reduce the effect of the ambient temperature. The Soft-Start block generates a start voltage ( $V_S$ ) which gradually increases from a  $V_{SS}$  to the reference voltage ( $V_{REF}$ ), ensuring system stability and reducing negative factors during the start-up phase. The current sensor block is built from the resistors  $R_S = R_Z = 150$  k $\Omega$ , capacitor  $C_S = 8$  pF, and the inductor current ( $I_L$ ) flowing through the inductor  $L = 4.7$   $\mu$ H, which is converted to a voltage sensor signal ( $V_{SEN}$ ). In order to regulate the output voltage ( $V_{OUT}$ ), a type III compensator based on a differential difference amplifier (DDA), which is used and analyzed in reference [31,32], and biased with an ultra-low current is employed to not only respond immediately and optimally to changes in the output but to also generate an error-amplifier voltage ( $V_{EA}$ ) at the DDA's output. The compensator, which employed passive components such as capacitors  $C_1 = 40$  pF,  $C_2 = 3.2$  pF,  $C_3 = 4$  pF,  $C_4 = 2$  pF, and resistors  $R_{f1,2} = 1.5$  k $\Omega$ ,  $R_{1,2} = 1$  M $\Omega$ , are used for system stability. During  $T_{SLEEP}$  under a light load and full cycle work in the ultra-light load mode, the ACP bias current is 30 nA, and 4  $\mu$ A under a heavy load. The ACP is utilized to compare  $V_{EA}$  with  $V_{SEN}$  to generate a compared control signal ( $S_C$ ), which is used to set the control signals  $C_{LKP}$  and  $C_{LKN}$ . The on-time detector (OTD) is applied to generate a fixed on-time  $T_{ON}$ , which is used to determine the inductor's charging time. When the output experiences a light load and ultra-light load, the zero-current detector (ZCD) is enabled to detect the sleep time of the PTS  $S_2$ , preventing an inversed current in the inductor  $L$ . The control bias generates the control signals  $S_A$  and  $S_B$ . The  $S_A$  controls the bias current of the ACP, while the  $S_B$  is the input control signal for the status time detector (STD). The oscillator generates a clock signal ( $C_{LK}$ ), which is used to control the negative voltage generator (NVG) block. The  $C_{LK}$ 's frequency is dependent on another clock signal  $C_{LKP}$ , which is generated by the control logic and the dead time block. The NVG is employed to produce a negative voltage  $V_{NEG}$  during the  $T_{ON}$  cycle to control PTS  $S_1$ . We note that  $V_{NEG}$  is created to help the output swing of the NLS increasing from  $V_{NEG}$  to the  $V_{BAT}$  voltage. This extended swing increases the throughput current of PTS  $S_1$  to be increased while its size is maintained. In addition, STD is employed to generate the detector load condition signal  $EN_{1,2}$ . The  $EN_{1,2}$  are bits of <11>, <10>, and <00> when the output load experiences a heavy, light, and ultra-light load, respectively. When the output current load is reduced to lower than the ultra-light current load, the  $T_{ON}$  of  $C_{LKN}$  is also reduced to zero, leading to the PTS  $S_2$  being completely turned off, and the output voltage  $V_{OUT}$  is not controlled. In this design, the  $S_{OFF\_M}$  generated by the off-min (OM) block with fixed cycle is employed so that the falling edge of the  $C_{LKN}$  is reduced to the falling edge of the  $S_{OFF\_M}$ . This means that the PTS  $S_2$  is turned on for a short time, maintaining control on  $V_{OUT}$ . The control logic and dead time block are used to produce the high side and low side, and to generate the delay time to avoid overlap between  $C_{LKP}$  and  $C_{LKN}$ .

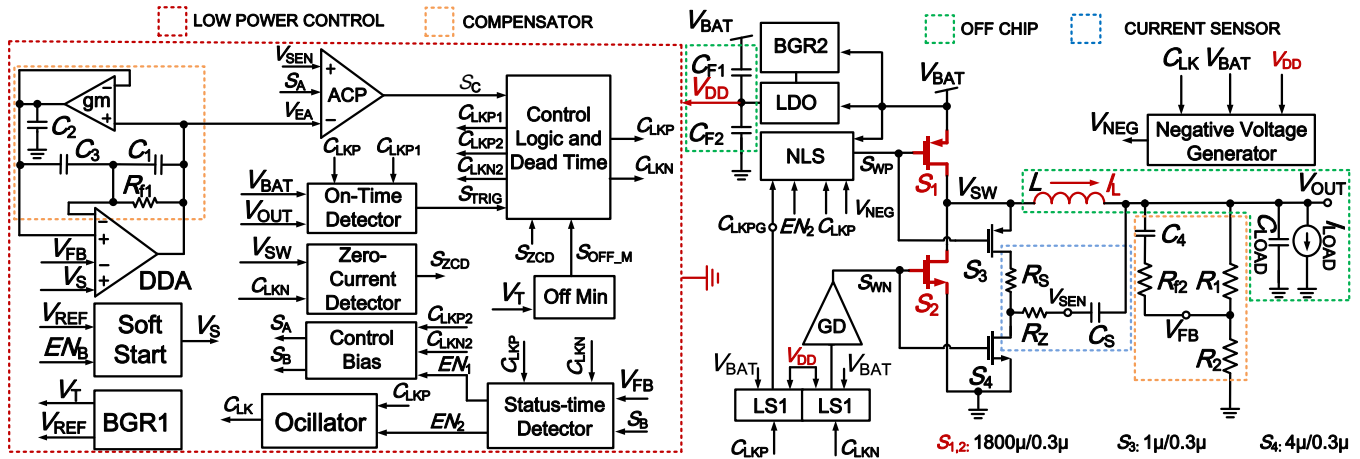


Figure 2. The architecture of the proposed buck converter using the AOT control and the negative level shifter (NLS).

In order to reach the goals mentioned in the introduction section, the proposed low power control (LPC) is designed using a voltage supply  $V_{DD} = 1.2$  V.  $V_{DD}$  is generated from  $V_{BAT}$  by an internal low drop output voltage (LDO) circuit. Depending on the output load, the LPC uses adaptive bias current due to only using suitable blocks for each operation mode to reduce power loss in internal circuits improving efficiency of the design. Each operation mode of STD is turned on/off based on the changed the output current load and the  $C_{LKP}$  and  $C_{LKN}$  during on-time ( $T_{ON}$ ), off-time ( $T_{OFF}$ ), and sleep time ( $T_{SLEEP}$ ) cycles, as shown in Figure 3.

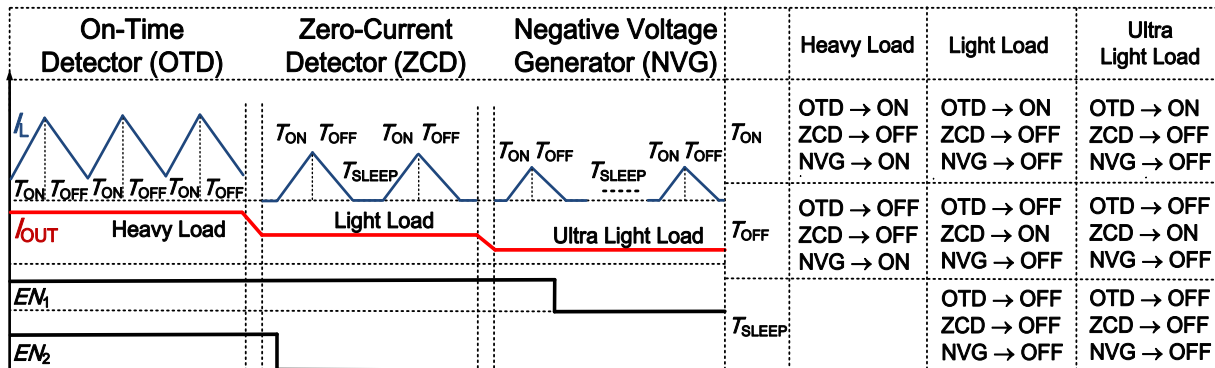


Figure 3. The process of the operation of OTD, ZCD, and NVG blocks.

## 2.2. The Circuit Implementation

The ACP's schematic is shown in Figure 4a. The ACP can be use in dual-mode with variable output current and impedance, leading to its DC gain and bandwidth being varied, following the output current load transition. The control logic block generates the control switch signal  $S_A$  depending on the output load conditions. With heavy and light loads,  $EN_1 = '1'$ ,  $S_A$  can be equal to '1' or '0', and when  $EN_1 = '0'$ ,  $S_A = '0'$  the proposed design operates in standby mode (ultra-light load), as shown in Figure 4b. Figure 5 illustrates, both the DC gain and bandwidth of the ACP. In order to reduce output ripple in the heavy load, the PTS switching frequency is set at around 1.3 MHz, thus needing enough bandwidth. Thus, if  $S_A = '1'$ , this leads to  $M_{A1,2}$  being added to reduce the output impedance. Simultaneously, when the ACP is biased with 4  $\mu$ A, the ACP's bandwidth is improved, leading to a faster comparison and transition. In this case, the DC gain is about 52 dB while having a 10 MHz bandwidth. As a result, the ACP can work at a high

frequency. In the ultra-light load mode, the PTS switching frequency can work at a low frequency of 0.25 kHz, the  $S_A$  can be set to '0', and  $M_{A1,2}$  are separated to increase the output impedance, and simultaneously the ACP bias current is now 30 nA, improving DC gain; therefore, the ACP is enabled to operate with high precision at low frequencies. Although the ACP achieves a high gain of 90 dB at a low frequency, the ACP's bandwidth is reduced to 100 kHz; hence, the ACP's operation in this case is suitable for ultra-light load conditions.

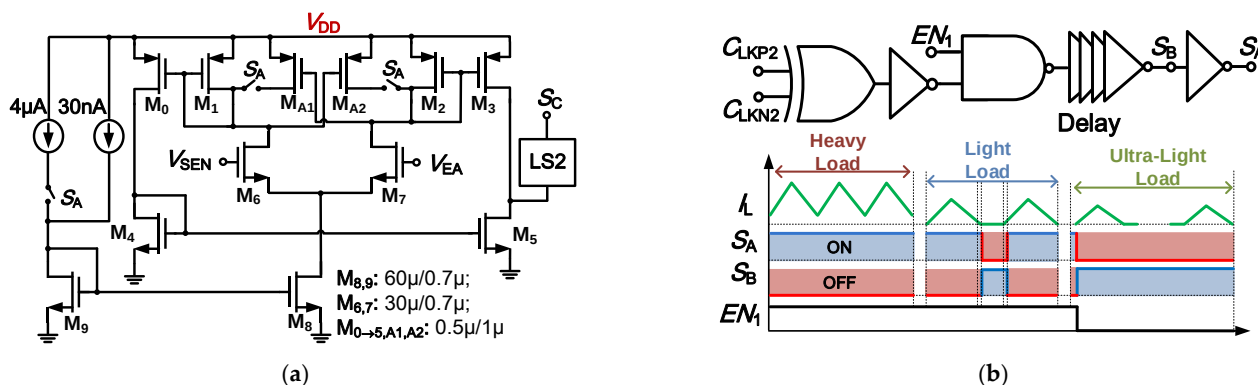


**Figure 4.** (a) Schematic of the proposed adaptive comparator (ACP); (b) schematic block control bias and switches control signals.

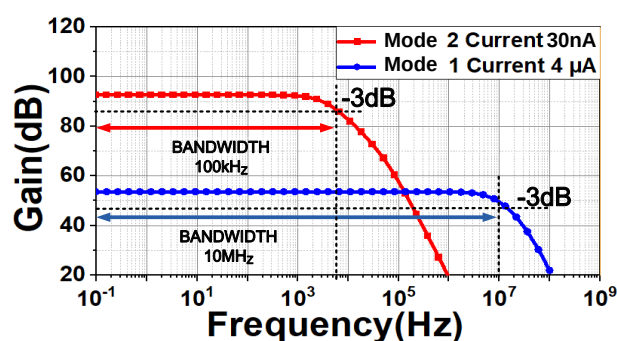


**Figure 5.** DC gain and bandwidth of the adaptive comparator ACP.

Figure 6a shows the schematic of the proposed oscillator, which generates a square wave with two different frequencies of 25 MHz (Cycle T = 40 ns) and 10 MHz (Cycle T = 100 ns) during  $T_{\text{ON}}$  and  $T_{\text{OFF}}$ , respectively. This structure reduces power consumption due to the average current dissipation depended on the changing frequency [33]. In order to generate a high negative voltage, the characteristics of capacitively coupled capacitors [34,35] are applicable. In Figure 6b, the negative generator (NEG) circuit uses high-frequency  $C_{\text{LKA}}$  pulses on one plate of the capacitors  $C_{\text{m4,7}}$ , and a negative voltage is generated on the other plate of the capacitors  $C_{\text{m4,7}}$ . The circuit operates with two phases,  $C_{\text{LKA}}$  and  $C_{\text{LKB}}$ , reducing charge leakage and reversal losses. The generating negative voltages uses n-MOS due to physical properties, all n-MOS are isolated upon implementation. The isolation loops are designed with separated deep n-wells. According to simulation results, three NEG's are connected in series to obtain a negative voltage of  $-0.5$  V.

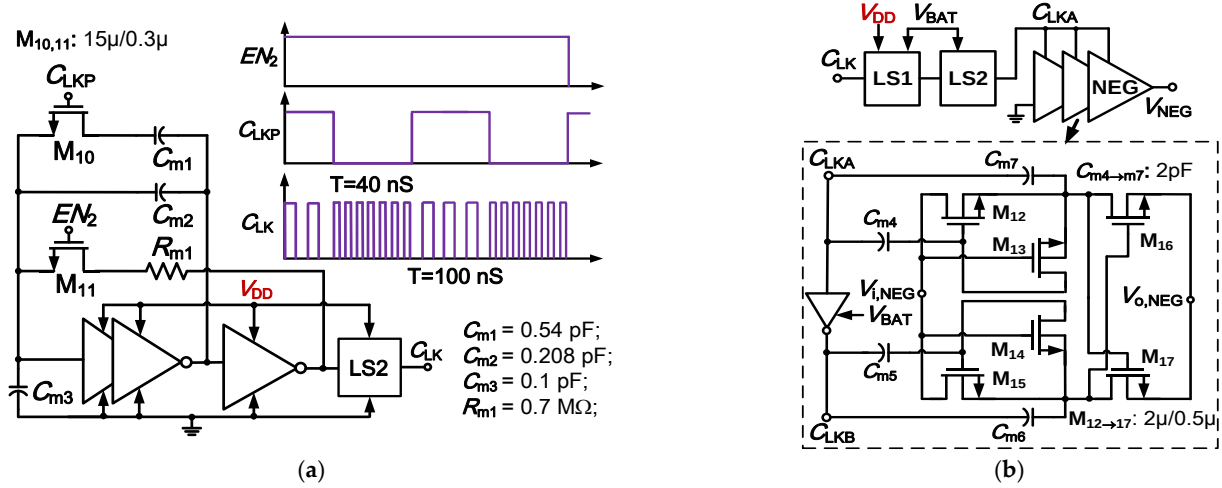


**Figure 6.** (a) Schematic of the proposed oscillator; (b) schematic of the negative voltage generator (NEG).

A negative voltage for the low side of  $S_{WP}$  signal generated by NLS is used to control PTS  $S_1$ . This helps reduce the on-resistance and sizing, leading to the parasitic  $C_{GS}$  of PTS  $S_1$  also being reduced. Therefore, the current consumption of the gate driver (GD) can be reduced. Under heavy loads, the low side of  $S_{WP}$  is a high negative voltage level, which is only required during the  $T_{ON}$ . A schematic of the proposed NLS is illustrated in Figure 7a. To implement on-chip, the size of  $C_{m4,5,6,7}$  must be small, leading to their lower charge. To use a negative voltage of  $-0.5$  V, the charges in the  $C_{GS}$  (which is bigger than  $C_{m4,5,6,7}$ ) of PTS  $S_1$  must be discharged completely to  $V_{SS}$  and then charged to the negative voltage  $V_{NEG}$  produced by NEG circuit. The discharge time of the  $C_{GS}$  of PTS  $S_1$  is very short, equal to the charging time of  $C_{m8}$ . In the heavy load mode, the  $S_{WP}$  signal swings from  $-0.5$  V to  $V_{BAT}$ . While in the light and ultra-light load modes, the swing of  $S_{WP}$  is between  $V_{SS}$  to  $V_{BAT}$ . The control signal of PTS  $S_1$  is shown in Figure 7b. The  $EN_2$  signal generated by the STD block is used to control the operation of the NLS. The  $S_N$  signal, which is produced by a level shifter, is always at a high level, and the low side of the  $S_{WP}$  signal is  $V_{SS}$ .

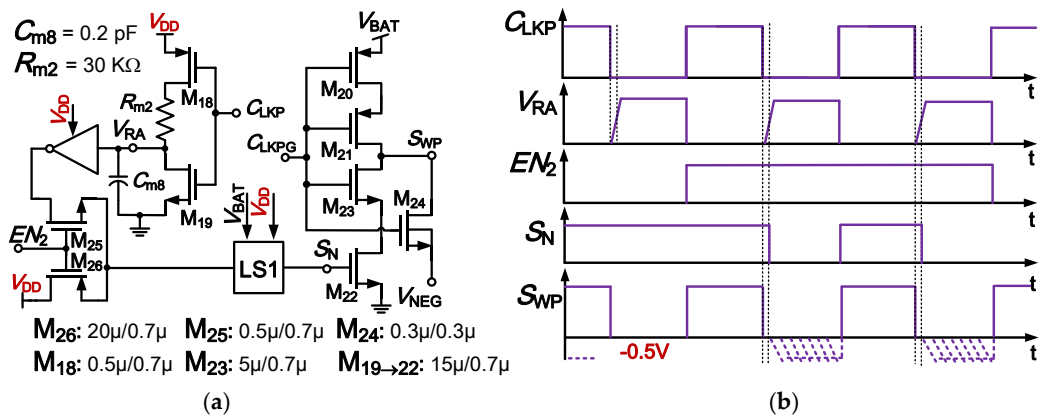


**Figure 7.** (a) Schematic of the proposed block negative level shifter (NLS); (b) the signal control generated by the NLS.

Figure 8a illustrates a current source providing small and stable current, which is continuously refreshed by the  $C_{LKP}$  cycle. In addition, an operational transconductance amplifier (OTA) with a low bias current of 15 nA is used to minimize power consumption. In Figure 8b, the STD detect light and ultra-light load conditions. In comparison to other structures, the STD can detect ultra-light load conditions with very low power consumption

using low current consumption comparators (CPs). The sample and hold (S&H) circuits help the voltages ( $V_{H1}$ ,  $V_{S1}$ ) and ( $V_{H2}$ ,  $V_{S2}$ ) to maintain balance when the converter operates under heavy loads. When the buck converter operates under the light load mode, the charging of  $C_{H2}$  is fast, being discharged through  $M_{46,47}$  during  $T_{SLEEP}$ , leading to  $V_{H2}$  being reduced faster. During  $T_{ON}$ , the charging of  $C_{S2}$  is discharged to  $C_{H2}$ , and thus,  $V_{S2}$  is also reduced. When  $V_{S2}$  is lower than  $V_{FB}$ , then  $EN_2$  is at a low level ( $V_{SS}$ ). As a result, the light load mode is detected. In another case, the buck converter operates under the ultra-light load mode, and  $C_{H1}$  is discharged through  $M_{42}$  during  $T_{SLEEP}$ , leading to  $V_{H1}$  also being reduced. During  $T_{ON}$ , the charging of  $C_{S1}$  is discharged to  $C_{H1}$ , and thus,  $V_{S1}$  is also reduced. When  $V_{S1}$  is lower than  $V_{FB}$ ,  $EN_1$  is at a low level ( $V_{SS}$ ). Thus, the ultra-light load mode is determined. The transistors  $M_{33}$ ,  $M_{35}$ ,  $M_{37}$ , and  $M_{39}$  work as charge storage elements to mitigate the voltage drop and reduce the noise for  $V_{S1}$  and  $V_{S2}$ . As shown in Figure 3, there are  $EN_1$  and  $EN_2$  signals, for which the high and low side are dependent on the  $T_{SLEEP}$  cycle to control the modes of the buck converter. When  $T_{SLEEP}$  cycles occur consecutively,  $V_{S1}$  and  $V_{S2}$  are adjusted gradually, and then compared to the fixed voltage  $V_{FB}$  according to the operating modes of the buck converter, as shown in Figure 8c.

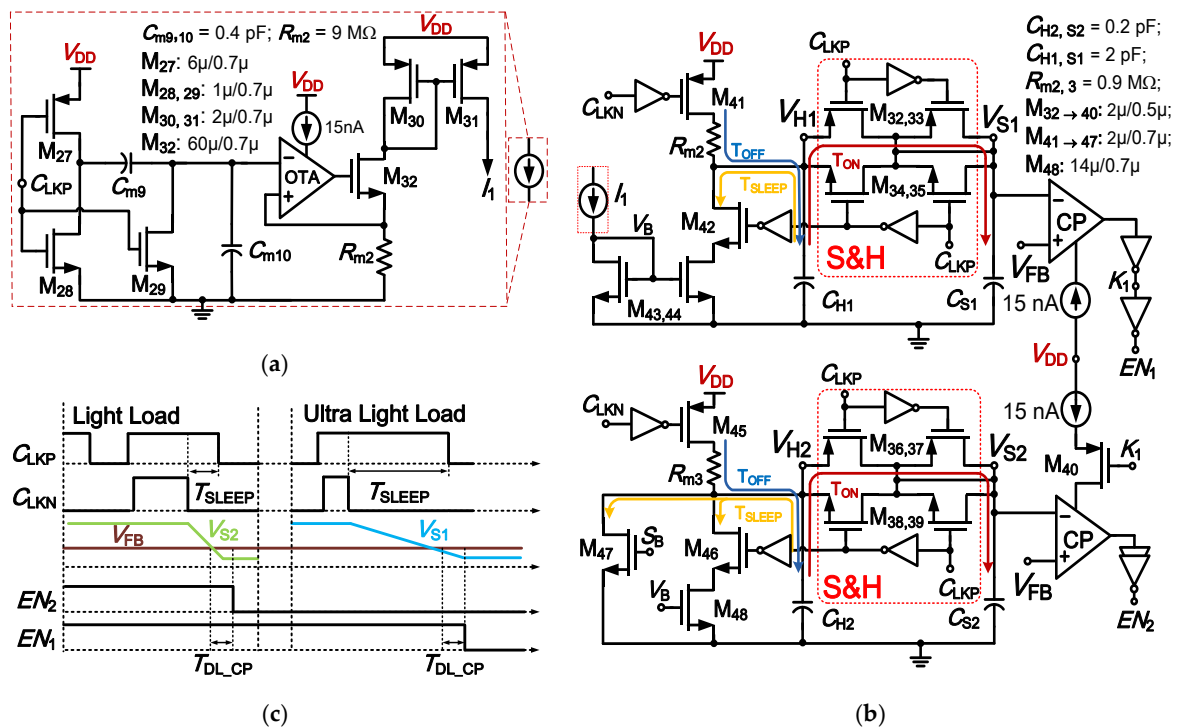


**Figure 8.** (a) Schematic of the small discharging current source; (b) schematic of the STD; (c) the signal control generated by the STD.

The delay time ( $T_{DL\_CP}$ ) is added, using a comparator (CP) with a low power consumption. In a buck converter, the duration of  $T_{ON}$  is controlled by the OTD as shown in Figure 9a. The comparator in OTD are periodically activated and deactivated based on  $EN$  signal, which is an inverted  $C_{LKP1}$ . By using the comparator in OTD,  $V_D$  is compared with sawtooth signal  $V_R$ , which is created by  $R_{ON}$  and  $C_{ON}$  circuit characteristics, to create  $S_{TRIG}$ ; when  $V_R$  is higher than  $V_D$ ,  $S_{TRIG}$  is used to detect the end of  $T_{ON}$  duration. When  $S_{TRIG} = <1>$ ,  $EN$  will be  $<0>$ , leading to  $V_D$  being low due to discharging through  $M_{51}$  and  $M_{52}$  while the comparator in OTD is turned off. The timing variation of  $C_{LKP1}$  and  $C_{LKP}$  is defined as  $T_{delay}$  which is generated from the control logic and deadtime. The duration of  $T_{delay}$  for the heavy load mode and light/ultra-light modes are shown in Figure 9b and Figure 9c, respectively.

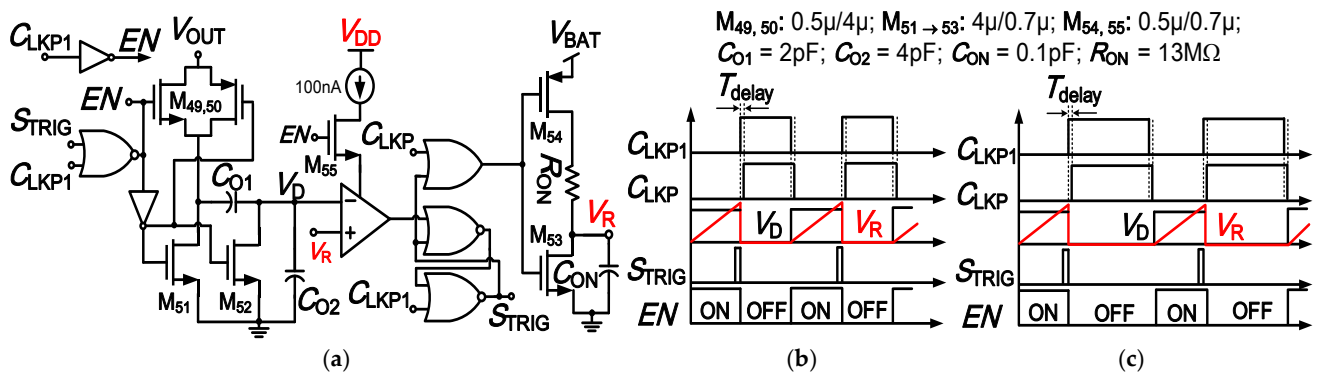


**Figure 9.** (a) The schematic of the on-time detector (OTD); the voltage of the signal controls of the OTD operation in (b) heavy load mode and (c) light and ultra-light load modes.

In the light load and ultra-light load modes, the discrete operation of PTS CMOS results in a inversed current in the inductor, which discharges to  $V_{SS}$ , leading to energy loss in the inductor. A zero-current detector (ZCD) has been added to identify the inversed current in order to mitigate inverter current in the inductor  $L$ . Figure 10 shows the schematic of the ZCD and its associated signal for ZCD operation. The ZCD block operates only during the  $T_{OFF}$  to reduce energy consumption. The  $M_{62}$  switch remains continuously activated to maintain balance between  $V_N$  and  $V_P$ . During  $T_{OFF}$ ,  $M_{64}$  is activated, and  $V_{SW}$  is compared directly to  $V_N$ , utilizing the difference between  $V_N$  and  $V_P$  to ascertain the inductor's current. In  $T_{OFF}$ , under the heavy load mode, the  $V_P$  signal consistently exhibits a lower magnitude than  $V_N$ . In the light and ultra-light load modes, when  $S_{ZCD}$  is elevated and the  $T_{OFF}$  time concludes, by initiating the  $T_{SLEEP}$  time, the  $S_{ZCD}$  signal set up high. The schematic of the off-min (OM) block is presented in Figure 11a, while the schematic of the control logic and deadtime are shown in Figure 11b. The OM is incorporated into the proposed design to produce the signal  $S_{OFF\_M}$  with a fixed cycle controlling PTS  $S_2$ . In the proposed converter operations, the reference voltage  $V_T$  is determined by the external voltage, which establishes the duration of the  $S_{OFF\_M}$  signal. When the  $S_{TRIG}$  signal concludes, the  $S_{OFF\_M}$  signal begins. The proposed converter operates using the  $S_{OFF\_M}$  signal, even when the output load is below ultra-light output loads. In this scenario, the  $C_{LKN}$  signal is not entirely deactivated, resulting in the DC-DC buck converter transitioning to standby mode. In Figure 11b, the schematic of the control logic block is used to regulate the duration of  $T_{ON}$  and  $T_{OFF}$  in real-time. The signal  $S_{ZCD}$  is used to prevent inversed current ( $I_L$ ) of the inductor, the low side of  $S_C$  is established for  $T_{OFF}$ , the high side of  $S_{TRIG}$  is established for  $T_{ON}$  duration. The special signal  $S_{OFF\_M}$  is used to ensure that the proposed converter is not turned off when the output load is too small. In addition, a deadtime duration ( $T_{DT}$ ) is generated by delay components to prevent p-MOS and n-MOS switches working simultaneously, as shown in Figure 12a for the heavy load mode and Figure 12b for the light load and ultra-light load modes.

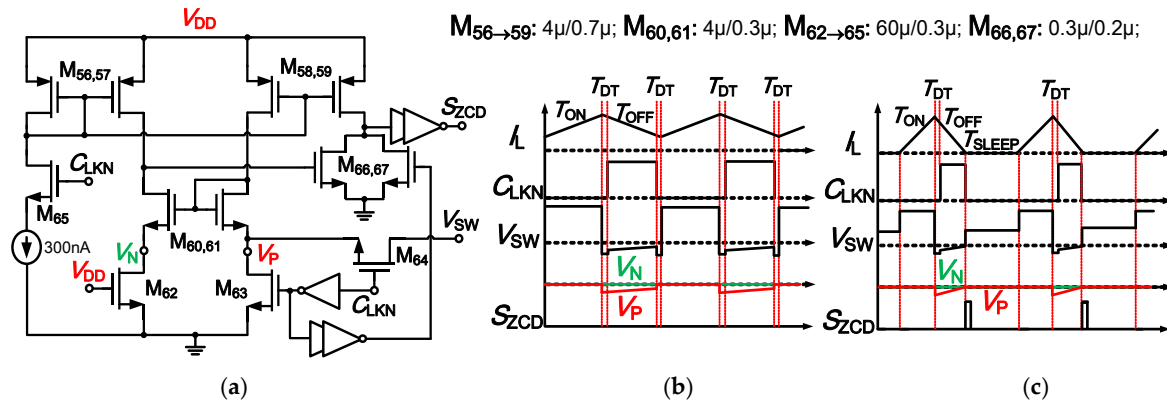


Figure 10. (a) The schematic of the ZCD; the signal for the ZCD operation in (b) heavy load mode and (c) light and ultra-light load modes.

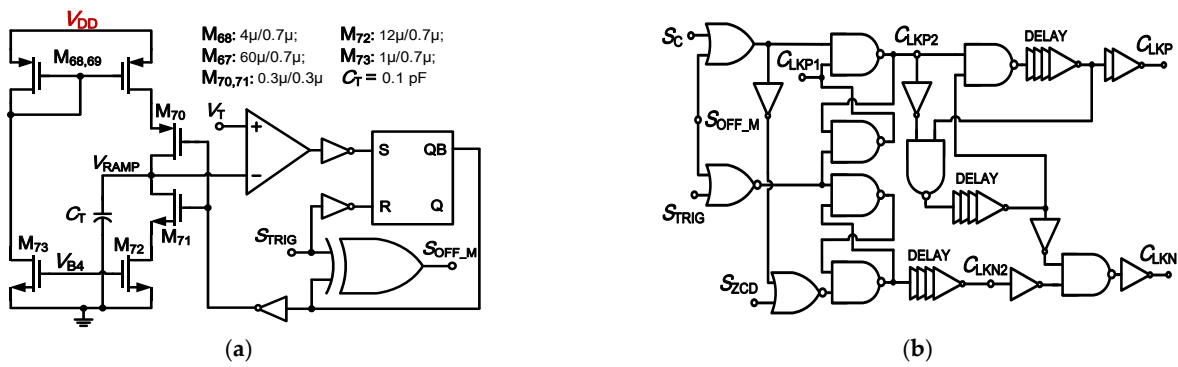


Figure 11. (a) Schematic of the off-min (OM) block; (b) schematic of control logic and deadtime.

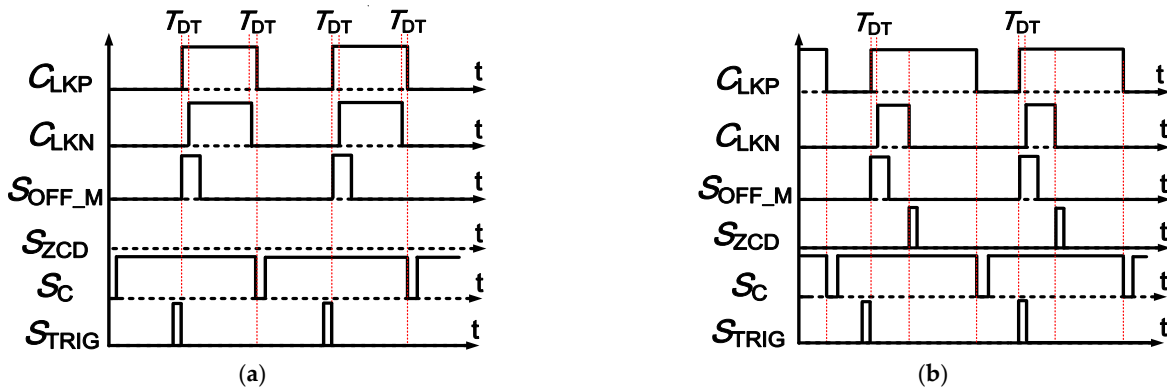


Figure 12. (a) The signals for the heavy load mode of ZCD; (b) the signals for the light and ultra-light load modes of ZCD.

As shown in Figure 13a, the schematic of the level shifter 1 (LS1) is shown. LS1 is used to increase the high-level voltage from  $V_{DD}$  to  $V_{BAT}$  to control the gate drive (GD). The schematic of the level shifter 2 (LS2), as shown in Figure 13b, is used to help achieve a lower slope for the output signal, making logic signal more accurate. Figure 14 shows the schematic of a differential difference amplifier (DDA) with two folded input pairs and sharing cascode with a bias current of 15 nA for each differential pair. The compensation based on the DDA circuit is complex, but it has the advantage of providing a quick response during transients. A conventional error amplifier typically has a differential pair of negative feedback inputs that force the difference between the two input voltages to be small. However, when the DDA circuit is used, there are no significant differences

between the pairs  $V_{IN1(-)}$  and  $V_{IP1(+)}$  with  $V_{IN2(-)}$  and  $V_{IP2(+)}$ , and at the same time, the fluctuating voltage  $V_{EA}$  does not affect the voltage  $V_{FB}$ . When DDA is in the stable state,  $V_{IN1(-)} = V_{IP1(+)}$  and  $V_{IN2(-)} = V_{IP2(+)}$ , at which point the voltage  $V_{EA}$  will be in a stable state. In the case of load changes,  $V_{EA}$  will change.

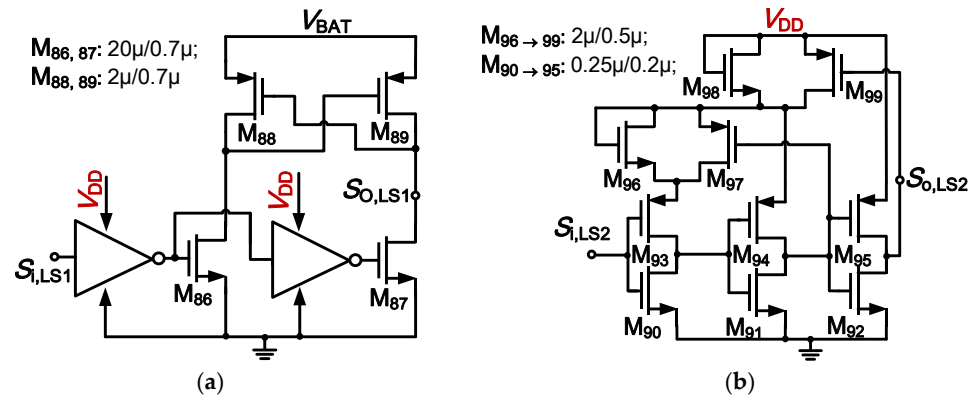


Figure 13. Schematic of the block (a) level shifter 1 (LS1) and (b) level shifter 2 (LS2).

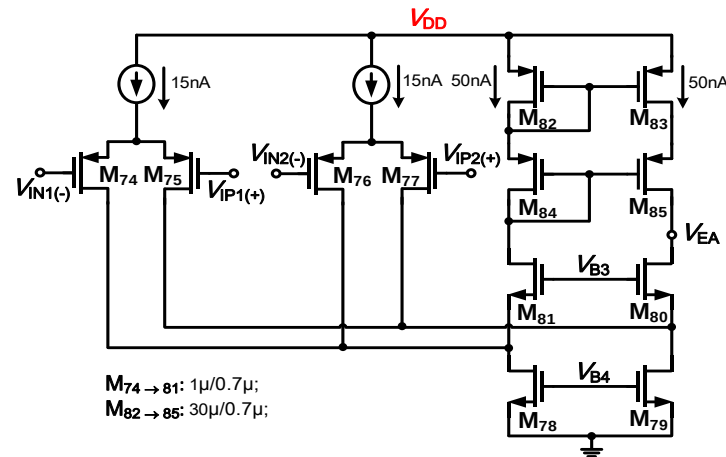


Figure 14. Schematic of the block differential difference amplifier (DDA).

### 3. Simulation Results

The proposal for a buck DC-DC converter with low biased current consumption in the control block is simulated by using a CMOS 180 nm technology. The deep n-well techniques is implemented in the NVG block. The proposed design is combined with an external capacitor of 10  $\mu$ F and an inductor of 4.7  $\mu$ F during running simulation. The chip area occupies 0.31 mm<sup>2</sup>, as shown in Figure 15. In order to avoid the crosstalk noise between the blocks, noise sensitivity, and process variation, we use the layout techniques such as common-centroid, symmetric placement, dummy devices for differential pairs and capacitors and CMOS transistors for each block. During the merging of all blocks, the analog and high-power switching blocks are physically isolated, with shielding and floor planning to minimize crosstalk and noise coupling. Moreover, to operate with a negative voltage of  $-0.5$  V, the deep n-well technique is used during the design layout of the proposed chip.

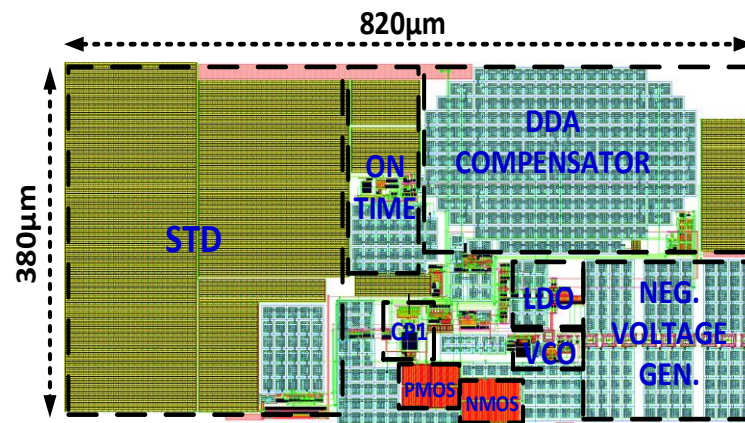


Figure 15. Layout of the proposed design.

Table 1 shows the performance of the proposed DC-DC buck converter using AOT, ACP, STD, ZCD, and NLS. Table 1 helps synthesize the results of this proposed converter, also giving an overview on the consistency of performance and important parameters across varying load conditions and input voltages. The buck converter with the AOT control achieves the expected results in terms of performance and stable operation. The voltage of the signals  $V_{OUT}$ ,  $V_{SW}$ , and  $I_L$  with each separate output load (given  $I_{LOAD}$  equal to 120, 12, 1.2, and 0.012 mA) are shown in Figure 16. In Figure 16a the  $V_{OUT}$  signal has a small ripple and  $V_{SW}$  has no damped oscillations during the falling edge of  $V_{OUT}$  because the  $C_{LOAD}$  capacitor has been charged and discharged at high frequency, and the average current  $I_L$  remains high under a heavy load. In this case, when  $V_{OUT}$  has exhibited an increasing ripple and  $V_{SW}$  has damped oscillations during the falling edge of  $V_{OUT}$  due to  $C_{LOAD}$  being charged and discharged at a low frequency, with the average load current  $I_L$  is low in the light and ultra-light load modes. The switching frequency and the average load current  $I_L$  have depended on the output load variation ( $I_{LOAD}$ ). As shown in Figure 16b–d, the  $T_{SLEEP}$  time varies from 3.7  $\mu$ s to 3.8 ms, the waveforms for  $V_{SW}$  and  $I_L$  annotated remain shape steady, while the  $V_{OUT}$  has a gradually increased ripple. To reduce the current loss in the inductor in the heavy load mode, both switches  $S_{WP}$  and  $S_{WN}$  have been turned off, creating an oscillation between  $L$  and  $C_{LOAD}$ , which causes the damped oscillations of  $V_{SW}$  during the falling edge of  $V_{OUT}$ .

Table 1. Synthesizing the performance of the proposed DC-DC converter.

| Condition        | Output Voltage (V) | Output Ripple (mV) | Frequency (kHz) | Efficiency (%) | Load (mA) | $T_{SLEEP}$ ( $\mu$ s) | Input Voltage (V) |
|------------------|--------------------|--------------------|-----------------|----------------|-----------|------------------------|-------------------|
| Heavy load       | 1.24               | 3                  | 1300            | 93.35          | 120       | 0                      | 3.3               |
| Light load       | 1.235              | 7                  | 260             | 88             | 12        | 3.7                    |                   |
|                  | 1.23               | 10                 | 30              | 83             | 1.2       | 30                     |                   |
| Ultra light load | 1.228              | 12                 | 0.27            | 65             | 0.012     | 3800                   |                   |
| Heavy load       | 1.231              | 2.8                | 1230            | 96.2           | 120       | 0                      | 2.8               |
| Light load       | 1.23               | 6.5                | 230             | 94             | 12        | 3.6                    |                   |
|                  | 1.228              | 9.2                | 28              | 89             | 1.2       | 28.5                   |                   |
| Ultra light load | 1.225              | 11.5               | 0.25            | 72             | 0.012     | 3750                   |                   |

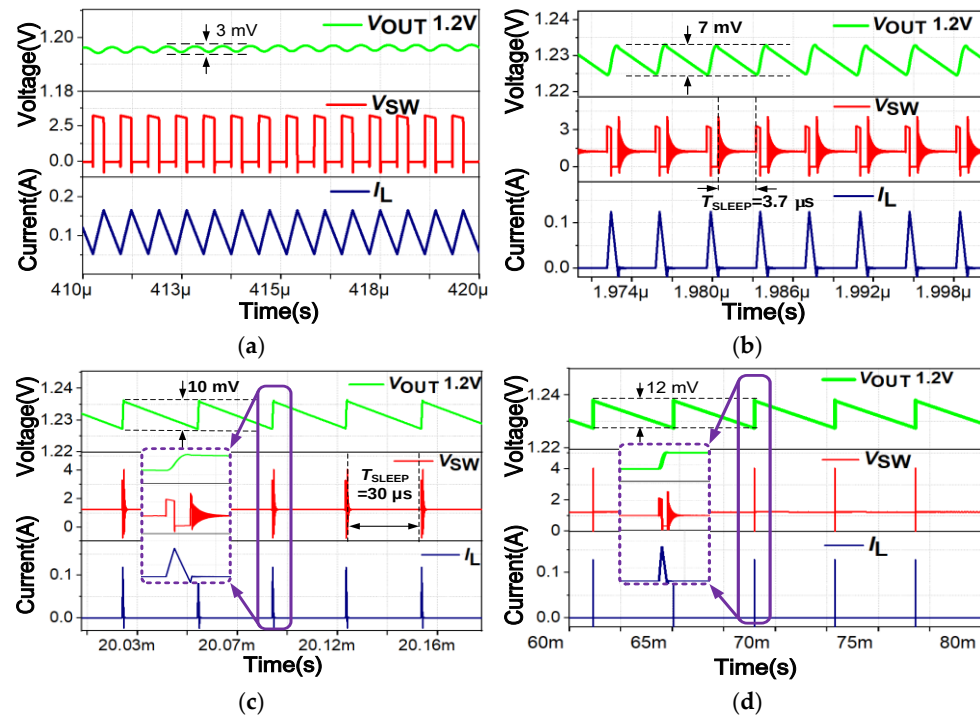


**Figure 16.** The waveforms voltage  $V_{OUT}$ ,  $V_{SW}$ , and current  $I_L$  (a)  $I_{LOAD} = 120$  mA; (b)  $I_{LOAD} = 12$  mA; (c)  $I_{LOAD} = 1.2$  mA; (d)  $I_{LOAD} = 12$   $\mu$ A at  $V_{BAT} = 3.3$  V and  $V_{OUT} = 1.2$  V.

In Figure 17, the simulation results of the adaptive on-time (AOT) controller generates the signal control  $S_{WP}$  and  $S_{WN}$  shown with two load conditions, which are set to 120 mA and 12 mA, respectively. In the heavy load condition of 120 mA, as shown in Figure 17a, the turn-on time ( $T_{ON}$ ) is 450 nS, and the switching frequency is 1.3 MHz, with the  $S_{WP}$  achieves a negative voltage of  $-0.5$  V. The utilization of two PTS  $S_1$  and  $S_2$  switches combined with the control logic block creates a dead time to prevent the conduction mechanism from being interrupted. Under the light load condition of 12 mA, as shown in Figure 17b, the switching frequency is only 250 kHz, and the  $T_{ON}$  is 205 nS. The  $S_{WN}$  turns off when a negative current is detected in the inductor to optimize efficiency. In this mode, noise may occur in the pulses at  $T_{SLEEP}$  due to the oscillation of  $L$  and  $C_{LOAD}$  when  $S_{WN}$  is closed. Figure 18a shows how the transient behaves when the load changes from 120 mA to 12 mA and reverses the process. The under voltage and overshoot voltage is 85/89 mV with a recovery time of 60/50  $\mu$ s. Figure 18b shows the transient response with a light load of 12  $\mu$ A to 12 mA. The output voltage occupies 20  $\mu$ s to recover stably, with an undershoot of 79 mV. The current inductor ( $I_L$ ) responds to changes in the condition of the output load optimizing the converter's performance. Figure 19 shows the effect of varying temperatures on the output voltage with the input 2.8 and 3.3 V. Under a heavy load, the temperature impact is more pronounced due to higher power dissipation in the switching transistors. As the ambient temperature increases, the junction temperature rises, leading to an increased  $R_{DS(ON)}$  of the power switches, which in turn increases the conduction loss and causes a slight drop in  $V_{OUT}$ . Under a light load, temperature impact is less significant since the internal power dissipation is already minimal. However, control circuits, bias current sources, and analog references may be affected by temperature drift if not properly compensated. During the entire stabilization process, there is no disturbance or oscillation that causes the instability of the output voltage. In particular, the current consumption of the low power control when the current load of 120, 12, and 0.012 mA is depicted in Figure 20. It reflects the average current consumption of the control blocks using a voltage  $V_{DD} = 1.2$  V from the LDO block. It can be observed that the current consumption of the

blocks decreases as the load current decreases, indicating that the system operates optimally with quite efficient current consumption. When the output current load is changed from 12  $\mu$ A to 120 mA: (1) As shown in Figure 21a, when the battery voltage  $V_{BAT}$  is 2.8 V, the efficiency is increased from 73% to 96.2%. Although the battery voltage  $V_{BAT}$  is increased to 3.3 V, the efficiency is also achieved, increasing from 65% to 93.35%. (2) When the battery voltage is investigated at 2.8 and 3.3 V, the ripple output voltage is as shown in Figure 21b, which changes insignificantly and shows stability around 1.2 V. (3) Figure 21c shows the situation where the switching frequency of the buck converter is varied from 250 Hz to 1.3 MHz. The low consumption of the low-power control block will improve the overall conversion efficiency while still maintaining the accuracy of the output voltage at 1.2 V.

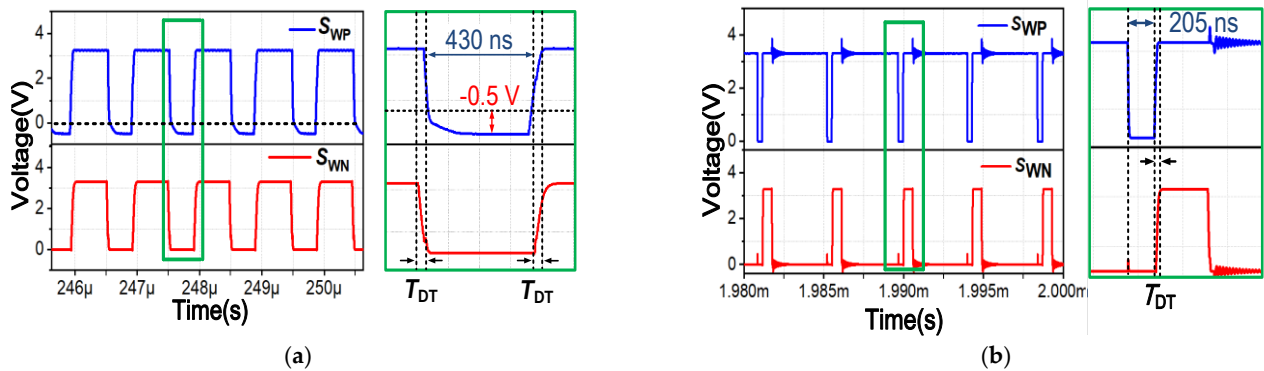


**Figure 17.** The control signal of SWP and SWN: (a) heavy load mode; (b) light and ultra-light load modes.

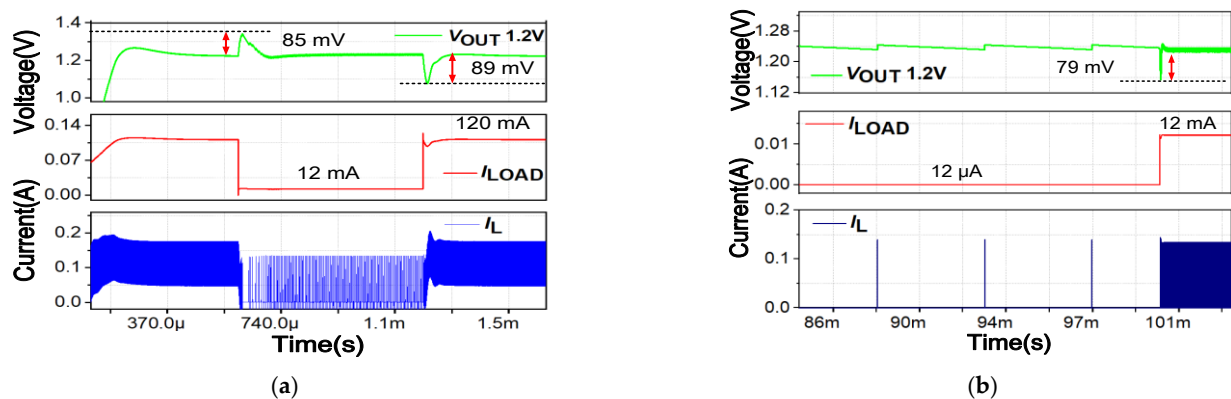


**Figure 18.** The voltage  $V_{OUT}$ ,  $I_{LOAD}$ , and current  $I_L$  at  $V_{BAT} = 2.8$  V (a) when the load changes from 120 mA to 12 m and (b) when the load changes from 12  $\mu$ A to 12 mA.

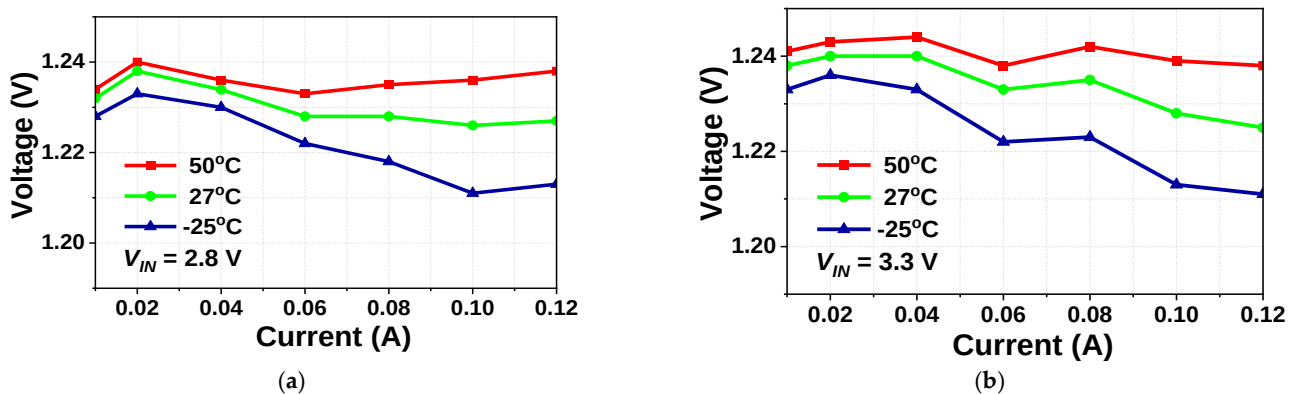


**Figure 19.** The effect of various temperature on the output voltage with an input voltage of (a) 2.8 and (b) 3.3.

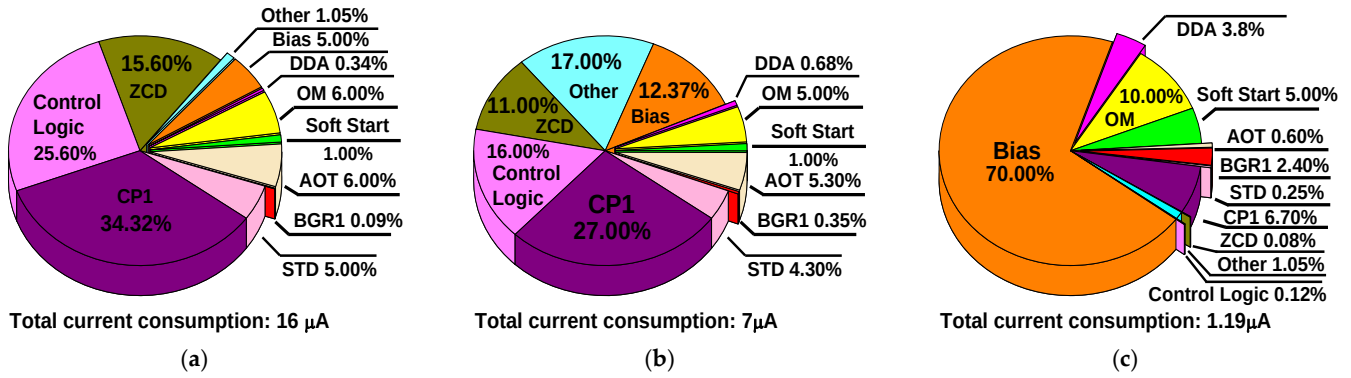


Figure 20. The AOT controller's consumption when the output load at (a) 120 mA, (b) 12 mA, and (c) 12 µA.

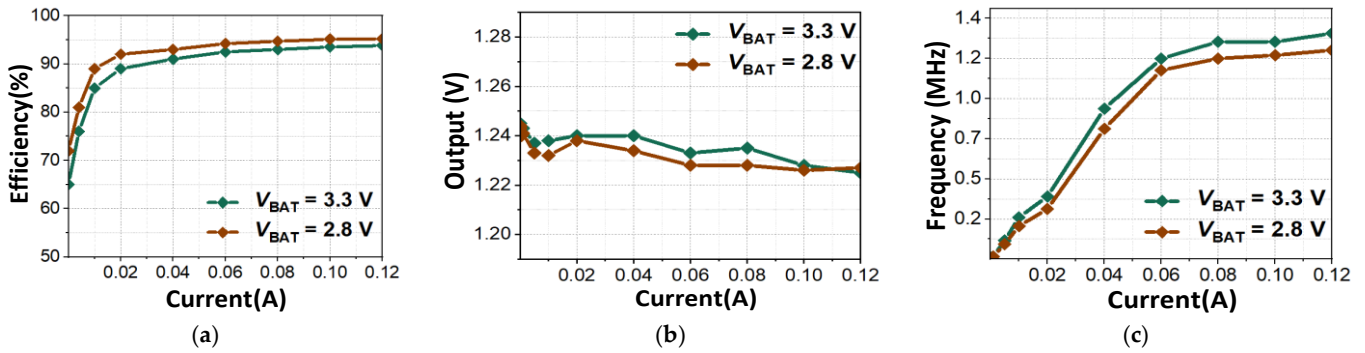


Figure 21. (a) Efficiency buck converter; (b) the output DC voltage value; (c) switching frequency adaptive.

The efficiency of the system can be calculated according to [36]:

$$\eta = \frac{P_{OUT}}{P_{IN} \cdot P_{Loss}} \quad (1)$$

where  $\eta$  is the efficiency of the systems;  $P_{IN}$  and  $P_{OUT}$  are the power of the input and output;  $P_{Loss}$  [37] is the power loss of the buck converter with the feedback loop.

$$\begin{aligned} P_{Loss} &= P_{in} - P_{out} = P_{Switching} + P_{Conduction} + P_{Gatedrive} + P_{Control} + P_{Other} \\ &= \frac{1}{2} \cdot V_{in} \cdot I_{load} \cdot (t_r + t_f) \cdot f_{sw} + I_{Load}^2 R_{DS(ON)} + Q_g \cdot V_{Gatedrive} \cdot f_{sw} + I_{Ctrl} \cdot V_{DD} + P_{Other} \end{aligned} \quad (2)$$

where  $P_{Switching}$  is the switching loss due to non-ideal CMOS switching power;  $P_{Conduction}$  is the conduction loss due to  $R_{DS(ON)}$  in power CMOS;  $P_{Gatedrive}$  is the gate charge/discharge loss of the power CMOS;  $P_{Control}$  is the feedback control loop loss;  $P_{Other}$  is the equivalent series resistance (ESR) loss of inductors, capacitors, and ringing;  $V_{in}$  is the input voltage of the buck converter;  $I_{Load}$  is the output load of the buck converter;  $t_r$  and  $t_f$  are the clock rise/fall delay;  $f_{sw}$  is the switching frequency;  $R_{DS(ON)}$  is the power CMOS (PMOS and NMOS) on-resistor;  $Q_g$  is the gate charge (PMOS and NMOS);  $V_{Gatedrive}$  is the gate control voltage;  $I_{Ctrl}$  is the quiescent current consumed by the feedback loop;  $V_{DD}$  is the voltage supply to the feedback loop. This study requires that the buck converter achieves high efficiency across a wide load range; hence, minimizing  $P_{Loss}$  is essential, particularly under ultra-light load conditions. The AOT (adaptive on-time) controller is presented with a supply voltage  $V_{DD}$  that is less than  $V_{IN}$  to reduce the biased current  $I_{Ctrl}$ , thus reducing  $P_{Control}$ . Furthermore, the control frequency of 1.3 MHz under substantial load situations is employed to mitigate output voltage ripple, whereby  $P_{Switching}$  and  $P_{Gatedrive}$  are comparatively elevated but negligible due to the considerable output power  $P_{OUT}$ . Nonetheless, when the frequency decreases to 250 Hz in the ultra-light load mode,  $P_{Switching}$

and  $P_{Gatedrive}$  considerably impact efficiency due to the minimal  $P_{OUT}$ ; however, these losses are substantially mitigated by the reduced switching frequency ( $f_{sw}$ ). For a fair comparison, Table 2 contains various references with simulated results, including [36–38]. The most important design specifications such as input voltage, output voltage, output ripple, current load, efficiency, and chip area are summarized in the table to compare the achieved performance levels of the proposed design with the state-of-the-art research. It is important to observe that in the application, the input voltage  $V_{BAT}$  ranges from 2.8 V to 3.3 V, requiring the stabilization of the output voltage and the adjustment of capacitors  $C_{F1}$  and  $C_{F2}$  to maintain  $V_{DD}$  at 1.2 V. At a voltage of  $V_{BAT} = 3.3$  V, with  $C_{F1} = 10$  nF and  $C_{F2} = 18$  nF, the value of  $V_{DD}$  is 1.19 V. At a voltage of  $V_{BAT} = 2.8$  V, with  $C_{F1} = 14$  nF and  $C_{F2} = 18$  nF, the voltage  $V_{DD}$  is 1.224 V. Any alterations to the input application will impact BGR2. Consequently, it is crucial to change  $C_{F1}$  and  $C_{F2}$  externally to obtain the requisite  $V_{DD}$  voltage within a specified input voltage range of 2.8 to 3.3 V for proper conversion functionality.

**Table 2.** Comparison between this work and other articles.

| Parameter                           | [20]        | [30]           | [38]        | [39]     | [40]        | [41] | This Work |
|-------------------------------------|-------------|----------------|-------------|----------|-------------|------|-----------|
| Result                              | Meas.       | Meas.          | Meas.       | Sim.     | Sim.        | Sim. | Sim.      |
| Num. of Control                     | 1           | 3              | 2           | 1        | 2           | 1    | 1         |
| Operation Modes                     | AOT         | PWM/<br>PFM/RM | PWM/<br>PFM | AOT      | PWM/<br>PFM | AOT  | AOT       |
| Process ( $\mu\text{m}$ )           | 0.13        | 0.13           | 0.18        | 0.18     | 0.18        | 0.18 | 0.18      |
| Input Voltage (V)                   | 1.8–3.3     | 2.2–3.3        | 2.2–5       | 5–12     | 3.3–5       | 5    | 2.8–3.3   |
| Output Voltage (V)                  | 1.2         | 1.7            | 1.8         | 0.33–1.2 | 0.5–3       | 1.2  | 1.2       |
| Inductor ( $\mu\text{H}$ )          | 4.7         | 3              | 4.7         | 2.2      | 500–3000    | 1.5  | 4.7       |
| Output Capacitor ( $\mu\text{F}$ )  | 4.7         | 3              | 1           | 47       | 50–200      | 20   | 4.7       |
| Output Ripple Max (mV)              | 30          | 180            | N/A         | N/A      | N/A         | 5    | 3         |
| $I_{LOAD}$ Max (mA)                 | 0.0001–2.65 | 0.01–20        | 0.2–200     | 5000     | 200         | 500  | 0.012–120 |
| Efficiency (@12 $\mu\text{A}$ ) (%) | 62          | 74.2           | 77          | N/A      | N/A         | 40   | 73        |
| Peak Efficiency (%)                 | 92.2        | 92.4           | 94          | 96       | 90          | 95   | 96.2      |
| Chip Area ( $\text{mm}^2$ )         | 0.14        | 1.1            | 0.405       | N/A      | N/A         | N/A  | 0.31      |

N/A: not available.

## 4. Conclusions

This paper presents a high-efficiency, low-power buck converter designed for a wide load range, targeting for mobile, IoT, and medical applications. The integration of an adaptive on-time (AOT) controller with a negative clock generator enables the converter to attain substantial efficiency across various output loads. The control block functions at 1.2 V ( $V_{DD}$ ) with an emphasis on reducing bias current usage in the BGR1, BGR2, ZCD, DDA, STD, OTD, and ACP blocks. The negative voltage generator (NVG) employs a deep n-well layout approach utilizing CMOS 180 nm technology, with the DC-DC buck converter occupying a chip area of 0.31  $\text{mm}^2$ . The simulation findings indicate that throughout an input voltage range of 2.8 to 3.3 V, the output voltage remains constant at 1.2 V, with a ripple variation of about 3 to 12 mV. The proposed converter achieves a peak efficiency of 96.2% at an output current load of 120 mA and 75% at 12  $\mu\text{A}$ . This indicates that a favorable comparison between the performance of the proposed DC-DC buck converter and the state of the art is possible.

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## References

1. Blaauw, D.; Sylvester, D.; Dutta, P.; Lee, Y.; Lee, I.; Bang, S.; Kim, Y.; Kim, G.; Pannuto, P.; Kuo, Y.-S. IoT design space challenges: Circuits and systems. In Proceedings of the 2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers, Honolulu, HI, USA, 9–12 June 2014; pp. 1–2. [CrossRef]
2. Roy, A.; Klinefelter, A.; Yahya, F.B.; Chen, X.; Gonzalez-Guerrero, L.P.; Lukas, C.J.; Kamakshi, D.A.; Boley, J.; Craig, K.; Faisal, M.; et al. A 6.45  $\mu$ W Self-Powered SoC With Integrated Energy-Harvesting Power Management and ULP Asymmetric Radios for Portable Biomedical Systems. *IEEE Trans. Biomed. Circuits Syst.* **2015**, *9*, 862–874. [CrossRef] [PubMed]
3. Pham, X.T.; Vu, T.K.; Nguyen, T.D.; Pham-Nguyen, L. A 1.2- $\mu$ W 41-dB Ripple Attenuation Chopper Amplifier Using Auto-Zero Offset Cancellation Loop for Area-Efficient Biopotential Sensing. *Electronics* **2022**, *11*, 1149. [CrossRef]
4. Pham, X.T.; Bo, Q.B.; Hoang, M.K.; Le, V.T.; Pham-Nguyen, L. 1.2  $\mu$ W 41dB Ripple Attenuation Chopper Instrumentation Amplifier Using Auto-Zero Offset Cancellation Loop. In Proceedings of the 2021 International Conference on Advanced Technologies for Communications (ATC), Ho Chi Minh City, Vietnam, 14–16 October 2021; pp. 167–171. [CrossRef]
5. Texas Instruments. 3 Quiescent-Current (Iq) Specifications to Understand. Technical Article SSZT118, November 2021. Available online: <https://www.ti.com/document-viewer/lit/html/sszt118> (accessed on 1 January 2022).
6. Poongan, B.; Rajendran, J.; Yizhi, L.; Mariappan, S.; Parameswaran, P.; Kumar, N.; Othman, M.; Nathan, A. A 53- $\mu$ A-Quiescent 400-mA Load Demultiplexer Based CMOS Multi-Voltage Domain Low Dropout Regulator for RF Energy Harvester. *Micromachines* **2023**, *14*, 379. [CrossRef] [PubMed]
7. Aguilon-Garcia, J.; Bañuelos-Sanchez, P. High-Efficiency DC-DC Converter for Large Input-Voltage Fluctuations in Solar Applications. *Chin. J. Electron.* **2015**, *24*, 502–507. [CrossRef]
8. Chen, W.-C.; Ming, D.-L.; Su, Y.-P.; Lee, Y.-H.; Chen, K.-H. A Wide Load Range and High Efficiency Switched-Capacitor DC-DC Converter with Pseudo-Clock Controlled Load-Dependent Frequency. *IEEE Trans. Circuits Syst. I* **2014**, *61*, 911–921. [CrossRef]
9. Hong, S.-W.; Park, S.-H.; Kong, T.-H.; Cho, G.-H. Inverting Buck-Boost DC-DC Converter for Mobile AMOLED Display Using Real-Time Self-Tuned Minimum Power-Loss Tracking (MPLT) Scheme with Lossless Soft-Switching for Light and Ultra-Light Load Mode. *IEEE J. Solid-State Circuits* **2015**, *50*, 2380–2393. [CrossRef]
10. Wibben, J.; Harjani, R. A High-Efficiency DC–DC Converter Using 2 nH Integrated Inductors. *IEEE J. Solid-State Circuits* **2008**, *43*, 844–854. [CrossRef]
11. Lee, C.-S.; Kim, S.-S.; Yu, J.-H. Load and Frequency Dependent CMOS Dual-Mode DC-DC Converter. *Microelectron. J.* **2019**, *92*, 104610. [CrossRef]
12. Yuan, B.; Liu, M.-X.; Ng, W.T.; Lai, X.-Q. Hybrid Buck Converter with Constant Mode Changing Point and Smooth Mode Transition for High-Frequency Applications. *IEEE Trans. Ind. Electron.* **2020**, *67*, 1466–1474. [CrossRef]
13. Kim, S.J.; Choi, W.-S.; Pilawa-Podgurski, R.; Hanumolu, P.K. A 10-MHz 2–800-mA 0.5–1.5-V 90% Peak Efficiency Time-Based Buck Converter with Seamless Transition Between PWM/PFM Modes. *IEEE J. Solid-State Circuits* **2018**, *53*, 814–824. [CrossRef]
14. Chen, P.H.; Wu, C.S.; Lin, K.C. A 50 nW-to-10 mW Output Power Tri-Mode Digital Buck Converter with Self-Tracking Zero Current Detection for Photovoltaic Energy Harvesting. *IEEE J. Solid-State Circuits* **2016**, *51*, 523–532. [CrossRef]
15. Shi, L.-F.; Jia, W.-G. Mode-Selectable High-Efficiency Low-Quiescent-Current Synchronous Buck DC–DC Converter. *IEEE Trans. Ind. Electron.* **2014**, *61*, 2278–2285. [CrossRef]
16. Li, Y.; Zhu, Z. A Constant Current Control Scheme for Primary-Side Controlled Flyback Controller Operating in DCM and CCM. *IEEE Trans. Power Electron.* **2020**, *35*, 9462–9470. [CrossRef]
17. Zhang, S.; Zhao, M.; Wu, X.; Zhang, H. Dual-phase DC–DC Buck Converter with Light-Load Performance Enhancement for Portable Applications. *IET Power Electron.* **2018**, *11*, 719–726. [CrossRef]
18. Nguyen, M.T.; Ha, T.P.; Pham, X.T.; Hoang, M.K. High-Efficiency Buck DC-DC Converter Using Automatic PWM/PFM Mode Control Based on Load Current Variation with Digital Soft Start. In Proceedings of the Electrical, Electronics, Mechanical and Systems Engineering Session of the 2023 International Research Conference of Sri Lanka Technology Campus, Colombo, Sri Lanka, 14–15 December 2023; pp. 310–317. Available online: <https://repo.sltc.ac.lk/handle/1/427> (accessed on 14 December 2023).

19. Kim, M.W.; Kim, J.J. A PWM/PPM Dual-Mode DC-DC Buck Converter with Load-Dependent Efficiency-Controllable Scheme for Multi-Purpose IoT Applications. *Energies* **2021**, *14*, 960. [\[CrossRef\]](#)
20. Santoro, F.; Kuhn, R.; Gibson, N.; Rasera, N.; Tost, T.; Graeb, H.; Wicht, B.; Brederlow, R. A Hysteretic Buck Converter with 92.1% Maximum Efficiency Designed for Ultra-Low Power and Fast Wake-Up SoC Applications. *IEEE J. Solid-State Circuits* **2018**, *53*, 1856–1868. [\[CrossRef\]](#)
21. Huang, T.-C.; Hsieh, C.-Y.; Yang, Y.-Y.; Lee, Y.-H.; Kang, Y.-C.; Chen, K.-H.; Huang, C.-C.; Lin, Y.-H.; Lee, M.-W. A Battery-Free 217 nW Static Control Power Buck Converter for Wireless RF Energy Harvesting with  $\alpha$ -Calibrated Dynamic on/off Time and Adaptive Phase Lead Control. *IEEE J. Solid-State Circuits* **2012**, *47*, 852–862. [\[CrossRef\]](#)
22. Zheng, L.; Song, Z.; Guo, P.; Guo, J.; Chang, C.; Huang, P.; Lu, L. An Ultra-low Quiescent Current Tri-mode DC–DC Boost Converter with 95.6% Peak Efficiency for Internet of Things Application. *IET Power Electron.* **2023**, *16*, 1527–1537. [\[CrossRef\]](#)
23. Gao, S.; Zhang, F.; Mei, H. Optimization Control Strategy for Light Load Efficiency of Four-Switch Buck-Boost Converter. *World Electr. Veh. J.* **2024**, *15*, 469. [\[CrossRef\]](#)
24. Asano, H.; Hirose, T.; Kojima, Y.; Kuroki, N.; Numa, M. A Fully Integrated, Wide-Load-Range, High-Power-Conversion-Efficiency Switched Capacitor DC–DC Converter with Adaptive Bias Comparator for Ultra-Low-Power Power Management Integrated Circuit. *Jpn. J. Appl. Phys.* **2018**, *57*, 04FF03. [\[CrossRef\]](#)
25. Hosseini, S.R.; Saberi, M.; Lotfi, R. A High-Speed and Power-Efficient Voltage Level Shifter for Dual-Supply Applications. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2017**, *25*, 1154–1158. [\[CrossRef\]](#)
26. Chandrasekhar, C.; Basha, M.M.; Das, S.M.; Hemakesavulu, O.; Dholvan, M.; Syed, J. Pass-Transistor-Enabled Split Input Voltage Level Shifter for Ultra-Low-Power Applications. *Micromachines* **2025**, *16*, 64. [\[CrossRef\]](#) [\[PubMed\]](#)
27. Lee, B.; Ma, D.B. A 20 MHz On-Chip All-NMOS 3-Level DC-DC Converter with Interception Coupling Dead-Time Control and 3-Switch Bootstrap Gate Driver. *IEEE Trans. Ind. Electron.* **2021**, *68*, 6339–6347. [\[CrossRef\]](#)
28. Liu, Z.; Cong, L.; Lee, H. Design of On-Chip Gate Drivers with Power-Efficient High-Speed Level Shifting and Dynamic Timing Control for High-Voltage Synchronous Switching Power Converters. *IEEE J. Solid-State Circuits* **2015**, *50*, 1463–1477. [\[CrossRef\]](#)
29. Yuan, B.; Ying, J.; Ng, W.T.; Lai, X.-Q.; Zhang, L.-F. A High-Voltage DC–DC Buck Converter with Dynamic Level Shifter for Bootstrapped High-Side Gate Driver and Diode Emulator. *IEEE Trans. Power Electron.* **2020**, *35*, 7295–7304. [\[CrossRef\]](#)
30. Park, Y.-J.; Park, J.-H.; Kim, H.-J.; Ryu, H.; Kim, S.; Pu, Y.; Hwang, K.C.; Yang, Y.; Lee, M.; Lee, K.-Y. A Design of a 92.4% Efficiency Triple Mode Control DC–DC Buck Converter with Low Power Retention Mode and Adaptive Zero Current Detector for IoT/Wearable Applications. *IEEE Trans. Power Electron.* **2017**, *32*, 6946–6960. [\[CrossRef\]](#)
31. Cheng, L.; Tang, K.; Ki, W.-H.; Su, F. Fast-Transient Techniques for High-Frequency DC–DC Converters. *J. Semicond.* **2020**, *41*, 112402. [\[CrossRef\]](#)
32. Nguyen-Thien, V.; Han, H.-D.; Pham-Nguyen, L.; Pham, X.T.; Hoang, M.K. 0.47- $\mu$ W Multi-Stage Low Noise Amplifier Employing 0.2-V-Supply OTA. In Proceedings of the 2022 IEEE Ninth International Conference on Communications and Electronics (ICCE), Nha Trang, Vietnam, 27–29 July 2022; pp. 190–194. [\[CrossRef\]](#)
33. Chauhan, S.; Mehra, R. CMOS Design and Performance Analysis of Ring Oscillator for Different Stages. *Int. J. Eng. Trends Technol.* **2016**, *32*, 234–237. [\[CrossRef\]](#)
34. Lee, C.; Yim, T.; Yoon, H. A Negative Charge Pump Using Enhanced Pumping Clock for Low-Voltage DRAM. *Electronics* **2020**, *9*, 1769. [\[CrossRef\]](#)
35. Tyagi, V.; Kalla, S.; Rana, V. Negative Voltage Generator and Current DAC Based Regulator for Flash Memory. In Proceedings of the 2021 34th International Conference on VLSI Design and 2021 20th International Conference on Embedded Systems (VLSID), Guwahati, India, 20–24 February 2021; pp. 17–22. [\[CrossRef\]](#)
36. Zhaoxia, L.; Qingfeng, L.; Jinkun, S.; Jian, L. A research of efficiency characteristic for Buck converter. In Proceedings of the 2010 the 2nd International Conference on Industrial Mechatronics and Automation, Wuhan, China, 30–31 May 2010; pp. 232–235. [\[CrossRef\]](#)
37. Liu, J.-M.; Wang, P.-Y.; Kuo, T.-H. A Current-Mode DC–DC Buck Converter with Efficiency-Optimized Frequency Control and Reconfigurable Compensation. *IEEE Trans. Power Electron.* **2012**, *27*, 869–880. [\[CrossRef\]](#)
38. Park, W.; Namgoong, G.; Choi, E.; Lee, B.; Park, H.; Ma, H.; Bien, F. A 94% Peak Efficiency Dual Mode Buck Converter with Fully Integrated On-Time-Based Mode Control for Implantable Medical Devices. *IEEE Trans. Circuits Syst. II* **2022**, *69*, 4458–4462. [\[CrossRef\]](#)
39. Zhang, Z.; Shi, H.; Lu, D.; Cao, P.; Hong, Z. An AOT Buck Converter with Adaptive TON Extender Achieving 2.5  $\mu$ s Settling Time in 4A Load Transient. In Proceedings of the 2022 IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA), Xi'an, China, 28–30 October 2022; pp. 176–177. [\[CrossRef\]](#)

40. Yu, J.; Hwang, I.; Kim, N. High performance CMOS integrated PWM/PFM dual-mode DC-DC buck converter. In Proceedings of the 2017 18th International Scientific Conference on Electric Power Engineering (EPE), Kouty nad Desnou, Czech Republic, 17–19 May 2017; pp. 1–4. [\[CrossRef\]](#)
41. Jiang, C.; Chai, C.; Han, C.; Yang, Y. A High Performance Adaptive On-Time Controlled Valley-Current-Mode DC–DC Buck Converter. *J. Semicond.* **2020**, *41*, 062402. [\[CrossRef\]](#)

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