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Using Triangular Gate Voltage Pulses to Evaluate Hysteresis and Charge Trapping Effects in GaN on Si HEMTs

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Abstract: Charge carrier traps due to crystal defects in GaN on Si HEMT devices are responsible for dynamic performance degradation, long-term reliability limitations, and peculiar failure modes. The behavior of traps depends on many variables including heterostructure quality, the specific device structure, and operating conditions. To study the short time dynamics of charge trapping and release on the threshold voltage shift and hysteresis of commercial normally off GaN HEMTs we use triangular 0–5 V gate voltage pulses in the μs to ms duration range. Measurements are performed for single pulses by varying pulse duration and for a train of a few pulses by varying their number. The results indicate that hysteresis and related threshold voltage shift occur after repeated pulses, suggesting an accumulation of trapped charges. However, for a triangular wave hysteresis vanishes, meaning that a dynamic balance between charge trapping and release is established in the device. This can be considered as a positive indicator of device robustness and reliability. The same method, used to measure the gate threshold voltage shift and dynamic R_{ON} after a 30 min off-state DC stress at V_{DS} = 55 V with a floating gate, highlights an appreciable performance degradation of the device.

Keywords: GaN on Si; normally off HEMTs; soft switching mode; triangular gate voltage pulses; hysteresis; charge trapping and release; dynamic R_{ON}; DC stress

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1. Introduction

In recent years, gallium nitride (GaN)-based high-electron-mobility transistors (HEMTs) [1] have emerged as a key technology in power electronics and RF communications due to GaN's unique combination of physical properties, such as a wide bandgap (3.4 eV), high electron saturation velocity, and excellent thermal conductivity. These attributes make GaN HEMTs particularly suited for high-temperature, high-voltage applications, including high-power switching converters where they offer low power losses and fast switching speeds.

Due to the lack of suitable substrates and to exploit the advantages given by integration, GaN is grown on (111) Si, whose orientation is the closest to the hexagonal wurtzite crystal structure of GaN [2]. Moreover, Si is much cheaper than other substrate materials such as sapphire or SiC. The different lattice constant of Si as compared to GaN gives quite a big lattice mismatch of 17% [2]. For this reason, a buffer layer is needed to reduce crystal defects formation, as an example an AlN nucleation layer followed by an AlN/GaN superlattice is often adopted among several possible solutions [3]. Whatever the solution used for the buffer layer, crystal defects are formed at different locations in the heterostructure. They act as traps for charge carriers, as shown schematically in Figure 1 for a normally off

p-GaN gate HEMT [4], and are responsible for degrading device performance and limiting long-term reliability.

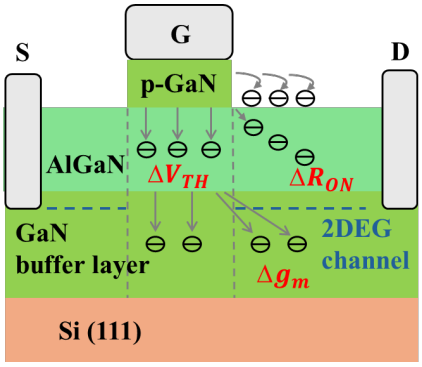

Figure 1. Schematic representation of surface and bulk traps in a normally off p-GaN HEMT affecting threshold voltage V_{TH}, dynamic R_{ON} and transconductance g_m.

Charge trapping occurs when carriers, such as electrons or holes, are captured by defect states at free surfaces, interfaces, or within the semiconductor layers themselves [5]. These trapping states can be due to structural defects, contamination during fabrication, or created from electrical and thermal stress during device operation [6]. Trapped electrons under the gate, both in the barrier (due to the small leakage gate current) and in the GaN buffer layer underneath the two-dimensional electron gas (2DEG) channel (due to channel depletion in the OFF state), can shift the threshold voltage (V_{TH}) of the GaN HEMT. This shift can manifest itself as a hysteresis in the drain current vs. gate voltage relationship, as measured by using a triangular gate voltage pulse where V_{GS} is first swept forward (rising) and then backward (falling) [7]. In a switching operation, hysteresis refers to a variation in the threshold voltage among switching cycles.

Understanding charge trapping and release dynamic mechanisms is critical for ensuring long-term reliability and performance stability. Moreover, failure modes of GaN HEMT devices during accelerated lifetime tests [8,9] are determined by traps [10] in contrast to standard power Si MOSFETs that are almost ideal. This study investigates hysteresis and threshold voltage shifts in GaN HEMTs by applying single and multiple triangular gate voltage pulses with a duration ranging from 1 µs to 10 ms to pristine devices, and to devices that undergo an extended time DC off-state stress test. The results indicate that for single pulses the V_{TH} shifts with associated hysteresis depend on pulse duration i.e., V_{GS} sweeping rate, whilst for a few pulse trains the V_{TH} shifts change with pulse number and hysteresis occurs after the first few repeated pulses, suggesting an accumulation of trapped charges. However, for extended time operation, i.e., with a triangular wave, hysteresis vanishes because a dynamic balance between charge trapping and release is reached. The presented results give useful insights into the short timescale dynamic and steady-state behavior of V_{TH} shift and hysteresis during a soft switching operation.

2. Materials and Methods

The circuit used for the measurements, shown in Figure 2, use a commercial normally off power GaN HEMT device produced by ST (SGT120R65AL, 650 V, V_{TH} = 1.8 V typ., DC R_{ON} = 75 mΩ typ., 15 A) operated in switching mode with a resistive load. The nominal switched drain current is set by choosing appropriate values for V_{DD} and R_D. For practical convenience, the circuit is implemented on a breadboard, ensuring the wire connections are as short as possible to minimize parasitic effects. A photo of the experimental setup for the measurements is shown in Figure 3.

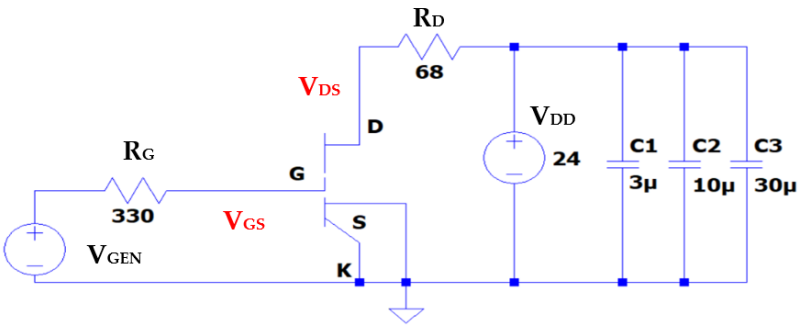

Figure 2. Circuit schematic used for measurements.

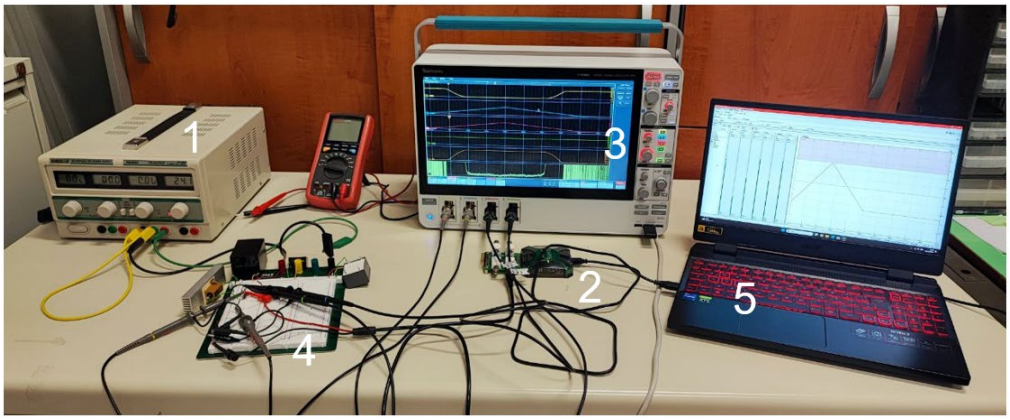

Figure 3. Experimental setup used for measurements. (1) LABPS23023 power supply, (2) Digilent analog discovery 2 multi-function programmable board, (3) Tektronix MSO54 digital oscilloscope, (4) breadboard with the measurement circuit and probes, and (5) PC with Waveforms 2 software program to generate triangular pulses.

The voltages across the gate and drain resistors, whose value is accurately measured in advance, are acquired by a four channels digital oscilloscope (Tektronix MSO54) through 1X accurately compensated probes. The triangular gate 0–5 V voltage pulses, with a duration ranging from 1 µs to 10 ms, are obtained through an arbitrary waveform generator (Tektronix AFG 31000 series or a Digilent analog discovery 2 multi-function programmable board). Relevant voltages together with the drain current $I_D = (V_{DD} - V_{DS})/R_D$ and the dynamic $R_{ON} = V_{DS}/I_D$ waveforms are shown in Figure 4 for a single triangular pulse of 10 µs duration. A triangular gate voltage pulse drives the device under a soft switching operation, as evidenced by the lack of drain current oscillations during the falling edge. It is worth noticing the non-specular shape of the rising and falling edges of I_D, a signature of the presence of charge trapping effects.

Polypropylene low-ESR capacitors (30 µF together with 10 µF and 3 µF) are connected in parallel between the power supply (LABPS23023 variable 0–60 V/0–6 A) voltage and ground for frequency compensation of its output impedance. This is necessary because, as shown in Figure 5 for nominal 24 V, we observe a drop in the output voltage of the power supply during device fast switching to the on state, where current sourcing is required. This occurs because during the response to a step current load, analog power supplies exhibit higher resistance than in DC because negative feedback is mostly ineffective, limiting the speed at which the current can change during fast switching events [11]. Figure 5 shows that with the shunt low-ESR capacitors the power supply voltage drop disappears almost completely.

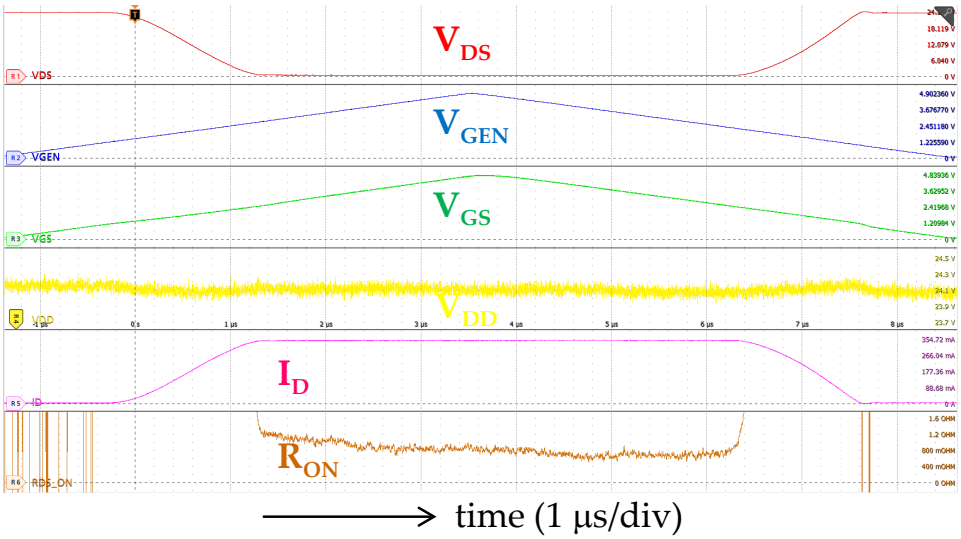

Figure 4. Waveforms of oscilloscope voltages (from top to bottom V_{DS}, V_{GEN}, V_{GS}, and V_{DD}), drain current I_D, and R_{ON} corresponding to a triangular voltage pulse of 10 µs duration. The horizontal time scale is 1 µs/div.

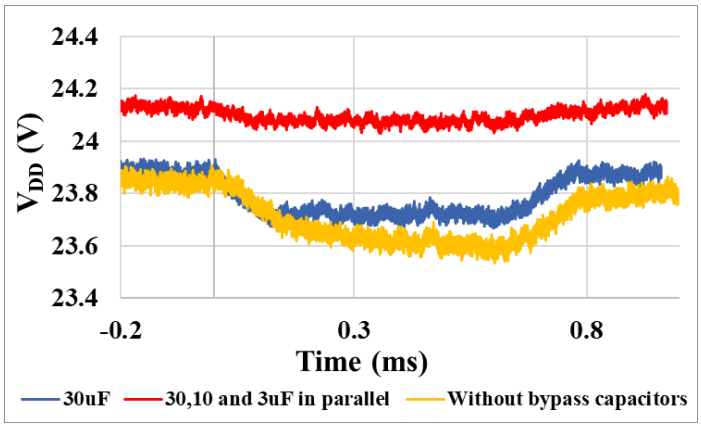

Figure 5. Power supply voltage drops during the on current drain conduction with and without compensating low-ESR polypropylene capacitors.

The 330 Ω gate resistor is used to limit the current required to the gate driver, in our case the analog output WaveGen of the analog discovery 2 board, which has a recommended output current of 10 mA at ± 5 V and a maximum absolute rating of 50 mA at ± 5.8 V. The value of this resistor is chosen to achieve a good trade-off between the gate charge/discharge peak current required to the driver and the fast switching time of the GaN HEMT in response to a rectangular gate voltage. We check in advance that even for a rectangular pulse duration of 1 µs the drain current can reach its regime value [12]. This has also been double-checked using an LTspice XVII software simulation of the circuit using the spice model of the device provided by the manufacturer.

As we are interested in measuring small voltages in the hundreds of mV range, such as the V_{DS} during the on state of the device, and so the oscilloscope is set to high-resolution mode, exploiting the maximum available bit dept (16 bits). Furthermore, to reduce noise, the bandwidth is limited for all four channels of the oscilloscope.

Before each measurement, the gate and drain terminals of the device are shorted to ground for two minutes to release any trapped charge leftover from the previous measurement and re-establish pristine condition, avoiding the presence of any form of 'memory effect'.

The HEMT under test has a typical threshold voltage of 1.8 V and a maximum V_{GS} of 7 V, hence, to drive it deeply into the ohmic region the gate is driven by triangular 0–5 V

voltage pulses of different duration. These are single pulses, a train of a few pulses, and a triangular wave, aiming at monitoring hysteresis and V_{TH} shift evolution from short to extended time intervals. The method allows for a detailed investigation of the dynamics of charge trapping and release and its influence on the threshold voltage shift. The same method is used to assess threshold voltage shifts after DC stressing the device in the off state for 30 min.

The plot of I_D vs. V_{GS} shows the possible presence of hysteresis, and the threshold voltage shift ΔV_{TH} is determined as the difference in V_{GS} values corresponding to I_D = 10 mA during the rising and falling edges of the drain current. The values of ΔV_{TH} and its sign give an indication of how the device accumulates or releases trapped charges under the gate heterojunction from material defects or interfaces between semiconductor layers.

To further study the initial transient behavior of the device a train of a few triangular V_{GS} pulses is used. This allows us to examine how the device responds to repeated pulses, and if and how hysteresis evolves with pulse number and charge accumulation. Moreover, important information can be drawn by comparing the response to a pulse train with the one to a single triangular pulse of duration equal to the pulse train. Finally, to complete the study a triangular V_{GS} waveform is also applied to evaluate long time dynamic steady-state hysteresis behavior.

As part of the device robustness evaluation, V_{TH} and R_{ON} are also evaluated after prolonged DC off-state stress tests to assess the possible presence of residual surface and interface traps in the drain access region and the device's ability to maintain operational performance after prolonged time electrical stress.

3. Results and Discussion

In actual devices, crystal defects and traps spatial distribution are not uniform and can change among devices. This can give different results for the actual numbers of hysteresis and threshold voltage shift. However, our measurements on several SGT120R65AL devices confirm that the general trend is well reproduced. For this reason and for consistency, the reported results are for the same single device. The voltage measurement errors can be assumed to be 5%, but for better clarity they are not indicated in the graphs.

The I_D vs. V_{GS} for the rising edge of single triangular pulses of increasing duration and for a nominal drain current of I_D =100 mA is reported in Figure 6. A reduction in threshold voltage V_{TH} is observed for longer pulse durations, suggesting the occurrence of reduced charge trapping (or increased charge release) under the gate of the GaN HEMT device.

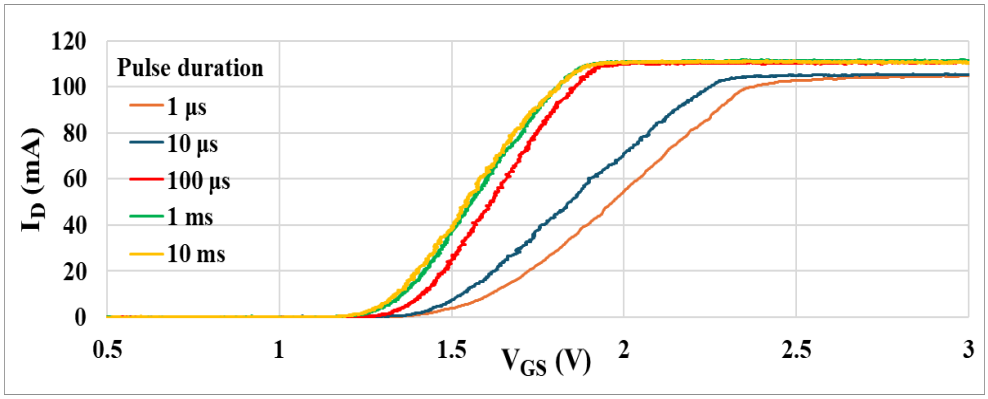

Figure 6. I_D (nominal 100 mA) rising edge vs. V_{GS} for single triangular pulses of increasing duration.

In GaN HEMTs, charges can be trapped in defects introducing localized deep states within the bandgap of the semiconductor materials, in the bulk, or at the interface between different layers (e.g., the p-GaN/AlGaN barrier). When longer pulses are applied, the

vertical electric field under the gate is applied for a longer time and this may help the release of trapped electrons in the p-GaN/AlGaN barrier originating from the very small gate leakage current flowing. Hence, the vertical electric field screening is reduced, and for the same channel conductivity, i.e., drain current, a smaller V_{GS} is required. The corresponding simultaneous increase in the large signal dynamic transconductance g_m is also indicative of a reduced dynamic current collapse, as shown in Figure 6.

The threshold voltage shift $\Delta V_{TH} = V_{GS\_UP} - V_{GS\_DOWN}$ as a function of pulse duration is reported in Figure 7 for the case I_D = 350 mA. The interesting feature highlighted by the graph is that the shift is negative and quite big for 1 µs pulse duration and then for longer pulses it becomes positive (apart from the 100 µs point) and much smaller. It can be said that ΔV_{TH} is positive or negative depending on the pulse duration.

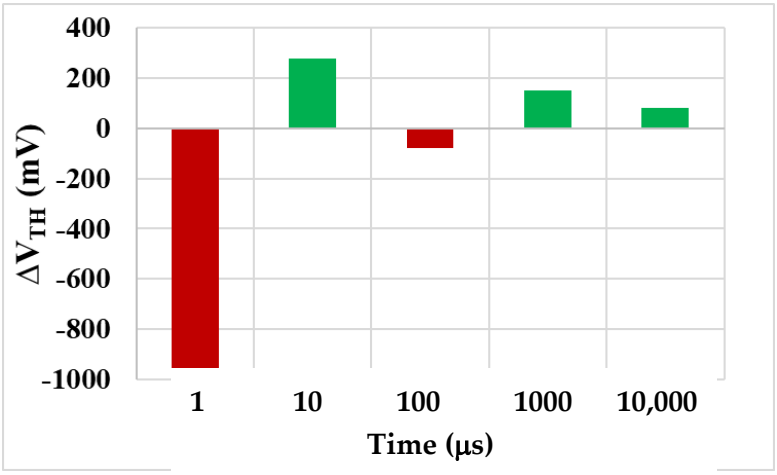

Figure 7. Threshold voltage shift ΔV_{TH} between rising and falling edges for a single triangular pulse as a function of pulse duration.

This behavior can be linked to a higher concentration of trapped electrons under the gate for shorter pulses that more effectively screen the gate voltage during the falling edge, in agreement with the rising edge seen in I_D vs. V_{GS} in Figure 6. In fact, for the same applied V_{GS} a negative variation in V_{TH} results in a higher I_D (which could damage the device), while a positive variation decreases the drain current, increasing conduction resistance and negatively impacting switching times.

To further study the dynamics of V_{TH} variations the response of the device to a train of a few triangular pulses is measured. First, a train of four triangular voltage pulses with a pulse duration of 250 µs is applied, hence a train duration of 1 ms, and the circuit parameters are set for I_D = 350 mA. The analysis of I_D vs. V_{GS} for each triangular pulse reveals that hysteresis does not occur right after the first pulse but becomes evident starting from the third pulse and becomes bigger for the fourth pulse, as shown in Figure 8.

This behavior can be explained for multiple pulses by the fact that during each on to off transition electrons in the channel are pushed towards the GaN buffer layer where they become trapped by bulk traps. When the device is driven back to the on-state by the next pulse of the train, these trapped electrons act as a "back gate" with negative bias, decreasing population in the 2DEG channel as compared to its equilibrium concentration and causing the V_{TH} shift under the gate [13–15]. Bulk traps in the GaN buffer layer can be assumed to be distributed in the whole device active area; hence, the "back gate" is extended in the gate-to-drain region as well, and this leads also to dynamic R_{ON} and g_m change [16].

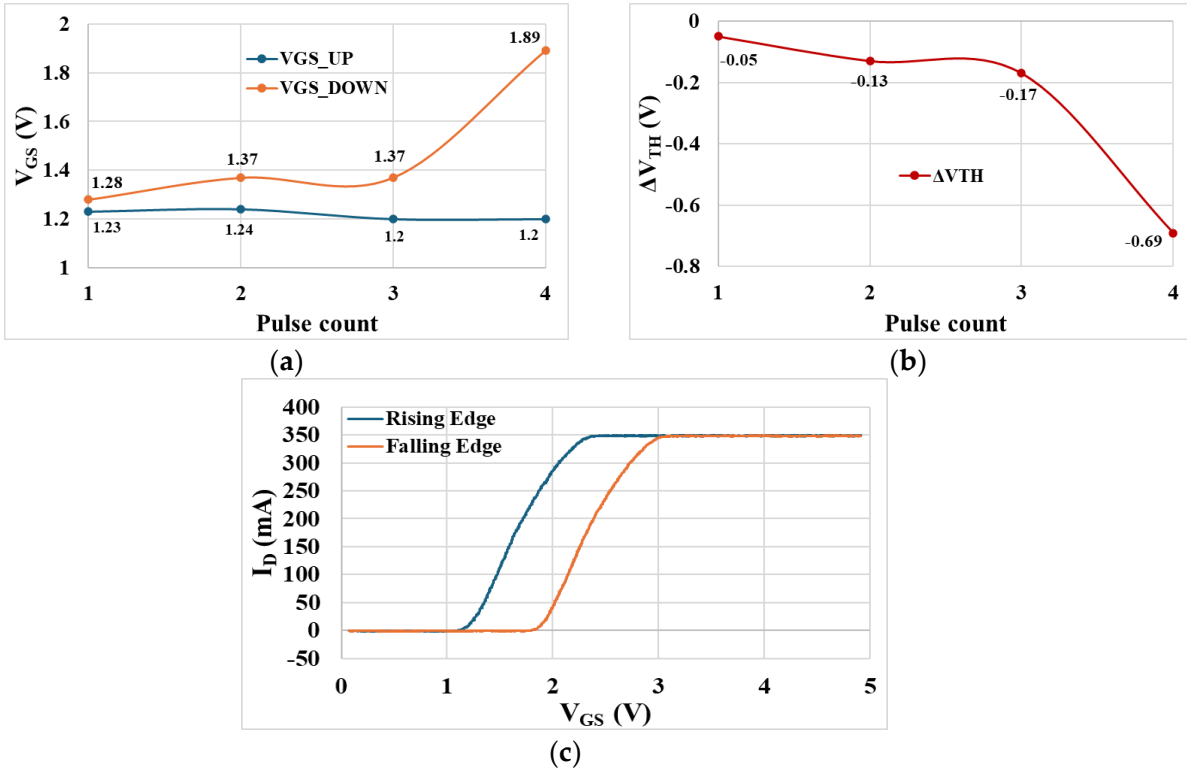

Figure 8. Response to a train of 4 pulses of 250 µs duration each (**a**) V_{GS_UP} and V_{GS_DOWN}, (**b**) ΔV_{TH}, and (**c**) hysteresis of I_D vs. V_{GS} of the fourth pulse.

If the response to a single triangular pulse of duration equal to the one of the four pulses train (i.e., 1 ms) is evaluated, the hysteresis in V_{GS} is almost negligible, as shown in Figure 9. This highlights how the application of a pulse train influences charge trapping in the buffer layer under the channel through a cumulative effect.

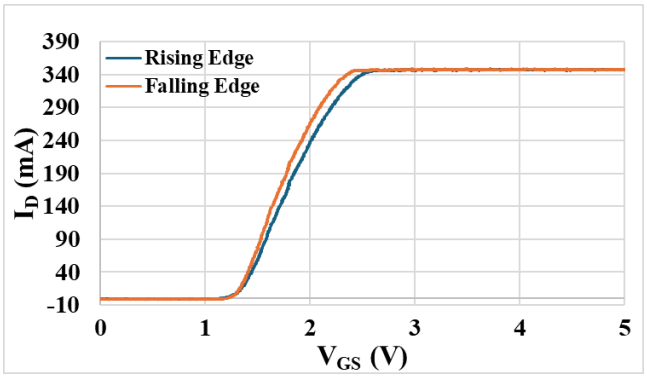

Figure 9. Hysteresis of I_D vs. V_{GS} for a single pulse with a 1 ms duration.

The slow electric field-assisted charge release dynamics are a key factor in explaining this behavior. If charge release mechanisms are slower than the pulse frequency, trapped charges accumulate over time, altering the internal electric field of the device and inducing hysteresis. This suggests that the device accumulates trapped charges across multiple switching cycles, and beyond a certain threshold hysteresis becomes evident. The absence of hysteresis during the first pulse of the train could indicate that the trapping process is associated with slow activation mechanisms or the progressive saturation of specific trapping states [17].

A further test, conducted by applying a train of 10 triangular V_{GS} pulses with a pulse duration of 100 µs, again for a train duration of 1 ms, suggests a progressive accumulation of trapped charges with pulse number. This is shown in Figure 10, where the hysteresis in V_{GS} is reported for the fifth and tenth pulse.

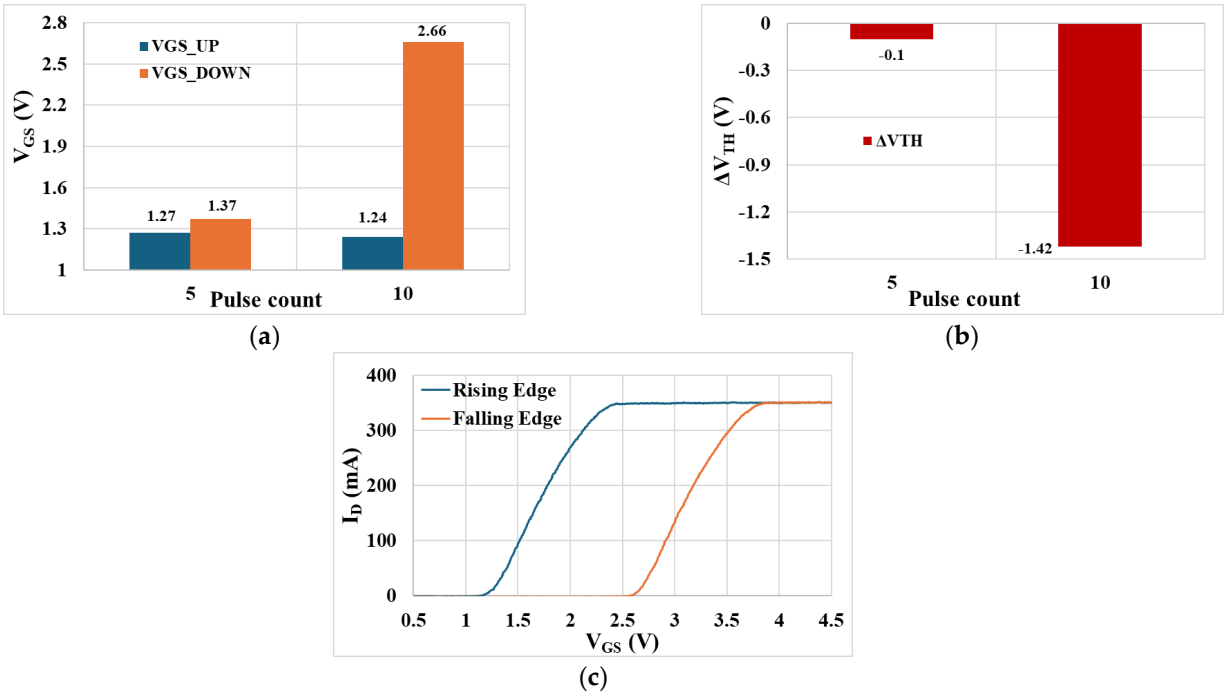

Figure 10. Response to a train of 10 pulses of 100 µs duration each (**a**) V_{GS_UP} and V_{GS_DOWN}, (**b**) ΔV_{TH}, and (**c**) hysteresis of I_D vs. V_{GS} of the 10th pulse.

The results show no significant hysteresis after the first few pulses, but as the pulse number progresses, particularly for the tenth pulse (the last one), a notable increase in hysteresis is observed, indicating substantial trapped electrons accumulation in the GaN buffer layer under the channel. It is important to note that the hysteresis at the tenth pulse ($\Delta V_{TH} = -1.42$ V) is greater than that at the fourth pulse in the four-pulse train ($\Delta V_{TH} = -0.69$ V). This confirms that hysteresis increases for a pulse train with a higher number of pulses.

Subsequently, a train of 10 longer triangular pulses with a pulse duration of 200 µs, for a train total duration of 2 ms, is applied and the device exhibits a similar trend, as reported in Figure 11. This suggests that the hysteresis phenomenon is primarily related to the progressive trapping of charges rather than just the pulse train period.

To investigate the release dynamics of trapped electrons in the buffer and barrier layer under the gate in the off-state we perform an additional test by driving the device with a train of 10 pulses, each with a period of 100 µs, followed by an off-state time interval of 100 µs and then a single 100 µs probe pulse.

As we can see from Figure 12, where the hysteresis of the tenth pulse and the one of the probe pulse are reported, the significant hysteresis of the tenth pulse has almost completely vanished after an off time of 100 µs, as measured by the probe pulse. Therefore, the 100 µs off time interval is sufficient to allow for the complete release of trapped electrons from the traps in the buffer and barrier layers under the gate.

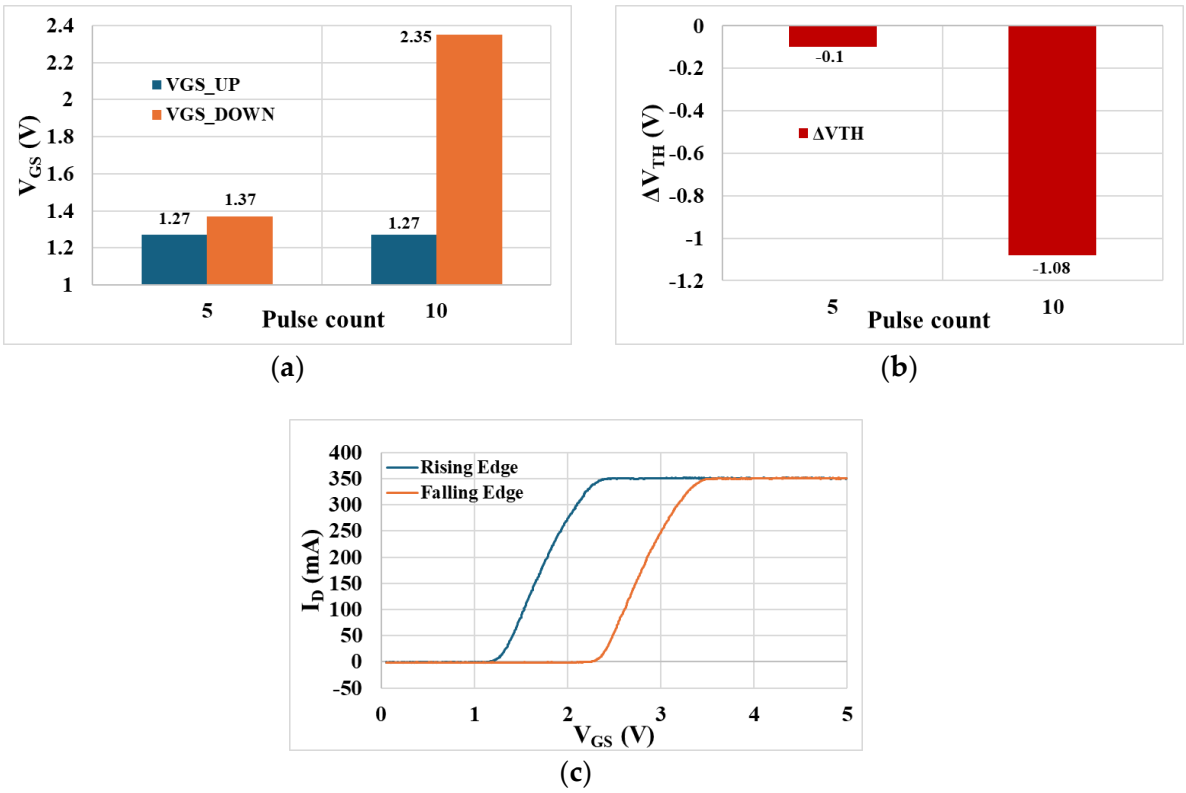

Figure 11. Response to a train of 10 pulses of 200 µs duration each (**a**) V_{GS_UP} and V_{GS_DOWN}, (**b**) ΔV_{TH}, and (**c**) hysteresis of I_D vs. V_{GS} of the 10th pulse.

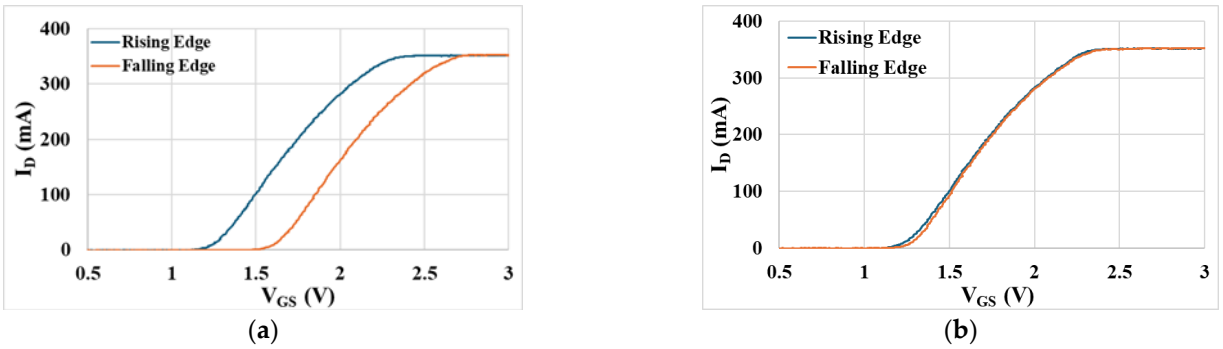

Figure 12. Hysteresis of I_D vs. V_{GS} for a train of ten pulses, each with a period of 100 µs, followed by an off-state time of 100 µs and then a single 100 µs probe pulse (**a**) of the tenth pulse, and (**b**) of the probe pulse after 100 µs off-state time.

For a shorter off-state time interval of 10 µs, hysteresis is observed for both the tenth pulse of the train and the probe pulse after the off-state time, as shown in Figure 13. This indicates that 10 µs is not a sufficient time interval for complete release and that residual trapped charges are still present under the gate. For the operating conditions under which the test is carried out, we can say that the average release time of trapped charges under the gate is at most 100 µs.

It is also interesting to note from Figure 13b that the hysteresis for the probe pulse has a positive shift in the threshold voltage, even though for all the preceding pulses of the train the shift is always negative. The explanation for this behavior can be as follows. The contribution to V_{TH} or V_{GS} shift can be twofold: (i) electrons trapped in the barrier under the gate giving a positive shift because of their screening bias effect for the positive V_{GS} and (ii) electrons trapped in the GaN buffer layer under the channel giving a positive shift of V_{GS} because they act as a back gate with negative bias. For an off time interval of

10 µs the release of trapped electrons under the gate is incomplete and it continues during the application of the probe pulse itself, resulting in the falling edge of the probe pulse experiencing a lower concentration of trapped electrons in respect to its rising edge, hence, the lower V_{TH} and V_{GS} for the same drain current.

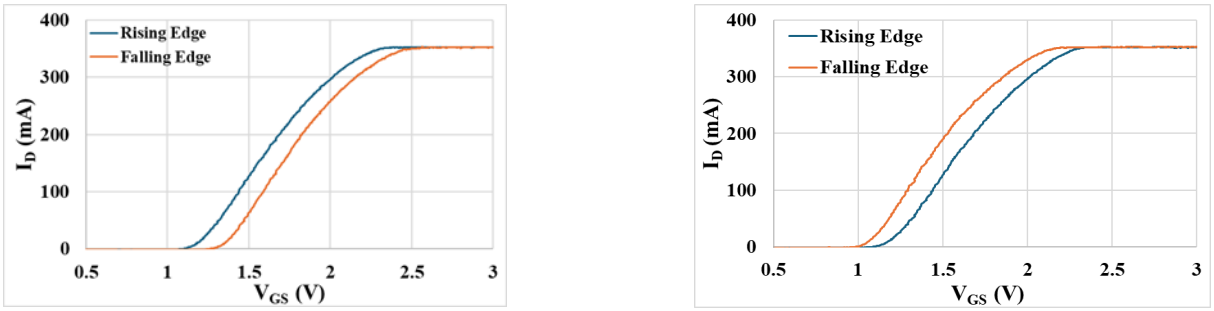

Figure 13. Hysteresis of I_D vs. V_{GS} for a train of ten pulses, each with a period of 100 µs, followed by an off-state time of 10 µs and then a single 100 µs probe pulse (**a**) of the tenth pulse, and (**b**) of the probe pulse after 10 µs off-state time.

A triangular wave driving the gate voltage can give an indication of hysteresis behavior at much longer times that we refer to as dynamic steady-state. In this case, the device behavior is monitored after a time interval of 1, 10, and 30 min from the application of the triangular wave gate voltage with pulse duration 1 ms, 100 µs, and 10 µs, corresponding to a repetition frequency, respectively, of 100 Hz, 1 kHz, and 10 kHz. The result shown in Figure 14 is for the measurement taken after 1 min with 100 µs pulse duration and nominal I_D = 350 mA.

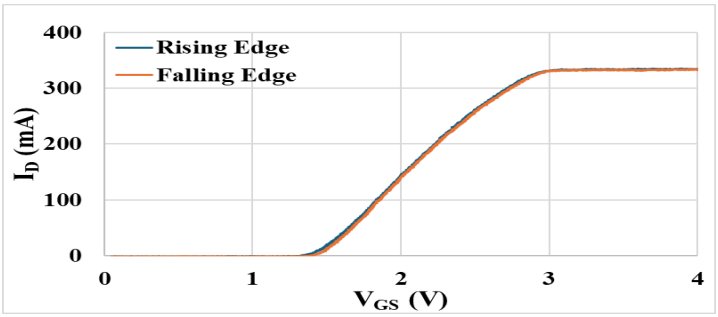

Figure 14. Hysteresis in response to a triangular waveform gate voltage with 100 µs pulse period and nominal I_D = 350 mA 1 min after the application of the driving voltage.

The primary observed result is that after 1 min there is no hysteresis and no significant threshold voltage shift. In fact, a difference smaller than 100 mV in V_{TH} can be considered negligible as compared to a V_{TH} = 1.4 V exhibited by the device in the specific operating conditions. In our case, this gives rising and falling edges of I_D vs V_{GS} very close one to each other. This behavior suggests that the device reaches a dynamic equilibrium between charge trapping and release both in the barrier layers under the gate and in the buffer layer under the channel, stabilizing the threshold voltage and limiting significant drain current variation over time.

Another relevant observation concerns the maximum I_D of 340 mA achieved, which is smaller than the nominal 350 mA value expected. Moreover, the slope of the I_D vs. V_{GS} rising and falling edge, which is indicative of the large signal dynamic transconductance g_m, is less steep, i.e., the g_m is reduced compared to the slope of the hysteresis graphs obtained with equivalent single pulses. Both of these results can be considered as a small

dynamic current collapse attributed to trapped charges in the barrier layers under the gate and in the GaN buffer layer under the channel.

An important observation is that the V_{TH} value of 1.5 V from Figure 14 is higher than the V_{TH} value of the first (single) pulse from Figure 8a, that is 1.23 V. In fact, the triangular wave is applied for a longer time interval, such as 1 min or more, and dynamic equilibrium between trapped and released charge carriers is reached, gradually eliminating the hysteresis. The increased V_{TH} value to 1.5 V is because the internal electric field due to trapped charges counteracts the external one due to the applied V_{GS}. The V_{TH} for a single pulse is lower because the device has not yet reached dynamic equilibrium in the trapping and release processes under the gate. This long-term dynamic steady-state equilibrium behavior can be interpreted as a positive indicator of device reliability.

In other words, when the device reaches this dynamic steady-state the traps in the semiconductor layers under the gate are either fully occupied by electrons or a balance in the trapping and release processes at each cycle is reached.

To further study the reliability of the device off-state, stress tests are carried out with a drain voltage of 55 V applied to the device for 1 min, 10 min, and 30 min, with the gate either short-circuited to ground or left floating. The small off-state leakage drain current flowing is supposed to promote charge trapping at the surface or interface traps of the p-GaN/AlGaN barrier in the gate-to-drain region [18]. This gives an increase in V_{TH} and R_{ON} and a decrease in g_m, indicating a degraded channel conduction due to trapped charges in the drain access region [14]. These off-state stress tests are non-destructive and repeatable with no creation of permanent defects, for example, those caused by the inverse piezoelectric effect at very high V_{DS} when applied even for relatively short times [19–21]. Immediately after each stress test the device is probed with a single 10 µs triangular pulse to measure V_{TH} and R_{ON}.

In the configuration with the gate short-circuited, negligible variations were observed for the stressed device compared to the pristine device. In fact, with the grounded gate the electric field at the drain side of the gate is zero. On the contrary, with the gate left floating the horizontal electric field generated by V_{DS} is the maximum and can induce charge trapping in the barrier region between the gate and drain. In this case, 1 min and 10 min off-state stress durations give no appreciable difference with a pristine device. On the contrary, after 30 min the stressed device exhibits an appreciable performance degradation, as shown in Figure 15.

Comparing Figure 15a,b, an increase in the V_{TH} from 1.2 V to about 1.5 V is evident for the stressed device, together with a decrease in the transconductance g_m that is the slope of the I_D vs. V_{GS} relationship. Moreover, hysteresis shows up for both pristine and stressed devices. For this kind of stress test, traps at different locations in the device contribute to the observed behavior. The R_{ON} reported in Figure 15c for the stressed device increases by about 25% compared to the one for the pristine device, suggesting a degraded channel current conduction efficiency or/and an increased drain side access resistance due to the trapped charges in the barrier layers and interfaces in the gate to drain region [22,23]. This effect may be even stronger for larger off-state V_{DS} voltages because of the increased electric field.

A longer switching delay in the off-to-on transition, as indicated by the blue trace being fully inside the red one in Figure 15c, is also evident. This implies that the stressed device requires more time to reach full conduction in response to the same applied gate voltage. This delay is likely associated with increased input and output capacitance due to the internal electric potential distribution that is modified by the charges trapped in the gate-to-drain access region.

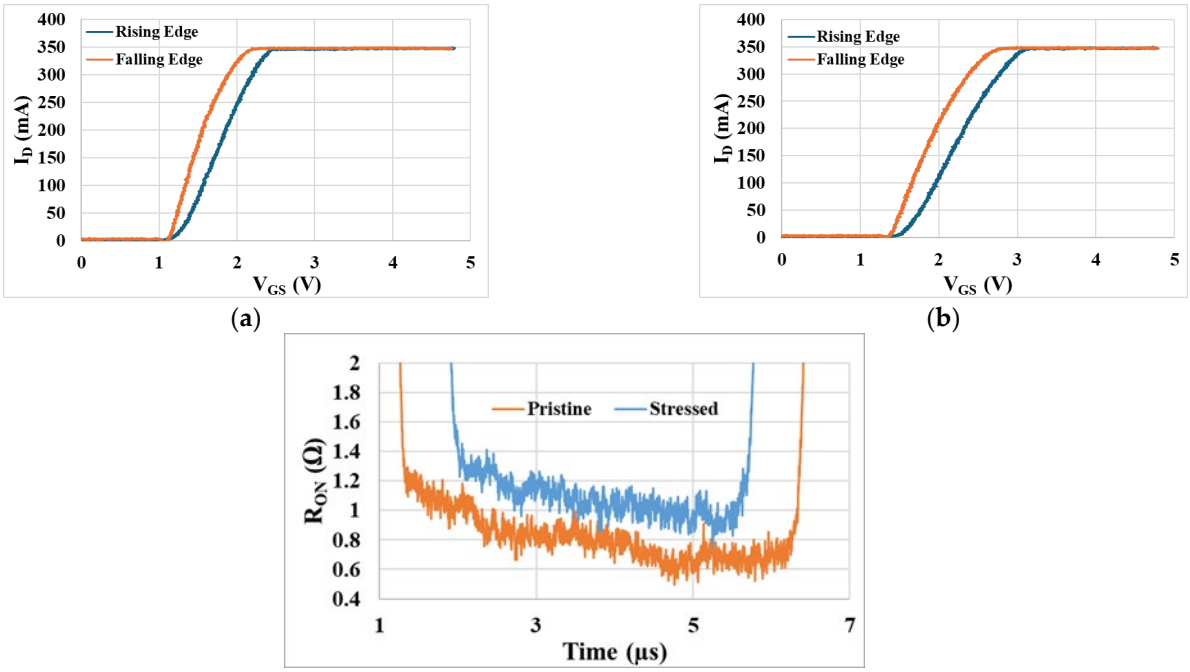

Figure 15. (**a**) Hysteresis of I_D vs. V_{GS} for a single pulse with a 10 µs duration before stress, (**b**) hysteresis of I_D vs. V_{GS} for a single pulse with a 10 µs duration of the same device after 30 min of off-state stress, (**c**) R_{ON} of the same device before (pristine) and after 30 min of off-state stress at 55 V, using a 10 µs triangular pulse and I_D = 350 mA.

4. Conclusions

This study demonstrates that charge trapping under the gate of GaN HEMT devices is a dynamic phenomenon that evolves over time and, for switching operations, through multiple switching cycles. By using triangular voltage gate pulses, hysteresis of I_D vs. V_{GS} appears only after a few repeated triangular gate pulses and the device reaches dynamic equilibrium between the trapping and release of charge carriers under the gate after 1 min of prolonged switching operation. Our results with trains of 4 or 10 triangular pulses indicate that hysteresis builds up through a progressive accumulation of trapped charges, influenced by semiconductor layers and interfaces quality and by the switching cycle duration. The results of the off-state stress test with a floating gate show that charge trapping in the drain access region takes place, leading to significant R_{ON} degradation, together with an increase in V_{TH} and a decrease in g_m. In summary, reliability and performance stability of GaN on Si HEMT devices for high-frequency and power applications can be improved by a reduction in defects and traps concentration. The absence of hysteresis after prolonged operation with triangular wave gate voltage suggests that the GaN HEMT device under study can achieve long-term operational stability, reducing the risk of threshold voltage instability which could compromise the efficiency and precision of circuits and systems utilizing these devices, such as high-power switching converters.

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Abbreviations

The following abbreviations are used in this manuscript:

HEMT	High-Electron-Mobility Transistor
2DEG	Two-Dimensional Electron Gas
V_{GS_UP}	Rising Edge Threshold Voltage
V_{GS_DOWN}	Falling Edge Threshold Voltage
R_{ON}	Dynamic Conduction Resistance
g_m	Dynamic Transconductance
V_{TH}	Threshold Voltage
ΔV_{TH}	Threshold Voltage Shift

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