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An Ultra-Wideband Low-Noise Amplifier with a New Cross-Coupling Noise-Canceling Technique for 28 nm CMOS Technology

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Abstract: This paper presents an ultra-wideband low-noise amplifier (LNA) with a new cross-coupling noise-canceling technique for 28 nm CMOS technology. The entire LNA contains two stages. The first stage employs inductively coupled Gm-booster technology, while the second stage is a novel asymmetric cross-coupling noise-canceling structure (ACCNCs). Through the introduction of these two key techniques, the LNA achieves balanced performance across a relative bandwidth of 56%. Input/output/inter-stage impedance matching uses a transformer-based network with series-parallel combinations of inductors and capacitors. The LNA is designed in a 28 nm CMOS process with a chip core area of $335 \times 665 \mu\text{m}^2$. The operating frequency range is 26–46 GHz. Post-layout simulation results show that the peak gain of the LNA is 12.6 dB, and the noise figure is between 2.9 and 4.2 dB across the wideband range. At a center frequency of 36 GHz with a supply voltage (V_{DD}) of 0.9 V, the input 1 dB compression point ($\text{IP}_{1\text{dB}}$) is -7.6 dBm , while the power consumption is 22 mW.

Keywords: CMOS; cross-coupling; Gm boosting; low-noise amplifier (LNA); noise cancelation; ultra-wideband



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1. Introduction

In recent years, with the rapid development of mobile internet and the widespread adoption of wireless communication devices, the demand for higher data transmission rates in wireless communication systems has been continuously increasing. The underutilized 5G millimeter-wave frequency band has gradually been recognized as an important solution to address the scarcity of low-frequency resources. Therefore, an increasing proportion of research focus has shifted toward millimeter-wave frequency. The low-noise amplifier (LNA) is a crucial part in the front end of millimeter-wave phased-array receivers, and its noise performance often determines key indicators such as the noise of the subsequent stages and the overall sensitivity of the receiver. On the other hand, the increasingly widespread application scenarios and the growing demand for transmission stability have made the operational bandwidth an important consideration for LNA design. As a result, wideband LNAs have gradually become a research focus. However, the strict requirements for noise, gain flatness, and input matching make it difficult to design an LNA with a matching network that fulfills these requirements. Maintaining such matching performance while operating over a wide bandwidth remains a significant challenge.

Different LNA architectures have different features and characteristics. Compared to traditional common-source (CS) LNAs [1], common-gate (CG) LNAs [2–4], cascode

(CS-CG) LNAs [5,6], or resistive shunt-feedback LNAs [7], noise-canceling LNAs [8–11] offer the advantage of canceling channel thermal noise without affecting other circuit performances; hence, this structure has been widely adopted. However, operating in a wide frequency range for 5G millimeter-wave communication still makes it very challenging to achieve a good balance among noise, gain, and input matching. Refs. [12,13] achieved good noise performance and high gain through advanced techniques. However, their operating bandwidths are limited, making them unsuitable for ultra-wideband operation. In contrast, ref. [14] extended the relative bandwidth to 59%, but the result required huge power consumption, which is a luxury in millimeter-wave applications, and its noise figure could not be maintained at a low level. The introduction of a Gm-boosted cross-coupling structure alters the original relationship between impedance and noise, effectively adding adjustable variables, which makes it possible to achieve an impedance that better satisfies performance requirements.

In this paper, an LNA with a new noise-canceling architecture is proposed. Inductive coupling is used at the input stage, and capacitive cross-coupling is employed at the second stage. The two noise-canceling paths are similar to a differential structure, which enables the implementation of capacitive cross-coupling. The circuit is designed using a 28 nm CMOS process, achieving a relatively good balance between gain, noise, linearity, and power consumption. The LNA provides an ultra-wideband operating range of 20 GHz and a fractional bandwidth (FBW) of 56%.

The structure of this paper is as follows: Section 2 discusses the principle and the analysis of key techniques implemented in the proposed LNA. Section 3 provides a detailed explanation of the LNA design methodology, outlining the step-by-step development process, including the design considerations for the transformer components. Section 4 presents the simulation outcomes to validate the proposed design, while Section 5 concludes the paper with a summary of the performance of the proposed LNA.

2. Principle of the Proposed LNA

The configuration of the proposed LNA is illustrated in Figure 1. The input RF signal is applied in a single-ended form and is simultaneously fed to the main amplifier M_1 in the first stage and the auxiliary amplifier M_2 along Path II. These two paths extend from the input to the two second-stage amplifiers and form the dual paths required for noise cancellation. At the output, the voltage signals from the two second-stage amplifiers are combined as differential input, while the in-phase noise components are canceled as part of the common-mode response. This differential output is converted back to a single-ended signal by an output balun, thus enabling a single-ended input and single-ended output LNA configuration. In this proposed LNA configuration, the first stage employs a Gm-boosted structure to enhance the effective transconductance of the main amplifier M_1 , and its noise contribution is reduced as a result. The second stage introduces an asymmetric cross-coupling structure, which makes the noise cancellation between the two signal paths better meet the design requirements. This cross-coupling structure also optimizes the matching process to achieve better minimum noise matching, maximum gain matching, and conjugate matching of the LNA. After a more effective trade-off among critical metrics, the LNA achieves preferable performance under ultra-wideband conditions.

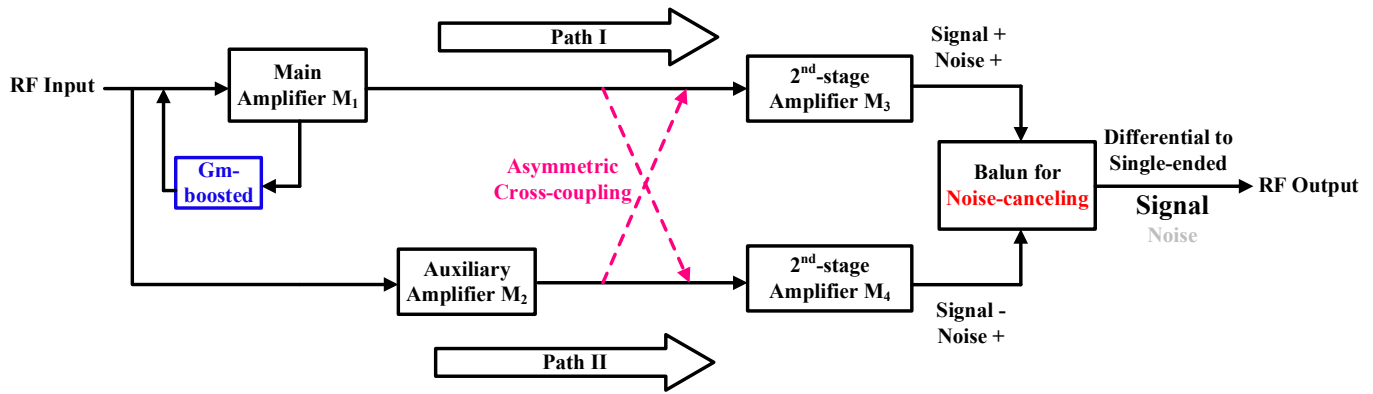


Figure 1. Configuration of the proposed LNA.

2.1. Transformer-Coupled Gm-Boosted Structure

The basic Gm-boosted structure is shown in Figure 2a, where Z_S represents the source impedance at the transistor input and Z_L is the load impedance; the noise factor of the common-gate transistor can be expressed as follows:

$$F = 1 + \frac{\overline{i_{nd}^2} \cdot \left(\frac{1}{1 + g_m Z_S} \right)^2}{\overline{i_{ns}^2} \cdot \left(\frac{g_m Z_S}{1 + g_m Z_S} \right)^2} = 1 + \frac{\overline{i_{nd}^2}}{\overline{i_{ns}^2}} \cdot \left(\frac{1}{g_m Z_S} \right)^2 \quad (1)$$

where i_{nd} represents the drain thermal noise current, and i_{ns} is the thermal noise generated by the source resistance; these two currents are calculated by the following:

$$\overline{i_{nd}^2} = 4kT\gamma g_{ds}\Delta f \quad (2)$$

$$\overline{i_{ns}^2} = \frac{4kT}{Z_S}\Delta f \quad (3)$$

the following can be further derived:

$$\begin{aligned} F &= 1 + \frac{4kT\gamma g_{ds}\Delta f}{4kTZ_S^{-1}\Delta f} \left(\frac{1}{g_m Z_S} \right)^2 \\ &= 1 + \frac{\gamma g_{ds}}{g_m^2 Z_S} \end{aligned} \quad (4)$$

Under input matching conditions, where $Z_S = 1/g_m$ and $\alpha = g_m/g_{ds}$, this expression becomes the following:

$$F = 1 + \frac{\gamma}{\alpha} \quad (5)$$

After introducing the Gm-boosted structure, the effective transconductance becomes $(1 + A)g_m$, and the matching condition is updated to $Z_S = 1/(1 + A)g_m$. By substituting these conditions into Equation (4), we obtain Equation (6):

$$F = 1 + \frac{\gamma}{\alpha(1 + A)} \quad (6)$$

It can be observed that the noise factor decreases. The reason for this improvement is that the effective transconductance has increased, while the minimum noise factor is still determined by process-related parameter α , and the g_m in $\alpha = g_m/g_{ds}$ remains the transistor's intrinsic transconductance, which is unchanged [15,16].

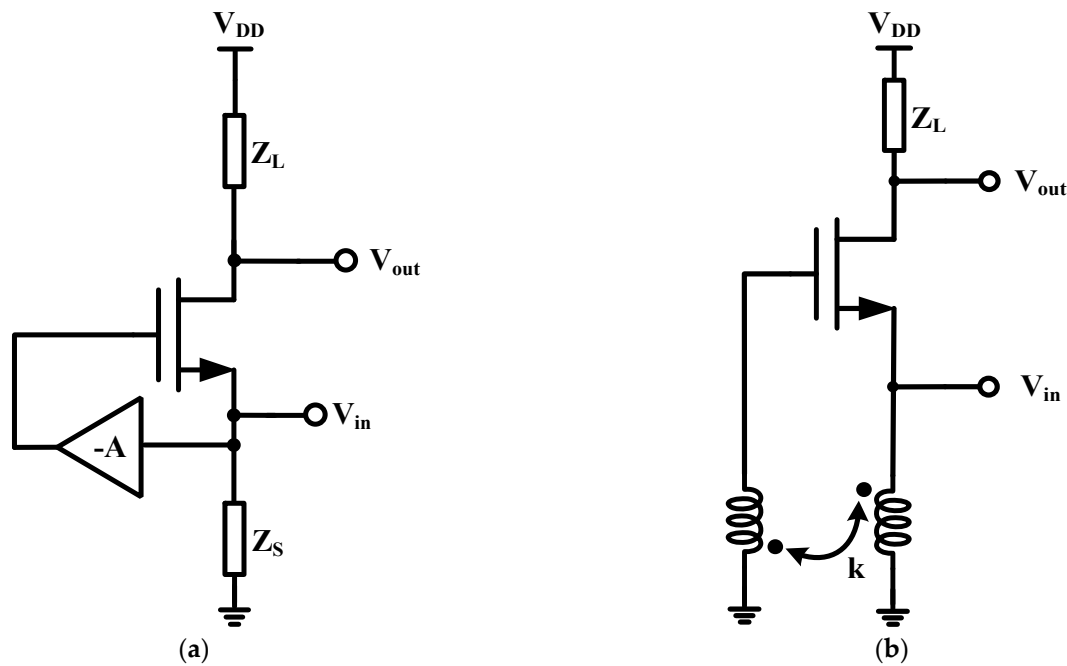


Figure 2. Gm-boosted structure and its implementation: (a) schematic of the common-gate amplifier with a Gm-boosted structure; (b) common-gate amplifier with a transformer-coupled Gm-boosted structure.

As shown in Figure 2b, the transformer-coupled structure represents a Gm-boosted implementation in which the signal is fed to the gate via transformer coupling. The transconductance-boosted ratio in this structure is $n \cdot k$, where n represents the turns ratio between the primary and secondary windings (equivalent to the square root of the inductance ratio), and k represents the transformer coupling coefficient.

In this design, the Gm-boosted structure and noise voltage coupling implemented through a transformer consume significant chip area. To validate the advantage of the Gm-boosted transformer structure, simulations were conducted on both optimized amplifier structures with and without the Gm-boosted transformer. The circuit without the Gm-boosted structure directly applies the input signal to the input of M_1 and the gate of M_2 , resembling the basic common-gate noise-canceling topology. Figure 3 shows the post-optimized gain and noise levels of the two topologies. The maximum gain and minimum noise figure are selected as the simulation parameters, thus excluding the influence of input impedance. It can be observed from Figure 3a that within the ultra-wideband operating range of 26–46 GHz, after the differential combination of the main and auxiliary amplifiers' output, the maximum gain of topology with the transformer-coupled Gm-boosted structure remains around 10.1–10.5 dB, while the maximum gain of the one without it drops to approximately 5.2–6 dB. Additionally, as shown in Figure 3b, the minimum noise figure of the first-stage amplifier with the Gm-boosted structure is about 2.2–2.4 dB, but upon removing the Gm-boosted transformer, the noise performance deteriorates significantly—minimum noise figure reaches 2.7–3.1 dB. Furthermore, to achieve optimized results, the topology without a Gm-boosted structure implements larger transistor dimensions, resulting in a DC bias current of 51.1 mA and a power consumption of 46 mW. In contrast, the amplifier with the transformer-coupled Gm-boosted structure uses a DC bias current of only 19.7 mA and a power consumption of 17.7 mW. This comparison clearly demonstrates the critical role of the transformer-coupled Gm-boosted structure in optimizing both performance and power consumption in the proposed design circuit.

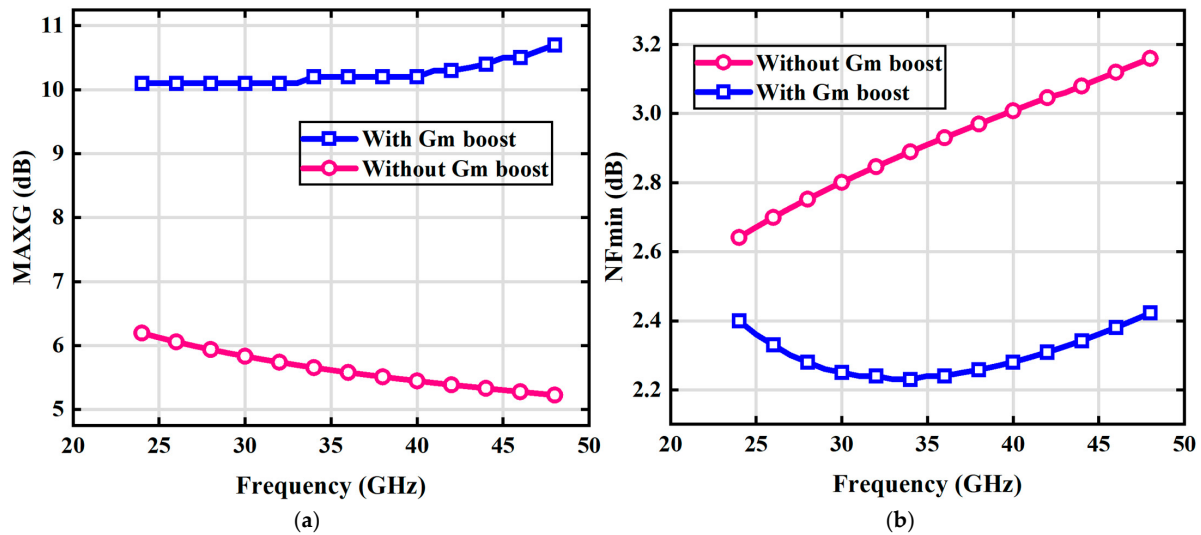


Figure 3. Post-optimization maximum gain and minimum noise figures of two topologies: (a) maximum gain with and without a transformer-coupled Gm-boosted structure; (b) minimum noise figure with and without a transformer-coupled Gm-boosted structure.

2.2. Asymmetric Cross-Coupling Noise-Canceling Structure

As shown in Figure 4, the second-stage common-source amplifier implements a capacitive cross-coupling structure on the terminals of source degeneration inductors L_{S1} , L_{S2} . At the input, a bias voltage is added to the gate of the common-source amplifier via an inductor, while the small AC signal is generally coupled from the first stage to the inductor connected to the gate. The cross-coupling structure works similarly to a Gm-boosted configuration. The inputs at the gates of the second-stage amplifiers, v_{in1} and v_{in2} , are out of phase, similar to differential signals. These signals are then capacitively coupled via C_{c1} and C_{c2} to the source of the other common-source amplifiers, enhancing the V_{gs} and thereby boosting the equivalent transconductance. After adding a cross-coupling structure to the second stage, the absolute value of the gate-source voltage can be approximately expressed as follows:

$$\begin{cases} |v_{gs1}| = |v_{in1}| + \frac{C_{c1}}{C_{gs1} + C_{c1}} |v_{in2}| \\ |v_{gs2}| = |v_{in2}| + \frac{C_{c2}}{C_{gs2} + C_{c2}} |v_{in1}| \end{cases} \quad (7)$$

In this structure, the two second-stage common-source amplifiers have different transistor dimensions, cross-coupling capacitances, and source degeneration inductances. Moreover, the output signal of the first stage is phase inverted but amplitude unequal. As a result, the entire structure forms an asymmetric cross-coupling topology, which allows for gain and noise optimization according to specific design requirements. Moreover, since cross-coupling is realized through passive capacitive components, little additional noise is introduced.

The effectiveness of the asymmetric cross-coupling can be demonstrated through simulation comparisons. Figure 5 shows the results of gain and noise after matching for the proposed LNA with and without the cross-coupling capacitor C_{c1} , C_{c2} . For the topology without cross-coupling, two different optimization strategies were applied, resulting in two different performance outcomes. It can be observed that the LNA with cross-coupling capacitors achieves both flat gain and low noise performance across the ultra-wideband frequency range of 26–46 GHz. In contrast, the LNA without cross-coupling capacitors under Optimization1 achieves a comparable noise figure but suffers from significant degradation in high-frequency gain and an excessively high gain peak at low frequencies. As a result,

its 3 dB gain bandwidth fails to cover the target frequency range. On the other hand, the non-cross-coupled LNA under Optimization2 exhibits gain performance similar to that of the proposed LNA but with a severely deteriorated noise figure—its minimum noise increases by approximately 1.2 dB, which is unacceptable for low-noise applications. In fact, the introduction of the cross-coupling structure modifies the relatively fixed parameters in the original second-stage noise-canceling structure. This provides greater design flexibility when facing the trade-off among noise matching, gain matching and conjugate matching in ultra-wideband scenarios, which are generally difficult to balance. The simulation results clearly demonstrate the effectiveness of the proposed asymmetric cross-coupling structure in improving the ultra-wideband performance of the LNA.

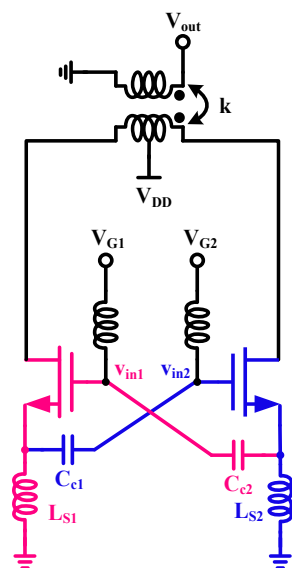


Figure 4. Cross-coupling structure implemented on a common-source amplifier with a source degeneration inductor.

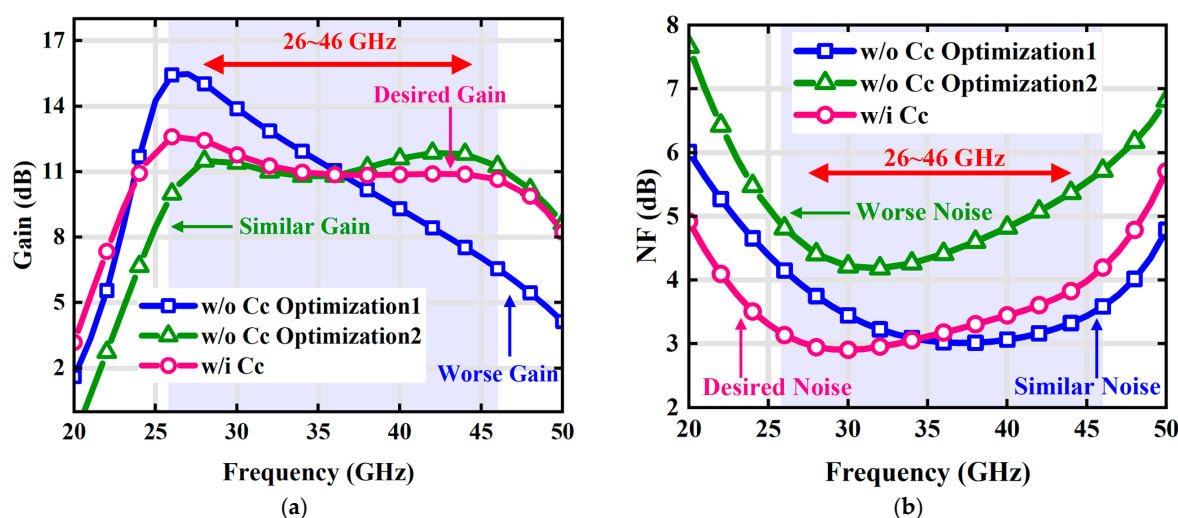


Figure 5. Performance comparison of LNAs with and without a cross-coupled structure: (a) maximum gain comparison; (b) minimum noise figure comparison.

3. Circuit Design

3.1. First-Stage Amplifier Design

In the millimeter-wave frequency range, transformer sizes are significantly reduced compared to those at low and mid frequencies. Furthermore, unlike transistor-based ac-

tive structures, the noise contribution from the transformer is negligible. In addition, the passive nature of the transformer structure results in lower nonlinearity, thereby maintaining the linearity performance of the original LNA design without introducing extra power consumption. The transformer-coupled structure also provides a flexible signal adjusting mechanism and makes it easier to transmit the input signal to the other amplifier. Considering these advantages, the transformer-coupled Gm-boosted structure is adopted in this work.

The complete circuit of the first-stage amplifier is illustrated in Figure 6. The main input amplifier M_1 adopts a common-gate topology, while the auxiliary amplifier M_2 utilizes a common-source structure. The second-stage amplifier is replaced by A_1 and A_2 and will be designed after the first-stage amplifier. The single-ended input signal is added to the source of M_1 , and the original input signal phase at M_1 's source is defined as positive. Furthermore, the noise voltage on the primary coil of the transformer in series with M_1 's source, which is generated by the channel thermal noise current I_n , is also defined as having a positive phase. The transformer is coupled according to the dot mark, as shown in the figure, with the coupling coefficient k . A DC bias voltage is applied at the center tap of the secondary coil, which serves as the small-signal ground, and it is mainly determined by the trade-off between gain and power consumption. The non-dot terminal of the secondary coil corresponding to the primary coil is connected to the gate of M_1 , thereby feeding a negative signal (i.e., an inverted signal) to achieve the Gm-boosted effect. On the other side of the secondary coil, the dot-marked terminal is connected to the gate of the auxiliary amplifier M_2 , delivering a positive signal in phase with the input signal and a positive noise voltage in phase with M_1 's source. In this structure, V_{G1} provides gate bias for both M_1 and M_2 . The direction of the channel thermal noise current is always from drain to source; thus, the noise voltage across the load inductor at the drain of M_1 is negative. In contrast, due to the characteristics of the common-gate amplifier, the signal at M_1 's drain remains in phase with the source input, i.e., positive. As for M_2 , due to the inverting amplification characteristic of the common-source topology, the signal and noise voltages at the drain are once again phase inverted, resulting in a negative output signal and a negative noise voltage. The resulting inverted signal and the in-phase noise voltage can be differentially combined and achieve noise cancellation. In this process, the noise voltage becomes part of the common-mode response, which means it is canceled by the differential architecture.

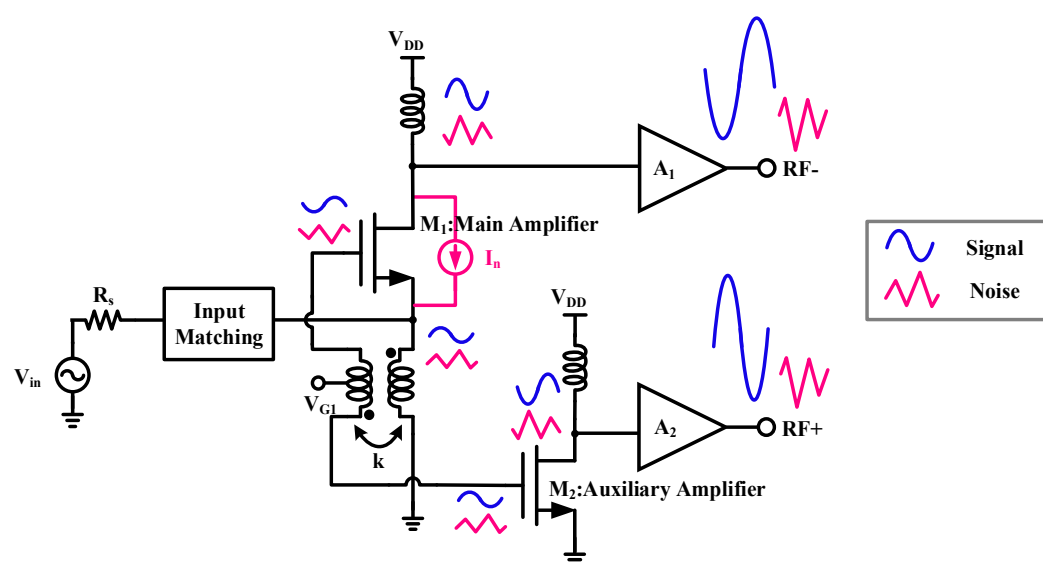


Figure 6. Construction of the first stage of the proposed LNA.

3.2. Second-Stage Amplifier Design

In this LNA design, it is necessary to simultaneously ensure the proper transmission of the output signal from the preceding stage, provide gate biasing, and introduce cross-coupling signals. At the same time, DC bias and AC signals should be added to correct nodes. To satisfy these requirements, a transformer is employed for signal transfer and inter-stage matching. Transformers on both paths are coupled to the dot-marked terminal, so they keep the original relative phase of the signal during transmission. The cross-coupling between the two paths of the second-stage amplifier is implemented as shown in Figure 6, which ensures that the bias voltage is not imposed on the source node of the opposite amplification path. Together with in-phase noise, the AC signal with opposite polarity at the gate of M_3 and M_4 is cross-coupled to the other transistor's source, thus adjusting the dimensions and parameters of devices in the second stage. According to the characteristics of inductors blocking DC and capacitors blocking AC, this process does not introduce complex feedforward issues. At the output of M_3 and M_4 , the inverted signal is combined through balun and converted into a single-ended signal, while the in-phase noise is canceled during this process.

Based on the selected amplifier topology and the cross-coupling technique introduced above, the proposed ultra-wideband LNA adopts an asymmetric cross-coupling noise-canceling structure (ACCNCS) for the second-stage design. The first-stage amplifier circuit designed in Section 2.1 is cascaded with the inter-stage matching network. The inter-stage matching network together with the ACCNCS is the part planned to be optimized via simulation in this design step. The schematic used for simulation is shown in Figure 7. In this step, the components mainly being tuned include the transistor dimensions of the second-stage amplifiers; the values of source degeneration inductors L_{S1} , L_{S2} and the cross-coupling capacitances C_{c1} , C_{c2} ; and the dimensions of passive components in the inter-stage matching network. Additionally, the selection of bias voltages V_{G2}/V_{G3} must consider both the effectiveness of noise cancellation and power consumption.

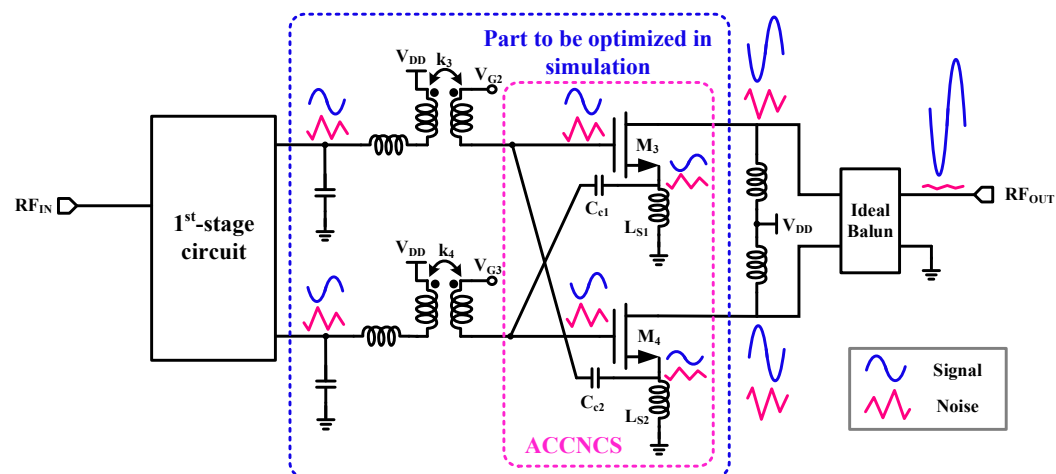


Figure 7. Schematic used for the optimization of the second-stage amplifiers and inter-stage matching network.

The effect of asymmetric cross-coupling capacitors is quite complex. As demonstrated above, their primary function is adjusting the noise-canceling process in the second stage. This allows the noise-canceling structure to cancel noise effectively while maintaining the gain level and flatness across the ultra-wideband frequency range. The value of the cross-coupling capacitances can be further tuned during the input matching and through multiple iterations, leading to improved overall LNA performance to meet ultra-wideband operation requirements.

3.3. Transformer Design

Among passive components, the modeling of transformers and inductors is most difficult, as their characteristics are more frequency-dependent than that of capacitors. These components also introduce a series of complex parasitic effects and non-ideal resistive losses. Such non-idealities can have a considerable impact on the overall performance of LNAs. To evaluate these effects, further circuit-level simulations were carried out, focusing on the transformers and inductors employed in the proposed design.

As an example, the transformer between the main amplifier M_1 and auxiliary amplifier M_2 in the first stage serves not only as a transmission path for the input signal but also as a key structure for realizing the G_m -boosted structure in M_1 . Therefore, its performance is critical to the function of the whole circuit. Detailed simulations are conducted to examine the influence of the first-stage transformer's parameters on circuit performance.

In Figure 8, the maximum gain and minimum noise figure at the center frequency of 36 GHz are selected as representative metrics to analyze the influence of the first-stage transformer's quality factor (Q) for the primary and secondary coil. The results clearly demonstrate that Q significantly affects both gain and noise performance. Higher Q values correspond to increased gain and a reduced noise figure. This is because the quality factor Q represents the magnitude of resistive loss at a given frequency for a specified inductance value, and the Q factor is defined as follows:

$$Q = \frac{2\pi f \cdot L}{R} \quad (8)$$

Resistance in the signal transmission path means thermal noise, which must be minimized in LNA design. This principle applies to most of the transformers and inductors used in the proposed LNA architecture. The difference is only that certain components—such as source degeneration inductors, which are not directly in the main amplification path—exhibit relatively limited influence on gain and noise performance, even when their Q factors are lower.

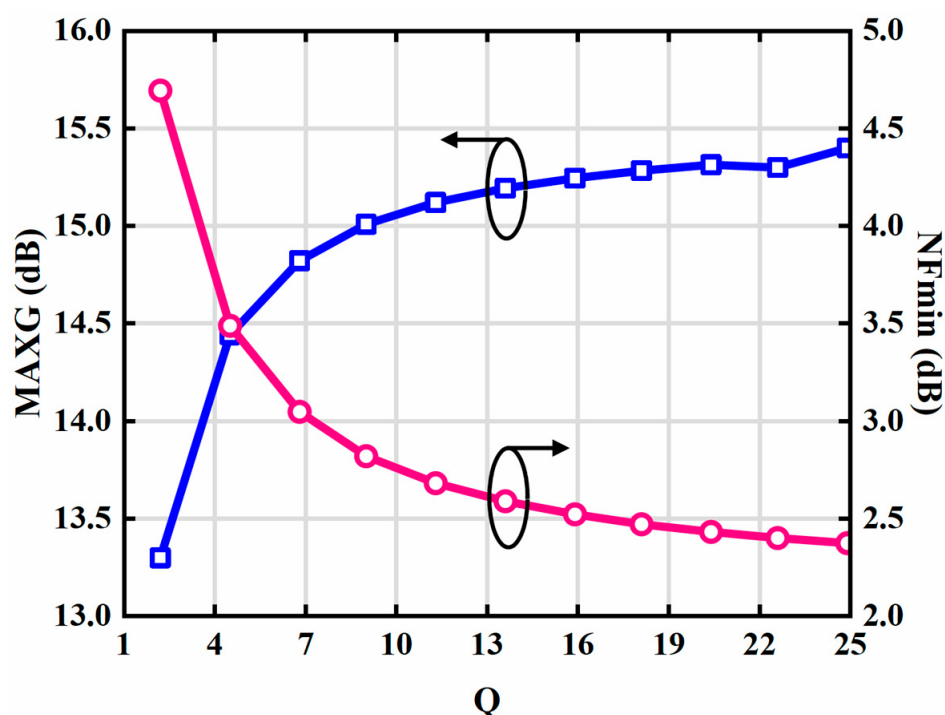


Figure 8. Simulated influence of the first-stage transformer coil quality factor (Q) on the LNA's maximum gain and minimum noise figure.

To ensure that the transformer and inductor meet the design requirements, electromagnetic modeling and simulation were performed. Figure 9a shows the model of the first-stage transformer, which serves both the Gm-booster structure of the main amplifier M_1 and signal transmission to the auxiliary amplifier M_2 . In this design, the thickest available top metal layer—Metal 9 (M9) (shown in blue in the figure) in the 28 nm process—is utilized as much as possible. With a thickness of 3.5 μm , M9 significantly reduces resistive losses and contributes to achieving high Q performance. Additionally, Metal 8 (M8) (shown in red in the figure) is used to bridge the windings, allowing both the primary and secondary coils to be fully implemented on the low-loss M9 layer. This strategy helps ensure a high Q factor for both coils. In addition, a center tap is drawn from the middle of the secondary coil to provide a DC bias voltage. Figure 9b,c presents the modeling parameters of the transformer. As shown in Figure 9b, the primary coil exhibits an inductance of approximately 280 pH, while the secondary coil has an inductance of about 380 pH. The coupling coefficient falls within the range of 0.6 to 0.7. Figure 9c illustrates that the Q factors of both the primary and secondary coils exceed 20 across the main operating frequency band of 26–46 GHz. Considering the previous analysis of the influence of the coil Q factor on circuit performance, the transformer exhibits characteristics that meet the performance requirements of the first-stage transformer in the proposed LNA. Its combination of moderate coupling and consistently high Q values ensures both effective signal transmission and a minimized noise contribution.

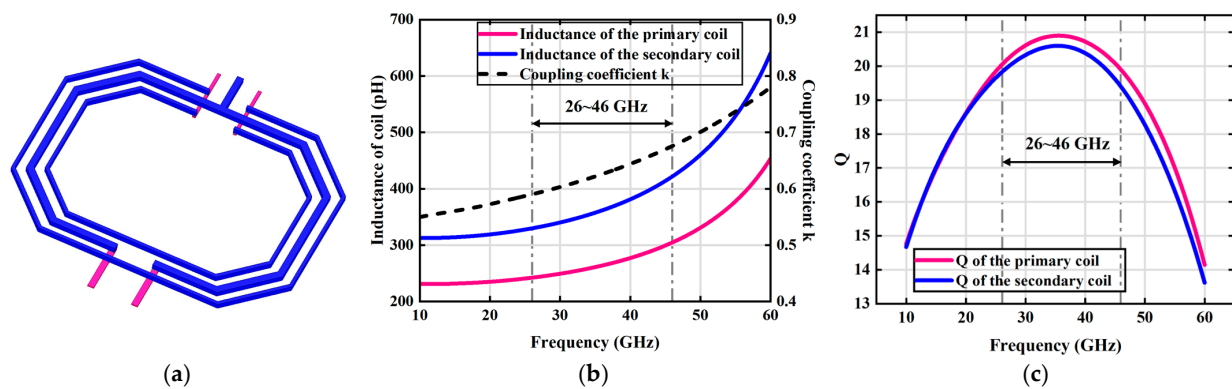


Figure 9. Model and key parameters of the first-stage transformer: (a) transformer model; (b) inductance of the primary coil, secondary coil, and coupling coefficient k ; (c) Q factor of the primary coil and the secondary coil.

3.4. Complete LNA Circuit with Input and Output Matching Networks

Figure 10 shows the complete circuit diagram of the proposed LNA with two paths. The input matching network is formed by the transformer T_1 and parallel capacitors. The first stage consists of two paths, formed by the CG amplifier M_1 and the CS amplifier M_2 . The inter-stage matching network for the two paths is composed of parallel capacitors, series inductors, and two transformers T_2 , T_3 . An asymmetric cross-coupling noise-canceling structure (ACCNCS) is achieved by two different CS amplifiers M_3 , M_4 with source degeneration inductors L_{S1} , L_{S2} and cross-coupling capacitors C_{c1} , C_{c2} . Following the ACCNCS, the output matching network is formed by a differential-to-single-ended transformer T_4 with two parallel capacitors. Top view of the models of all four transformers T_1 – T_4 implemented in the LNA are shown below the schematic. In this technology, the simulated results show that the transition frequency (f_T) of the transistors used in this design is approximately 305 GHz, while the maximum oscillation frequency (f_{max}) is approximately 230 GHz. This ensures that the transistors can operate stably at high frequencies. Table 1 lists the dimensions and parameters of the main devices corresponding to the schematic of the proposed LNA.

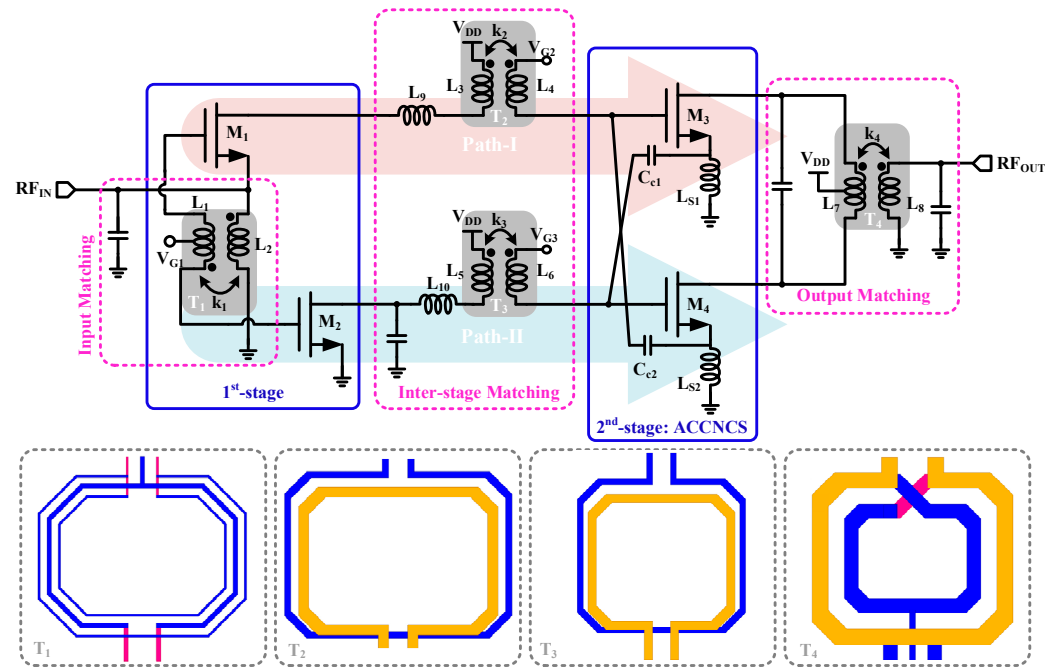


Figure 10. Schematic of the proposed LNA with a new cross-coupling noise-canceling technique.

Table 1. Main device dimensions and parameters.

Device	D/P	Device	D/P	Device	D/P	Device	D/P
M ₁	(1.5 $\mu\text{m}/30\text{ nm}$) $\times$ 16	L ₁	270 pH	L ₇	320 pH	k ₁	0.7
M ₂	(1 $\mu\text{m}/30\text{ nm}$) $\times$ 16	L ₂	400 pH	L ₈	200 pH	k ₂	0.7
M ₃	(2 $\mu\text{m}/30\text{ nm}$) $\times$ 32	L ₃	300 pH	L ₉	300 pH	k ₃	0.6
M ₄	(1 $\mu\text{m}/30\text{ nm}$) $\times$ 16	L ₄	400 pH	L ₁₀	300 pH	k ₄	0.6
C _{c1}	10 fF	L ₅	300 pH	L _{s1}	80 pH	V _{G1}	0.55 V
C _{c2}	500 fF	L ₆	250 pH	L _{s2}	350 pH	V _{G2/VG3}	0.5 V

4. Simulation Results

The complete layout of the proposed LNA with GSG and DC pads is shown in Figure 11. And the whole circuit (with PAD) occupies a chip area of $513 \times 837\text{ }\mu\text{m}^2$, which is 0.43 mm^2 , while the core circuit occupies only an area of $335 \times 665\text{ }\mu\text{m}^2$, which is 0.23 mm^2 .

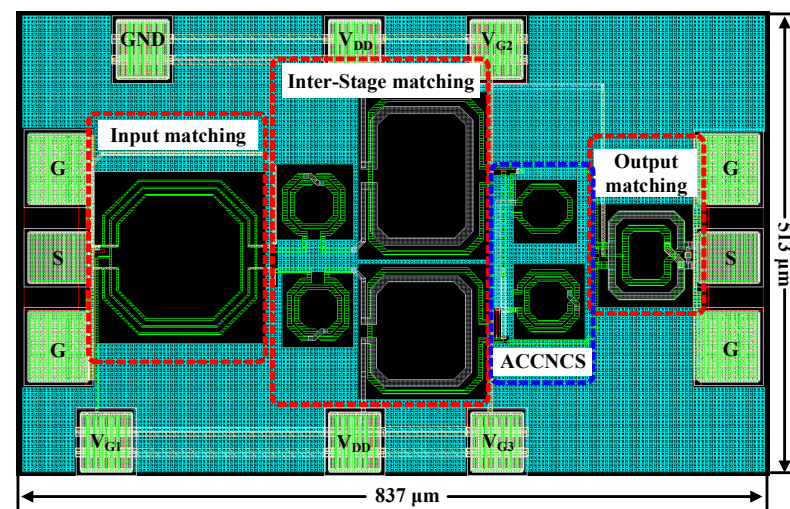


Figure 11. Layout of the proposed LNA.

Figure 12a shows the post-simulation results of the S parameters for the proposed LNA. The gain reaches 10.6–12.6 dB over the entire operating frequency band, with S_{22} less than 10 dB and S_{11} below -8 dB across 90% of the bandwidth, achieving wideband matching. In addition, Figure 12b shows the noise figure curve of the LNA with ACCNCS, and it can be observed that the LNA maintains a noise figure ranging from 2.9 dB to 4.2 dB across the ultra-wideband frequency range of 26 GHz to 46 GHz. Furthermore, as shown in Figure 12c, the LNA exhibits an IP_{1dB} greater than -11.5 dBm across the operating band, reaching -7.6 dBm near the center frequency.

Table 2 summarizes the performance of the proposed LNA and compares it with state-of-the-art publications. Compared with other LNAs, this work achieves good gain, noise, and linearity performance over a wide operating frequency band, with a competitive fractional bandwidth (FBW) of 56%. In order to evaluate and compare the overall performance of LNAs, a widely recognized figure of merit (FoM) is employed, defined as follows [17]:

$$FoM = \frac{Gain_{MAX}[dB] \times BW[GHz]}{(NF_{min}[dB] - 1) \times P_{DC}[mW]} \quad (9)$$

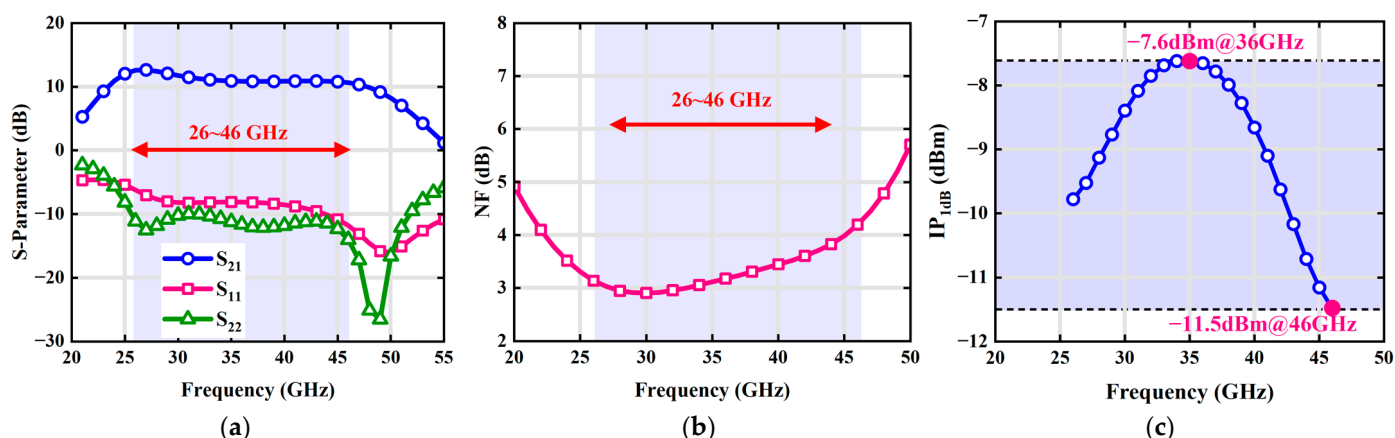


Figure 12. Post-simulation results of the proposed LNA: (a) S parameters; (b) noise figure; (c) input 1 dB compression point.

Table 2. Performance summary and comparison with state-of-the-art alternatives.

Reference	This Work ^S	[12] ^M	[13] ^M	[18] ^S	[19] ^M	[20] ^M	[21] ^S	[22] ^S
Tech	28 nm CMOS	65 nm CMOS	40 nm CMOS	65 nm CMOS	180 nm BiCMOS	28 nm CMOS	40 nm CMOS	40 nm CMOS
Frequency (GHz)	26–46	24.9–32.5	26–33	26–33.4	23–32	24.7–29.5	24–40	24–27
Gain _{MAX} (dB)	12.6	18.3	27	18.5	12	19.1	20	13.6
NF (dB)	2.9–4.2	3.25–4.2	3.3–4.3	3	4.5–6.3	3.3–3.5	3.7	5.8
IP _{1dB} (dBm)	−11.5 to −7.6	−24	−21.6	−24.5	−16.3 to −14.5	−8.7	−15.9	−4.2
P _{DC} (mW)	22	20.5	31.4	17	13	25.5	47.2	50.8
Core Area (mm ²)	0.23	0.11	0.26	0.08	0.25	0.17	0.22	0.34
FBW *	56%	26%	24%	25%	42%	18%	50%	12%
FoM	6.03	3.02	2.62	4.03	2.37	1.56	2.51	0.14

S: simulated result; M: measured result; *: fractional bandwidth, $FBW = 2(f_H - f_L)/(f_H + f_L)$.

5. Conclusions

This paper presents an ultra-wideband LNA with a new cross-coupling noise-canceling technique designed using a 28 nm CMOS process. The first stage employs the CG Gm-boosted technique, while the second stage (ACCNCS) utilizes capacitive cross-coupling to improve wideband gain matching and noise matching. Input, output, and inter-stage

matching are achieved through transformer, inductor, and capacitor networks. The LNA occupies a core layout area of 0.23 mm^2 and operates across a frequency range of 26 to 46 GHz, for which the FBW is 56%. Post-layout simulation results demonstrate a peak gain of 12.6 dB and a noise figure ranging from 2.9 to 4.2 dB over the entire operation band. Under a 0.9 V supply, the input 1 dB compression point ($IP_{1 \text{ dB}}$) is -11.5 to -7.6 dBm, with a total power consumption of 22 mW.

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