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A 2.25 ppm/°C High-Order Temperature-Segmented Compensation Bandgap Reference

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Abstract: This paper presents a bandgap reference (BGR) with high-order temperature-segmented compensation. The compensation signal is generated using the voltage difference between two bipolar junction transistor (BJT) emitter bases, each of which individually loads a proportional-to-absolute temperature (PTAT) current and a zero-to-absolute temperature (ZTAT) current. The proposed BGR achieves a low-temperature coefficient (TC) over a wide temperature range. Simulations using the 0.18 μm Bipolar-CMOS-DMOS process show a typical TC of 2.25 ppm/°C from −40 °C to 125 °C. With an active area of 0.07986 mm^2, it consumes 36 μW power under an operating voltage of 1 V. The integrated output noise from 0.1 Hz to 10 Hz is 81.1 μV.

Keywords: bandgap reference; high-order nonlinearity; temperature compensation; process; mismatch

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1. Introduction

Bandgap reference (BGR) is an essential component in many analog, digital and mixed-signal integrated circuits. The output voltage of the traditional voltage-mode BGR is 1.25 V, which is approximately equal to the semiconductor material's extrapolated energy bandgap voltage [1]. Due to the fixed output voltage, the minimum supply voltage for the traditional voltage-mode BGR would be around 1.5 V. Consequently, the traditional voltage-mode BGR [2,3] is not suitable for low-voltage applications. It is important to have a low-voltage and low-power PVT-insensitive reference circuit for battery-operated portable devices such as hearables and wearables. The current-mode BGR transforms the proportional-to-absolute temperature (PTAT) voltage and the complementary-to-absolute temperature (CTAT) voltage to a temperature-independent current to produce a temperature-independent bandgap voltage reference under 1.2 V, as proposed by H. Banba [4]. The minimum supply voltage for the current-mode BGR can be lower than 1.2 V. Current-mode BGRs are more flexible in output voltages [5], and various compensation methods for current-mode BGRs have been proposed.

Traditional bipolar junction transistor (BJT)-based BGRs with the first-order temperature compensation have typical temperature coefficients ranging from 20 ppm/°C to 100 ppm/°C [6]. To achieve high accuracy and stability over a wide temperature range, the high-order temperature compensation is used to eliminate the nonlinear component of the PN junction voltage. Various curvature compensation methods were proposed to enhance the accuracy and stability of low-voltage BGRs. For instance, Bill Ma and Fengqi Yu used metal oxide semiconductor (MOS) transistors operating in the weak inverse region, which have a positive second-order temperature coefficient opposite to BJTs [7], to compensate for high-order nonlinearity. In [8], a method based on multistage currents with different temperature thresholds was proposed to compensate for the temperature-dependent nonlinearity term. The scheme using the voltage difference between V_{eb} at a PTAT current and V_{eb} at a zero-to-absolute temperature (ZTAT) current was implemented to compensate for the high-order nonlinear term in V_{be} [9]. However, this approach introduced additional

high-order nonlinear currents. But the minimum supply voltage of BJT-based voltage reference cannot be lower than 0.7 V due to the presence of the BJT. To obtain a lower supply voltage, metal oxide semiconductor field effect transistors (MOSFETs) that operate in the subthreshold region are used instead of BJTs. V_{eb} and ΔV_{eb} are replaced by V_{GS} and ΔV_{GS}, respectively. Current-mode BGRs and current references (CRs) consisting only of MOSFETs were proposed [10–12]. A current reference based on a minimum current search principle implemented current compensation, which is similar to piecewise compensation, to improve the temperature coefficient [13]. Different topologies of MOSFET threshold-based voltage references are shown [14]. Although the threshold voltage-based reference can be used at lower supply voltages, it is more susceptible to variations in the CMOS fabrication process than the BJT-based reference [14]. In order to obtain a lower supply voltage, the low-threshold-voltage (LVT) or zero-threshold-voltage (ZVT) MOSFET was introduced [15].

In this paper, we present a low-voltage current-mode BGR with standard-threshold-voltage (SVT) MOSFETs implementing high-order temperature-segmented compensation. Two BJTs operating at PTAT currents and ZTAT currents, respectively, jointly generate a compensation signal. Unlike previous works, our design avoids additional high-order nonlinear currents when the ZTAT current flows into V_{eb}. Additionally, our approach achieves the segmented compensation of the temperature curve.

The remainder of this paper is organized as follows: Section 2 explains the principle of high-order temperature compensation for the proposed BGR. Section 3 discusses the startup circuit. Section 4 presents the trimming and simulation results. Finally, Section 5 provides the conclusion.

2. Principle of High-Order Temperature Compensation

2.1. Traditional Low-Voltage BGR

The traditional low-voltage BGR achieves first-order temperature compensation by utilizing two components with opposite first-order temperature coefficients. On the one hand, the positive first-order temperature coefficient is provided by the voltage difference of two emitter-bases, ΔV_{eb}, which both load PTAT currents. On the other hand, the negative first-order temperature coefficient is usually generated by the emitter-base voltage V_{eb}. The traditional low-voltage current-mode BGR is shown in Figure 1. The PTAT voltage, ΔV_{eb}, is converted into the PTAT current, I_p, by dividing the resistor R0. The CTAT voltage, V_{eb}, is converted into the CTAT current, I_n, by dividing the resistor R1. The resistance of R2 is equal to R1. The current I_{p+n}, which is the sum of I_p and I_n, achieves first-order temperature compensation. I_{p+n} is multiplied by resistance, R3, and is converted to a reference voltage V_{ref_1st} with first-order temperature compensation. The temperature characteristics are derived as follows.

The PTAT current I_p can be written as

$$I_p = \frac{\Delta V_{eb}}{R0} = \frac{V_T ln N}{R0} = \frac{kTlnN}{qR0} \tag{1}$$

where N is the ratio of emitter area of Q1 to Q2.

The CTAT current I_n can be written as

$$I_n = \frac{V_{ebQ2}}{R1} \tag{2}$$

The temperature model of V_{eb} can be expressed as the following expression:

$$V_{eb}(T) = V_g(T) - \left(V_g(T_R) - V_{eb}(T_R)\right)\frac{T}{T_R} - (\eta - \alpha)V_T ln\frac{T}{T_R} \tag{3}$$

where T_R is the specified reference temperature, $V_g(T_R)$ is the bandgap voltage at T_R, $V_{eb}(T_R)$ is the emitter-base voltage at T_R and η is a process-dependent constant around 4 [16]. α is

equal to 1 when the BJT loads the PTAT current and equal to 0 when the BJT loads ZTAT current. $V_g(T)$ is the bandgap voltage as a function of temperature.

$$V_g(T) = V_{g0} - bT - cT^2 \tag{4}$$

where V_{g0} is 1.17885 V to 1.20595 V, b is 9.025×10^{-5} V/K to 2.7325×10^{-4} V/K and c is 3.05×10^{-7} V/K^2 to 0 if the temperature is between 150 K and 400 K [17].

Therefore, the expression of I_{p+n} can be obtained.

$$I_{p+n} = \frac{V_T lnN}{R0} + \frac{V_{ebQ2}}{R1} \tag{5}$$

The expression of V_{ref_1st} is formulated as

$$\begin{aligned} V_{ref\_1st} &= \left(\frac{V_T lnN}{R0} + \frac{V_{ebQ2}}{R1}\right) \times R3 \\ &= \frac{R3}{R1} V_{g0} + \frac{R3}{R1}\left(\frac{R1}{R0}\frac{klnN}{q} - \frac{V_g(T_R) - V_{ebQ2}(T_R)}{T_R} - b\right)T - \frac{R3}{R1}\left[cT^2 + (\eta - \alpha)V_T ln\frac{T}{T_R}\right] \end{aligned} \tag{6}$$

where $V_{ebQ2}(T_R)$ is the emitter-base voltage V_{ebQ2} at T_R.

Obviously, the traditional low-voltage BGR can achieve the first-order temperature compensation by eliminating the second term in (6). Therefore, the first-order temperature term can be easily eliminated by adjusting the ratio of the resistor R1 to R0 and the value of N to satisfy (7).

$$\frac{R1}{R0} lnN = \frac{q}{k}\left(\frac{V_g(T_R) - V_{ebQ2}(T_R)}{T_R} + b\right) \tag{7}$$

Typically, V_{ref_1st} presents a second-order parabola going downwards due to the presence of the third term in (6). Taking into account the trade-off between power consumption and the area of the circuit, the value of N is 13 in this work. In order to improve the power supply rejection ratio (PSRR) of the traditional low-voltage current-mode BGR, cascode current mirrors are used [18].

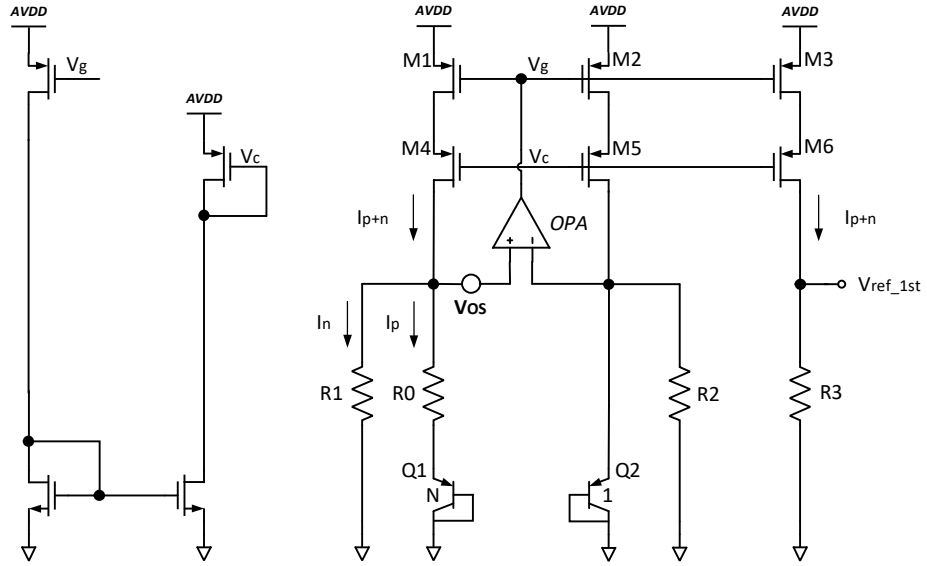

Figure 1. Traditional low-voltage BGR.

2.2. The Proposed Low-Voltage BGR

The curvature compensation method depicted in Figure 1 can realize the first-order temperature compensation. However, the presence of the third term in Equation (6) still causes V_{ref_1st} to vary across the whole temperature range. In order to obtain a more stable reference voltage, it is necessary to suppress the influence of the nonlinear term in

Equation (6). Various methods were proposed [19–21] to correct the nonlinear term. The basic ideas in [22,23] can be used in this scheme, as depicted in Figure 2.

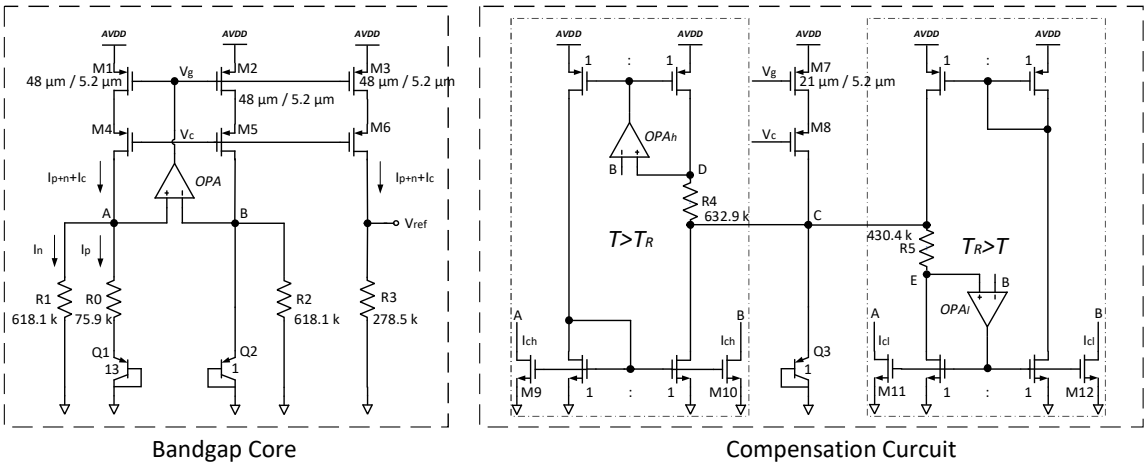

Figure 2. Schematic of proposed low-voltage BGR with high-order compensation.

Even without the presence of the high-order compensation circuit, the current through M7 mirrored from I_{p+n} is still a first-order temperature-compensated current. When the compensation circuit operates, the compensation current, I_c, is usually small in order to cancel the high-order nonlinear terms. Compared to the PTAT current or the CTAT current, $I_{p+n} + I_c$ cannot change much with varying temperatures. To simplify calculations, the load current of Q3, I_{Q3}, mirrored from M1 or M2, $I_{p+n} + I_c$, can be approximately regarded as a ZTAT current. The curve of I_{Q3} with varying temperatures is shown in Figure 3b. Therefore, the emitter-base voltage, V_{ebQ3}, of Q3 can be expressed by the following formula:

$$V_{ebQ3}(T) = V_g(T) - \left(V_g(T_R) - V_{ebQ3}(T_R)\right)\frac{T}{T_R} - \eta V_T ln\frac{T}{T_R} \tag{8}$$

where $V_{ebQ3}(T_R)$ is the emitter-base voltage V_{ebQ3} at T_R.

The load current of Q2 is a PTAT current. Thus, the emitter-base voltage, V_{ebQ2}, of Q2 can be expressed as

$$V_{ebQ2}(T) = V_g(T) - \left(V_g(T_R) - V_{ebQ2}(T_R)\right)\frac{T}{T_R} - (\eta - 1)V_T \ln\frac{T}{T_R} \tag{9}$$

The expression of the compensation signal can be obtained by (8) and (9).

$$V_{ebQ2}(T) - V_{ebQ3}(T) = (V_{ebQ2}(T_R) - V_{eb3}(T_R))\frac{T}{T_R} + V_T ln\frac{T}{T_R} \tag{10}$$

The second term in Equation (10) has the same expression form as the high-order nonlinear term in Equation (6). The first item in Equation (10) is the first-order term. Therefore, to achieve better compensation, the first item in Equation (10) will be eliminated. The following expression needs to be satisfied by adjusting the collector currents of Q3 and Q2.

$$V_{ebQ2}(T_R) = V_{ebQ3}(T_R) \tag{11}$$

Combining Equations (9) and (10), the intersection of V_{ebQ3} and V_{ebQ2} is obviously at T_R. Curvature compensation is implemented, making the cross point of V_{ebQ3} and V_{ebQ2} located in the stationary point of the curve of V_{ref_1st}, with the varying temperatures in Figure 3a.

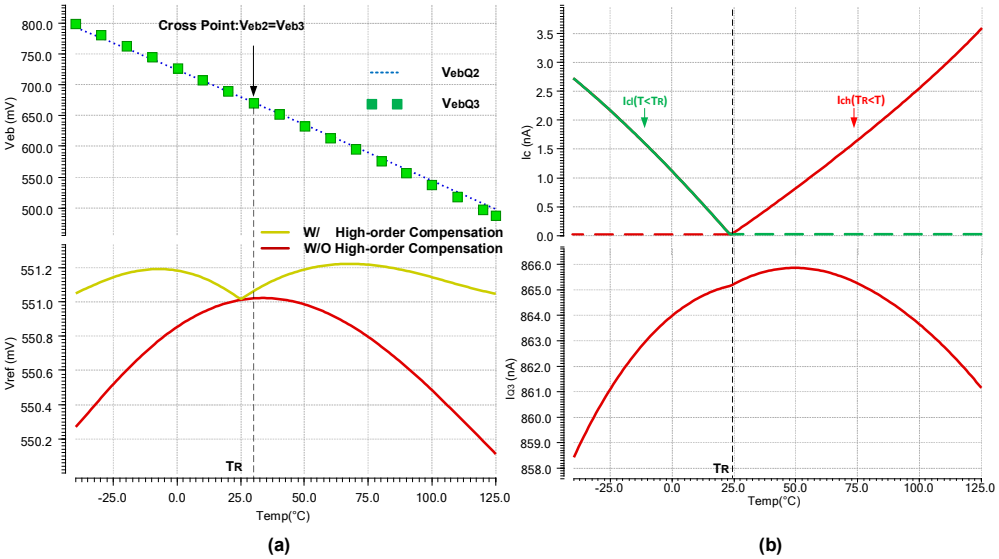

Figure 3. (**a**) The curve of V_{ebQ3}, V_{ebQ2} and V_{ref_1st} with varying temperatures. (**b**) The curve of load current, I_{Q3}, of Q3 and the compensation, I_c, with varying temperatures.

When the temperature is higher than T_R, V_{ebQ2} is larger than V_{ebQ3} in Figure 3a. In Figure 2, the right half of the circuit is the compensation circuit. $V_B = V_{ebQ2}$ and $V_C = V_{ebQ3}$ can be obtained. So, when the temperature is higher than T_R, V_B is larger than V_C. And if the OPA_l is working properly under such conditions, V_E will be equal to V_B. This will result in an unreasonable result where V_E is greater than V_C. Therefore, there is no current flowing through R5, resulting in V_E being equal to V_C. Since the positive input voltage of the OPA_l is lower than the negative input voltage, the output voltage of the OPA_l is low, resulting in zero load current flowing M11 and M12. However, the OPA_h can work properly when the temperature is higher than T_R. It can be obtained that $V_B = V_D$ when OPA_h can operate properly. The high-order compensation signal voltage, $V_T ln(T/T_R)$, is converted into a current through the resistor R4. Transistors M9 and M10 produce curvature compensation current I_{ch}.

$$I_{ch} = \frac{k_4 V_T ln \frac{T}{T_R}}{R4} \tag{12}$$

where k_4 is the compensation current gain at high temperature. The higher the temperature, the greater the compensation current. In this work, the default value of k_4 is 0.2.

When the temperature is lower than T_R, the output voltage of the OPA_h is high. The load current of M9 and M10 is zero. OPA_l can work properly under low temperatures, and it can be obtained that $V_B = V_E$. The high-order compensation signal voltage, $-V_T ln(T/T_R)$, is converted into a current through the resistor R5. Therefore, when the temperature becomes lower than T_R, transistors M11 and M12 produce a curvature compensation current I_{cl}.

$$I_{cl} = -\frac{k_5 V_T \ln \frac{T}{T_R}}{R5} \tag{13}$$

where k_5 is the compensation current gain in a low-temperature scenario. The lower the temperature, the greater the compensation current. In this work, the default value of k_5 is 0.25.

V_{ref_1st} without high-order compensation presents a second-order parabola going downwards whose vertex is around T_R, as shown in Figure 3a. As the temperature moves further away from T_R, the voltage drops more. When the compensation circuit is active, the compensation current, I_c, which is the sum of I_{cl} and I_{ch}, appears as shown in Figure 3b. As the temperature moves further away from T_R, the compensation current, I_c, increases more. The compensating current, I_c, flows through the resistor, R3, to cause a

positive ΔV_{ref} and, thus, suppress the drop of V_{ref_1st}. The smaller the V_{ref_1st}, the larger the compensation current I_c. Therefore, the compensation curve for V_{ref} displays a segmented compensation pattern, as shown in Figure 3a. Consequently, the segmented compensation has been successfully realized in this work. When V_{ref_1st} is heavily affected by process and mismatch, V_{ref_1st} may resemble a diagonal line. In such situations, T_R needs to be set outside the temperature range, and V_{ref} will exhibit a second-order parabolic behavior.

2.3. The Design of OPA

The operational amplifier (OPA) plays a crucial role in the proposed low-voltage BGR. One important parameter of the OPA is offset. The input offset of an OPA includes both systematic offset and random offset. Systemic offset arises due to the limited gain of the OPA. The higher gain in the OPA results in a smaller systematic input offset. Random offset, on the other hand, is caused by device mismatch. Increasing the chip area can help reduce mismatch, but this involves a trade-off between chip area and performance, as mentioned in reference [24].

It is evident that the input common-mode voltage of the OPA is V_{eb}, which is between 800 mV and 500 mV from −40 °C to 125 °C. If PMOS differential input stages are used, the minimum supply voltage must meet the following formula: $AVDD_{min} > |V_{thp}| + V_{DSp} + V_{ebmax}$. As the supply voltage is approximately 1 V, the NMOS differential input stage is chosen instead of the PMOS differential input stage, and the minimum supply voltage is $AVDD_{min} = 2V_{DSp} + V_{ebmax} \approx 950$ mV < 1 V, which is suitable for our design. $2V_{DSp}$, which is approximately 150 mV, represents the sum of the V_{DS} of M2 and the V_{DS} of M5 in Figure 2. In our process, the threshold voltage of the NMOS varies from 258 mV to 415 mV when W/L = 10 µm/10 µm and from 366 mV to 514 mV when W/L = 10 µm/0.18 µm, which satisfies the design requirements. The implementation of the OPA is illustrated in Figure 4.

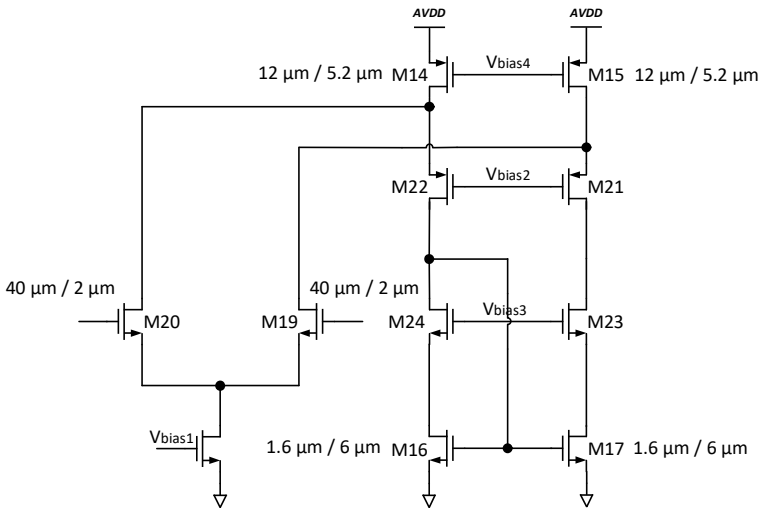

Figure 4. Schematic of the OPA used.

3. Start-Up Circuit

The start-up circuit shown in Figure 5 is an important component of the BGR circuit. The BGR core circuit, depicted in Figure 1, can exist in three possible stable states. The first state occurs when the two arms of the BGR core circuit carry zero current. The currents I_p and I_n in Figure 1 are zero under the first state. The second state is characterized by a very small current flowing through R1 and R2, with Q1 and Q2 remaining inactive. Only the current I_p in Figure 1 is zero under the second state. The third state represents the desired operating state when the current in the two arms of the BGR core circuit matches the design value [25].

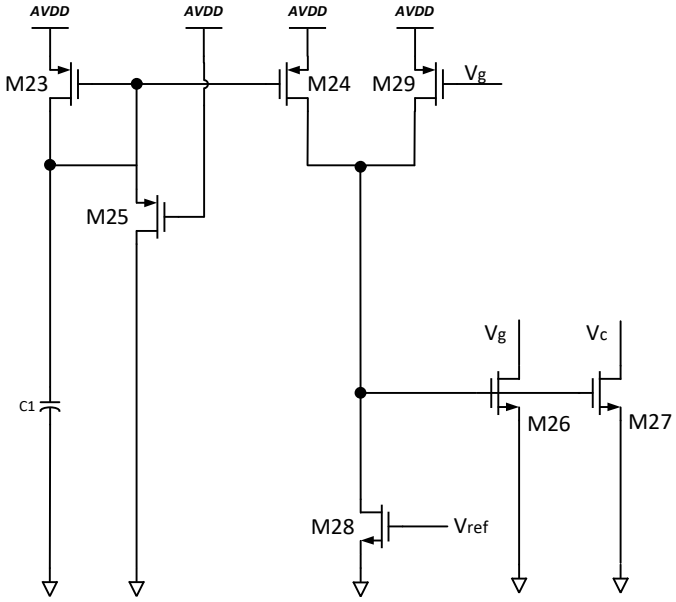

Figure 5. Start-up circuit.

Upon powering on, the BGR core circuit initially enters the first state. V_{ref} is zero, and transistor M28 is turned off. At this stage, transistor M23 begins to charge C1; meanwhile, transistor M24 charges the gate of transistors M26 and M27. Consequently, M26 and M27 turn on, resulting in V_g and V_c being pulled down. Currents begin to flow in the two arms of the BGR core circuit. Subsequently, the BGR core circuit may transition to the second state, where V_{ref} is between the desired value and zero. Additionally, M28 turns on. To ensure the BGR core circuit exits the second state and reaches the expected stable state, M26 and M27 cannot be turned off. Therefore, it becomes necessary to introduce transistor M29 to continue charging the gates of M26 and M27. Once the circuit is functioning properly, V_{ref} becomes sufficiently large to drive M28 into the linear region. Finally, M26 and M27 remain off. During power-off, transistor M25 is utilized to discharge the charge stored in C1. Figure 6 illustrates the simulated start-up waveforms of the proposed BGR.

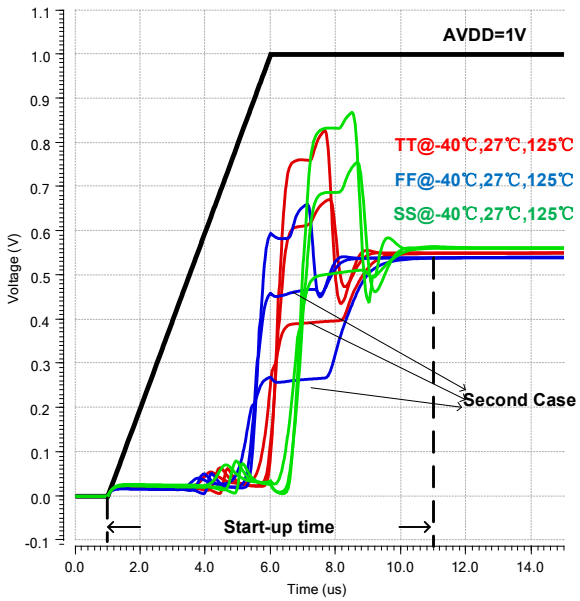

Figure 6. Simulated start-up waveforms of the proposed BGR.

4. Trimming and Simulation Results

4.1. Trimming

Trimming at the wafer level is primarily designed to overcome process extensibility and random device variation during circuit manufacturing. The temperature trimming of the proposed BGR is mainly a high-order temperature trimming technique to achieve better temperature coefficient performance.

To realize high-order temperature compensation, $(W/L)_{M7}$ should be adjusted so that the cross point of V_{ebQ3} and V_{ebQ2} is adjustable. As shown in Figure 7, the control word T_{trim}<3:0> decides $(W/L)_{M7}$, which changes the load current of Q3. The range of current variation is from $-2I_T$ to $1.75I_T$.

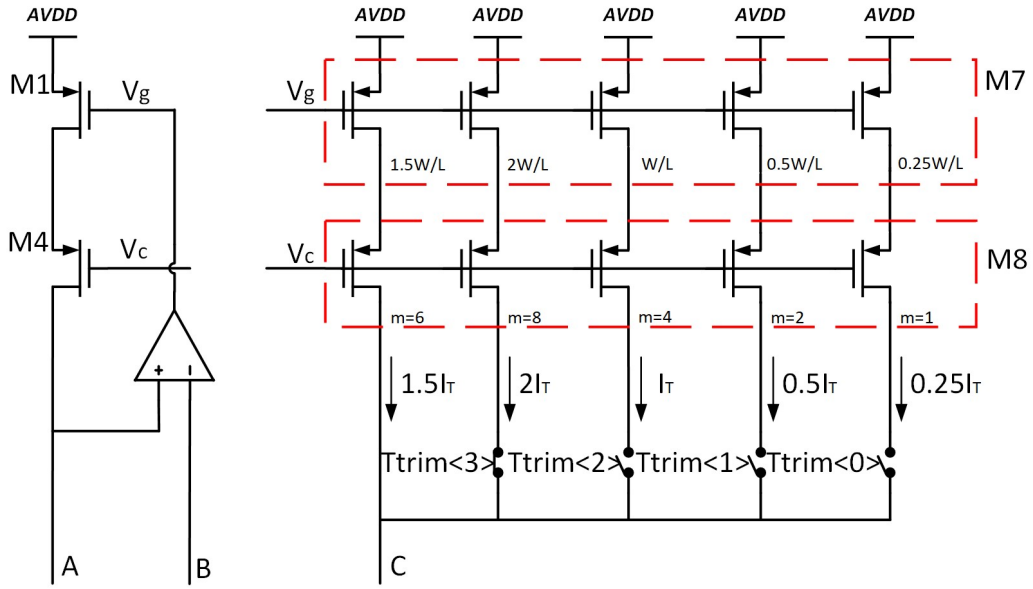

Figure 7. Trimming network of $(W/L)_{M7}$.

For high-order temperature trimming, the coefficients k_4 and k_5 are adjusted, as determined by Formulas (12) and (13). Similar to $(W/L)_{M7}$, $(W/L)_{M9–12}$ is used to adjust k_4 and k_5. In this work, K_{4trim}<4:0> and K_{5trim}<4:0> are utilized to adjust k_4 and k_5, respectively.

4.2. Simulation Results

Figure 8 shows the simulated temperature behavior of V_{ref} at the TT process corner with varying supply voltage. It is observed that the proposed scheme successfully implements high-order temperature curvature compensation. In order to accurately evaluate the effect of process variation and power supply voltage on the circuit performance, the simulated TC results for different supply voltages and corners are summarized in Table 1. When the supply voltage is set to 1.3 V or 1.6 V under the SS process corner, V_{ref} without high-order compensation is approximately a diagonal line. As a result, the TC with high-order compensation is larger than the TC values for other cases.

Table 1. The simulated TC results for different supply voltages and corners.

	TC_bt (1 V)	TC_at (1 V)	TC_bt (1.3 V)	TC_at (1.3 V)	TC_bt (1.6 V)	TC_at (1.6 V)
TT	2.25 ppm/°C	2.25 ppm/°C	9.73 ppm/°C	4.47 ppm/°C	8.3 ppm/°C	4.09 ppm/°C
FF	14.3 ppm/°C	5.61 ppm/°C	15.87 ppm/°C	6.69 ppm/°C	12.96 ppm/°C	6.21 ppm/°C
SS	17.11 ppm/°C	5.87 ppm/°C	28.52 ppm/°C	11.43 ppm/°C	26.21 ppm/°C	11.32 ppm/°C

TC_bt: The TC value before trimming. TC_at: The TC value after trimming.

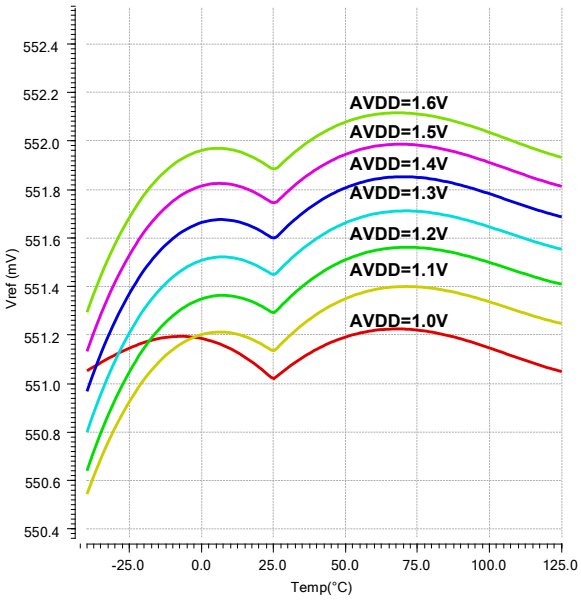

Figure 8. The simulated temperature behavior of V_{ref} at TT process corner, with varying supply voltage.

To assess the impact of process variation and device mismatch on the reference output V_{ref} and TC, Monte Carlo simulations were completed using foundry-supplied statistical device models with activated mismatch and process variations. In order to observe the worst-case results, no specific correlation coefficients were defined for the matched devices. Figure 9a displays the estimated TC results without high-order compensation from 500 Monte Carlo runs under 1 V power supply voltage. Figure 9b shows the estimated TC results with high-order compensation from 500 Monte Carlo runs under 1 V power supply voltage. Comparing Figures 9a and 9b, it is clear the normal distributions of TC are similar under fixed trimmed conditions. This is because high-order compensation is dependent on the outcome of first-order compensation. In certain process and mismatch conditions, the V_{ref} will deviate significantly from the expected result. Therefore, trimming is necessary to ensure better measurement results.

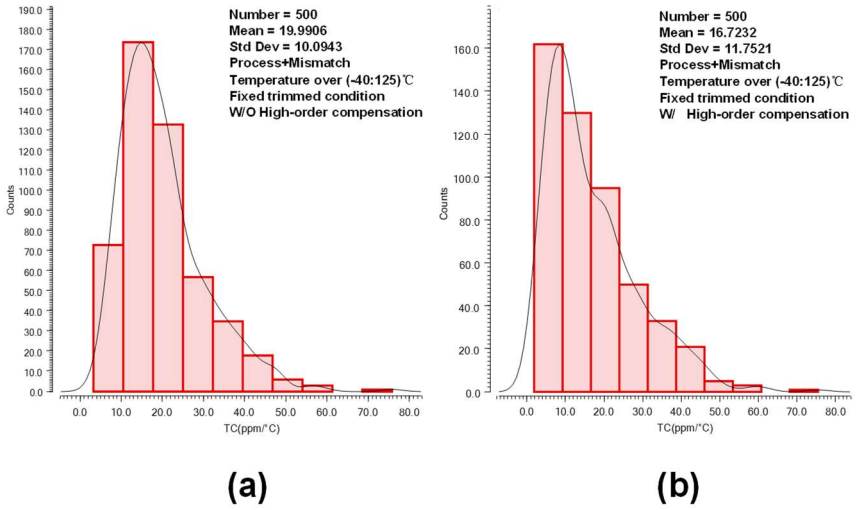

Figure 9. (**a**) The estimated TC results without high-order compensation from 500 Monte Carlo runs under 1 V power supply voltage. (**b**) The estimated TC results with high-order compensation from 500 Monte Carlo runs under 1 V power supply voltage.

Figure 10a displays the results of the estimated reference voltage V_{ref} from 500 Monte Carlo runs under 1 V power supply voltage, indicating its stability. Figure 10b shows the

noise spectrum of the simulated bandgap output under 1 V power supply voltage. The integrated output noise from 0.1 Hz to 10 Hz is 81.12 µV. The simulated PSRR of the BGR circuit under 1 V power supply voltage is shown in Figure 10c, where the PSRR at a low frequency is −67.5 dB at 27 °C.

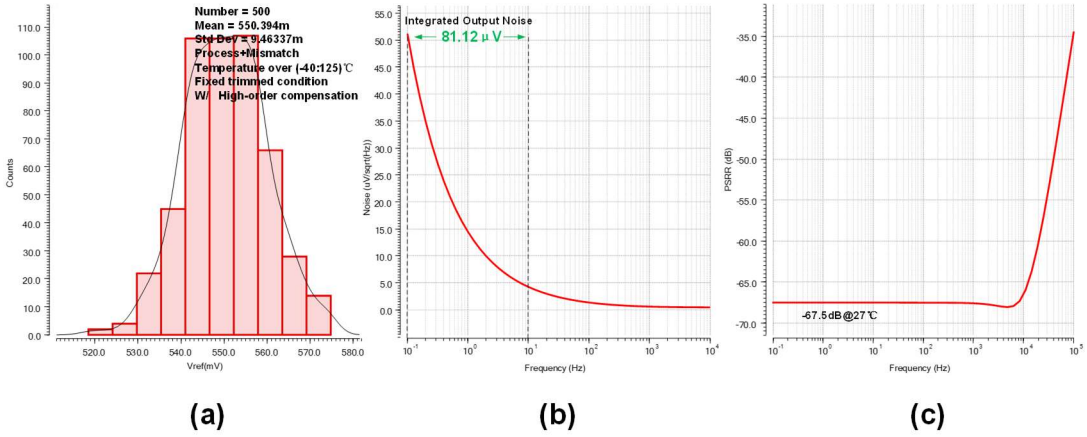

Figure 10. (**a**) The results of the estimated reference voltage output V_{ref} from 500 Monte Carlo runs under 1 V power supply voltage. (**b**) The noise spectrum of the simulated bandgap output under 1 V power supply voltage. (**c**) The simulated PSRR of the BGR circuit under 1 V power supply voltage.

In order to verify the effect of the trimming circuit, the results w/trimming and w/o trimming are shown in Figure 11a and used for a comparison. The estimated TC results w/trimming and TC results w/o trimming from 100 Monte Carlo runs under 1 V power supply voltage are presented in Figure 11a. The estimated TC results w/o trimming are in the range of 2 ppm/°C to 50 ppm/°C. The estimated TC results w/trimming are from 1.2 ppm/°C to 17 ppm/°C. The variance and mean of TC results w/trimming were improved to a great extent. This verifies the effectiveness of the trimming circuit. The V_{ref} is mainly affected by the input-referred offset voltage within OPA in Figure 1. The temperature dependence of the input-referred offset is not modeled in this analysis, which assumes that the variation in temperature is small. Hence, the impacts on V_{ref} can be captured with the following equations:

$$I_p = \frac{\Delta V_{eb} + V_{OS}}{R0} \tag{14}$$

$$I_n = \frac{V_{eb} + V_{OS}}{R1} \tag{15}$$

$$V_{ref}^{OS} = V_{ref} + \left(\frac{R3}{R1} + \frac{R3}{R0}\right) V_{OS} \approx V_{ref} + 4.12 V_{OS} \tag{16}$$

The σ of V_{OS} are 1.5 mV, which is assessed based on the Monte Carlo simulations from 500 runs. Figure 11b displays the estimated V_{ref} results w/trimming and V_{ref} results w/o trimming. According to Equation (16), the σ of V_{ref} affected by V_{OS} is 6.18 mV. The estimated V_{ref} results w/trimming and V_{ref} results w/o trimming under 1 V power supply voltage presented in Figure 11b are essentially consistent. The variance and mean of V_{ref} results are essentially the same. The σ of V_{ref} is 9.5 mV, which is primarily affected by the V_{OS} of OPA. This is generally consistent with the analysis. To reduce the systematic offset, a folded cascode amplifier with a gain greater than 60 dB is employed. To reduce the random offset, the sizes of transistors M14–M17 (the current mirrors in the OPA) and M19–M20 (the input pairs of the OPA) are enlarged. The extra methods, such as auto-zeroing and chopping techniques, are applied in the existing literature. These techniques are not used in this article because it is not the key point of this paper. Figure 12 shows the layout of the proposed BGR circuit implemented using a 0.18 µm Bipolar-CMOS-DMOS

process. The performance summary and comparison of the proposed bandgap circuit is given in Table 2.

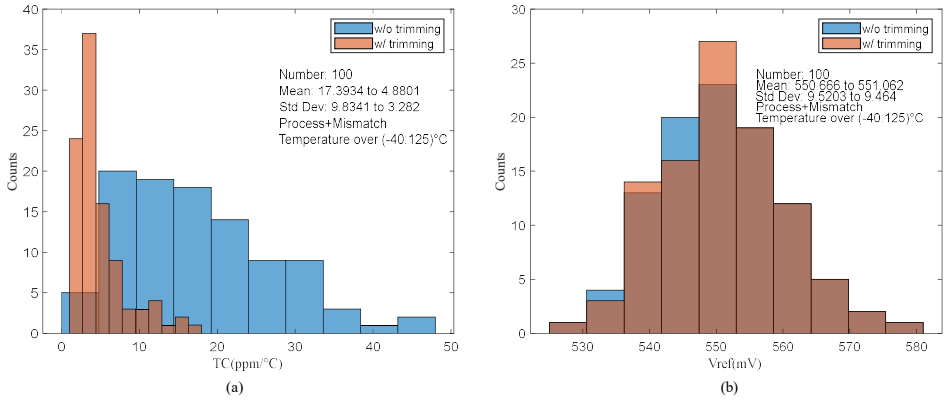

Figure 11. (**a**) The estimated TC results w/trimming compared with TC results w/o trimming from 100 Monte Carlo runs under 1 V power supply voltage. (**b**) The estimated V_{ref} results w/trimming compared with TC results w/o trimming from 100 Monte Carlo runs under 1 V power supply voltage.

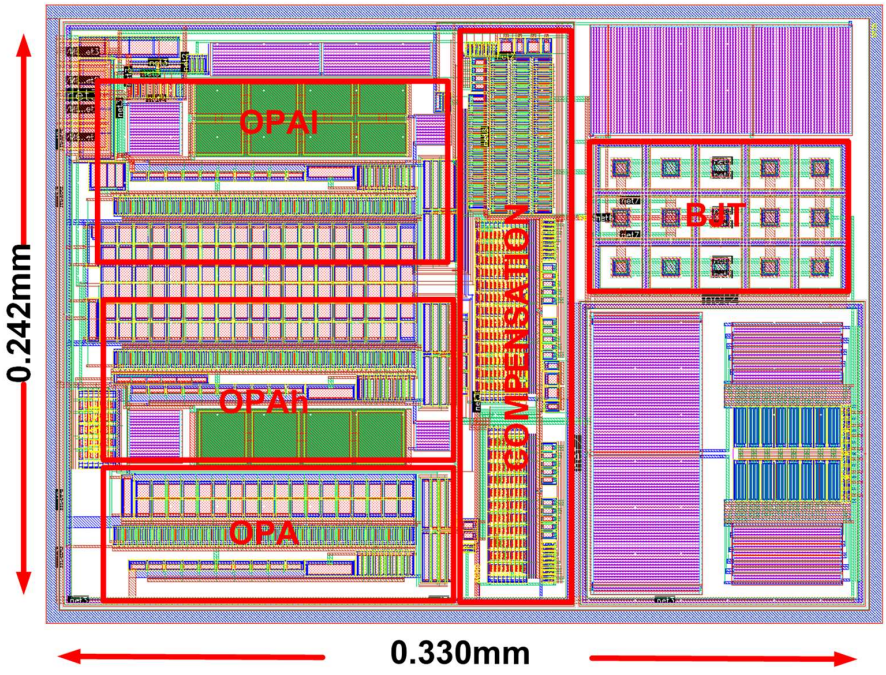

Figure 12. The layout of the proposed BGR with 0.18 µm Bipolar-CMOS-DMOS process.

Table 2. Performance summary and comparison of the proposed bandgap circuit.

Parameter	This Work *	[7]	[9]	[22]	[23]
Technology	0.18 µm	0.18 µm	0.35 µm	0.35 µm	130 nm
Type	Current-mode	Current-mode	Current-mode	N/A	Current-mode
Supply Voltage (V)	1	1.2	2.5	1.0–1.8	3.3
Current Consumption (µA)	36	36	38	N/A	120
Reference Voltage (V)	550 m	767 m	617.7 m	692.6 m	1.16
TC (ppm/°C)	2.25	3.4–6.9	3.9	25	5.8–13.5
Temperature Range (°C)	−40–125	−40–120	−15–150	−20–100	−40–150
Active Area (mm^2)	0.07986	0.036	0.1019	0.0045	0.08
PSRR (dB)	−67.5 dB@DC	−84 dB@DC	N/A	−55 dB@100	−30 dB @100K
OUTPUT NOISE (V)	81.1 µ (0.1–10 HZ)	5.4 µ@320 Hz	20 nV (0.1–50 HZ)	26.8 µ (0.1–10 HZ)	84.3 µ (0.1–10 HZ)

* Simulation results.

5. Conclusions

This proposed BGR with high-order temperature compensation was simulated using a 0.18 µm Bipolar-CMOS-DMOS process. The voltage difference of V_{eb} at PTAT currents and ZTAT currents is used to generate a high-order compensation signal. The scheme presented in this work achieves a typical temperature coefficient of 1.2–15.5 ppm/°C from −40 °C to 125 °C. The probability of exceeding this TC range is about one percent, based on Monte Carlo simulations. Under 1 V supply voltage, it dissipates 36 µW power with an active area of 0.07986 mm^2 at room temperature (27 °C). The integrated output noise from 0.1 Hz to 10 Hz is 81.1 µV. The PSRR at low frequency is −67.5 dB at 27 °C. The high-order temperature-segmented compensation BGR proposed in this work demonstrates superior stability and is well-suited for low-voltage and low-power applications.

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