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Review

A Brief Review of Single-Event Burnout Failure Mechanisms and Design Tolerances of Silicon Carbide Power MOSFETs

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Abstract: Radiation hardening of power MOSFETs (metal oxide semiconductor field effect transistors) is of the highest priority for sustaining high-power systems in the space radiation environment. Silicon carbide (SiC)-based power electronics are being investigated as a strong alternative for high power spaceborne power electronic systems. SiC MOSFETs have been shown to be most prone to single-event burnout (SEB) from space radiation. The current knowledge of SiC MOSFET device degradation and failure mechanisms are reviewed in this paper. Additionally, the viability of radiation tolerant SiC MOSFET designs and the modeling methods of SEB phenomena are evaluated. A merit system is proposed to consider the performance of radiation tolerance and nominal electrical performance. Criteria needed for high-fidelity SEB simulations are also reviewed. This paper stands as a necessary analytical review to intercede the development of radiation-hardened power devices for space and extreme environment applications.

Keywords: power MOSFET; single-event burnout; silicon carbide; radiation-hardening

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1. Introduction

The power electronics market is experiencing a significant shift towards a "smaller, better, cheaper, faster" philosophy, driving the increasing utilization of microelectronics manufactured through commercial processes. Advancements in commercial processes, specifically in achieving smaller feature sizes, have resulted in higher component density within power systems. However, this increase in component density has led to a significant rise in radiation sensitivity for these advanced systems. Using such dense power systems, which are commercially developed, poses a notable risk if the onboard electronics are not adequately 'hardened' to withstand the radiation environment. Currently, there is a growing interest within the power electronics market in wide-bandgap (WBG) semiconductors. WBG materials possess a larger energy gap compared to traditional semiconductor materials like Silicon (Si) and Gallium Arsenide (GaAs), enabling power devices to operate at much higher voltages, frequencies, and temperatures, with lower specific on-state resistance ($R_{on,sp}$). The resilient characteristics of WBG materials make them strong contenders for developing radiation-hardened power device solutions. Although research has demonstrated that WBG power devices exhibit superior radiation tolerance compared to their conventional semiconductor counterparts, radiation-induced reliability issues persist at high operating voltages, rendering this technology still in need of further development [1].

Given the current ambitions and innovations of industry, the demand for efficient, radiation-hardened, and highly thermal-conductive power devices are crucial for sustaining high-power systems in high-radiation environments. The design of advanced radiation-tolerant electronics has boundless use in the extreme environments that exist both terrestrially and in outer space. Due to the rapid growth in the commercial high-voltage WBG-based power electronics, rad-hard WBG technology has the potential to transition into

the mainstream power system market for space. Advances in the application of a variety of semiconductor materials, processing technologies, and design techniques have opened unprecedented opportunities for the enhancement of space electronics in the areas of power management, surveillance, on-board computation, and communication. A development such as this comes at an imperative time as NASA plans to establish a sustained human presence on the Moon. Rad-hardened technology will be critical for delivering high-power infrastructure systems in the lunar environment, vastly benefiting exploration capabilities and demanding missions. Compared to the current Si-based power management and distribution systems (PMAD), the implementation of WBG power components have been shown to add triple the amount of voltage. The faster switching speeds and lower $R_{on,sp}$ reduce system power losses by more than 50%. Due to WBG power component size, weight, and power (SWaP) potential, there is less need for more Si-based devices, shown to save an estimated 20% in mass and volume [2,3]. By satisfying multiple requirements with an optimized PMAD system, there is now more space and mass available for additional functionality, better efficiency, and greater energy production. Additionally, with the increasing adoption of electrically powered propulsion systems for deep space exploration missions and all-electric aircrafts, an advancement in rad-hard electronics would greatly benefit the power needs for these concepts. By providing high power conversion for all parts needed in the power distribution system, an electrically propelled vehicle can perform at a much more desirable capability. This opens the gateway to a completely new method of propulsion that is imperative for a new age of travel and deep space exploration.

Terrestrially, the development of radiation tolerant electronics would provide reliable instrumentation for monitoring advanced nuclear reactor systems. Providing novel sensors to measure the structural health of reactors, maintenance and system reliability can be considerably optimized. Moreover, military and air force systems can be bolstered against radiation exposure. With the emergence of neuromorphic computational paradigms of new device and circuit architectures, and of specific device structures and coupled oscillators as computational elements, there is a new frontier to be explored systematically. These architectures and algorithms are highly dependent on radiation sensitivity performance and power requirements. The security and reliability of all these emerging technologies would drastically benefit from advancements in radiation-hardened power systems.

The use of silicon carbide (SiC) has emerged among WBG materials as a leading candidate to replace Si for high-power applications. Out of the many polytypes, 4H-SiC has shown the most optimal intrinsic density (n_i), critical electric field (E_c), electron mobility (μ_e), and thermal conductivity (k) characteristics for SiC power devices [4,5]. WBG materials like gallium nitride (GaN), and ultra-wide band gap (UWBG) materials like gallium oxide (Ga_2O_3), aluminum nitride (AlN), and diamond, have also demonstrated characteristics superior to traditional semiconductors. Challenges with packaging plague the technology readiness of UWBG devices [2]. While there are electronic performance tradeoffs between 4H-SiC and GaN (see Figure 1), there is a noticeable difference in the thermal management of the materials. SiC has a higher melting point and over 3.5× the thermal conductivity of GaN, making the material more capable of handling the stress of high temperatures that extreme environments induce [6]. Additionally, device reliability issues cause limitations on GaN upper voltage limits [1]. While UWBG semiconductors have a promising future in power devices and for radiation hardening, the technology readiness of 4H-SiC makes this material of particular interest for current study.

SiC device fabrication and techniques have been systematically explored over the past few decades, bolstering the technology readiness and maturity of this material compared to more novel researched WBG semiconductors. Junction barrier Schottky (JBS) diodes and metal oxide semiconductor field effect transistors (MOSFETs) have been identified as the two most critical power devices for space applications [3]. Experimental data have shown that SiC power devices are most susceptible to the single-event effects (SEEs) caused by heavy ions [7–9] and neutrons [10,11], primarily failing due to single-event burnout (SEB). Although SiC devices perform more optimally at higher voltages than Si-based

devices under irradiation, the threshold voltage at which the devices experience SEEs is still undesirably around 40% of the device's rated operating voltage [12]. Many experimental and simulation studies have been conducted in an attempt to improve this percentage; however, there remains no commercially available device that fulfills the high voltage rad-hard need of industry. In order to advance the limit of this current technology, a fundamental understanding of each device's failure mechanisms needs to be reviewed.

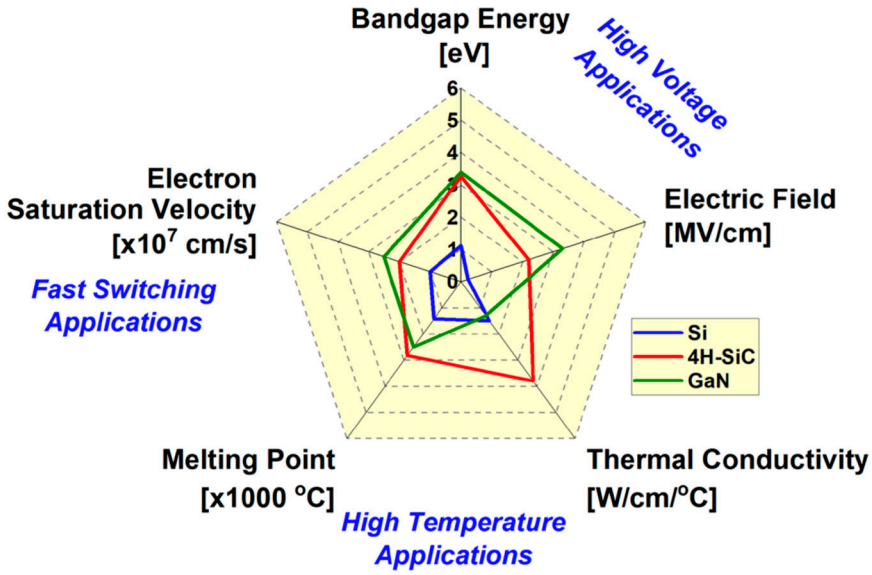

Figure 1. Material characteristic comparison between 4H-SiC, GaN, and Si, reproduced from [1].

Motivation and Objective

Studies have proposed numerous theories for the power MOSFET failure mechanisms, each with their own respective reasons. Ion bombardment experiments on Si bipolar junction transistors (BJTs) shown in [13] demonstrated that the generated charge carriers flowing through the P-base region create a voltage drop that can turn on the transistor. This phenomenon is known as a BJT turn-on and is a mechanism that causes a localized positive feedback current, inducing the generation of carriers and eventually leading to thermal runaway and destruction of the device. Experimental and simulation studies conducted in the 1990s revealed that Si MOSFET burnouts were induced by the turn-on of the parasitic BJT inherent in MOSFET designs [14–18], and this claim has since been supported. The Si diode, where a BJT structure is not present in the design, has been studied under ion bombardment to evaluate its SEB threshold voltage. It has been shown that Si Schottky diodes can survive heavy ion strikes up to 100% of its rated voltage and can operate reliably at 75% of the rated breakdown [19]. However, Si MOSFETs at a linear energy transfer (LET) greater than 15 MeV-cm^2/mg experience failure at or below 40% of their rated voltage [1]. This contrast in SEB threshold adds complementary support to the device's differing failure mechanisms: turn-on of the BJT in Si MOSFETs and a plasma-induced joule heating thermal breakdown in Si diodes.

It was commonly assumed that the BJT turn-on mechanism would be responsible for SEB in SiC-based MOSFETs. Differing from experimental studies on Si JBS and MOSFETs where the SEB failure and degradation thresholds are starkly different, experimental studies of SiC JBS and SiC MOSFETs are almost exactly the same [1,20,21]. The similarity in burnout characteristics suggests a common SEB failure mechanism between the devices. Shoji et al. [22] was one of the first to propose a failure mechanism opposing the conventional ideas previously documented for the SiC MOSFET. The similar failure characteristics between the SiC JBS (does not have parasitic BJT) and SiC MOSFET (does have parasitic BJT) support the claims made, and since then many studies have supported [8,23–26] and

refuted the parasitic BJT [20,22,27–31] as the regenerative failure mechanism responsible for SEB in SiC MOSFET.

A comprehensive review of these theories is necessary to elucidate discrepancies and further the understanding of 4H-SiC power devices to move this technology further. While SEB failure mechanisms in diodes are relatively agreed upon, the mechanisms that corrupt SiC MOSFETs are still debated and will be the primary scope of Section 2 of this paper. Similarly, an analytical review of proposed rad-hard MOSFET designs is necessary to intercede the practicality of development. The desire of industry requiring the most research and future work is fully efficient MOSFETs that can survive catastrophic SEEs up to 1200 V [3]; this 1200 V burnout mark will be a standard when analyzing and attributing merit to rad-hard designs. This paper presents a review of these design models as proposed throughout history, explaining their merits, limitations, similarities, and differences. The objective of this paper is to give current developers a transparent idea of the SEE failure mechanisms effecting SiC power devices and the suitability of the proposed rad-hard designs to help lead to the commercialization of devices that meet the performance standards of industry.

This paper is organized, first, to discuss the evidence provided for the SEB failure mechanisms chronologically proposed for Si and SiC power diodes and MOSFETs. Section 3 compares the radiation tolerances of different SiC MOSFET structures and assesses the merits of the rad-hardened counterparts. Section 4 reviews the background for high-fidelity simulations and failure criteria, and discusses future simulation developments to accurately replicate heavy ion strikes on rad- and non-rad-hardened devices. Lastly, in Section 5, the conclusion discusses the current state of the technology readiness and future work needed to bring radiation tolerant devices to market.

2. Review of SEB Failure Mechanisms

Unexpected failures and reliability issues were observed in high-power silicon devices that had expected lifetimes of over 25 years soon after their development [32]. The effect of the SEB was first observed in 1986 by Aerospace Corp, who reported a destructive "latched current" effect in several N-type MOSFETs [16]. Experimental studies determined a correlation between failure rate and high DC voltage. It was not long before a group discovered that these failures stopped happening when tested in a salt mine 140 m below ground. Kabza et al. [32] attributed these failures to the terrestrial cosmic radiation that is experienced on Earth. Throughout the late 1980s and 1990s, many groups employed experimental and simulation radiation studies on Si power devices to determine the failure mechanisms responsible for SEB. To properly establish a context for the present SiC MOSFET failure mechanism review, a brief background of the earlier Si power device radiation studies is given first. The background will serve to: (1) outline the conceptualization of Si MOSFET failure mechanisms; (2) explain the methodology for validation–verification studies; and (3) illustrate the establishment of the conventional MOSFET burnout wisdom.

2.1. Evidence of the BJT Turn-On in Si MOSFETs during SEB

Experimental studies of the Si bipolar junction transistor revealed that heavy ion radiation could parasitically turn on the transistor while it was in the OFF state. Johnson [14] was one of the first to describe the physical mechanisms behind this phenomenon. Upon ion strike, electron-hole pairs are generated along its track length. This ionization creates a plasma filament able to support a short-lived current source where holes flow towards the lateral base region and the electrons flow towards the collector. This hole current can sufficiently forward-bias the base-emitter junction, surpassing the threshold voltage required to turn on the BJT. Once the BJT is turned on, the currents within the device will regeneratively increase until the simultaneous high current and high voltage trigger a second breakdown, leading to thermal destruction of the device. This mechanism was experimentally validated by varying current-limiting resistance between the stiffening capacitor and the collector lead [13]. The addition of a resistor suppressed the regenerative

feeding of current in the turned-on BJT and prevented the reaching of second breakdown when exposed to monoenergetic ions. Titus et al. [13] also noted that low stiffening capacitance (<5 μF) in the circuit circumvented burnout. Removal of current limiting resistance and increased capacitance triggered burnout behavior in all cases.

A cross-sectional layout of a generic vertical double-diffused MOSFET (VDMOSFET) is provided in Figure 2. The parasitic BJT structure is inherent to the MOSFET design: the N+ source act as its emitter, the P-body is its base, and the N-epitaxial region as the collector. It was thought the built-in structure could also be activated from radiation-induced currents. Figure 2 depicts a traditional N-channel VDMOSFET under high-energy particle bombardment.

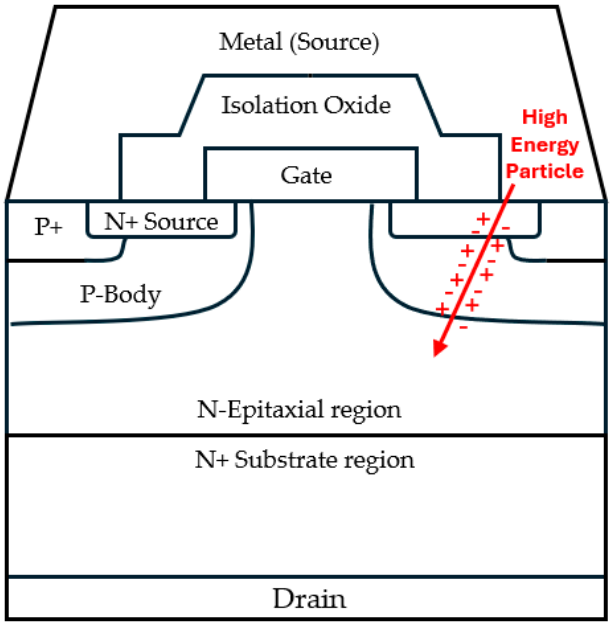

Figure 2. Traditional vertical power N-channel DMOSFET under high-energy particle strike at parasitic BJT region.

Experimental and simulation studies determined that BJT activation was responsible for the Si MOSFET SEB [14–18,33–41]. The charges deposited from a radiation strike begin flowing towards their respective terminals, inducing a potential on the parasitic structure, causing it to locally latch on. The N+ source begins emitting charge, and current begins regeneratively increasing until the device catastrophically breaks down. Kuboyama et al. [17] experimentally documented the enhanced charge collection from the N+ source in a Si MOSFET. This result was compared to a Si MOSFET that was fabricated without this N+ source, resembling the structure of a diode. The enhanced charge collection was not seen in this device, which, as a result, had a better SEB tolerance. The result indicated the condition for the parasitic BJT to trigger SEB and verified its enhanced current effect. It was shown in [42,43] that limiting current with a series resistor also prevented burnout in a Si MOSFET. When the parasitic BJT turns on, it draws current from the source to regeneratively feed into the device. The addition of a resistor at the source has shown to improve SEB susceptibility in both Si MOSFETs and Si BJTs, experimentally supporting the BJT turn-on failure mechanism. The studies quantified improvements are dynamically compared in Table 1; the voltage at which the device experiences burnout (V_{SEB}) was normalized with its rated voltage (V_R). The MOSFET without the N+ source in [17] did not burn out at any of the voltage biases tested, indicating that its V_{SEB}/V_R likely aligns with that of the diode. Note that some of the V_{SEB}/V_R results in Table 1 are in ranges due to the large number of sample devices tested. Nuances during the fabrication process cause burnouts at a varying threshold. These experiment types establish a foundation

for validating the BJT turn-on mechanism in MOSFETs. A more detailed review of the Si MOSFET SEB failure mechanisms is made by Titus et al. [44].

Table 1. Experimental Si power device studies with normalized burnout thresholds.

Device Type	LET (MeV-cm^2/mg)	V_{SEB}/V_R	Ref.
MOSFET	14	0.54	[1]
JBS Diode	59	0.75–1.0	[19]
MOSFET with N+ source	30	0.40–0.56	[17]
MOSFET removed N+ source	30	>0.68	[17]
No in-line resistor MOSFET	12–15	0.40–0.50	[42]
Resistor-protected MOSFET	12–15	0.70–1.0	[42]

Since Si diodes lack the parasitic BJT structure in their design, the conventional wisdom for many years was that these devices (other than high-voltage designs) were immune to destructive SEEs [10,32,45–47]. Charge-collection studies conducted on high-voltage PiN Si diodes observed charge amplification when voltage at the cathode is increased due to an increase in the internal electric field. This effect was reported as the charge multiplication phenomenon and was used to explain failures in high-voltage diodes [19,46,48]. Since this failure mechanism was dependent upon the application of a high voltage, the low-voltage diodes remained to be considered immune to destructive SEEs. In 2012, an experimental study testing JBS diodes DC-DC conversion failed due to SEB under heavy ion bombardment. These diodes failed at 50% V_R, including a diode rated at 45 V [49]. It was revealed that the JBS diode was more susceptible to SEEs because of their lack of protection at the Si/metal interface, causing melting at this area from a shorting between the anode and the cathode. This failure was not observed in diodes that protected the metal/Si interface [19]. The generated current from a heavy ion caused melting at this interface, shorting the anode and the cathode, leading to premature failure.

Although the diode is susceptible to SEEs, Si diodes have shown a greater SEB normalized threshold compared to Si MOSFETs. The experimental work in [1] showed 83% of Si Schottky diodes biased at 75% of its rated reverse voltage irradiated by an LET of 59 MeV-cm^2/mg can survive without permanent damage. Additionally, it was shown that all Si Schottky diodes under the same radiation conditions can survive with no damage when biased at 50% V_R. These data show considerably more radiation tolerance compared to a Si MOSFET in comparable conditions. These results suggest there are discordant mechanisms effecting these two types of devices. A comparison of the rad-tolerance between devices is listed in Table 1.

More recent experimental and simulation studies have described the failure mechanisms for Si PiN and Si JBS diodes [1,10]. Lauenstein et al. [1] deemed impact ionization insufficient for Si PiN diode SEB. Under ion strike, impact ionization leads to localized heating at the N-epitaxial/N+ substrate interface that causes a thermal generation of intrinsic carriers. The increase in intrinsic carrier concentration overwhelms the background doping in the device, leading to more local heating and creating a thermal runaway feedback loop until the device is thermally destructed. This is described in Equation (1) illustrating n_i as a function of temperature (T):

$$n_i(T) = e^{\left(-\frac{E_g(T)}{2kT}\right)}\sqrt{N_c(T)N_V(T)} \quad (1)$$

As temperature increases, the term E_g, which is the bandgap of the material, decreases; however the terms N_c, describing the conduction density-of-state, and N_V, describing the valence density-of-state, increase. The result causes n_i to increase with increasing temperature, eventually reaching the intrinsic temperature. This is the point where the intrinsic density equals the background doping concentration and marks the beginning of the thermal instability process.

In JBS power diodes, peak lattice temperatures are observed from the same mechanism leading to sublimation at the N-epitaxial/N+ interface [10]. Figure 3 illustrates the feedback loop between intrinsic carrier concentration and peak temperature with respect to device depth.

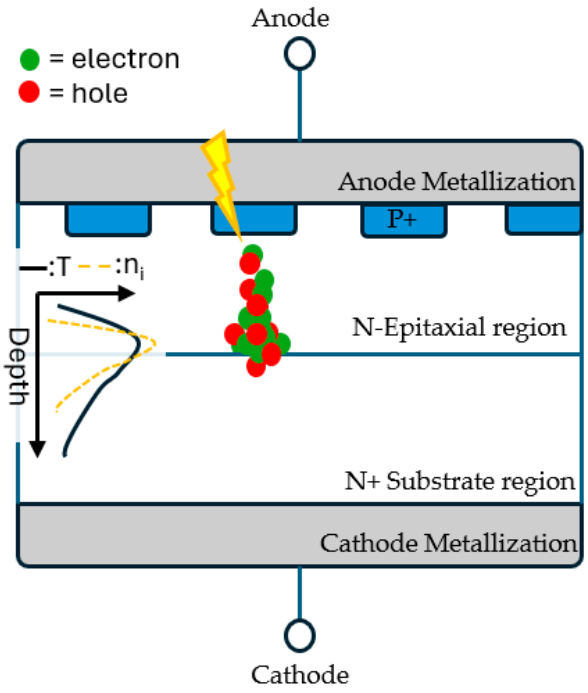

Figure 3. Power diode under radiation strike. Carriers generated from impact ionization with 1D intrinsic carrier concentration and device temperature response.

The increase in intrinsic carriers becomes regenerative since it increases current density, leading to further heating of the lattice, leading to thermal generation of even more carriers. This process continues until the device catastrophically fails from a thermal runaway and describes the second breakdown process that power devices undergo when stressed beyond their blocking capabilities. The Si diodes failure mechanisms are inherently differentiated from Si MOSFETs. The studies highlighted present substantial data to support the claims, and the failure mechanisms between these two devices are well established.

2.2. Review of SiC MOSFET SEB Failure Mechanisms

In SiC-based MOSFETs, it was commonly assumed that the BJT turn-on mechanism would be responsible for SEB. This became the conventional way of thinking, which may have led to confirmation bias when investigating the device. Zhang [23] was one of the first to investigate SiC MOSFET SEB failure mechanisms, in 2006. Zhang credits the extensive Si MOSFET studies carried out in the 1990s as the basis for the understanding of the SEB failure mechanism in these devices. The simulations conducted were in 2D and did not verify the results with an experimental study on SiC devices, but rather were verified with previous Si MOSFET studies. The SiC MOSFET under heavy ion bombardment with LET ranges between 17–19 MeV-cm^2/mg showed burnout at 215 V. The device also showed burnout on the order of nanoseconds, which disagrees with SiC device simulations completed in recent years [20,22,25–27,29]. Although the static breakdown voltage (BV) of the device was not given, the N-drift doping (N_D) profile of 3×10^{15} cm^{-3} was given. Using ideal breakdown methods derived from [50] listed in Equation (2), the BV should be on the order of thousands:

$$BV = 4.77 \times 10^{14} N_D^{-\frac{5}{7}}. \quad (2)$$

A breakdown due to SEB at 215 V leaves a V_{SEB}/V_R of 0.05 or smaller, which is lower than any threshold voltages recorded experimentally. The simulations were conducted in 2D with a coarse tri-meshing scheme. The impact ionization was modeled with equations from Selberherr [51], which did not include temperature dependence. Common impact ionization models, such as the Okuto-Crowell model and the van Overstraeten–de Man model, include temperature dependence to optimize simulation fidelity [52]. Similar to the SEB mechanisms in Si, Zhang [23] provides evidence of a SiC MOSFET exhibiting BJT turn-on. Zhang showed greater SEB susceptibility when the strike location was at the channel (N+/P-body/N-drift) region. When ions were struck vertically over the device source region, the parasitic BJT structure of the MOSFET burnout was triggered at lower voltage biases than striking at the channel or the P-body regions. However, in more recent experimental and simulation SiC MOSFET studies that explored ion angle and strike location dependence, it was revealed that the channel region is no more susceptible to SEB than the source region [25,27,28]. In [23], Zhang provides additional evidence for a BJT turn-on by displaying the electric field peak shifts during strike. Prior to impact, the peak electric field in the device is at the N+ source/P-base junction; however, during the strike the peak shifts to the N-drift/N+ substrate interface. Zhang explains this shift as "base pushout" due to the current injection of the parasitic BJT, which shifts carrier concentration and impact ionization to the N-epitaxial/N+ substrate region. However, this "base-pushout", known as the Kirk effect, has been observed in power devices without a parasitic N+/P/N structure [53]. SiC diodes have shown peak electric field shifts from the P+/N-drift region to the N-drift/N+ substrate in simulations [22] and may not be a phenomenon unique to MOSFETs. Zhang [23] concludes that the failure mechanism of SiC MOSFETs is no different from Si MOSFETs and characterizes the sequence of SEB exactly as stated in Si MOSFET studies [14–18]. There are still many questions about the accuracy of the simulation models employed and the logic used to advocate for the failure mechanisms described. During the time Zhang was completing this work, the MOSFET SEB failure mechanism was well documented and understood for Si-based devices. It is not unreasonable to speculate that conventional ideas from previous works influenced this SiC failure mechanism study. Such confirmation bias would preclude alternative failure mechanisms during investigation of the device.

Advocacy for the BJT turn-on in SiC MOSFETs continued in 2011. Griffoni et al. [24] documented the first experimental neutron exposure testing on SiC power MOSFETs. Testing 1200 V rated devices, no SEB events were observed when irradiated with neutron fluxes of 1.5×10^4 cm^{-2}-s^{-1} and 5.7×10^4 cm^{-2}-s^{-1} for 50 MeV and 80 MeV neutrons, respectively. However, the Si counterparts rated at lower voltages all experienced failure. Griffoni argued that the lack of SEB in SiC MOSFETs was attributable to a larger built-in potential between the N+ source and the P-base region requiring higher energy particles to turn on the parasitic BJT. The basis for Griffoni's failure mechanism understanding came from Zhang in [23].

More recent simulations investigating the physical mechanisms of SEB in these devices have also agreed with Zhang. Johnson et al. [25] aimed to find experimental evidence of the BJT turn-on mechanism. Johnson et al. employed a pulse-laser two-photon absorption experiment to observe charge collection in a SiC MOSFET. The collected charge results from the MOSFET were compared against a SiC JBS diode and are displayed in Figure 4. The devices were exposed to an ionizing source while reverse-biased, and their collected charge measurements were recorded. The charge amplification seen in Figure 4 in the MOSFET suggests parasitic BJT activation, where the diodes results indicate less severe internal carrier generation. While the structure inherent to MOSFETs showed more collected charge than the diode without it, it is not clear how much this mechanism drives the SEB process. The authors do note that charge amplification has complimentary mechanisms.

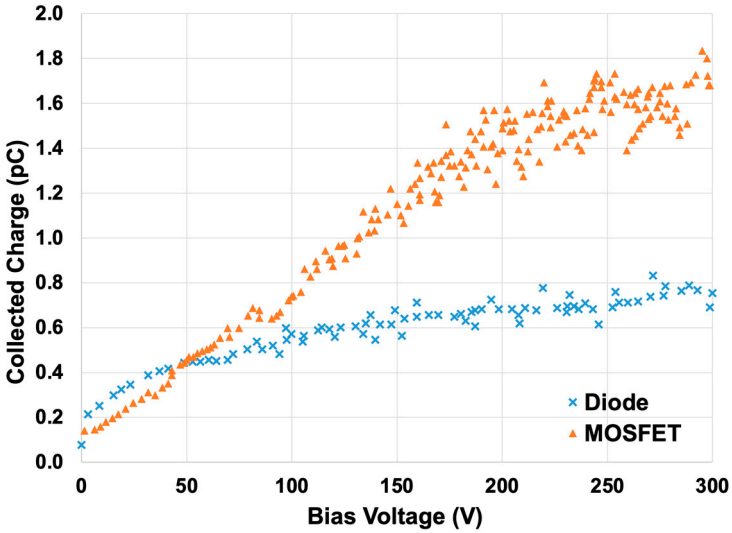

Figure 4. Diode and MOSFET collected charge at reverse biases of 0 to 300 V, based on the data from [25].

Johnson et al. further conducted 2D simulations of the devices under heavy ion strike to investigate the charge collection at specific regions. The results from the simulations in Figure 5b show the diodes are independent of collected charge with respect to position, where the MOSFET in Figure 5a exhibited significant gain in collected charge for a strike near the parasitic N+/P/N region.

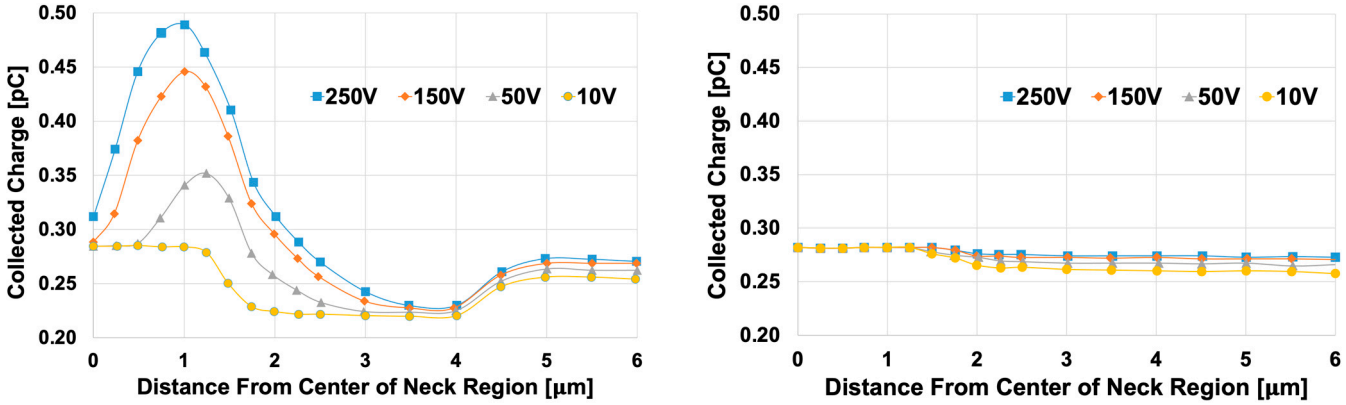

Figure 5. Collected charge simulation results of (**a**) MOSFETs; (**b**) diodes with respect to devices lateral position where ion strike occurs, based on the data from [25].

While the evidence of BJT activation seems overt, Johnson et al. did not observe SEB unless impact ionization was implemented in the MOSFET simulation. The charge amplification from the N+/P/N region alone was not enough to cause thermal destruction of the device, and the authors suggest there is another complimentary mechanism responsible for SEB. Johnson et al. concluded the parasitic bipolar amplification is an important mechanism contributing to SEB, but did not quantify the amount of contribution it provides with respect to the impact ionization. Additionally, the positional dependence observed in the simulation revealing the significant charge contribution from the N+/P/N region was not supported by the experimental results originally examined, leaving a discrepancy between the two studies. Although the evidence displayed in both simulation and experiment heavily indicates that the BJT is activated, no conclusion about its contribution towards SEB as a primary mechanism can be drawn.

Zhou et al. [26] compared Si and SiC MOSFETs SEB susceptibility by exploring the failure modes of each device. Drawing from previous work in [54,55], Zhou et al. attempted to verify the turn-on of the parasitic BJT in a SiC MOSFET by observing the 'base-pushout' phenomenon. Two different heavy ion strike conditions were simulated on 600 V Si and SiC devices. Condition A is at a drain-source voltage (V_{ds}) of 500 V and LET = 1.51 MeV-cm^2/mg; condition B is at V_{ds} = 80 V and LET = 151 MeV-cm^2/mg. Electric field distributions were shown over time throughout the simulation for each condition. In condition A, the Si MOSFET experienced SEB and the SiC MOSFET does not. The Si MOSFET showed a peak electric field shift from the N+/P-body interface to the N/N+ homojunction region, while the SiC MOSFET suppressed an electric field shift. Zhou et al. postulated that the reason the SiC MOSFET did not burn out in condition A is due to the high doping profile (two orders of magnitude larger than Si) in the drift region. The low LET of the particle can be more easily suppressed because a larger number of electrons from injection are needed to trigger BJT turn-on. In condition B, the Si MOSFET did not burn out, however the SiC MOSFET did. The electric field distributions showed the same shift in peak electric field to the N+/N junction in the SiC MOSFET that the Si MOSFET experienced except on a picosecond timescale. Zhou et al. claim that the base-pushout phenomenon from the BJT turn-on induced a peak electric field, but they could also be describing the Kirk effect. The electric field eventually surpasses the critical electric field, triggering second breakdown in the device. Since both the Si and SiC MOSFETs saw the same electric field shift, Zhou et al. argue that the failure mechanisms are subsequently the same. Since it is established that Si MOSFETs fail due to BJT turn-on, Zhou et al. explain that this must be the case for SiC. The shifting of the peak electric field has been observed in SiC diodes from the P+/N drift region to the N-drift/N-substrate in [10] and is not a phenomenon unique to MOSFETs. Additional evidence via carrier current density distributions needs to be obtained in order to show the true biasing of the parasitic BJT.

Witulski et al. [8] investigated a SiC MOSFET via 3D TCAD simulation. Their approach was directed at determining the contribution of the BJT turn-on mechanism during burnout. Two MOSFET models were employed: one with nominal impact ionization and one with impact ionization artificially turned off. The results showed that without impact ionization, the device did not experience SEB. The current densities of two models illustrating the difference in impact are redrawn in Figure 6.

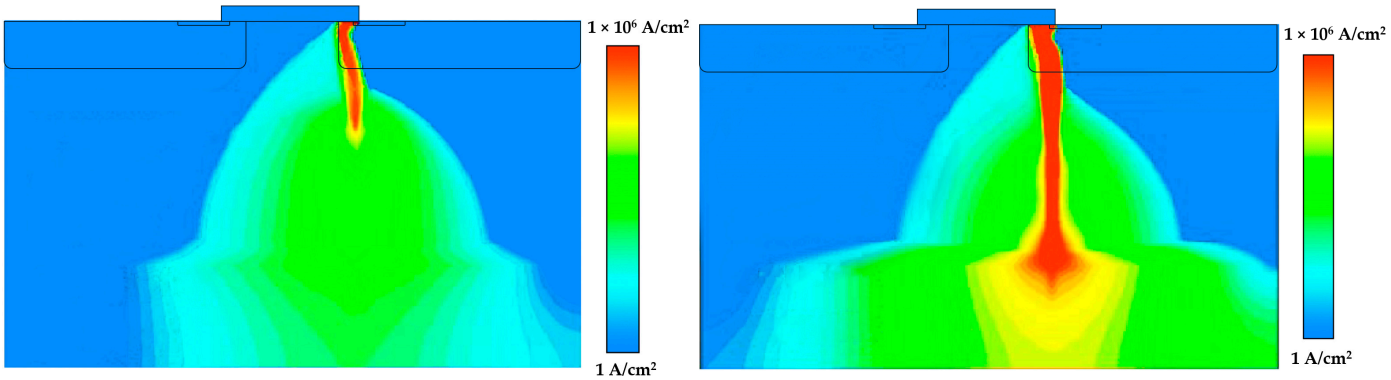

Figure 6. Electron current density contours of models with (**a**) impact ionization turned off, isolating for BJT contribution; (**b**) impact ionization turned on, based on the data from [8].

Peak current density was observed at the N+/P/N region in Figure 6a; however, it could not trigger SEB independently when modeled without impact ionization. Witulski et al. argued that the impact ionization at the epitaxial drain junction works as a complementary mechanism to the parasitic turn-on of the BJT. The failure mechanism proposed can be simplified into three phases: (1) strike-induced carriers bias the parasitic BJT on; (2) electric field peak shift at the N-epi/N+ region is high enough to initiate additional

carrier multiplication; and (3) carrier generation from both BJT and impact ionization short the source to the drain, causing avalanche effects leading to SEB. The contribution of each mechanism, however, is not quantified in this study. Similar to the work in [25], the BJT mechanism may turn on, but may not contribute an amount comparable to the impact ionization at play. It was shown when isolated, the BJT turn-on could not cause SEB, but the isolation of the impact ionization mechanism was not explored in this study.

Differing from experimental studies on Si JBS and MOSFETs where the SEB failure and degradation thresholds are starkly different, experimental studies on SiC JBS and SiC MOSFETs yield almost exactly the same results [1,19,20]. Table 2 quantifies the V_{SEB}/V_R between devices and illustrates the similar radiation tolerance. The alignment of the degradation in SEB thresholds of the two SiC-based devices are compared in [8,21,56–58] and show that diodes and MOSFETs experience burnout and degradation at the same voltages over a wide LET range. The overlap in degradation and SEB threshold suggests a common mechanism corrupting the two devices. Structurally, a SiC diode does not have a parasitic BJT, suggesting this cannot be the mechanism responsible in a SiC MOSFET. Analytical studies in [22] showed that SiC devices experience heat generation density 100× faster than Si showing burnout on two separate timescales. Additionally, it has been shown experimentally in [1,59,60] that SiC devices are more prone to permanent degradation damage than Si devices. These characteristics suggest different physical mechanisms take place, causing either partial or catastrophic destruction of the device.

Table 2. SiC power device normalized SEB threshold comparison.

Device Type	LET (MeV-cm^2/mg)	V_{SEB}/V_R	Ref.
MOSFET	24	0.50	[1]
JBS Diode	27	0.42	[57]
No in-line resistor MOSFET	22	0.42	[20]
Resistor-protected MOSFET	20	0.41	[20]

Shoji et al. [22] was also interested in the contribution of the mechanisms that cause power device SEB. Similar to the Si study in [17], where the parasitic BJT was removed from a MOSFET to see if SEB susceptibility was affected, Shoji et al. removed the N+ source in a SiC MOSFET. This technique showed 22–70% increases in V_{SEB}/V_R for Si MOSFETs. However, the traditional MOSFET and diode-like structures compared in Figure 7 show trivial differences in SEB current flow and maximum lattice temperature, exhibiting no increased tolerance in burnout voltage.

Shoji et al. argued that these results indicate little contribution from the parasitic N+/P/N transistor towards SEB in SiC power MOSFETs. Using experimental and simulation results, they observed that the sublimation temperature is rapidly reached at the N/N+ substrate junction. The mechanism proposed is a three-part process: (1) mass injection of carriers causes a "punch through" peak electric field at the N/N+ interface; (2) a spike in the electric field initiates impact ionization, causing high electron currents in this region; and (3) simultaneous high current and high electric field leads to extreme heating of the lattice until the device is thermally destructed. The modulation of the electric field in a MOSFET under high-energy particle strike is illustrated in Figure 8. The initial electric field, E_0, has a peak at the N+ source/P-body interface. As carriers are injected from the strike, the kinetic electric field, E_k, distribution demonstrates the peak shift (Kirk effect) to the N-epitaxial/N+ substrate region. This spike in electric field drives the carrier multiplication process and is important to highlight for alternative SEB failure mechanisms. Overall, the agreement between simulation and experimental capabilities by Shoji et al. demonstrates a high-fidelity validation and verification research methodology.

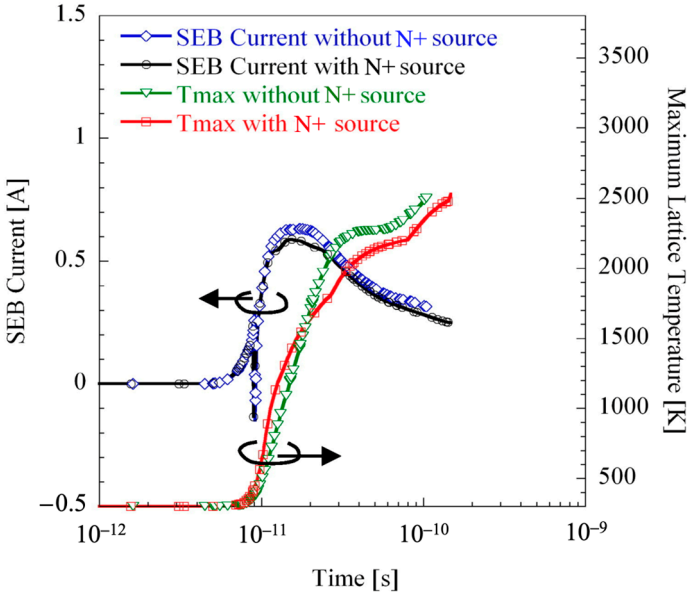

Figure 7. Simulated SEB currents and max lattice temperatures with and without the N+ source region in SiC MOSFET, reproduced from [22].

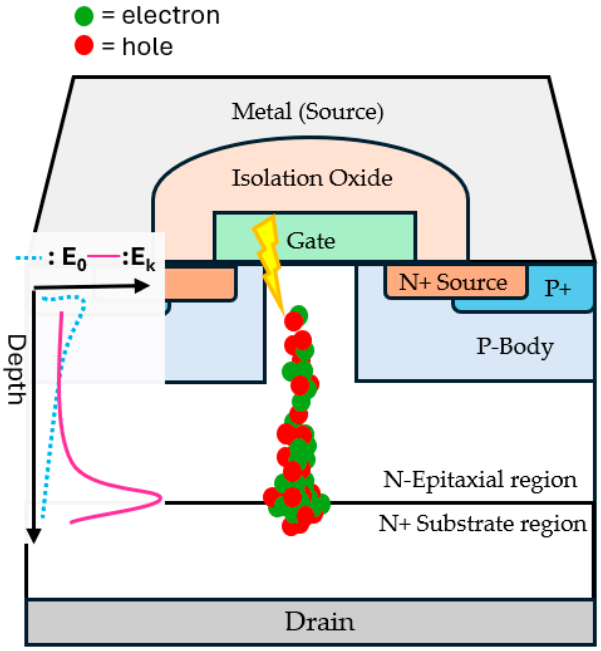

Figure 8. Vertical N-channel double-diffused power MOSFET under radiation strike with 1D electric field distribution and carrier mapping. The peak electric field shift or Kirk effect is illustrated.

The timescale of the BJT was also investigated by Ball et al. [20]. In this study, they attempted to improve SiC MOSFET susceptibility by implementing an in-line resistor with the source contact. This technique worked in Si as shown in [13,42,43] because it was able to suppress the parasitic BJT current upon activation. The data in Figure 9 showed no change in the SEB voltage with the in-line resistor and suggests that the timescale for the resistor to work is too slow (on the order of nanoseconds) to assist with SiC burnout current. The V_{SEB}/V_R results are listed in Table 2. Where this technique showed a 40–150% improvement in the Si MOSFET, the technique in SiC showed a trivial 0.59% decrease in the threshold ratio. Figure 9 shows that the MOSFET has a current injecting mechanism that the diode lacks, which is likely the avalanching and parasitic BJT. Adding the in-line resistor works to successfully suppress the current transient after 1.2 ns; however, it had

no effect on preventing SEB in either device. While the BJT may turn on in a MOSFET, it should be noted the SEB mechanism is occurring on a timescale faster than the time constant of the device.

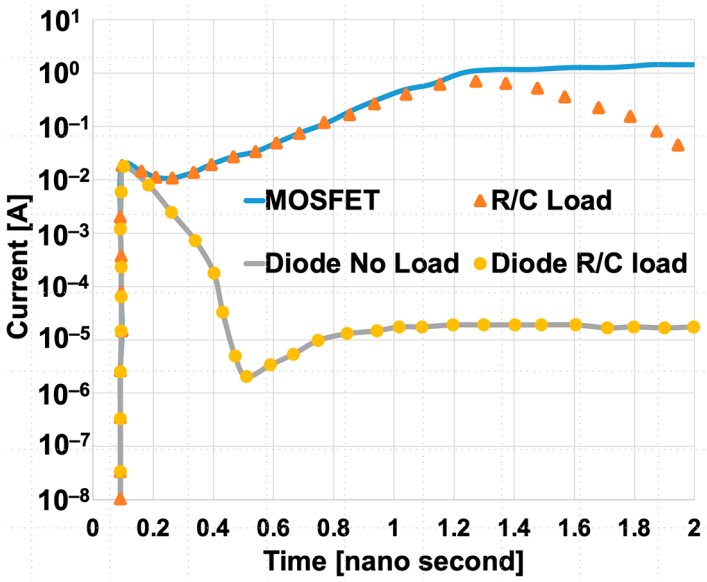

Figure 9. Current plot comparison of diode and MOSFET with and without implementation of the in-line resistor, based on the data from [20]. The diode matches the MOSFET for the first 0.15 ns, then responses begin to differ.

Instead of the parasitic transistor as the primary SEB mechanism, Ball et al. proposed a high-pulse energy failure mechanism. Applying a power density double integral, they stated that the high leakage current generated during ion strike while under high voltage bias results in energy dissipation that can exceed the capabilities of the semiconductor. The mechanism can be summarized in three phases: (1) ion strikes in SiC induce high current transients that occur due to resistive shunts; (2) simultaneous high current and high voltage causes excessive power dissipation; and (3) energy pulses accumulate until the material limits of the device are surpassed, causing various degrees of damage. Figure 10 describes the total energy dissipation required to onset degradation and SEB. The authors suggest a unified energy dissipation threshold as a function of LET and voltage bias. While the energy dissipation threshold has some supported evidence to suggest areas of degradation and SEB, devices have predisposed differences upon fabrication. The threshold values amongst a wide range of devices likely cannot be categorized into SEB/degradation based on one power dissipation calculation using the values from [20] alone.

In 2020, McPherson et al. [28] demonstrated SiC MOSFET failure mechanisms via 3D simulation that agreed to a high degree with Shoji et al. [22]. McPherson et al. simulated a 1200 V SiC MOSFET under heavy ion strike of LET 46 MeV-cm^2/mg to correspond with experimental data collected in [61]. McPherson et al. showed burnout at 500 V and later proposed design changes to increase the SEB threshold voltage. In the simulation from the traditional MOSFET burnout, McPherson et al. provide time evolution 2D and 1D plots of the temperature and electric field. The burnout McPherson et al. described can be simplified into three phases after carrier injection: (1) transit of carriers to their respective terminals, causing modulation of the electric field; (2) impact ionization induced by the new peak electric field at the N/N+ region leads to carrier multiplication; and (3) high carrier density causes a regenerative thermal carrier generation process that forms a mesoplasma. The runaway process continues until the sublimation temperature is reached. Instead of a BJT turn-on at the N+/P/N junction, McPherson et al. describe a shorting phenomenon between the N+ source and N-epitaxial region from carrier flooding that overwhelms the P-body. This shorting phenomenon diffuses carriers into the drift region from the source,

but is not a significant source in the carrier multiplication process. McPherson et al. observe SEB at 120 ps, which agrees with other simulation studies [10,22]. This burnout timescale is orders of magnitude faster than the induced BJT turn-on shown in Si MOSFETs.

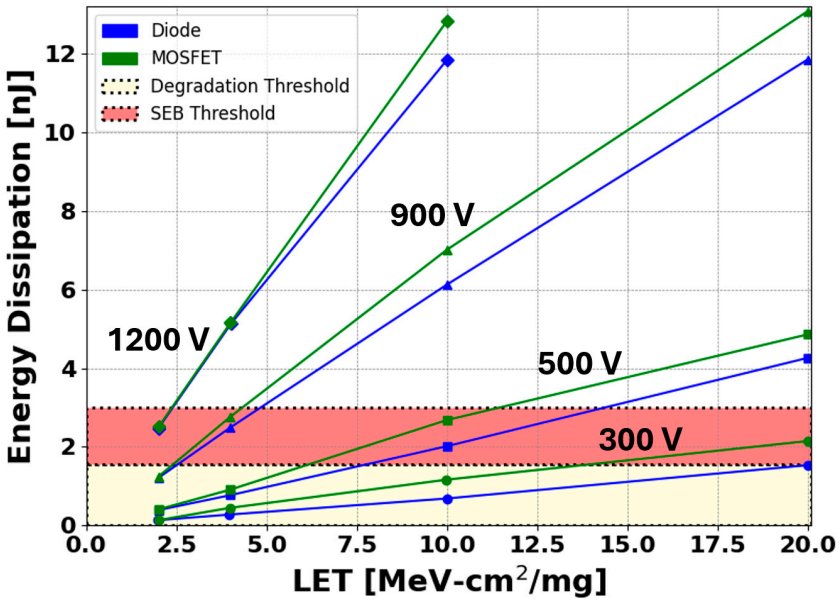

Figure 10. Calculated energy dissipation for 10 ps after heavy ion strike with degradation and SEB threshold conditions, based on the data from [20].

The primary failure mechanisms reviewed are summarized in Table 3 and are organized in three primary stages. Internal carrier generation characterizes the carrier-generation mechanism outside of injected carriers from the radiation strike. The regenerative feedback mechanism outlines how carriers and currents are self-continued within the device. Runaway failure is the distinct signature for SEB and catastrophic device failure.

Table 3. Summary of proposed SiC MOSFET burnout mechanisms into three primary stages.

	BJT Turn-on Primary Mechanism [1]	Coupled BJT-Impact Ionization Mechanism [2]	Mesoplasma Formation Mechanism [3]	High-Energy Pulse Mechanism [4]
Internal Carrier Generation	Injected carriers flow toward terminals, forward biases BJT	Injected carriers flow toward terminals, forward biases BJT	Mass carrier transit modulates E-field, initiates impact ionization	Resistive shunts cause increased current
Regenerative Feedback Mechanism	BJT turns on, begins regeneratively feeding current into device	BJT produces constant current. Peak E-field initiates impact ionization generation of carriers.	High carrier density heats device, thermally generating carriers leading to higher density.	Simultaneous high current and high voltage cause energy dissipation
Runaway Failure	Simultaneous high current and high voltage causes second breakdown and thermal runaway	Mass carrier multiplication leads to avalanche effect causing SEB	Regenerative carrier creation forms a self-sustained mesoplasma until sublimation of material	Energy pulses cumulate until surpassing device limit

[1] [23,24,26]; [2] [8,25]; [3] [27–29]; [4] [20].

The SiC MOSFET single-event burnout failure mechanism has been debated since the device began to be studied. The conventional ideas about SiC MOSFETs have been questioned as more thorough experimental and simulation studies have been performed. Although the BJT turn-on theory has had support in the past and has been well documented

in Si, experimental studies and high-fidelity simulations have come out in support of alternative mechanisms that are similar to the physics of Si and SiC diodes. The same experiments that verified the BJT turn-on in Si MOSFET SEB have shown contradictory results when performed on SiC MOSFETs. This section of the paper serves as a record of these studies and the arguments made to support and refute the proposed power device failure mechanisms.

3. SEB Performance Review of Power Device Designs

An ideal radiation-hardened power device would expand the SEB threshold voltage past its rated voltage ($V_{SEB}/V_R \geq 1.0$) with trivial degradation of the leakage current. The ideal device should additionally maintain the same performance in its forward and blocking states under static conditions. Rad-hard desires from industry state the need for power devices with a safe operating area (SOA) up to 1200 V, operating with the same electrical performance and efficiency as traditional devices [3]. While V_{SEB}/V_R is useful for quantifying overall radiation tolerance, designs with lower V_{SEB}/V_R can still satisfy the SOA and operation requirements desired. Figures of merit (FOM) typically used to optimize rad-hard devices consider the SEB threshold voltage with respect to the $R_{on,sp}$ [27,62–64]. Measured on-resistance is a function of the devices design, considerably affected by doping concentration, substrate thickness, and die area. The method for calculating the ideal $R_{on,sp}$ is seen in Equation (3), where t is device thickness and q is elementary charge, derived from [27].

$$R_{on,sp} = \frac{t}{qN_D\mu_e} \tag{3}$$

The $R_{on,sp}$ is a critical characteristic for quantifying the power loss during normal operation; the higher the $R_{on,sp}$, the worse the performance. Moreover, it is imperative that the evaluation of simulations employed be hyper-critical. Criteria for high-fidelity simulations and future work needed to bolster radiation-effect modeling are provided in Section 4. This section reviews the SEE design tolerances for three SiC MOS structures: the VDMOSFET, the trench gate MOSFET (UMOSFET), and the superjunction (SJ) MOSFET. The viability of each design is measured by (1) establishing the baseline device performance and characteristics; (2) analytically comparing proposed rad-hardened designs to fit industry requirements; and (3) evaluating the set-up that the designs are tested in.

3.1. Baseline VDMOSFET SEB Performance

The effects of radiation on Si and SiC VDMOSFET have been thoroughly simulated and experimentally studied. To classify the performance of a hardened SiC DMOSFET design, the baseline SiC structure must be quantified. For a 1200 V device, experiments have shown that SEB consistently occurs around 500 to 550 V, around 40% of its rated voltage [1,12,19–21]. Figure 11 shows the thresholds at which a 1200 V SiC DMOSFET experiences burnout with respect to heavy ion LET. The burnout threshold remains about the same for any ion LET greater than 10 MeV-cm^2/mg.

The $R_{on,sp}$ of a typical commercial 1200 V SiC VDMOSFET is in the range 2–3 mΩ-cm^2 [27,65–67]. A comparison of the SiC and Si 1D performance limits is made in Figure 12, showing the $R_{on,sp}$ with respect to the breakdown voltages from analytic data in [65]. A 10^2 magnitude improvement is illustrated between the materials.

Ball et al. [67] proposed using high-voltage rated DMOSFETs to have a SOA around the industry-desired 1200 V mark. The study introduced a 3300 V rated SiC MOSFET and experimentally showed the SEB threshold voltage can be improved under heavy ion strike. Although the 1200 V mark was not reached, Ball et al. showed that SEB occurred at 825 V and proposed a SOA of 650 V (57% improvement) in intense radiation environments (LET > 10 MeV-cm^2/mg). However, this improvement in SOA comes with a tradeoff because a device with this breakdown has a much thicker epitaxial layer. Subsequently, the $R_{on,sp}$ of the 3300 V device is 10 mΩ-cm^2 (233% more than the 1200 V device). As a result, this device exhibits 3× the resistive losses to its 1200 V counterpart, making the operation

of this device impractical. This derating method was also applied via 3D simulation in [27]. In this work, McPherson et al. increased the thickness of the epitaxial layer on a DMOSFET until the electric field was net zero at the N/N+ interface. As a result, the breakdown voltage was 3450 V, leaving a rated voltage in the range of 3000 V. The device experienced SEB at 1200 V, while the $R_{on,sp}$ was 7.6 mΩ-cm^2. Recent experimental and simulation studies suggest a unified degradation threshold that exists among high-voltage power devices. Johnson et al. [68] found that regardless of the rated voltage of the device, undesirable leakage currents occur at 180 V in intense radiation environments. The derating studies are compared in Table 4 to baseline and improved designs. The undesirable on-state resistance losses cause $\geq 2.5\times$ the cumulative leakage degradation than a traditional DMOSFET, making this method impractical for radiation hardening [19,27,68,69].

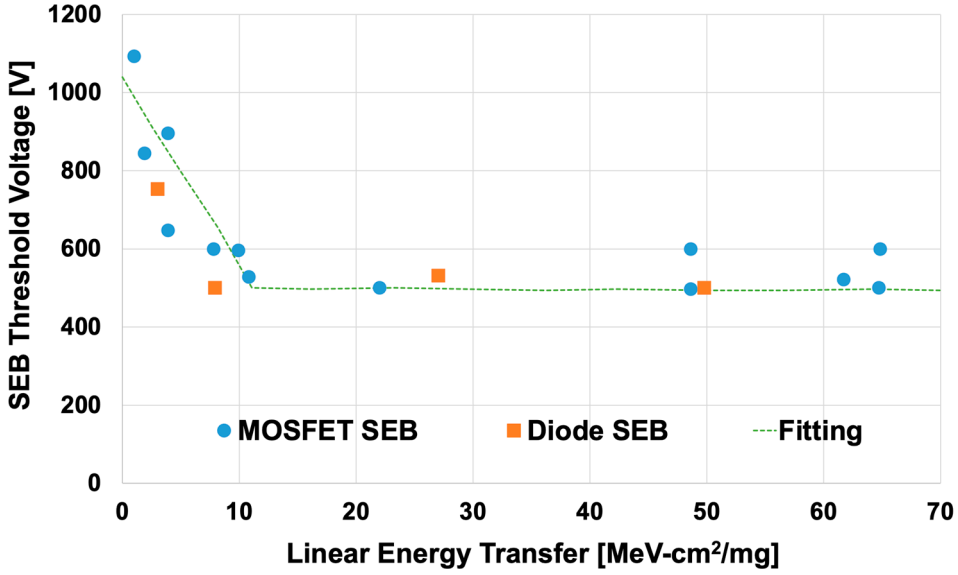

Figure 11. Experimentally determined SiC MOSFET and diode burnout threshold voltage, based on the data from [8,20].

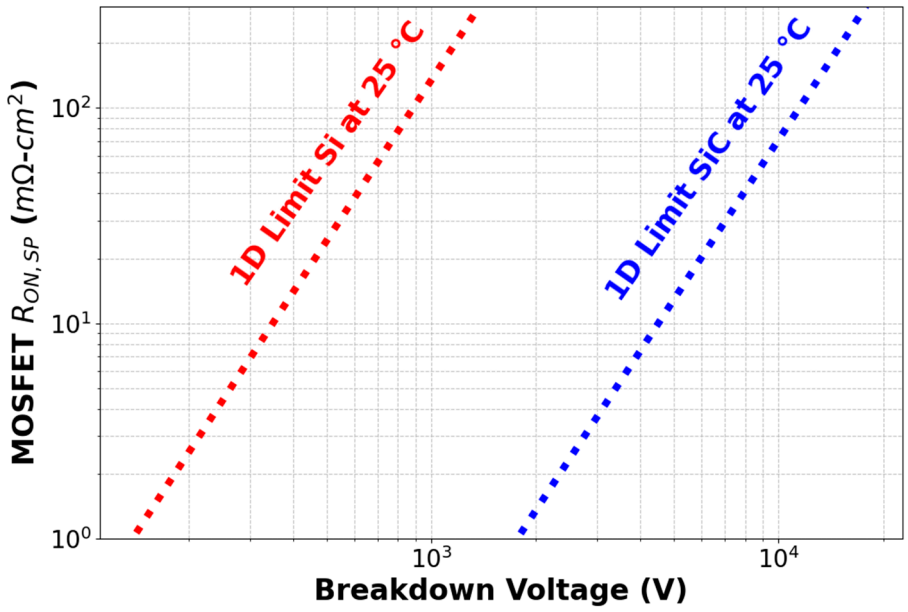

Figure 12. 1D specific on-resistance versus breakdown voltage comparing Si and SiC.

Table 4. SiC VDMOSFET baseline and improved design summary.

Device Design	Study Type	LET (MeV-cm^2/mg)	V_{SEB} (V)	$R_{on,sp}$ (mΩ-cm^2)
[1200 V] DMOSFET [1]	Experiment	10–65	500–600	2–3
[3300 V] Derated DMOSFET [2]	Experiment	60	825	10
[3000 V] Derated DMOSFET [3]	3D Simulation	46	1200	7.6
[1500 V] Buffer Layer DMOSFET [3]	3D Simulation	46	1200	3.2
[1200 V] DMOSFET [4]	3D Simulation	46	525	3.7
[1200 V] Non-uniform Buffer Layer DMOSFET [4]	3D Simulation	46	925	3.9
[1200 V] Narrow-channel DMOSFET [5]	2.5D Simulation *	40	1000–1200	N.A.

[1] [20]; [2] [67]; [3] [27]; [4] [28]; [5] [9]; * isothermal.

Hardened VDMOSFET Designs

The definition of a hardened MOSFET is a design that has been intentionally modified to improve radiation tolerance. Many techniques have been employed to correct radiation induced malfunctions that occur on power modules; however, a hardened device design has not been commercially employed [3,70]. As we know in the case of Si, the SEB performance of a MOSFET can be improved using an optimized buffer layer design [38]. The buffer layer is typically placed between the N/N+ homojunction to reduce the peak electric field that has been shown to generate at this location and can achieve a higher second breakdown voltage. By reducing peak electric fields at sensitive areas during radiation strike, higher operating voltages are required to initiate regenerative feedback loops that lead to burnout. This type of design has also been simulated in SiC power devices. Zhou et al. [26] looked to improve the SOA of 600 V breakdown SiC DMOSFETs and was one of the first to implement a buffer layer in SiC. Using a 2D simulation, Zhou showed the SOA of a traditional SiC VDMOSFET when exposed to high LET ions (15.1 to 151 MeV-cm^2/mg) was 15 V, whereas the 600 V Si counterpart had an SOA of 110 V. These results do not align with experimental Si and SiC parts that have been tested [1,19,67]. To improve the SiC SOA threshold to 600 V, Zhou introduced a 350 µm buffer layer doped on the order of 10^{18} cm^{-3}. Although SEB improvement was shown, the thickness of the hardened device increased the $R_{on,sp}$ undesirably more than 29%. The baseline and hardened design were not explicitly given. A buffer layer that large is impractical for device design, and the simulation conducted was strongly unaligned with baseline experimental values. Zhou et al. concluded that alternative solutions should be implemented to consider SEB ruggedness and overall performance.

A buffer layer was also attempted by McPherson et al. [28]. Using high-fidelity 3D simulations, two styles of buffer layer were implemented into a 1200 V rated SiC DMOSFET. One uniformly doped and one non-uniformly doped buffer layer, both 2 µm thick, were applied at the N-epitaxial/N+ substrate interface. The baseline 1200 V MOSFET ($R_{on,sp}$ = 3.68 mΩ-cm^2) struck by a 46 MeV-cm^2/mg ion showed burnout at 525 V, while the two buffer layer designs showed improved thresholds at 900 V and 925 V, respectively. Both designs behaved similarly in dynamic simulations; however, McPherson et al. recommended the non-uniform buffer layer because of the less sharp electric field peaks it generated in comparison to the baseline and uniform designs. The addition of either type of buffer layer increased $R_{on,sp}$ by 5%. McPherson et al. [29] later proposed SEB failure mechanisms for the buffer layer design. Studying a uniformly doped buffer layer design, 2 µm thick doped at 4 × 10^{16} cm^{-3} ($R_{on,sp}$ of 3.3 mΩ-cm^2), McPherson et al. observe the SEB location shift from the N/N+ region to 3–4 µm from the surface in the epi layer. Impact ionization is argued not to drive the burnout here; instead it is driven by the thermal generation of carriers. McPherson claims the buffer layer design failure mechanisms are also caused by the formation of a mesoplasma at the failure location that generates thermal carriers and increases current density to induce a thermal runaway. A more optimized buffer layer design was displayed in [27]. The 3D model had a static breakdown of 2038 V, experienced SEB at 1200 V, and had a $R_{on,sp}$ of 3.2 mΩ-cm^2. This buffer layer design

exhibits SEB over twice as long after ion strike as the baseline design and shows strong suitability for rad-hard applications. Table 4 compares the buffer layer designs with respect to the baseline studies and effect on $R_{on,sp}$.

Additional buffer layer designs showed improved SEB tolerance in SiC MOSFET designs. Some research studies have proposed improving the performance of power devices through the introduction of multiple buffer layer and dosage combinations [71,72]. Through 2D simulation, Lu et al. [73] implemented three different buffer layer designs: single-layer, double-layer, and triple-layer, where each layer is a different doping concentration. The exact dimensions of the optimal design were not disclosed; however, the buffer thickness were in the range of 4 to 50 µm and the doping concentrations ranged from 10^{16} to 10^{19} cm^{-3}. The baseline 1200 V SiC DMOSFET showed SEB from 350–500 V, depending on the ion LET. The lower threshold voltages could be owed to the 1500 K lattice temperature failure criteria Lu et al. employed, taken from [74]. The introduction of just the single buffer layer increased the SEB SOA to its 1200 V rating. The double- and triple-layer designs showed even better tolerance. The thickness and doping concentration added to the structure inherently increased the static breakdown voltage of the device. While the device was rated at 1200 V, the breakdown voltage was much higher. Lu et al. acknowledged that this design would involve an increase in $R_{on,sp}$, but did not quantify it in this study. Applying Equation (3), a device this thick and with that many doping regions would have a considerably undesirable electrical performance. Disclosure of the optimized design parameters is needed to accurately assess the suitability of this design for rad-hard applications.

2D simulations where isothermal effects are assumed have shown very acceptable SEB designs [9,75]. In a 2D axisymmetric (2.5D) and isothermal simulation, Zhu et al. [9] demonstrated a channel-narrowing technique in 1200 V SiC DMOSFETs that improves the SEE threshold from 500–600 V to 1000–1200 V. This type of technique can reduce peak electric fields within the device to improve SEB tolerance and gate damage, but it trades off with the $R_{on,sp}$ of the device [9,76]. Although the baseline design aligns with experimental data, the ion strike in this simulation environment caused the electro-thermal response to be non-physical. In turn, the material properties were temperature independent, and the lattice temperature of the device was under-approximated. This is problematic when accurately trying to determine SEB. To accurately assess the effect of this design technique, a 2D axisymmetric or 3D simulation with temperature dependence must be employed.

Research into localized carrier lifetime control suggested that Si VDMOSFETs can improve the SEB threshold and SOA [77]. McPherson et al. [29] investigated SiC material property effects on SEB by artificially fixing them via 3D simulations. A 100× increase or decrease in the carrier lifetime had a minimal effect (25 V decrease and 25 V increase, respectively) on the relative SEB threshold voltage. The most profound effect on SEB threshold voltage was associated with a 10× decrease in saturation velocity or a fixed 4.9 W/cm-K thermal conductivity value in the SiC lattice. The change in either of these two parameters yielded an additional +650 V and +700 V, respectively, to the baseline SEB threshold voltage. Despite the improvement to threshold voltage associated with decreasing the saturation velocity, there exists a trend in semiconductor materials where the saturation velocity increases as the bandgap increases. Since WBG materials have the best electronic performances, wider band-gap semiconductors are always going to be preferred in power device applications, so this saturation velocity will never be able to decrease to the level performed in this simulation [78]. However, thermal conductivity is a more plausible route as there are many UWBG semiconductor materials with extremely resilient thermal conductivities. Diamond, for example, has been shown to be one of the best semiconductor materials known on the planet and could potentially solve the rad-hard dilemma if the jewelry market was not so lucrative [79].

3.2. Baseline Trench Gate MOSFET SEB Performance

The trench gate or UMOSFET design has been studied as an alternative to the DMOSFET in power electronics because it can reduce the $R_{on,sp}$ owing to its smaller cell pitch

and high channel mobility on the trench sidewall [75,76,80]. The structural differences are illustrated in the cross-section in Figure 13. A parasitic BJT structure exists in this device that is qualitatively the same as a VDMOSFET. Looking at Figure 13a, the N+ source becomes an emitter, the P-body acts as a base, and the N-epitaxial region becomes a drain. Some other common power UMOSFET designs include a "buried" P+ layer underneath the gate oxide to act as a shield (see Figure 13b). This additional layer can reduce peak electric fields at this area when under high voltages to enable optimization, but it trades off with on-resistance [81].

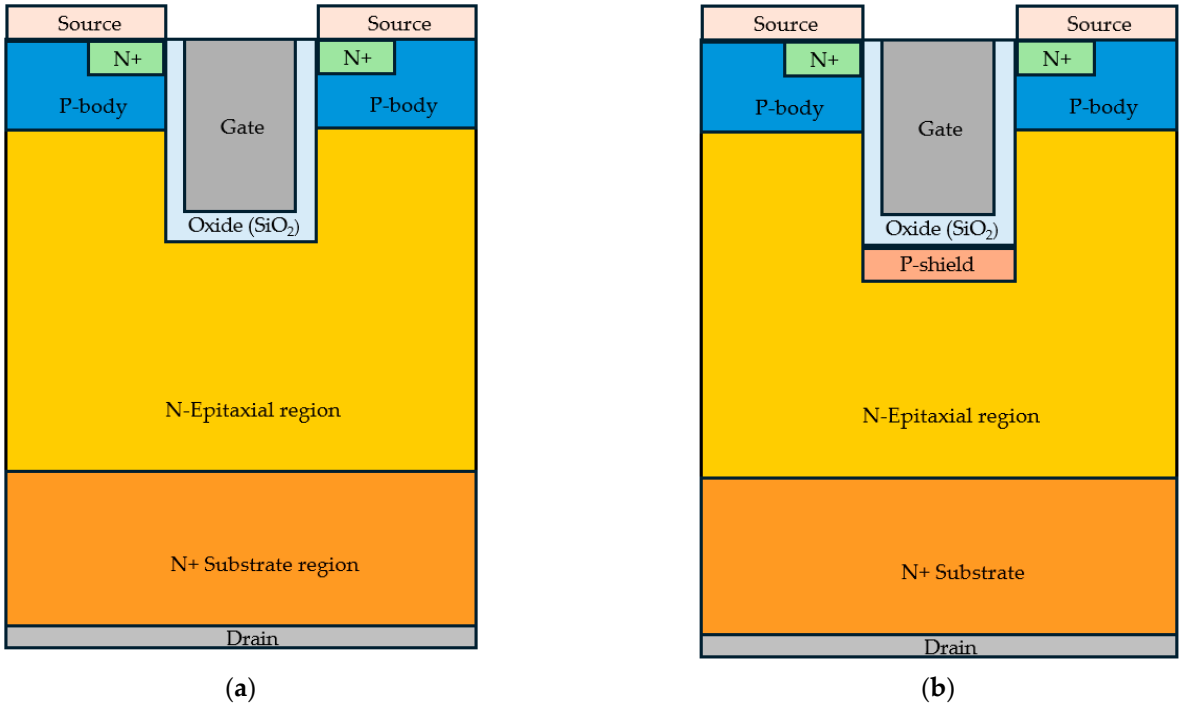

Figure 13. UMOSFET cross section (**a**) of a traditional vertical N-channel double-trench and (**b**) with a buried P-shield layer (not to scale).

Experimental studies of Si UMOSFETs show their susceptibility to degradation and catastrophic SEEs under radiation [82–89] and reveal similar performances to VDMOSFETs. A good review of Si UMOS radiation failure and degradation is outlined in [83]. Experimental SEE studies on SiC MOS structures primarily focus on the planar structure, leaving few reports on the trench gate. Most simulation work on SiC UMOSFETs has been conducted in 2D, which leaves more work to be undertaken on the validation effort in this field. A recent experimental study showed that a 1200 V SiC UMOSFET experiences SEB near 500 V for an LET of 75 MeV-cm^2/mg [90]. Kim et al. [91] via 2D simulation studied the device at low LET ion strikes (1.51–13.6 MeV-cm^2/mg). A 1200 V rated SiC UMOSFET had a SEB threshold of 530 V from a 7.6 MeV cm^2/mg ion strike. Wang et al. [92] studying the same device showed a SEB threshold voltage of 450 V. However, the model in [92] showed a max lattice temperature of 492 K at SEB, well below the sublimation temperature of SiC, suggesting improper thermal modeling. Higher-voltage UMOSFETs were more recently simulated in [93] to investigate derating of the device for rad-hardening. Using a P-buried layer UMOSFET design, the 3300 V rated device experienced SEB at 900 V. Despite its improved SEB tolerance, the $R_{on,sp}$ for the design was 185% higher than the conventional 1200 V UMOSFET. SiC MOSFETs with double trenches rated for 1200 V have been reported to have a $R_{on,sp}$ between 2.99 and 3.3 mΩ-cm^2 [75,80]. A summary of the baseline SiC UMOSFET performances are listed in Table 5.

Table 5. Summary of SiC UMOSFET baseline and improved design studies.

Device Design	Study Type	LET (MeV-cm^2/mg)	V_{SEB} (V)	$R_{on,sp}$ (mΩ-cm^2)
[1200 V] UMOSFET [1]	Experiment	75	500	3.0–3.3 [2,3]
[1200 V] UMOSFET [4]	2D Simulation	7.6	530	16.6
[1200 V] SAS UMOSFET [4]	2D Simulation	7.6	660	16.6
[3300 V] P-shield UMOSFET [5]	2D Simulation	75	900	9.4
[3300 V] DGF UMOSFET [5]	2D Simulation	75	1500	5.5
[900 V] Multi-buffer Layer UMOSFET [6]	2D Simulation	75	650	6.0
[650 V] UMOSFET [7]	2D Simulation	75	71	1.9
[650 V] L_{mesa} Adjusted UMOSFET [7]	2D Simulation	75	320	2.9

[1] [94]; [2] [75]; [3] [80]; [4] [91]; [5] [93]; [6] [94]; [7] [76].

Despite the different gate structures, the reported SEB failure mechanisms in SiC UMOSFETs are qualitatively the same as planar SiC DMOSFETs. The BJT turn-on has been advocated as the regenerative feedback source in [91,93]. However, it has been demonstrated that Si and SiC MOSFETs operate on much different time-scales and material limits, suggesting that Si failure mechanisms cannot be translated. More recent simulation work in [94] noted that SEB occurs before the BJT can fully turn on. The regenerative feedback mechanism causes thermal damage on a shorter timescale. From [90], the mechanism can be functionally simplified to three phases: (1) injected carriers modulate the electric field to create localized peaks at the SiO_2/N-epitaxial region and the N-epitaxial/N+ substrate region; (2) sustained peak electric fields generate more carriers from impact ionization; and (3) high carrier density increases lattice temperature, thermally creating carriers until the regenerative process reaches the sublimation temperature. The SEB mechanisms for the UMOSFET are still debated. More explicit SiC UMOSFET experimental studies are needed to conclusively validate the failure mechanisms proposed.

The high electric field in the gate oxide of a SiC trench MOSFET is a major concern when operating under reverse blocking mode [76,95]. Experimental and simulation studies on UMOSFETs show greater susceptibility to single event gate rupture (SEGR) [76,83,90]. Zhou et al. [76] simulated 650 V SiC Trench MOSFETs under heavy ion strike (LET of 151 MeV-cm^2/mg) that showed a safe operating area at 70 V (11% V_R) for SEB and 20 V (3% V_R) for SEGR.

Hardened Trench Gate MOSFET Designs

There are many hardening techniques that have been employed on Si UMOSFETs to improve SEE tolerance; however, a review of these Si-based designs is not within the scope of this paper. They are more properly discussed in [83]. In SiC power devices, few studies have been conducted. Owing to the high electric field, improvement of the catastrophic SEE threshold is particularly difficult in UMOSFETs. Wang et al. [94] showed that baseline SiC UMOSFET designs with static breakdown of 1217 V indicated that near 300 V (LET = 75 MeV-cm^2/mg) the sublimation temperature in the lattice had been far surpassed and damaging electric field peaks had been reached in the gate oxide. The $R_{on,sp}$ of the baseline design was 10 mΩ-cm^2, more than three times that of typical UMOSFET and DMOSFET designs, due to the buried P-layer under the oxide. The improved design proposed a multi-layer buffer and P+ shielding region that wraps the bottom of the trench gate. The methodology behind the buffer layers is the same as for DMOSFETs. The P+ shielding region was added to suppress the electric field at the gate oxide. The improved design had a $R_{on,sp}$ of 6.0 mΩ-cm^2, static breakdown of 1257 V, and SEB threshold of 650 V. Although there was considerable improvement to the SEB threshold, it was still not at the level desired by industry. Additionally, the $R_{on,sp}$ was impractical for general usage and more tests should be undertaken to consider the effects of SEGR on this particular device. It should also be noted that 2D simulations conducted are only a qualitative characterization of a heavy ion strike.

Previously, Wang et al. [92] had proposed island buffer layers in the trench-gate MOSFET. In this 2D simulation work, the initial designs with a breakdown of 1200 V experienced SEB at 450 V. Although Wang et al. deduced SEB by tracking drain current, the maximum global device temperature only reached 492 K within the device at burnout. The temperature dependence of the models employed was not disclosed, though the temperature being underapproximated suggests that it was isothermally modeled. Initial improved designs in this study added two buffer layers, each 1 µm thick, doped at 5×10^{16} cm^{-3} and 3×10^{17} cm^{-3}, which brought the SEB threshold to 550 V. The most successful SEB design in this work was the island buffer layer redrawn in Figure 14. This design incorporates a heavily doped N+ region within a more lightly doped N-buffer region, which drastically reduces electric field peaks during ion strike. The most optimized design (V_{BR} 1183 V), parameters disclosed in Figure 14, improved the SEB threshold voltage to 660 V (47% improvement).

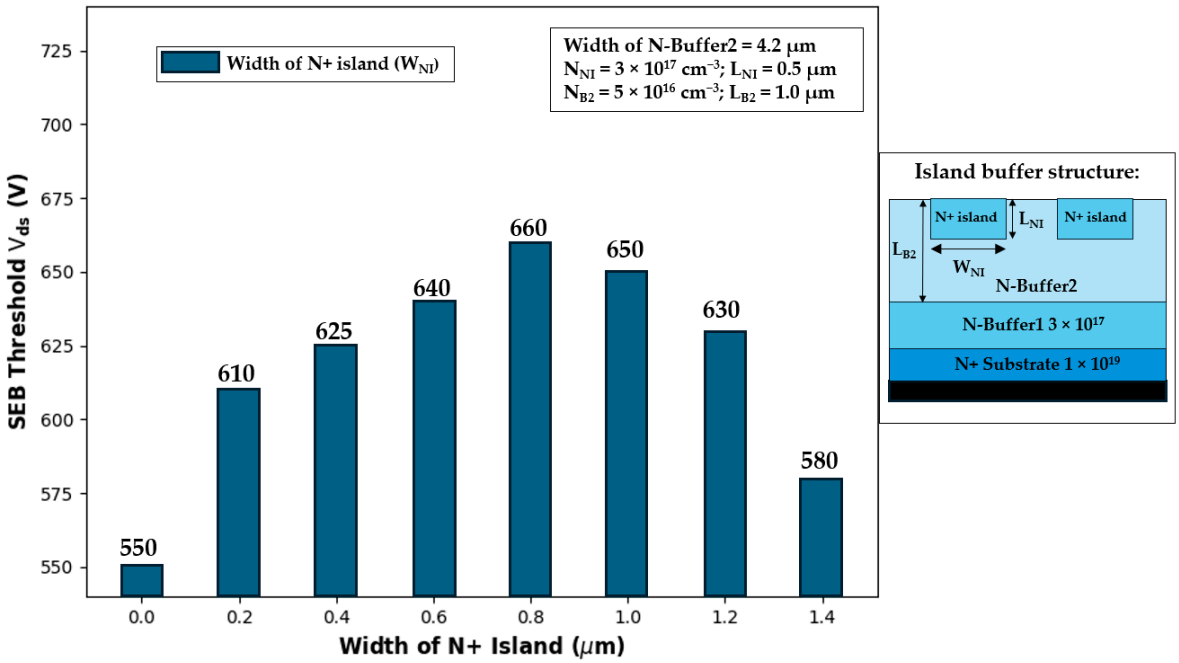

Figure 14. Island buffer layer SEB results and optimized design parameters, based on the data from [92].

The baseline design had an $R_{on,sp}$ of 2.91 mΩ-cm^2; the $R_{on,sp}$ of the island design was higher but was not quantified. This congested buffer layer scheme more than likely increased $R_{on,sp}$ to an undesirable amount. Additionally, Wang et al. [92] showed that the max temperature at SEB was on the order of hundreds, leaving questions about the simulation parameters employed. Other studies have implemented buffer layer designs in pursuit of SEB improvements in SiC UMOSFETs [76,96].

Kim et al. [91] implemented a self-aligned sidewall (SAS) heterojunction diode due to its excellent body diode characteristics and its reduction of the bipolar degradation effect from work shown in [97]. They saw a 25% increase in the SEB threshold as compared to a traditional double trench MOSFET with this design. However, the $R_{on,sp}$ in their baseline and improved designs were both unacceptable at 16.55 mΩ-cm^2. Of the proposed hardened UMOS designs reviewed, the SAS design had the highest $R_{on,sp}$ (see Table 5).

Another method of SEE hardening proposed by Zhou et al. [76] suggested adjusting the mesa width (L_{mesa}). The mesa width is the length between the P+ and the gate underneath the P-base and source contact in a double trench MOSFET. The L_{mesa} plays a critical role in modulating the peak electric field in the gate oxide and can be changed to help improve SEE ruggedness in a design. Zhou et al. showed by decreasing the width at this interface,

the SOA for SEB in a 650 V design was improved from 70 V to 320 V with a 56% increase in $R_{on,sp}$. The SOA for SEGR with the smaller L_{mesa} only improved from 20 V to 35 V. Although such an increase in $R_{on,sp}$ would still be better than the Si UMOSFET counterpart, the SOA for this device renders it impractical.

A more recent study simulated high-voltage SiC UMOSFETs with buried P-shield layers rated for 3300 V [93]. The baseline UMOSFET SEB performance is listed in Table 5. Shen et al. investigated the effect of the P-shield on SEB tolerance and proposed a novel structure with ground and floating P-buried layers (DGF UMOSFET). By reducing electric field peaks at sensitive regions in the device, the proposed structure reduced the baseline $R_{on,sp}$ by 41% and worked to improve SEB tolerance by 67%. The study properly approximates lattice heating in the simulation and terminates when the device heats to 2200 K. The structure is promising for SEB tolerance applications, though a more quantitative study is needed via 2.5/3D simulation. Additionally, for UMOSFET survivability SEGR should be evaluated for the DGF design.

Overall, preliminary SiC simulations suggest the electric field at the gate oxide in a trench gate MOSFET makes this device far too susceptible to SEEs. For high-power applications in intense radiation environments, alternative MOSFET structures should be preferred. More experimental studies on SiC UMOSFETs are needed to verify the simulation work mentioned above and to push this device structure forward.

3.3. Baseline Superjunction MOSFET SEB Performance

It has been shown in the above sections that an improved SEB tolerance can be achieved with traditional MOSFETs by increasing the breakdown voltage. However, to reach the 1200 V SEB rating with these methods, the $R_{on,sp}$ increases over 100% [27]. A potential solution to this tradeoff has been proposed in terms of a superjunction structure. The SJ structure (see Figure 15) replaces the uniformly doped epitaxial layer with an array of alternating N+ and P+ pillars. This configuration has horizontal and vertical electric fields giving the device a rectangular electric field profile. Consequently, the doping concentrations of the pillars can be higher than conventional epitaxial layers, yielding a significant reduction in $R_{on,sp}$ without affecting the breakdown voltage. This SJ MOSFET offers reduced gate and output charges, which allows for more efficient switching at higher and lower frequencies [98]. A parasitic BJT structure exists in the SJ MOSFET between the N+ source, P-body, and N-pillar regions. The first demonstration of this structure in Si was in the late 1990s [50]. Due to the unique electric field profile and space charge balance in the device, Huang et al. [99] hypothesized that a Si SJ MOSFET would have a greater SEB tolerance than a VDMOSFET and confirmed this with 2D heavy ion strike simulation. Ikeda et al. [100] later showed experimentally that an SJ offered no improvement to SEB tolerance over a VDMOSFET. Further simulation and experimental studies on Si SJ MOSFETs showed there was no inherent advantage in SEE tolerance [101–105]. More recently, it has been demonstrated that SJ theory can be effective for SiC power MOSFETs [106], and the first SiC SJ MOSFET was demonstrated in [107] at the 2016 ESCRM. Kang et al. [108] showed the reduction in $R_{on,sp}$ for a SiC SJ MOSFET can actually surpass the 1D limit ($R_{1DLimit}$) in standard 4H-SiC. Later simulation work in [109] adjusted the 1D SiC SJ limit with more suitable assumptions, but still found two orders of magnitude in tradeoff between the conventional 4H-SiC 1D limit and the SJ counterpart. The specific on-resistance versus breakdown voltage for the vertical superjunction in comparison to the SiC MOSFET 1D limit in Figure 16 demonstrates the tradeoff. Figure 16 also includes the simulation data from Zhou et al. [109] that validated this 1D SJ limit.

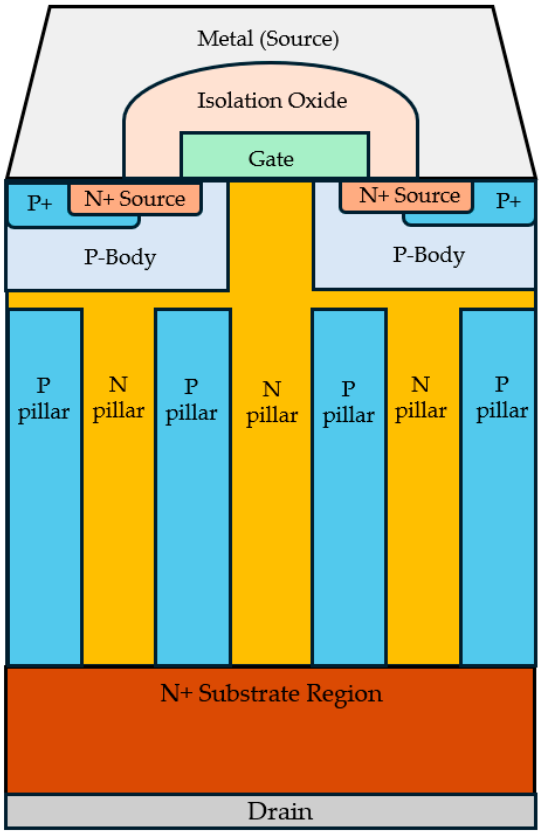

Figure 15. Traditional vertical N-channel double-diffused SJ MOSFET cross section (not to scale).

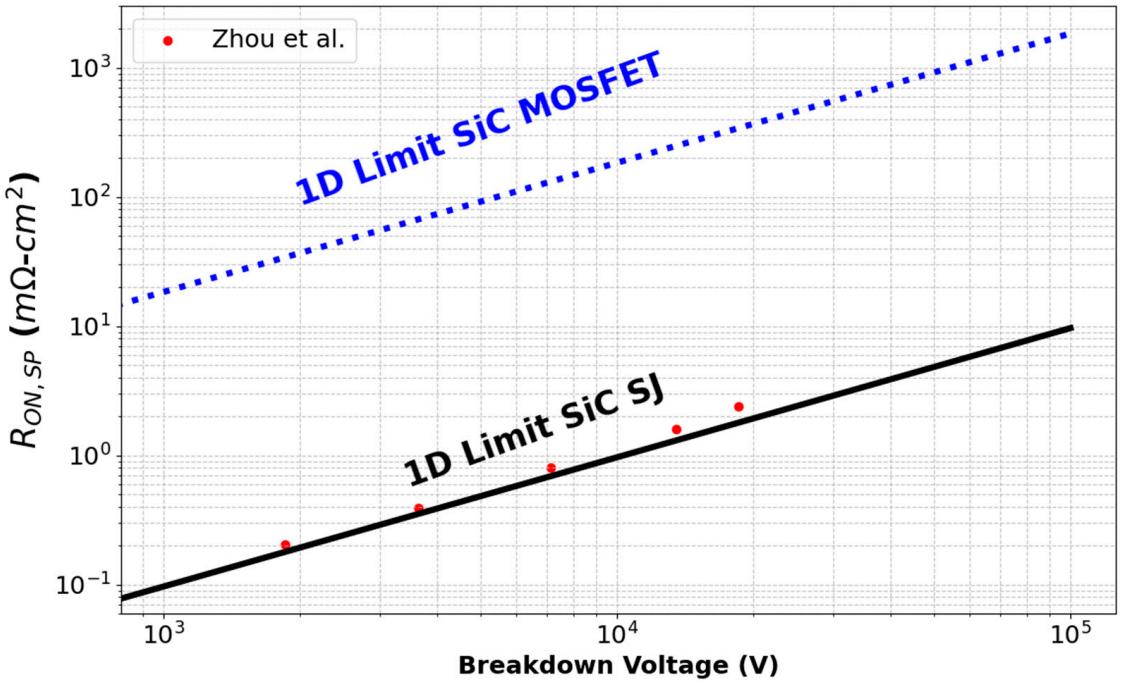

Figure 16. SiC 1D limit and SJ structure tradeoff with respect to Zhou et al. [109] vertical SJ model.

This allows for the derating method that showed SEB tolerance improvement for the traditional MOSFET to be implemented without the costly $R_{on,sp}$ tradeoff. McPherson et al. [62] demonstrated a SiC SJ DMOSFET 3D design that had a breakdown voltage of 5932 V and experienced SEB (LET 46 MeV-cm^2/mg) at 1150 V, while the $R_{on,sp}$ was only

3.0 mΩ-cm^2. In this work, the authors found a relationship between pillar width, V_{SEB}, and $R_{on,sp}$ and optimized these values to achieve the best design by implementing an FOM that takes the (V_{SEB}/BV) with respect to the ($R_{1DLimit}/R_{on,sp}$) for each design iteration. This FOM is quite useful for selecting suitable rad-hard designs and is suggested for future work on this technology. Few reports have described the SEB failure mechanism for this structure. The study in [62] described a failure qualitatively similar to SEB mechanisms in SiC VDMOSFETs. Three critical phases take place: (1) injection of carriers that modulate electric field peaks at pillar side-walls and the pillar/N+ substrate region; (2) peak electric fields cause impact ionization that generates carriers, high carrier density thermally generates more carriers; and (3) regenerative mesoplasma forms where each process drives heat until the sublimation temperature is reached. It should be noted the study observed a "shorting phenomenon" between the N+ source and N-pillar region from the initial flooding of injected carriers inducing excess current into the device. However, the current and electric field produced by this phenomenon were quickly suppressed. Semantics aside, this could be documentation of the turn-on of the parasitic BJT, but the mechanism is too short-lived to contribute to SEB triggering. Other SiC SJ MOSFET simulation studies have also described the SEB failure mechanism from a regenerative thermal runaway standpoint [64]. Although these designs have shown promise for increasing SEB tolerance, experimental and simulation work in [102] suggests single-event gate rupture can damage SJ MOSFETs at a more premature rate. This type of SEE should be explored and compared for SiC SJ MOSFETs in future rad-hard studies. Due to the novelty of the design, the fabrication of a SiC SJ MOSFET has not been commercialized. Experimental SEE testing has not been pursued; however, it is needed for validation of the SEB success in these devices.

Hardened Superjunction MOSFET Designs

Most hardened designs for the SJ structure have been studied on Si. Muthuseenu et al. [105] showed SEGR-hardened improvements in a Si device from the adoption of a trench-gate, buffer layer, and modified P-body combination. By inserting a buffer layer between the pillar/N+ substrate region, the electric field generated from radiation strike can be extended, reducing its magnitude and subsequently its charge multiplier effects. Changes in the $R_{on,sp}$ between designs are given in Table 6, and the ion strikes tested were in a isothermal 2D simulation. Additionally, Table 6 highlights the benefits between Si and SiC $R_{1DLimit}$ for proposed designs. Although the study showed improvement from the design, fidelity in the simulation cannot be attributed. Wang et al. [101] implemented two different buffer layer designs on 650 V rated Si SJ MOSFETs of 35 and 42 µm thick uniform and graded doping, respectively, to investigate their effect on V_{SEB} via 2D simulation. The resulting structures each had a >25% increase in $R_{on,sp}$; however, the uniform design increased the SEB threshold from 103 V to 605 V and from 103 V to 695 V for the layered design. The baseline result does not align with experimental Si SJ MOSFET tests from [100] (see Table 6). Wang et al. also showed a V_{SEB} improvement to 695 V for a novel P-type buried layer design. The layered buffer and buried layer design have a sufficient V_{SEB} to safely operate around its rating of 650 V. However, its effect on $R_{on,sp}$ is not known and the thermal assumptions in the simulation were not disclosed. Additionally, the onset of performance degradation prior to SEB was not quantified. These data are needed for a fair comprehensive evaluation.

Few studies have been employed to investigate the SEB performance of SiC SJ MOSFETs. No hardened structures were suggested by McPherson in [62]. In later works, McPherson et al. [110] proposed a semi-superjunction (semi-SJ) design that was tested via 3D simulations. Similar to a buffer layer, the semi-SJ design inserts a uniformly doped layer between the SJ pillars and the substrate. This layer extends electric fields to reduce their magnitude and subsequent impact ionization carrier generation. Actively placing it at peak temperature areas can increase the blocking voltage needed for avalanche breakdown and ion-induced mesoplasma formation. The structure employed is shown in Figure 17.

Table 6. Performance summary of SJ MOSFET devices and improved designs.

Device Design	Study Type	LET (MeV-cm^2/mg)	V_{SEB} (V)	$R_{on,sp}$ (mΩ-cm^2)
[600 V] Si SJ MOSFET [1]	Experiment	35	350	N.A.
[5500 V] SiC SJ MOSFET [2]	3D Simulation	46	1150	3.0
[650 V] Si SJ MOSFET [3]	2D Simulation *	151	103	7.5
[1200 V] SiC SJ MOSFET [4]	2D Simulation	77.9	500	3.5
[650 V] Si Graded Buffer Layer SJ [3]	2D Simulation *	151	695	10
[4500 V] SiC Semi-SJ MOSFET [5]	3D Simulation	46	1750	3.2
[1200 V] SiC Buffer Layer SJ MOSFET [4]	2D Simulation	77.9	800	3.9

[1] [100]; [2] [62]; [3] [101]; [4] [64]; [5] [110]; * isothermal.

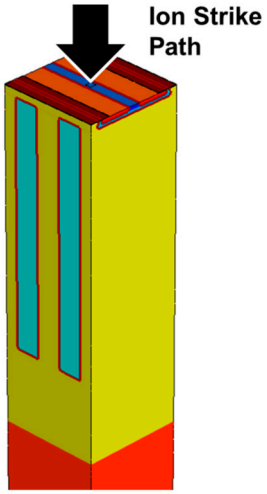

Figure 17. Isometric view of 3D Semi SJ model, reproduced from [110].

The most optimized semi-SJ model had alternating 1.2µm pillars covering 90% of the drift layer, leaving the bottom 10% uniformly N doped. The baseline SJ model had a breakdown of 5077 V, V_{SEB} of 950 V, and $R_{on,sp}$ of 3.2 mΩ-cm^2. The most optimal semi-SJ design had a BV of 4897 V, V_{SEB} of 1750 V, and $R_{on,sp}$ of 3.2 mΩ-cm^2. For the same on-state performance, this SJ design showed an 84% increase in V_{SEB}, leaving the SOA of this device near the level desired by industry. It was noted that a DMOSFET with a drift layer as thick as the semi-SJ design (31 µm) has a BV of 3354 V, V_{SEB} of 1250 V, and $R_{on,sp}$ of 8.0 mΩ-cm^2. This comparison highlights the overt benefit and suitability this semi-SJ design provides. More recently, Yu et al. [64] implemented a buffer layer on a SiC SJ MOSFET in pursuit of SEB improvement. In 2D simulations, a 5 µm uniformly doped buffer layer improved degeneration tolerance from 500 V to 800 V on a 1200 V rated design. Yu et al. observed failure at the SiC/metal contact interface (>1500 K) and advised this be considered in future designs. The SJ design has a major $R_{1DLimit}$ to $R_{on,sp}$ advantage over traditional device designs, suggesting high-voltage and hardened SJ designs are promising candidates for radiation hardening applications.

4. High-Fidelity Simulation

Modeling the proton, neutron, and heavy ion transport process to analyze the SEB in SiC power devices can be achieved using high-fidelity Monte Carlo simulation technology, deterministic transport codes, and related software. Inputting energy distributions obtained from radiation transport simulations, TCAD programs can perform coupled transient thermoelectric simulations in semiconductor power devices under high-energy particle strikes. These simulations can provide insight into the failure mechanisms responsible for device heating and catastrophic failure [111]. Using that insight, design configurations can be im-

plemented to help mitigate these effects and improve SEB tolerance. However, there is still a necessary process that needs to be completed to assure high-fidelity within a simulation. The use of 2D TCAD simulations has raised skepticism among researchers because the deposition of heavy ion strikes is inherently three dimensional in nature [27,32,94]. In a 2D simulation, a particle strike is read as a plane, rather than as a point charge in 3D. Thus, the transport processes in 2D simulations have difficulty accurately estimating the effects of corrupting plasma and device electric field. It is strongly suggested that 2D results be taken qualitatively instead of quantitatively [90,94–96,101]. To verify a simulation, the parameters and set-up need to align with an experimental study undertaken previously. The devices design and breakdown voltage need to be identical and verified separately in a static simulation. In the dynamic simulation, the radiation type, energy, LET, and SEB threshold need to match those in the experimental study. While impact ionization effects are understood in Si, the anisotropic material properties of 4H-SiC cause different characteristics. It has been strongly suggested the anisotropic effects be accounted for when modeling impact ionization for wide-band gap materials [112]. It should also be noted that parameters, such as but not limited to impact ionization coefficients, only have data available up to relatively low temperatures [113]. Although there are default values and models available to replicate the device physics under dynamic conditions, it is only an extrapolation of the known data. This should be considered with all simulations when assessing the suitability and merit of design results from simulations. Once this step has been taken, fidelity can be attributed to the simulation, and design tactics can be implemented to help improve SEB tolerance.

The ranges of devices and materials in use or envisioned for use, coupled with the complexity of radiation damage effects on the properties and performance, severely limit what can be learned from just experiments. Existing tools for modeling and simulation must be adapted to study radiation damage with an atomistic perspective. Due to recent technological advances in the past five years, it is not hard to believe more advances can be accomplished. Ideal test structures can now be produced from the progress that has been made in synthesis and fabrication that allow precise control of chemistry and structure. Individual point defects caused by radiation events can now be imaged using new scanning and transmission electron microscopy techniques. New atomic-scale modeling can make use of these new experimentally developed methods to give a comprehensive carrier capture and inelastic-scattering cross-section theory. It is now feasible to develop device-scale Monte Carlo codes that incorporate full band structures. The various new inputs can be used in multiscale engineering-level models for device degradation. Development of this technology will ultimately lead to the highest precision SEE simulations that will inevitably clarify discrepancies in device failure mechanisms and lead to designs of reliable and radiation-tolerant power devices.

Single Event Burnout Criteria

In a dynamic simulation, a failure criterion needs to be identified to signal the point at which SEB occurs. The use of SiC sublimation temperature [10,22,27–29,90], critical electric field (required for avalanche breakdown) [20], and leakage current [23–26] have all been previously used. The parameter critical electric field is a derived value based on the devices design in static conditions. Derived from [50], Equation (4) shows the analytical critical electric field as a function of the depletion width at breakdown (W_{BV}):

$$E_c = 6.13 \times 10^{16} W_{BV}^{-1/6}. \quad (4)$$

During a dynamic event, the high carrier density and high current that flood the device can cause a narrowing effect in the depletion width [50,114]. The narrowing of the depletion width, as the relationship in Equation (4) states, directly causes increases in the critical electric field. For cases that undergo a heavy ion strike and do not experience SEB, the electric field can transiently reach extreme levels that far surpass the static critical electric field. That being said, surpassing the critical electric field and exhibiting SEB are

not mutually exclusive, making this parameter unreliable for determining if a device has burned out.

Monitoring the drain current for runaway is another common method of determining an SEB event. When the drain current increases to a high enough magnitude while the device in its blocking state, energy begins to dissipate, eventually leading to the thermal destruction of the device. The equations in the TCAD simulator that output these values are dependent upon the temperature, power dissipation, and thermal properties of the device. This is an accurate method of SEB measurement and can give an idea of the SEB timescale, but it is highly dependent on more potent characteristics and cannot detail the exact moment SEB occurs.

As shown experimentally in [1,10,22], SEB is inherently a thermally terminated event. In the post-teardown study of devices, SiC MOSFETs have shown cracks as a result of expansion stress due to the sublimation of SiC. Stereomicroscopy and slice-and-view techniques have revealed that the destructed crystal structure of SiC forms in the drift region as a result of the rapid temperature increase within the device. Simulations can use the SiC sublimation temperature as the SEB failure criteria, which details the exact moment and timescale when SEB occurs. This is amongst the most accurate methods of SEB determination. Monitoring all three of these characteristics in conjunction is suggested for proper SEB analysis.

5. Conclusions

This review summarizes the current state of knowledge regarding the failure mechanisms of silicon carbide power devices from high-energy particle exposure and hardened designs proposed to improve radiation tolerance. Published work has demonstrated power MOSFET vulnerability to SEEs and catastrophic failures from SEB and SEGR. The physics of SEB in SiC devices have shown different characteristics than in Si devices, which has led to debate regarding the source of the regenerative current that leads to device burnout. Although it was originally thought that BJT turn-on was the primary mechanism for SEB in SiC MOSFETs, recent high-fidelity simulation studies strongly support alternative mechanisms. Failure mechanisms proposed in the literature are distinguished by how they label three burnout phases: (1) internal carrier generation; (2) the regenerative feedback mechanism; and (3) the runaway failure signature. Recent experimental and simulation studies agree that the SEB mechanisms in SiC DMOSFETs are caused by peak shifts in the electric field triggering a carrier multiplication process. The resulting high carrier density generates heat and thermal carriers until the device reaches its sublimation temperature. Although there is no current way to experimentally verify the exact mechanism, advances in simulation capabilities in the future will be able to provide more fidelity to this understanding.

Many designs have been employed to improve the SEB and SEGR thresholds of MOSFETs, but few have demonstrated suitable on-state performance for device operation under static conditions. Promising designs include, first, a VDMOSFET with a thin buffer layer that adds <5% to the $R_{on,sp}$. Fabrication of this design is manageable and should be the next step in validating device performance. Additionally, SiC SJ and hardened SJ MOSFETs have shown very promising results, providing high SEB thresholds with no sacrifice in $R_{on,sp}$. More work should be undertaken to test susceptibility to SEGR. Additionally, fabrication of SJ designs may be complex and may not be cost effective. Conclusive support for rad-hard designs can be drawn once experimental static and SEB tests have been conducted. Additionally, more work must be undertaken to understand the tolerance to degradation onset that occurs before catastrophic events. The degradation affects both hardened and non-hardened device performance. Additional refinement of the models for simulation and experimental methods will advance SiC MOSFET hardened design analysis and development. This review stands as an objective evaluation of this technology to assist in the provision of selection criteria for radiation-bound power systems.

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