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A DC-DC Converter with Switched-Capacitor Delay Deadtime Controller and Enhanced Unbalanced-Input Pair Zero-Current Detector to Boost Power Efficiency

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Abstract: This proposed work introduces a DC-DC converter with Switched-Capacitor Delay Deadtime Controller (SCD-DTC), Digitally Controlled Start-Up Block (DC-SUB), and Enhanced Unbalanced-Input Pair Zero-Current Detector (EUIP-ZCD) that helps to improve the overall power efficiency. It also introduces the discussion of key signal waveforms and the two major optimization flowcharts. This proposed DC-DC converter can simultaneously achieve optimized deadtime (body diode conduction < 3 ns) and almost fully eliminate the phenomenon of reverse inductor current (RIC). Furthermore, it also shows that it can achieve a well-regulated output voltage of 1.8 V with <0.01% of output ripple riding on it. All the post-layout simulation results are carried out using 0.18 µm 1P6M CMOS process using Cadence Virtuoso Spectre Circuit Simulator. The silicon chip area of our proposed work (including the output pad frame) is 1.44 mm^2. The chip fabrication was sent out in January 2024 and the return of the measurement dies is expected in March 2024. The post-layout simulation results will no doubt closely resemble the measurement results since the proposed work is mostly controlled by digital blocks.

Keywords: deadtime control; enhanced level shifter; comparator; current detector; power efficiency

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1. Introduction

The objective of deadtime control is to mitigate cross-conduction/shoot through current and to reduce the time interval when the body diode of the transistor conducts. The examination of previous and ongoing investigations pertaining to deadtime control can be categorized into three overarching groups: fixed, adaptive, and predictive, as outlined by [1]. First, DC-DC controllers employed long fixed deadtime, to cater to the worst-case scenarios with regard to PVT variations and also to avoid cross-conduction. Therefore, for most of its operation, this leads to a sub-optimal design whereby body-diode conduction is observed for a long duration and will hence degrade the overall system efficiency. Hence, the design of deadtime controller begins to favor an adaptive approach [2–4], whereby it operates with an optimum deadtime and can be adjusted when there are variations in the load current condition. They are also known as current mode deadtime controllers as load current sensing is critical to its operation. This step-by-step calibration tuning according to load condition [5] to achieve an optimized deadtime can be carried out by calculating the required minimum duty-cycle command. However, the drawback comes at the expense that an integrated load current-sensing block is needed and the deadtime controller is unable to accurately optimize the deadtime when there are variations in process, voltage supply, and temperature (PVT). On the other hand, there are some deadtime controllers that detect the node voltage of VX using very high-speed comparators [6–8] to optimize the deadtime (TD1). However, this is not power-efficient as it will consume a large quiescent

power during steady-state conditions and the systematic offset voltage in the comparator may lead to inaccurate sensing of VX. At the same time, in [7], the source terminal of a dedicated transistor (MD) is used to detect the switching-node voltage, VX, whereby the drawback is that the accuracy will certainly be prone to PVT variation. Overall, this detection technique will bring about an inherent delay as one action has to be completed before the next corrective action kicks in.

Thus, there is an inclusion of a discrete-time fully differential switched-capacitor comparator [9] which utilizes the concept of auto-zeroing to mitigate DC off-set errors and improves input sensitivity. The tradeoff comes at the expense of having a very high clock frequency which is power consuming. To avoid a power-inefficient high-speed comparator, there is another novel approach [10] that which can minimize body-diode conduction by sensing the voltage across an on-chip capacitor using only a very slow comparator. At the same time, its current consumption is low and independent of switching frequency. Thus, it is suited for high-frequency DC-DC converters. However, the offset error presented by the slow comparator may cause inaccuracies in the voltage across the capacitor, leading to an increase in body-diode conduction losses. Therefore, for improved optimization of deadtime, there are several sensor-less techniques/algorithms proposed [11–13] which use theoretical calculation methods to accurately model the optimized deadtime required and then tune the circuit accordingly to achieve high efficiency. They accomplished it either by minimizing the input current [12,14,15] or the duty-cycle ratio [11] of the converter's control loop. For a multi-phase converter [3], it is also feasible by detecting the duty-cycle difference of each phase. However, the tradeoff is the fact that the algorithm-optimization process is far too time consuming, thereby not feasible for converter applications with fast-changing load-transient conditions. Nevertheless, there are some other interesting deadtime-control techniques which use a power-efficient diode control rectifier [16,17] to detect the drain to source voltage of the power transistor. This helps to provide vital information on how to optimize the deadtime to achieve the best-possible efficiency. However, the inherent delay attributed by the analog comparators and driving buffers can lead to an inaccurate optimization of deadtime. Therefore, in [18], whereby this work focuses on the deadtime management for Quasi Square Wave (QSM) operation and tries to mitigate the inherent delay problem by introducing a fixed offset voltage in the DC-level detection threshold of the comparator. However, an accurate offset voltage is highly vulnerable to changes in environmental operating conditions and die-to-die variation. Though the objective of deadtime controllers is to optimize the deadtime to minimize body-diode conduction, it must also be able to totally prevent the occurrence of shoot-through current. Otherwise, it will permanently damage the converter.

Some proposed methods [1,19,20], use the cross-coupled topology on the gate voltage of the two power transistors to eliminate any possibility of a shoot-through current. But they are definitely not the solution to yield an optimal deadtime. The next proposed era of deadtime controllers is based primarily on a predictive approach [1,21–25] whereby it uses vital information from the previous switching cycle and adjusts the deadtime accordingly for future switching cycles. Instead of using analog comparators, this technique uses a digital NOR gate [26] and a ONE step approach [27] to optimize the deadtime by performing careful calibration and quantizing the error in time domain. After which, this information is being subtracted from the current delay time. The limitation is the fact that the digital NOR gate cannot prevent cross-conduction or shoot-through current, which can potentially damage the converter's functionality. There exist alternative and captivating predictive methods [28,29] that utilize a counter regulated by a delay generator to execute linear modifications in the step delay. Nevertheless, this gives rise to a sluggish response and produces unsatisfactory precision. Analog delay-lock-loop (A-DLL) [30] is implemented to curtail the system's optimization time, albeit at the expense of power-inefficient comparators. Lastly, in [22], the prediction approach involves estimating the discharging slope of VX to establish a linear correlation. However, this may not always be

true for a wide range of load currents. In this next sub-section, the past research works on ZCD controllers will be reviewed thoroughly.

1.1. ZCD Controller

The primary goal of ZCD control is to detect the zero-crossing point of VX and prevent RIC. In [7,8,19], a ZCD system is implemented to effectively deactivate the power NMOS and avoid RIC. However, this approach utilizes high-speed comparators that are not energy efficient and may introduce significant system loop delay before corrective action can be taken. To address this, Ref. [9] proposes the use of a switched-capacitor comparator structure to detect RIC and deactivate the power NMOS transistor. Unfortunately, this solution results in higher current consumption. Alternatively, ref. [31] suggests the utilization of an on-chip integrated current-sensing block to perform the ZCD function. Another approach, as described in [16,32,33], involves employing a CMOS rectifier to detect the voltage across the synchronous power transistor, which offers higher accuracy. Specifically, Ref. [16] can reduce the overall system switching delay to several tens of nanoseconds, effectively preventing RIC. However, in the design of modern DC-DC converters, high-frequency operation is favored to reduce the size of the inductor. Therefore, a delay of several tens of nanoseconds can still result in significant power losses due to RIC. One possible solution, as proposed in [34], is to strategically incorporate a fixed DC offset voltage in the comparator system to mitigate the overall system response delay. However, this approach may prove ineffective as determining the exact values of DC offset voltages is challenging and they can vary greatly with temperature and noise. Furthermore, a specially designed comparator with an embedded unbalanced input pair employs a novel calibration technique to tune the offset delay of the system to achieve precise gate switching regardless of PVT variation. This helps to eliminate RIC and reduce the timing error down to approximately <1 ns. However, the improvement in power efficiency is minimal as power-consuming analog components are used and the sizes of power transistor are not well-optimized for low load conditions.

1.2. Voltage Level Shifter

In this sub-section, it will introduce the rationale behind the escalating demand for voltage level shifters and review the most recent research works being carried out in this field. With the escalating demand for higher integration and lower silicon cost, the feature size of CMOS technology has been reduced significantly. Hence, the scaling down of supply voltage domain [35–37] is crucial so as to achieve optimal circuit performance. On the other hand, most of the peripherals of the circuit system are still utilizing higher supply voltages (3.3 V/5.5 V). Therefore, the huge gap in supply voltage domain is the main driving factor for the demand of input/output buffers [38] to be embedded with very fast level-shifting capabilities. There are several modern applications whereby it must operate at a supply voltage that is much higher than the circuit's core. In the field of portable mobile devices, for the power-management unit (PMU), the buck converter is designed so that it is able to accommodate the high supply voltage of the Lithium-Ion battery, which ranges from 2.8 V–4.2 V. One of the circuit techniques introduced [39] is to cascode the power transistors so that they can withstand the high electric field coming from the input supply voltage. Furthermore, in the field of LED operating system, the LED driver [40,41] must yield a very high output voltage so as to provide power to the many series-connected LEDs. Since several supply voltage domains are always present in modern circuit's system or portable devices, voltage level shifters are therefore necessary to shift the signal waveform from one level to the next in the shortest-possible time frame, yielding the highest power efficiency. The conventional voltage level-shifter design [42,43] whereby some of the important design considerations include the contentious and shoot-through current during a high-to-low transition or vice versa. Basically, contentious current is the amount of quiescent current that must be overcome for the transition to take place, whereas shoot-through current occurs because of the formation of a low impedance path between

supply and ground. The detrimental drawbacks of a sub-optimal voltage level-shifter design are the impact on the overall system's power efficiency, the propagation delay in the state transition, and the amount of silicon area overhead. For the design, it exhibits huge dynamic power consumption and unnecessary propagation delay. Furthermore, the current can only be further reduced by minimizing the aspect ratio of MP1 and MP2. The tradeoff lies in the increase in the circuit's propagation delay. One possible solution [44–46], is to cascode the high-voltage-tolerant PMOS transistor (MPC and MPD) between the pull-up and pull-down transistor (MN1, MP1) and (MN2, MP2). However, the tradeoff is the inclusion of another biasing voltage, VB1, which will increase the silicon area overhead. For a power-efficiency level shifter, a small amount of contentious current is highly desirable to improve the overall system's performance.

In the recent literature, there are several publications [47–49] that focus their attention on mitigating the contentious current consumption. There are also other circuit techniques to reduce the quiescent power in the DC steady state. This can be done by using a Wilson Current Mirror approach [50]. However, the drawback is that the shoot-through current phenomenon is still dominant for the various voltage level transitions during the transient state. Furthermore, because of the negative feedback mechanism, it creates a very high impedance node at the output, VA which is vulnerable to noise disturbance. Another circuit methodology includes the addition of another current-saving transistor (MCS) [51,52], to block all possible DC-current paths present in the voltage level shifter. In addition, transistors MPX and MPY [53,54] can be employed so as to regulate and mitigate the current between the pull-up and pull-down transistor (MN1, MP1) and (MN2, MP2). However, this technique may not be effective in regulating the contentious current when the difference of the two-supply voltage domain (VDD_L and VDD_H) increases. This is because the current regulating capability of both MPX and MPY may have weakened and lost its effectiveness. The contentious current also imposes an upper limit for the higher supply voltage domain (VDD_H). Therefore, to effectively circumvent the limitation mentioned above, several research works [48,55] have included a basic current mirror (MC1 and MC2). This helps to offer an infinite voltage level (VDD_H) but results in a much weaker device, MC2, than the conventional approach. Therefore, this will increase the inherent transient delay for the low-to-high transition of VIN. There are also other interesting circuit techniques to circumvent the upper limit for the higher supply voltage domain (VDD_H). One way is to cascode several voltage level shifters together [42,56], to achieve the required VDD_H. This helps to reduce the voltage difference between VDD_L and VDD_H of a single voltage level shifter. However, the tradeoff comes at the expense of increased quiescent power and silicon area.

Some circuit techniques employed the bootstrapping circuit [57] to improve the driving capability of the NMOS pull-down transistors (MN1 and MN2). Furthermore, a bootstrap capacitor (CB1 and CB2) [58] and reduced swing inverter [59,60] are also included to reduce the contentious current. For the technique of bootstrapping, the drawback lies in the fact that large silicon area consuming capacitors are required and its dark/leakage current has a drastic impact on the circuit's operating bandwidth. Nevertheless, for the reduced swing inverter technique, the node voltage VRSI_OUT, is extremely susceptible to noise and parasitic capacitances. Some other voltage level shifters include the addition of series-connected diodes [61,62], which are self-regulating. However, the tradeoff is the constant sub-threshold quiescent power being consumed during the DC steady state. In the next sub-section, the proposed work will be presented and analyzed in greater detail. At the same time, there are other DC-DC converters which can provide a wide load range with good efficiency while consuming very low quiescent current, which will no doubt be the major power consumption in sensing or low-load mode [63–70].

2. Proposed Work

In this section, it will introduce the proposed work which can simultaneously optimize deadtime and RIC to achieve the maximum power efficiency in a DC-DC buck

converter meant for smartphone applications [24–32]. Therefore, it will also reduce all the different power losses as mentioned in Section 1. As compared to the past research works introduced in Section 1, this proposed work undertakes a streamlined approach whereby it can optimize deadtime and concurrently reduce the impact of RIC. Hence, in the following sub-sections, the individual proposed blocks will be introduced and explained in greater detail.

2.1. System Architecture

The proposed work, as shown in Figure 1, comprises of three major circuit blocks —Digital Controlled Start-Up Block (DC-SUB), Switched-Capacitor Delay Deadtime Controller (SCD-DTC) and the enhanced unbalanced-input zero-current detector (EUIP-ZCD). The DC-SUB helps to start up the circuit properly during the initial state of operation for the DC-DC buck converter. Its operation is explained in Section 2.2. After which, the SCD-DTC will operate to reduce and optimize deadtime (TD1) to an acceptable value. It is known that the optimized deadtime will change according to variations in PVT, load/line, temperature, and environmental operating conditions. Therefore, there is a fast calibration tuning methodology to adjust it to an optimum value. Its detailed operation will be explained later in Section 2.3. At the same time, the EUIP-ZCD operates simultaneously to activate NMOS power transistor to turn OFF accurately. Its operation is explained in Section 2.4. For both SC-DTC and EUIP-ZCD, there will be a flowchart shown later to better illustrate its operation.

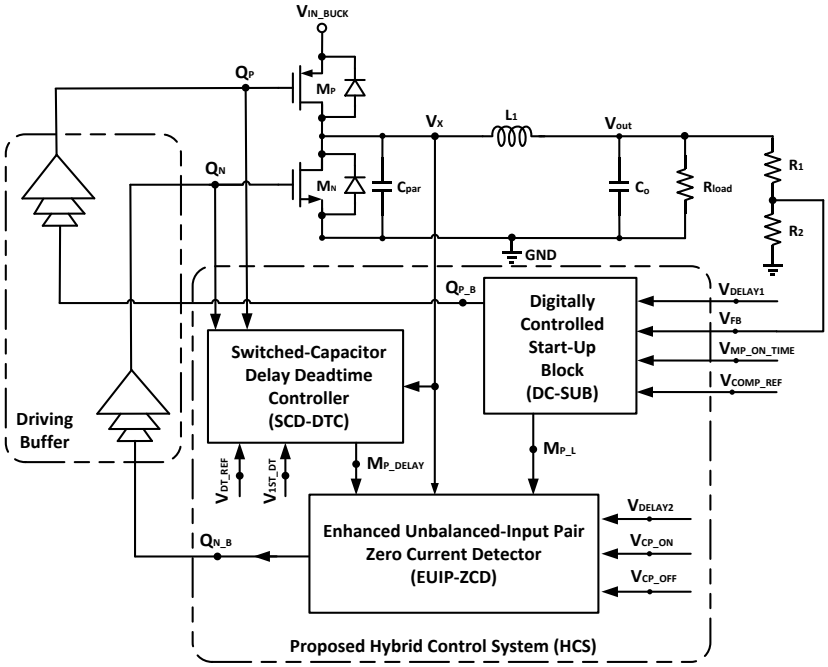


Figure 1. Proposed Work (Switched-Capacitor Delay Deadtime Controller and Enhanced Unbalanced-Input Pair Zero-Current Detector).

2.2. Digitally Controlled Start-Up Block

The proposed Digitally Controlled Start-Up Block (DC-SUB), as shown in Figure 2, is meant to provide an initial proper working operation for the DC-DC buck converter. In the DC-SUB, some of the major blocks include the comparator, current-starved voltage-controlled oscillator (CS-VCO), a delay line cell, and an external voltage pulse source.

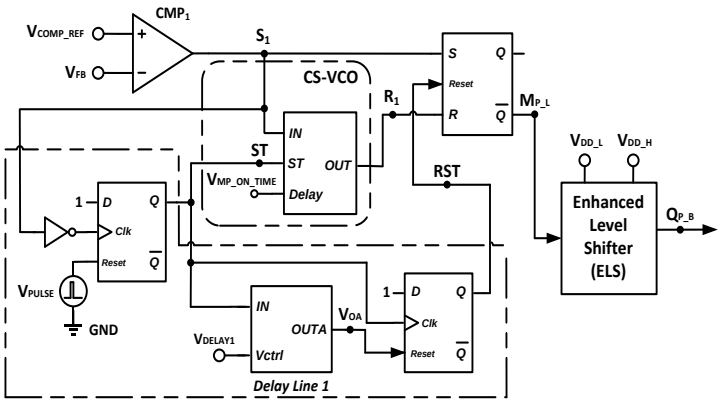


Figure 2. Proposed Digitally Controlled Start-Up Block (DC-SUB).

To gain a good insight and understanding on the purpose and operation of each circuit block mentioned above, a timing diagram is presented and shown in Figure 3. At the very initial state of operation, $T < T_1$, the parameters S_1, $R_1 = 0$ and $M_{P_L} = 1$ state that the power PMOS transistor is switched off before T_1. Furthermore, there is an applied short-duration external pulse to reset the signal node ST which forces it to be zero initially. At the instant T_1, $V_{FB} < V_{COMP_REF}$, the SR latch becomes activated and the value of S_1 rises to 1. This causes M_{P_L} to be 0 and the power PMOS transistor is turned ON. At this instant, the CS-VCO block is not activated as the ST signal holds on to a value of 0. At T_{start}, $V_{FB} > V_{COMP_REF}$, the comparator changes state and causes S1 to drop to 0 instantly. This sharp drop in voltage causes ST to rise quickly, RST becomes 1 and reset the SR latch. This helps to free up the power PMOS transistor and switches it OFF. The above-mentioned circuit operation is important otherwise this transistor will always be switched ON and the DC-DC buck converter will not operate well. After which, the delay line cell becomes activated, V_{OA} rises to 1 and resets the RST signal to place the SR latch in operation again. After T_{start}, all the power-hungry blocks in the DC-SUB will be powered down to save quiescent power consumption. At the instant T_2, $V_{FB} < V_{COMP_REF}$, S_1 rises to 1 instantly and after a controlled delay time by $V_{MP_ON_TIME}$, causes R_1 to rise at T_3 which is pre-defined. This duration is the turn-on period for the power PMOS transistor and will be fixed in this proposed work. In the next sub-section, the transistor level of the enhanced level shifter (ELS) and CS-VCO will be presented.

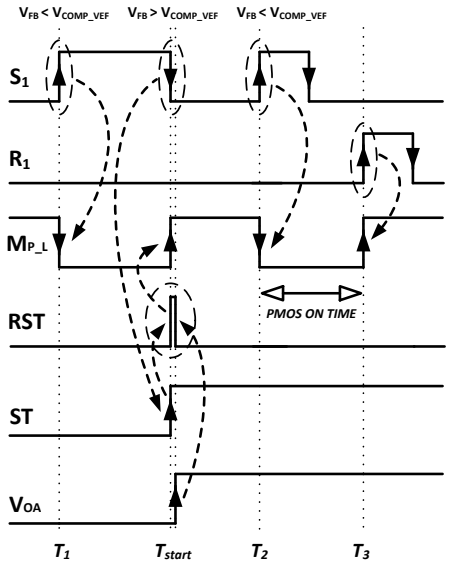


Figure 3. Timing diagram of DC-SUB.

As shown in Figure 1, there are dual voltages domains present in the proposed work. This is because, for this proposed portable application for smartphone applications, the DC-DC buck converter has to be compatible with the high input battery voltage supply originated from the lithium-ion battery, which spans from 2.8 V to 4.2 V. Hence, the DC-SUB has to be embedded with voltage level-shifting capability. Therefore, the ELS is proposed, shown in Figure 4, which can reduce the contentious quiescent current and also the shoot-through current. However, a balance between speed and power consumption has to be carefully considered.

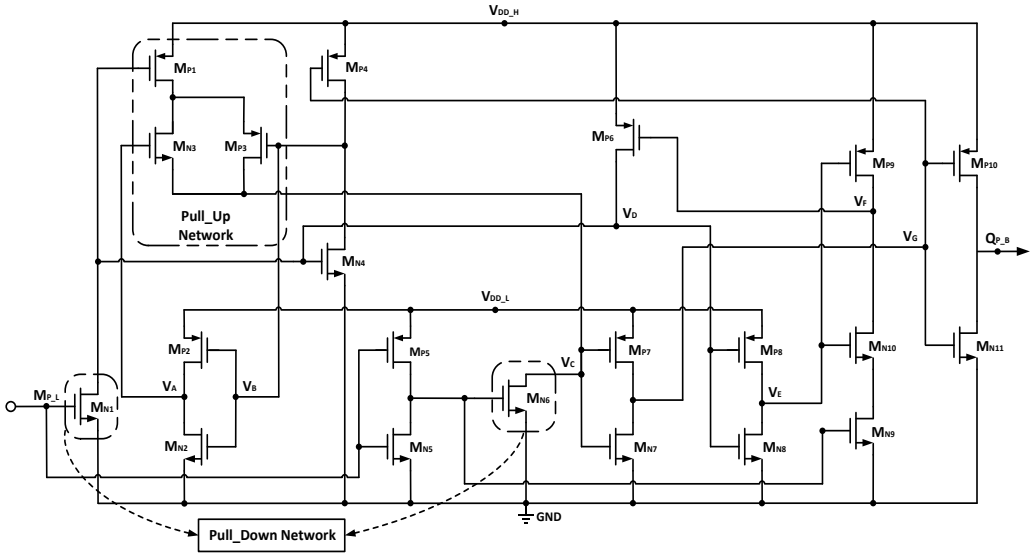


Figure 4. Enhanced Level Shifter (ELS).

Referring to Figure 4, the node voltages M_{P_L}, V_B, V_C, V_E and Q_{P_B} have a value of 0 while V_A, V_D, V_F and V_G have a value of 1. When the input signal, M_{P_L} changes from low to high, the transistor M_{N6} switches off. At the same time, it turns on M_{P1}, since the CMOS switch M_{N3} and M_{P3} is active, it will pull the node V_C to a high voltage. This is also possible given the fact that V_F is high, which causes M_{P6} to be in the off state. Thus, V_G will be pulled to low and the output signal, Q_{P_B} will be pulled up to V_{DD_H} immediately. Hence, to further reduce quiescent current consumption, after V_G becomes low, it will activate M_{P4} to pull up node voltages V_B and pull V_A to ground immediately. This action will turn off the CMOS switch M_{N3} and M_{P3}. Do take note that transistor M_{N9} is always in the off state during the low-to-high transition of input signal M_{P_L}. Therefore, the above detailed explanation will also be similar to the high-to-low transition for input signal, M_{P_L}.

With reference to the above operation, it is evident that the crucial transistors responsible for the pull-down and pull-up network are (M_{N1}, M_{N6}) and (M_{P1}, M_{P3}, M_{N3}), respectively. To improve the speed of transient response, this group of transistors should be sized with a relatively larger aspect ratio so that it will yield a lower on-resistance. However, the tradeoffs lie in the silicon area overhead. The optimum W/L aspect ratio of all the transistors in the ELS is shown in Table 1. The proposed AND gate-controlled CS-VCO is shown in Figure 5. The out signal, OUT will only be high if both the IN and ST signal are simultaneously high. This structure satisfied low quiescent power as the current drawn is limited by the input signal, Delay. With reference to Figure 2, the OUT signal will determine the on-time duration of the power PMOS transistor.

Table 1. Transistor Sizing for ELS.

NMOS	$(W/L)_N$	PMOS	$(W/L)_P$
M_{N1}	60/1.5	M_{P1}	32/1.5
M_{N2}	0.5/0.22	M_{P2}	1/0.22
M_{N3}	7/1.5	M_{P3}	22/1.5
M_{N4}	4/1.5	M_{P4}	6/1.5
M_{N5}	0.5/0.22	M_{P5}	1/0.22
M_{N6}	22/1.5	M_{P6}	27/1.5
M_{N7}	0.5/0.22	M_{P7}	1/0.22
M_{N8}	0.5/0.22	M_{P8}	1/0.22
M_{N9}	8/1.5	M_{P9}	5/1.5
M_{N10}	0.5/0.22	M_{P10}	1/0.22

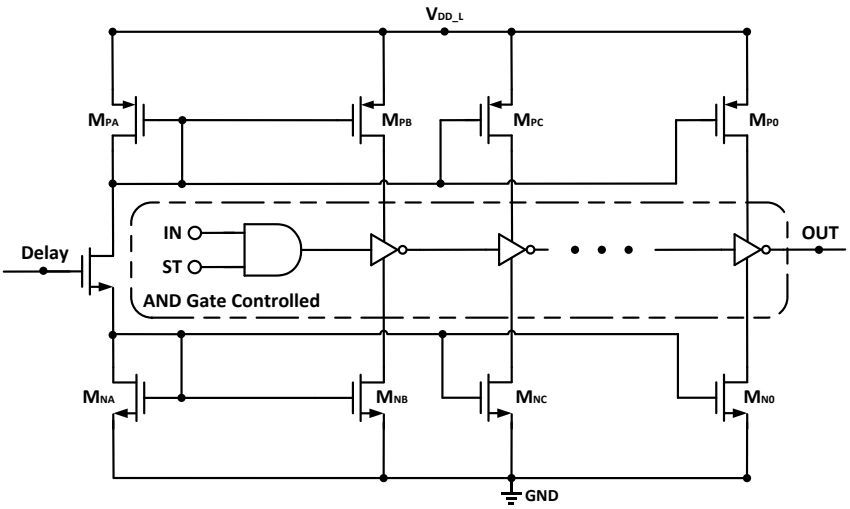


Figure 5. Proposed AND Gate Controlled CS-VCO.

2.3. Switched-Capacitor Delay Deadtime Controller

The proposed deadtime controller (SCD-DTC) and its corresponding sub-blocks are shown in Figures 6 and 7, respectively. To fully understand the design implementation, the transistor level of the switched-capacitor delay block and the UP/DOWN counter are presented in Figures 8 and 9, respectively. For a good understanding of the SCD-DTC circuit, as shown in Figure 6, a well-illustrated timing diagram and the deadtime optimization flowchart are presented in Figure 10 and Figure 12, respectively.

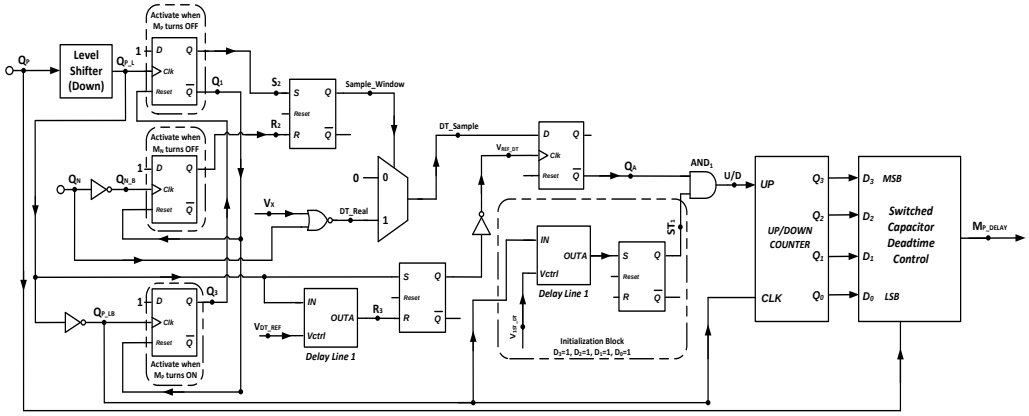


Figure 6. Proposed Delay Deadtime Controller (SCD-DTC).

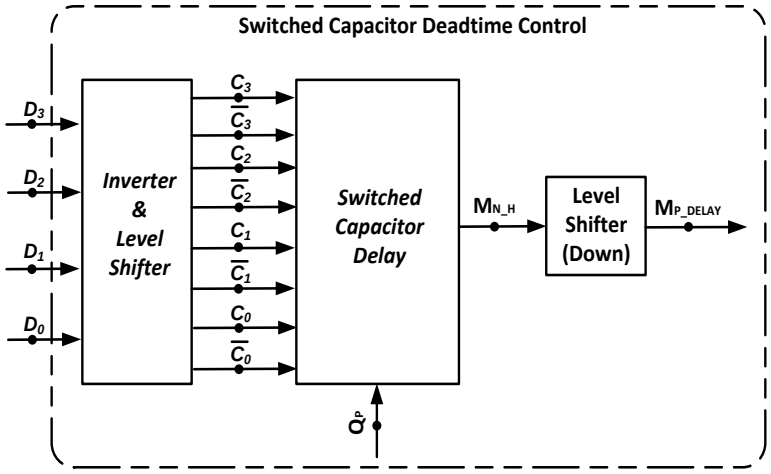


Figure 7. Switched-Capacitor Deadtime Control.

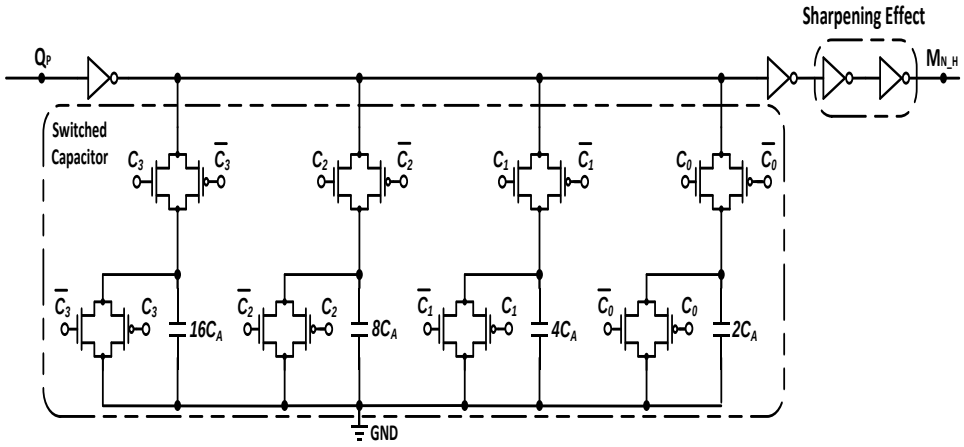


Figure 8. Switched-Capacitor Delay.

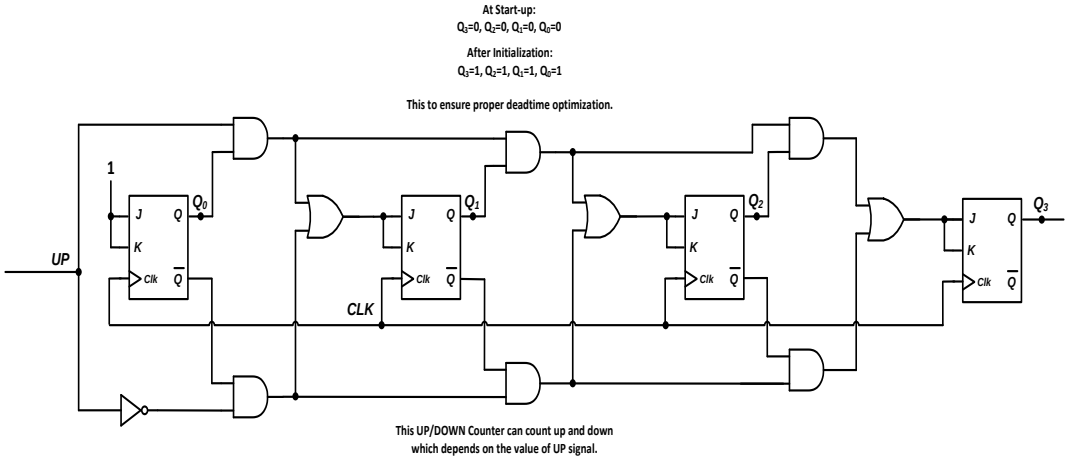


Figure 9. UP/DOWN Counter.

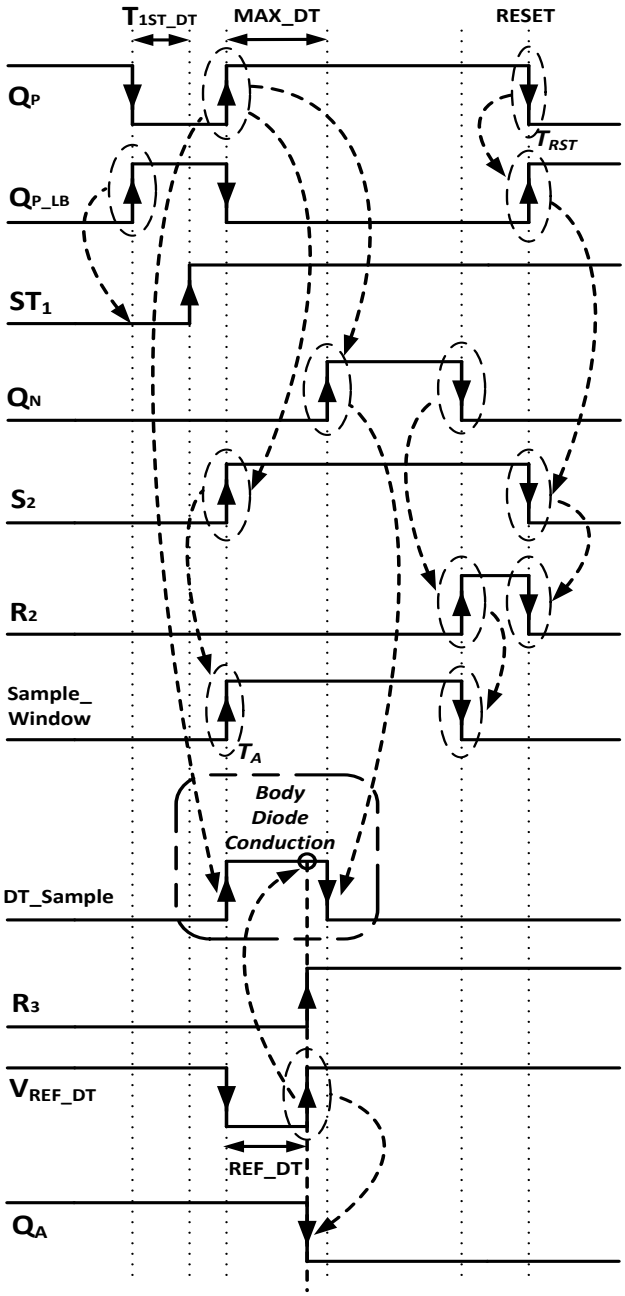


Figure 10. Timing Diagram of SCD-DTC.

To gain a comprehensive understanding of the functioning of the circuit, the timing diagram depicted in Figure 10 will serve to elucidate the proposed SCD-DTC, as shown in Figure 6. During the initial start-up phase, in the absence of the AND1 gate and the initialization block, the U/D signal will remain at a value of '1' because the complement output of the D latch is '1'. This, in turn, causes the counter to increment and results in the four outputs (Q_3, Q_2, Q_1, Q_0) of the switched-capacitor deadtime control to be 0, 0, 0, and 1, respectively. This gives rise to an error as it is expected that all the outputs (Q_3, Q_2, Q_1, Q_0) should be high initially, with a value of '1'. This is because the switched-capacitor deadtime delay is intended to count down from a maximum value to an optimized value. The specifics of the switched-capacitor deadtime control will be expounded upon subsequently. To address the constraint, the inclusion of the initialization block and the AND1 gate is necessary. As depicted in Figure 10, when the power PMOS transistor (QP = 0) is turned on, the input clock (QP_LB) for the UP/DOWN counter experiences an increase. This rise

is caused by the delay line unit, V1ST_DT, which in turn leads to the rise of ST1 after a specific time interval, T1ST_DT. Consequently, this allows the counter to register a value of '0' and proceed with the countdown process, resulting in Q_3, Q_2, Q1, and Q_0 attaining a value of '1'. This represents the accurate functioning of the switched-capacitor deadtime control. Subsequently, the signal (QN) will rise to a value of '1' following a maximum initial deadtime delay interval (MAX_DT), as depicted in Figure 10. This rise is attributed to the switched-capacitor deadtime control cell. It will be explained in Section 2.4 that this is the signal to turn on the power NMOS transistor in the power stage, as shown in Figure 1. Furthermore, the value and rationale for the maximum deadtime delay will be presented and discussed later.

At the same time, as illustrated in Figure 10, when QP increases to '1', it will initiate the activation of the D flip-flop and subsequently result in S2 rising to '1' rapidly. This action will trigger the commencement of the Sample_Window period at time TA, during which the 2-to-1 MUX will be operational and transmit the signal value DT_Real to DT_Sample. DT_Sample represents an exact replica of the DT_Real signal during the active Sample_Window period. Upon the deactivation of the PMOS transistor (QP = 1), the voltage of node VX decreases below the ground voltage, thereby causing DT_Sample to ascend to '1', signifying the initiation of body-diode conduction. Subsequently, when the NMOS transistor is activated, this indicates the termination of body-diode conduction, leading to the decline of the DT_Sample signal to '0'. In summary, the DT_Sample signal window provides a reliable estimation of the time interval during which the power NMOS transistor's body diode conducts, with minimal delay attributed to the digital cells. As the duration of body-diode conduction can be measured, the subsequent challenge involves gradually reducing it to achieve an optimized period within the shortest possible timeframe. Consequently, in the proposed SCD_DTC, the actual deadtime period, DT_Sample, will be repeatedly compared against a reference deadtime, VREF_DT, in order to generate an appropriate value for the UP/DOWN counter. To generate the reference deadtime (REF_DT), a delay line unit is employed to adjust the rising edge of the R3 signal, which corresponds to the rising edge of VREF_DT. At the rising edge of VREF_DT, the value of the DT_Sample signal is detected. If the detected value is '1', it indicates that the current deadtime (body-diode conduction) is excessive.

Hence, the resultant output of the D flip-flop (QA) will yield a value of '0', thereby causing the counter to count down. Consequently, this will activate the switched-capacitor deadtime control, resulting in a reduction of the deadtime for the subsequent cycle. Conversely, if the detected value is '0', it signifies that the current deadtime is insufficient, which may lead to cross-conduction (shoot-through). In such a scenario, the value of QA will be '1', causing the counter to count. This, in turn, activates the switched-capacitor deadtime control and increases the deadtime for the next cycle. The optimization of deadtime, along with the detailed circuit operation of the switched-capacitor deadtime control, will be elucidated later, with the assistance of Figure 12. It is important to note that the circuit operation solely encompasses the first half of the cycle, during which MP turns off and subsequently MN turns on. However, to ensure a robust working operation for the entire cycle, the second half of the cycle is equally critical and necessitates proper design. Referring to Figure 10, when QN falls to '0', indicating the turning off of the power NMOS transistor, the signal R2 promptly rises to '1'. This action leads to the closure of the Sample_Window, thereby terminating the estimation of the body-diode conduction period. At time TRST, the signal QP transitions to '0', while QP_LB rises to '1'. This results in the resetting of S2 and the subsequent rise of Q1 to '1'. Consequently, R2 and Q3 are also reset. The sequence in which the individual blocks are reset holds great significance and must be effectively managed. Therefore, all the pertinent circuit blocks are reset prior to the commencement of the next cycle, during which QP rises to '1' once again. In the subsequent sub-section, the proposed switched-capacitor deadtime control will be presented, with the assistance of the deadtime-optimization flowchart depicted in Figure 12. Note that there will be a minor voltage glitch due to parasites, however it will not propagate to the MP_DELAY

as the Initialization block shown in Figure 6 will completely remove it. Hence, it has no impact on the operation of the DC-DC converter. We have started preliminary testing for the returned fabricated chips and initial measured results are aligned with simulation and theoretical results.

The proposed deadtime control, as shown in Figure 7, comprises the switched-capacitor delay block. Its schematic level representation is shown in Figure 8. A simplified circuit representation of Figure 8 is shown in Figure 11.

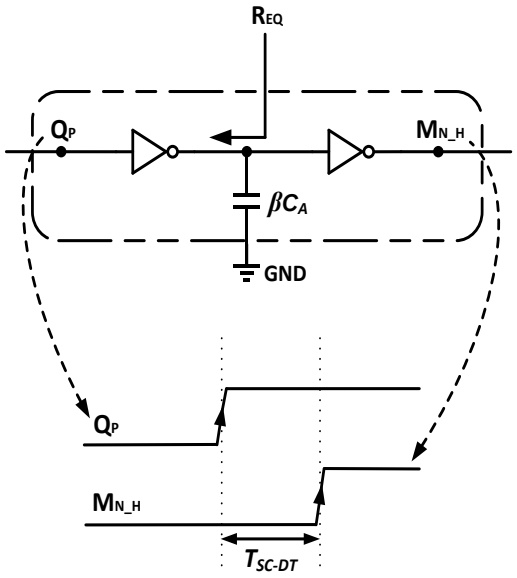


Figure 11. A simplified Delay Circuit based on switched-capacitor concept.

Supposed that delay time, $T_{SC\text{-}DT}$, is the time/interval for M_{N_H} to reach α% of Q_P. ΔT_β corresponds to the delta in $T_{SC\text{-}DT}$ for the respective delta change in β.

$$T_{SC-DT} = -R_{EQ} \cdot \beta C_A \cdot ln(1- \propto) \quad (1)$$

$$\Delta T_\beta = -R_{EQ} \cdot \Delta\beta C_A \cdot ln(1- \propto) \quad (2)$$

where β is a constant ($0 < \beta \leq 30$) and R_{EQ} is the equivalent resistance.

The deadtime-optimization flowchart together with the full illustration of its operation is presented in Figure 12. Note that it may be necessary to refer to Figures 6 and 10 for a more holistic understanding of the SCD-DTC. At the very initial start-up phase, the four inputs (D [3:0]) to the deadtime control circuit are all held to '0'. However, with the introduction of the initialization block as mentioned in Section 2.3, the D [3:0] will have a value of 'high'. This corresponds to the initial highest deadtime, MAX_DT, as mentioned in Section 2.3. Furthermore, this circuit operation is performed by the delay circuit shown in Figure 8 or Figure 11 whereby $\beta >= 30$. The value of MAX_DT must be calibrated carefully so as not to degrade power efficiency during the initial start-up phase. Therefore, the primary goal of the Switched-Capacitor Drive Deadtime Control Technique (SCD-DCT) is to achieve an optimized deadtime duration in the subsequent cycles, as depicted in Figure 12. This objective can only be accomplished by comparing the current deadtime with the reference deadtime (REF_DT), as mentioned in Section 2.3. Through extensive modeling efforts, the value of REF_DT is determined, which allows for the minimization of body-diode conduction duration while preventing shoot-through current. Note that when the dead time reaches the desired value, the UP/DOWN counter will cease to operate to save power. This is because we have included a disable pin inside the schematic of the UP/DOWN counter such that the outputs (Q3, Q2, Q1 and Q0) in Figure 6 will remain unchanged. The optimized deadtime will vary with different operating load conditions and different external circumstances. However, the optimized deadtime will avoid/prevent

any form of shoot-through current that will occur in the power transistors, hence ensuring that the power efficiency will not be degraded. Additionally, the impact of extreme Process, Voltage, and Temperature (PVT) variations, diverse environmental conditions, and lot-to-lot variation is taken into consideration. It is important to note that the work is conducted with the awareness that the ultimate application pertains to powering advanced 3G/4G Smartphones. However, it is worth noting that the value of REF_DT may vary if there are changes to the operating conditions or specific application of the DC-DC buck converter.

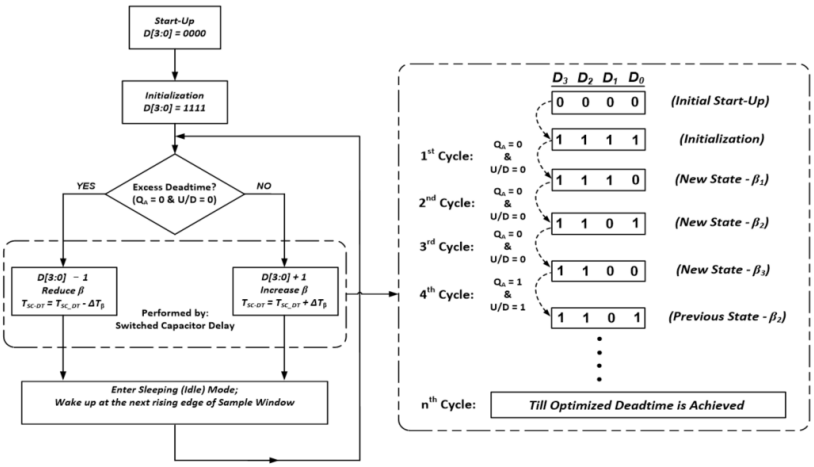


Figure 12. Deadtime-Optimization Flowchart.

As illustrated in Figure 12, the value of β decreases with each cycle if the sampled deadtime (DT_Sample) is determined to be greater than the reference deadtime (REF_DT). This reduction is made possible by modifying the arrangement of capacitors in the switched-capacitor delay circuit, as depicted in Figure 8. Consequently, the deadtime is decreased by a quantity denoted as Tβ. Subsequently, the system enters a state of dormancy until it is reactivated at the next rising edge of the Sample_Window. This optimization process continues until an optimized deadtime (equilibrium) is attained, which closely resembles the reference deadtime (REF_DT). When it is at equilibrium, there will be a constant toggle between two states. However, the power losses are minimal since the proposed SCD-DTC comprises of mainly power-efficient digital blocks which do not draw static quiescent current and switching losses are almost negligible. In the next sub-section, the enhanced unbalanced-input pair zero-current detector (EUIP-ZCD) will be proposed. When the SCD-DTC is operating to find the optimized deadtime, the EUIP-ZCD also works simultaneously to find the exact zero-current-crossing point of node voltage V_X which indicate the accurate turning off for the power NMOS transistor (M_N). This helps to prevent the occurrence of reverse inductor current flow which will degrade the power efficiency of the DC-DC buck converter.

2.4. Unbalanced-Input Pair Zero Current Detector

The enhanced unbalanced-input pair zero-current detector (EUIP-ZCD) is shown in Figure 13. It consists of two crucial blocks—Zero Crossing V_X Sensor and the Unbalanced Input-Pair (UIP) comparator. The detailed operation of each block will be presented respectively. The primary aim of the EUIP ZCD, as illustrated in Figure 13, is to identify the zero-crossing point of V_X and determine the moment at which power NMOS transistor, MN, should be turned off. When M_N is deactivated, the signal M_{N_L} transitions from '1' to '0', resulting in the rise of $M_{NB_D_L}$ from '0' to '1'. Following a brief response time (T_R) for V_X to react, the V_X sensor block becomes operational. This block generates an output signal, V_{CTRL_R}, which serves to modify the imbalanced input conditions of the UIP comparator. Consequently, the value of V_{CTRL_R} varies based on the detected V_X signal. Subsequently, the UIP comparator modifies the transition of the output signal, ZCD_INT, from '0' to '1'. Consequently, the signal RST_MN experiences a delay in transitioning from

'0' to '1'. Consequently, the signal Q_{N_B}, which is sent to the driving buffer of M_N, is reset to '0' at a different moment depending on the waveform of VX. It should be noted that the signal M_{P_DELAY}, which is directed to the 'S' input of the sole rising-edge triggered SR latch, originates from the SCD-DTC, as depicted in Figure 6. Referring to Figure 13, the circuit solely employs a rising-edge triggered SR latch. The rationale is that the signal M_{N_L} will only respond to the rising edge of M_{P_DELAY} and RST_MN. Therefore, it is obvious that the SCD-DTC (Figure 6) and EUIP-ZCD (Figure 13) are important signals for the switching of power transistor, M_N.

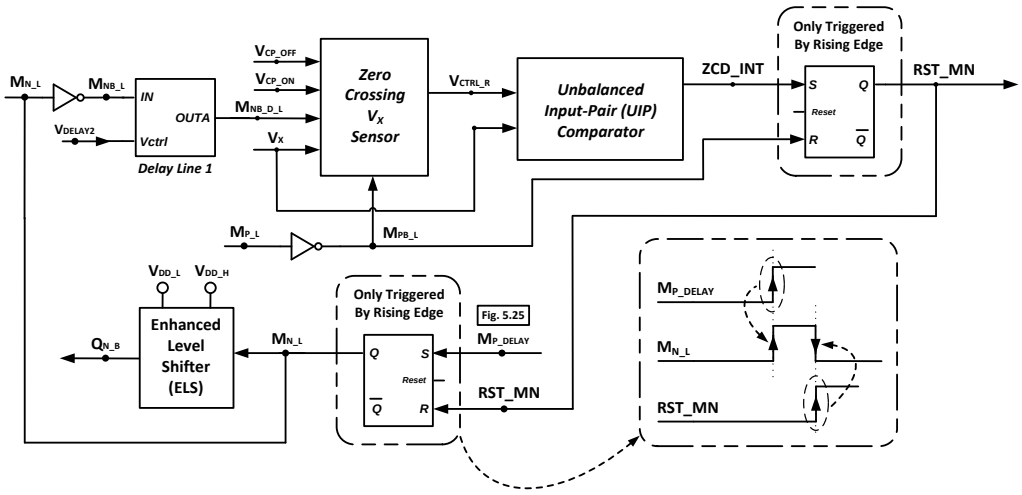


Figure 13. Proposed Enhanced Unbalanced-Input Pair Zero-Current Detector (EUIP-ZCD).

To fully understand the optimization for the turning OFF of power transistor M_N, a flowchart of the proposed EUIP-ZCD is presented in Figure 14. Do take note that the EUIP-ZCD only gets activated on the edge of $M_{NB_D_L}$. Hence, it is observed that the optimization algorithm will ensure that equilibrium is achieved whereby M_N turns off exactly at the instant when inductor current falls to zero. This will prevent the occurrence of reverse inductor current and improve the power efficiency of the system. In the next sub-section, the V_X sensor will be discussed in greater details.

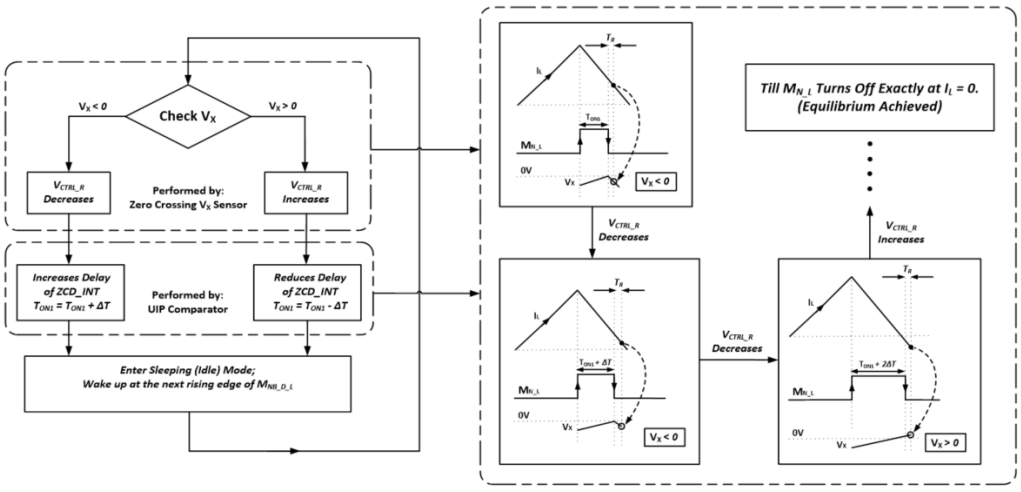


Figure 14. EUIP-ZCD Optimization Flowchart.

The proposed zero-crossing V_X sensor is shown in Figure 15. This block will work after M_N turns off or when $M_{NB_D_L}$ goes high. When M_N turns off, after time interval T_R controlled by V_{DELAY2}, the clock signal to the D latch ($M_{NB_D_L}$) rises from '0' to '1'. However, at the very instant when M_N turns off, V_X will yield a polarity sign (either > 0 or

<0) as shown in Figure 14. Hence, the input to the D latch is ready even before $M_{NB_D_L}$ rises from '0' to '1'. At this stage, there is an important design parameter. The sensor transistor M_{NX} has to detect the V_X polarity accurately so that it can pull V_{RX} to low or to V_{DD_L}. Furthermore, it must withstand extreme PVT variation, e.g., slow-slow corner at temp of −55 °C where threshold voltage, V_{TH}, will be large. Hence, M_{NX} will remain off with minimal change in V_X after time interval, T_R. Therefore, there is a tuning pin included in this block during the chip fabrication so as to circumvent all possible variation during the post-fabrication measurement stage.

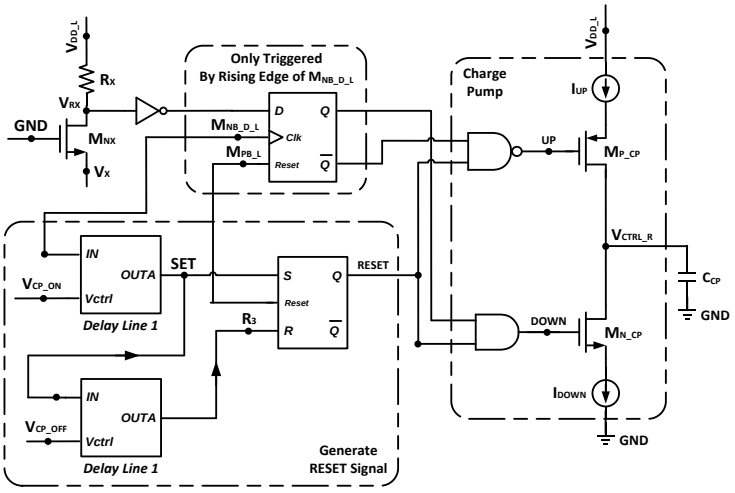


Figure 15. Zero-Crossing VX Sensor.

Referring to Figure 15, when $V_X < 0$, output of D latch is '1' and it waits for the RESET signal before it activates the charge pump. At this instant, the value of RESET = 0, hence the charge pump will be idling before the next rising edge of SET is observed. When $M_{NB_D_L}$ rises from 'low' to 'high', only after a brief time period T_{ON_CP}, the SR latch gets activated and RESET rises from '0' to '1'. During $T_{U/D}$ when RESET is high, the charge pump becomes activated, turns on transistor M_{N_CP}, and discharges the output capacitor, C_{CP}. As a result, it reduces V_{CTRL_R} by a small margin. The same occurs vice versa when $V_X > 0$. This signal will gear towards changing the imbalanced condition in the UIP comparator, which will be discussed later. After which, RESET is reset to '0' with the rising edge of R_3, which is controlled by V_{CP_OFF}. At the end of the cycle, M_{PB_L} rises from '0' to '1' (Refer to Figure 13); reset both the D and SR latches, and wait for the next rising edge of $M_{NB_D_L}$ or when power transistor M_N turns off.

There is an important design parameter which involves the desired change in V_{CTRL_R} whenever a charging or discharging event takes place in the charge pump. This has to be designed with a properly selected capacitor value and then calculating its slew rate within the charging/discharging time interval, $T_{U/D}$. The constant current source, I_{UP} and I_{DOWN}, will no doubt have a great influence on the slew rate and the overall power consumption of this block. Hence, the balance and tradeoff has to be considered carefully. In the next sub-section, the UIP comparator will be presented and discussed in greater details.

The proposed unbalanced-input pair (UIP) comparator and its corresponding aspect ratios (W/L) are shown in Figure 16 and Table 2, respectively, and referred to in Figure 14. This block is exclusively activated during the rising edge of MNB_D_L, and its purpose is to modify the delay of the ZCD_INT output signal (TON1) transitioning from '0' to '1'. Consequently, it causes the power transistor MN to turn off either slightly later or earlier to accomplish optimized switching. As illustrated in Figure 16, an unbalanced condition arises at the gate voltage of MN2 and MN3 due to their differing aspect ratios, where $(W/L)_{MN3} > (W/L)_{MN2}$. Additionally, the gates of MN3 and MN2 are linked to an unbalanced controlled block, which is connected via a triode transistor, MN_UNB. The on-resistance of MN_UNB can be directly regulated by the output signal, VCTRL_R, origi-

nating from the Zero-Crossing VX Sensor as depicted in Figure 15. Therefore, MN_UNB is directly accountable for achieving the imbalanced gate drive voltage for both MN2 and MN3, thereby aiding in reducing the delay time in the system's response time. Furthermore, by adjusting the on-resistance of MN_UNB with a small varying VCTRL_R signal, it is possible to fine-tune the rising edge of the output signal ZCD_INT. This is evident in Figure 14. The EUIP_ZCD optimization flowchart, with the assistance of the UIP comparator, seeks to identify the most favorable optimized TON1. Simultaneously, the UIP comparator also incorporates a dual detection scheme, consisting of a common-source gain stage (MP3) and a common-gate gain stage (MN3), to expedite the detection of VX and the rising transition of ZCD_INT from 'low' to 'high'.

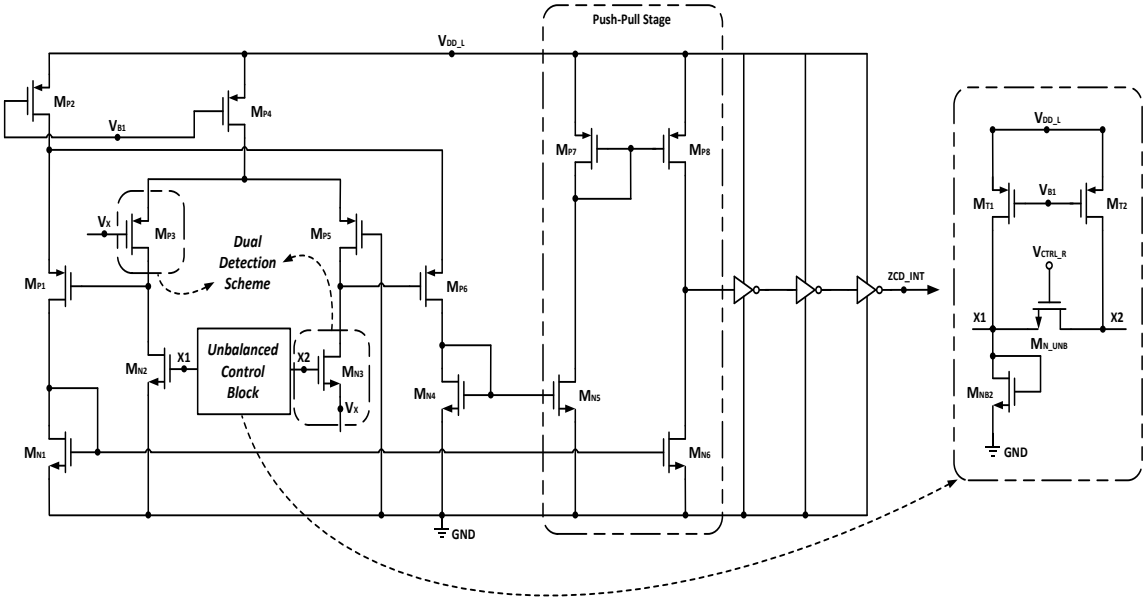


Figure 16. Unbalanced-Input Pair (UIP) Comparator.

Table 2. Transistor Sizing for UIP Comparator.

NMOS	$(W/L)_N$	PMOS	$(W/L)_P$
M_{N1}	5/1.0	M_{P1}	20/1.0
M_{N2}	30/1.0	M_{P2}	80/1.2
M_{N3}	4.5/1.0	M_{P3}	20/1.0
M_{N4}	5/1.0	M_{P4}	80/1.2
M_{N5}	5/1.0	M_{P5}	20/1.0
M_{N6}	5/1.0	M_{P6}	20/1.0
M_{NB2}	10/1.0	M_{P7}	20/1.0
M_{N_UNB}	1.5/14	M_{P8}	20/1.0
		M_{T1}	35/1.0
		M_{T2}	0.6/1.0

To further assist the dual detection scheme at the input stage, a push-pull output stage is employed so that a fast slew rate is achieved for the output signal, ZCD_INT. In addition, the unbalanced condition in the overdrive voltages of MN2 and MN3 will help to reduce the systematic and random offset voltage present in the dual detection pair transistor (MP3 and MN3). The Equations (3)–(9) will show the unbalanced conditions presented in the unbalanced circuit whereby it comprises of transistors MN2, MN3, MT1, MT2, MNB2 and MN_UNB. The transistor parameters represented by μN, VTH, COX, L and W are the electron mobility, threshold voltage, capacitance of gate oxide, and channel length and width, respectively.

For MN2 and MNB2, they share the same gate-source voltage,

$$V_{GS,N2} = V_{GS,NB2} \tag{3}$$

$$\frac{I_{D,N2}}{(W/L)_{N2}} = \frac{I_{T1} + I_{T2}}{(W/L)_{NB2}} \tag{4}$$

Since MP4 is a tail current source, under symmetric and balanced condition for MN3 and MN2,

$$I_{D,N3} = I_{D,N2} \tag{5}$$

Substitute Equation (5) into (4),

$$I_{D,N3} = \frac{I_{T1} + I_{T2}}{(W/L)_{N2}} \cdot (W/L)_{NB2} \tag{6}$$

The unbalanced condition for transistor pair M_{N3} and M_{N2} is given as,

$$\begin{aligned} \Delta V_{GS,UNB} &= V_{GS,N3} - V_{GS,NB2} \\ &= \sqrt{\frac{2(I_{T1}+I_{T2})}{\mu_N C_{OX}(W/L)_{NB2}}}\left[\sqrt{\frac{(W/L)_{N2}}{(W/L)_{N3}}} - 1\right] \end{aligned} \tag{7}$$

The purpose of M_{N_UNB} is certainly to give rise to a stark difference between the gate voltages of M_{N2} and M_{N3}, $V_{DS(MN_UNB)}$, given by:

$$\begin{aligned} V_{DS(MN_UNB)} &= I_{T1} \cdot R_{ON,MN_UNB} \\ &= \frac{I_{T1}}{\mu_N C_{OX}(W/L)_{N_UNB}\left[V_{CTRL_R} - V_{GS,NB2} - V_{TH_MN_UNB}\right]} \end{aligned} \tag{8}$$

Therefore, in an ideal condition, to yield zero input offset voltage at the gates of M_{N2} and M_{N3}, Equations (7) and (8) will be equal. Hence, the tunable voltage, V_{CTRL_R}, coming from the output of the zero-crossing V_X sensor block can be calculated to be:

$$V_{CTRL_R} = V_{GS,NB2} + V_{TH_MN_UNB} + \frac{I_{T1}}{(W/L)_{N_UNB}\frac{\sqrt{2(I_{T1}+I_{T2})\cdot\mu_N C_{OX}}}{\sqrt{(W/L)_{NB2}}}\left[\sqrt{\frac{(W/L)_{N2}}{(W/L)_{N3}}} - 1\right]} \tag{9}$$

This value of V_{CTRL_R} is able to adjust the cycle-to-cycle rising transition of ZCD_INT signal, which will optimize the turning OFF of the power NMOS transistor and eliminate any possibility of the occurrence of reverse inductor current. All the aspect ratios and relevant parameters found in the derivation of V_{CTRL_R} have to be sized carefully and take into account the spread in PVT variations. Overall, the circuit's diagrams and its detailed operations have been presented in Section 2.1–2.4. Hence, in the next section, the post-layout simulation results for the proposed work will be presented.

3. Post-Layout Simulation Results

The post-layout simulation results of the proposed work, shown in Figure 1, are carried out with 0.18 µm 1P6M CMOS process using Cadence Virtuoso Spectre Circuit Simulator. The specification of the proposed HCS and its component values are given in Table 3. The silicon chip area of the proposed HCS (including the output pad frame), as shown in Figure 17, is 1.44 mm^2. The chip fabrication was sent out in January 2024 and the return of the measurement dies is expected in March 2024. Hence, the following subsections will focus on presenting the post-layout simulation results, which will no doubt resemble closely the measurement results since the proposed work is mostly controlled by digital blocks.

Table 3. Specification of Proposed HCS.

	Units	Value
CMOS Technology	µm	0.18
Input Voltage	V	2.8–3.3
Output Voltage	V	1.8
External Inductor	µH	10
DCR	mΩ	130
External Capacitor	µF	4.7
ESR	mΩ	10
Switching Frequency (DCM Operation)	kHz	250
Load Current	mA	5~30
Chip Area (Including Pads)	mm^2	1.44
Power Efficiency [1]	%	95.8

[1] Considering estimated power losses due to wire bonding, package leads, PCB traces and other undesired parasitic effects.

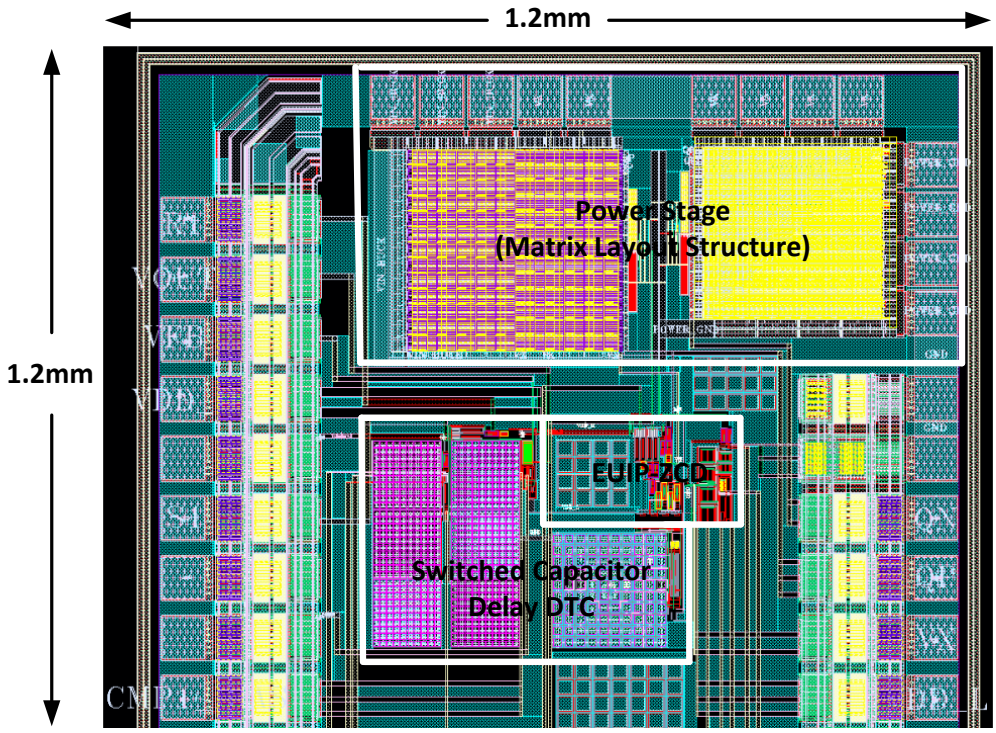


Figure 17. Silicon Chip Area of Proposed HCS.

The post-layout simulation result for the DC-SUB is shown in Figure 18 and proves that its operation is aligned according to the theoretical analysis presented in Figure 3. After ST rises to '1', the RST signal rises to '1', which will switch OFF the power PMOS transistor. This is an important circuit operation, otherwise the DC-DC buck converter will not operate well. In the duration of a few nanoseconds, the signal V_{OA} rises to '1', which resets the RST signal, and the SR latch will be in operation again.

The post-layout simulation result for the SCD-DTC is shown in Figure 19. The rising edge of S_2 signal starts the sampling window to detect the duration of body-diode conduction. The result is shown explicitly in the DT_Sample waveform. After which, the rising edge of V_{REF_DT} signal will detect the waveform of DT_Sample and gives the command for Q_A to reduce to '0' when the actual body-diode conduction is greater than the reference deadtime. After which, Q_A signal will activate the UP/DOWN counter and the switched-capacitor deadtime controller in order to reduce the value of ß. Please refer to Figures 6–11 for the full explanation of the operation above. In Figure 19, there may be

some occasional small glitches as the post-layout simulation includes parasitic inductance and capacitance from bond pads and layout routing. For this design, the sample window will be disabled when the power NMOS transistor shuts OFF. This signifies the end of the optimization and enters sleeping (idle) mode as shown in Figure 12.

A more detailed understanding of the deadtime-control optimization or fine-tune process is shown in Figure 20. Do refer to Figure 12 as a supplement. The initial deadtime is sub-optimal and results in huge power losses due to body-diode conduction. Hence, the D [3:0] is reduced gradually and leads to the decrement of β after every cycle. This repetitive action will allow the most optimized deadtime to be realized in the shortest time frame. The proposed HCS operates in the DCM, hence V_X will exhibit under-damped oscillations when the two power transistors are in idle condition. This is due to the presence of the LC tank formed by the parasitic capacitance at V_X together with the external filter inductor and capacitor. The post-layout simulation results for the Zero Crossing V_X Sensor in the EUIP-ZCD are shown in Figure 21. Do refer to Figure 15 as well for a more explicit understanding of its operation. As shown in Figure 21, the signal V_{CTRL_R} changes only during the ON time of the RESET waveform. The slew rate or simply the step increment/decrement of V_{CTRL_R} can be designed accordingly as per discussed previously in Section 2.4.

Furthermore, as shown in Figure 22, during the 1st cycle, it can be seen that there was a huge flow of reverse inductor current, which causes V_X to be charged up rapidly. This in fact draws current from the load in the reverse direction which degrades the power efficiency of the buck converter.

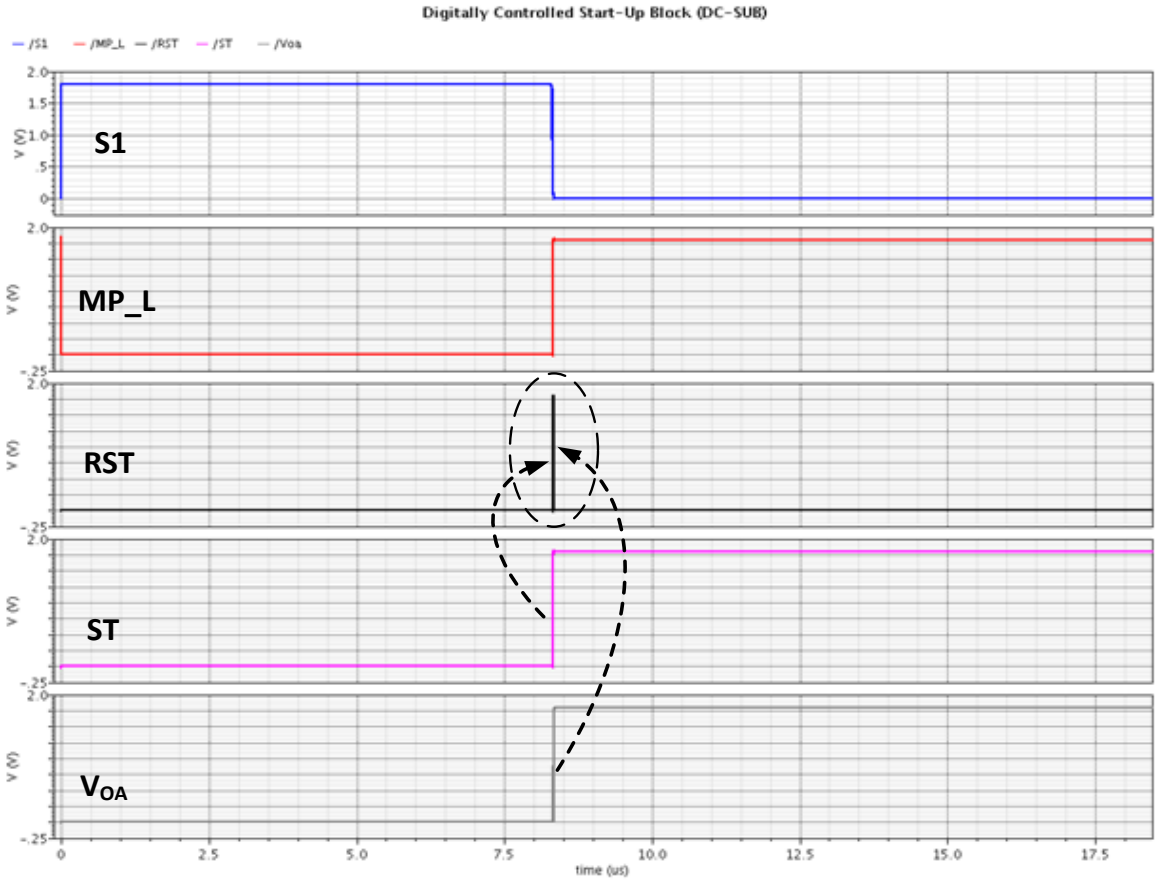


Figure 18. Post-Layout Simulation Results for DC-SUB.

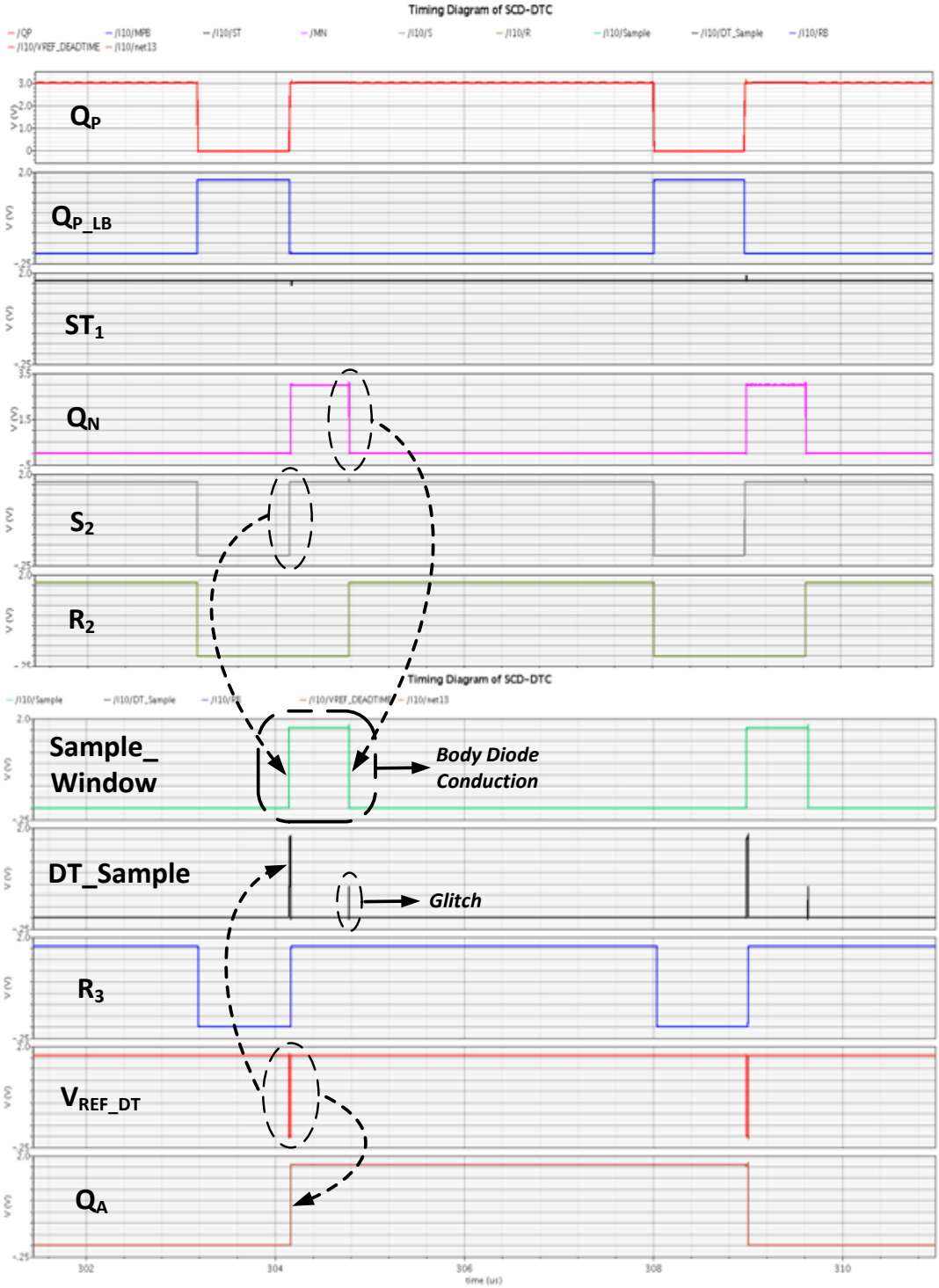


Figure 19. Post-Layout Simulation Result for SCD-DTC.

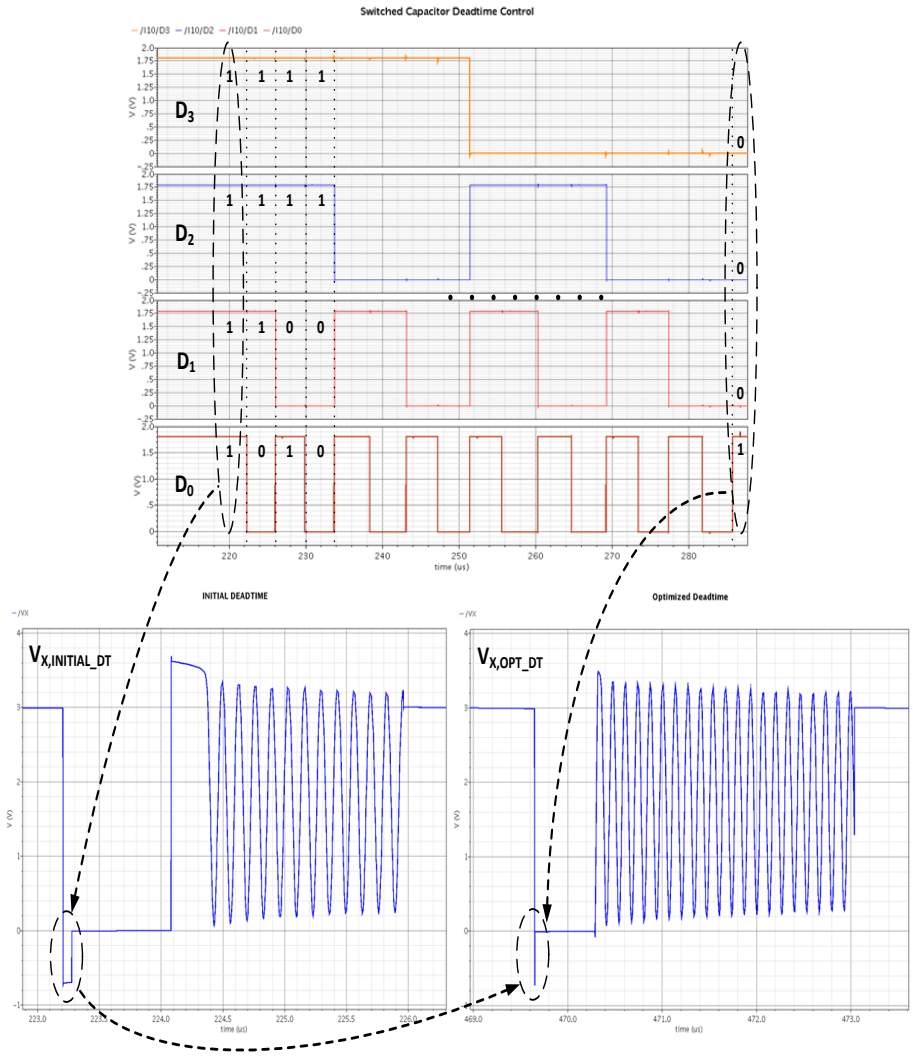


Figure 20. Post-Layout Simulation Result for Deadtime Optimization.

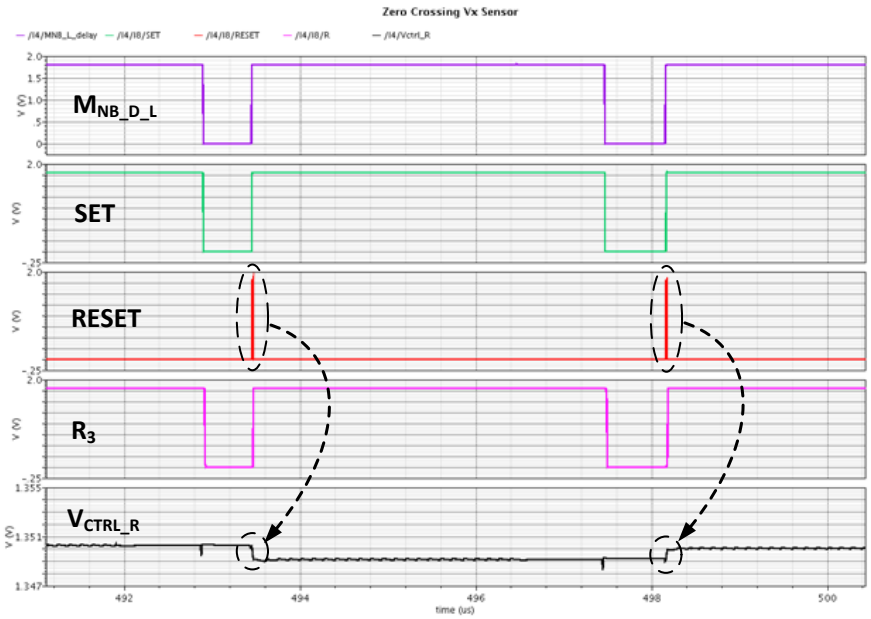


Figure 21. Post-Layout Simulation Result for Zero-Crossing V_X Sensor.

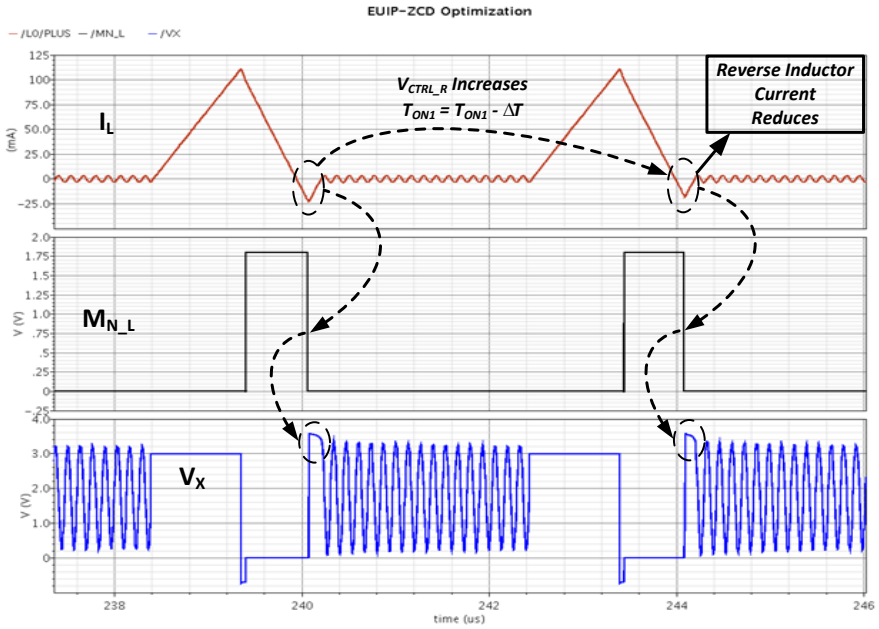


Figure 22. Post-Layout Simulation Result for EUIP-ZCD Optimization.

Hence, in accordance with the optimization flowchart presented in Figure 14, the EUIP ZCD will proceed to increase the value of V_{CTRL_R} via the Zero-Crossing V_X Sensor block, which will then turn OFF the power NMOS transistor earlier. Hence, reverting to Figure 22, in the 2nd cycle, the duration of the reverse-inductor-current phenomenon subsided as the power NMOS transistor is turned OFF earlier. This in fact helps to improve efficiency as less current is drawn from the load. This optimization process will continue till an optimized turning OFF for power NMOS transistor is realized. This is shown in Figure 23 whereby reverse inductor current is almost completely eliminated as the power NMOS turns OFF exactly at the very instant when the inductor current, I_L, falls to zero. This proves that the EUIP-ZCD optimization has achieved equilibrium as stated previously in Figure 14.

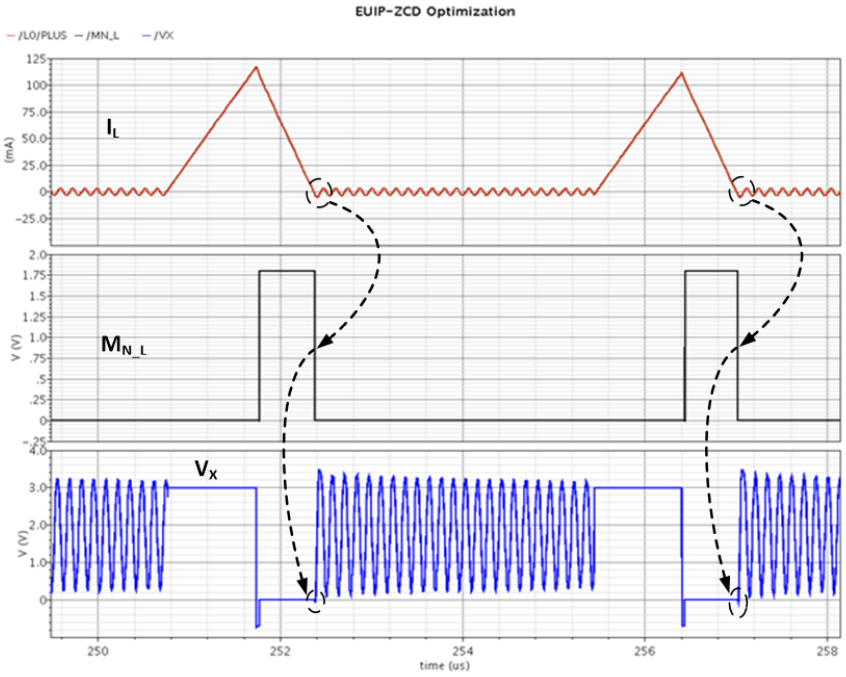


Figure 23. Final Optimization of EUIP-ZCD.

The post-layout simulation results for the proposed HCS which can simultaneously achieve optimized deadtime and reduce the phenomenon of reverse inductor current is presented in Figure 24. It is obvious that the proposed deadtime optimization, as discussed in Figure 12, has almost fully eliminated the occurrence of body-diode conduction (<3 ns). At the same time, with the implementation of the proposed EUIP-ZCD optimization, the phenomenon of reverse inductor current has been eliminated (<2 ns). This helps to improve the overall power efficiency to 95.8%. Furthermore, the final output voltage (V_{OUT}), of the proposed HCS is presented in Figure 25. It can be shown that the peak-to-peak ripple of the output voltage is <10 mV and the percent output voltage ripple is about 0.01%. This shows that the proposed HCS is stable during deadtime and reverse-inductor-current optimization. In addition, it can yield a fairly regulated voltage of 1.8 V.

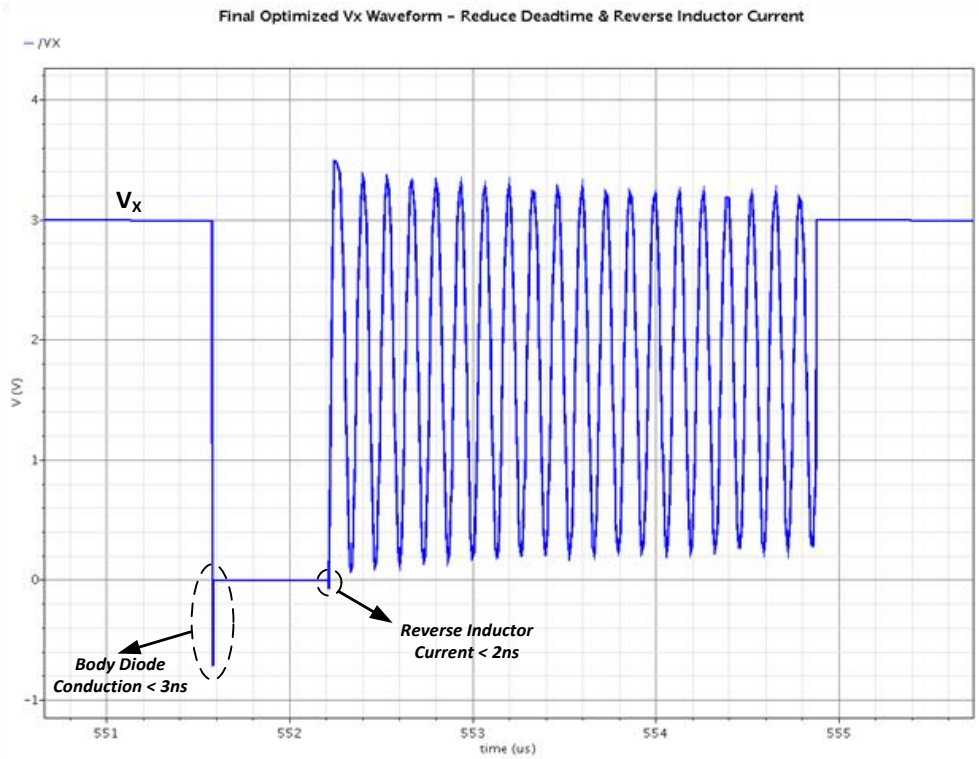


Figure 24. Final Optimization of Deadtime and Reverse Inductor Current.

Furthermore, the proposed Enhanced Unbalanced-Input Pair Zero-Current Detector (EUIP-ZCD) is expected to make a vital contribution to the overall power efficiency and stability of the DC-DC converter in several ways. Its effectiveness lies in its ability to accurately detect and handle unbalanced-input pairs. The presence of unbalanced-input pairs can lead to an uneven distribution of current within the converter, resulting in inefficiencies and potential power losses. The EUIP-ZCD ensures that the converter operates under balanced load conditions, thereby optimizing its efficiency. Moreover, unbalanced-input pairs can lead to increased switching losses and place stress on the converter's components. In this regard, the EUIP-ZCD assists in mitigating these losses by dynamically adjusting the converter's operation to compensate for unbalanced conditions. This adaptive approach reduces stress on components like switches and inductors, resulting in a reduction in overall losses and an improvement in converter efficiency. On the other hand, unbalanced-input conditions can also have an impact on the stability of the converter, potentially leading to issues such as output voltage fluctuations or instability in the control loop. Hence, the EUIP-ZCD enhances stability by ensuring that the converter operates under balanced load conditions, thus minimizing the risk of instability in the output voltage. Lastly, the EUIP-ZCD has a feedback mechanism that allows it to dynamically adjust the converter's control parameters based on input conditions. This adaptive control approach enables the

converter to maintain optimal performance across a range of operating conditions, thereby further enhancing its power efficiency and stability. By mitigating losses, enhancing stability, and optimizing control, the EUIP-ZCD ensures that the converter operates efficiently under varying load conditions.

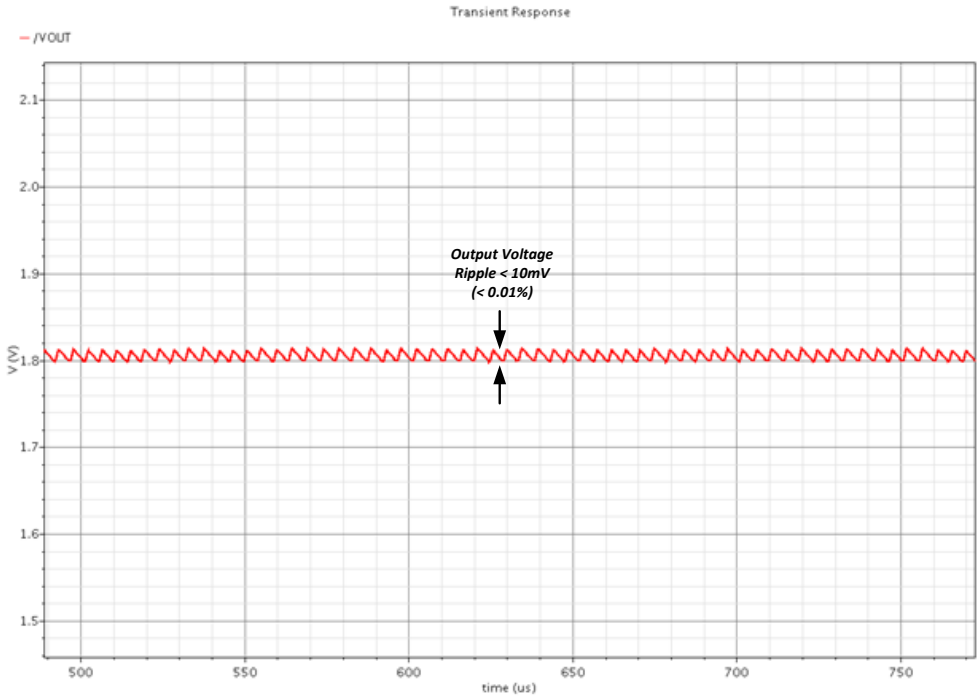


Figure 25. Final Output Voltage.

4. Discussion

The post-layout simulation results demonstrate the effectiveness of the proposed Switched-Capacitor Delay Deadtime Controller (SCD-DTC) in achieving optimized deadtime. Deadtime optimization aims to minimize the duration during which the body diode of the switch conducts, reducing power losses and improving overall efficiency. The post-layout simulation results show that the achieved deadtime is within the specified target (<3 ns), indicating successful optimization of switching times and control parameters. For the reduction in reverse inductor current (RIC), by effectively controlling the switching events and timing, the proposed design aims to minimize RIC, which can lead to reduced losses and improved converter efficiency. The post-layout simulation results show that RIC is negligible and within acceptable limits when benchmarked to industry standards, validating the effectiveness of the design in mitigating this undesirable phenomenon. Lastly, post-layout simulation results, which include transient response testing, have proved that the output voltage remains within desired limits during load transients and remains stable during all load conditions.

To attain an optimized deadtime and the reduction of reverse inductor current (RIC) in the proposed DC-DC converter, numerous design factors and parameters were presumably considered.

The Switched-Capacitor Delay Deadtime Controller (SCD-DTC) assumes a pivotal role in governing the deadtime within the converter. Significant design considerations, which include the appropriate selection of capacitor values, switching frequencies, and control logic, help to ensure meticulous deadtime control.

The Digitally Controlled Start-Up Block (DC-SUB) necessitates a critical startup process for ensuring a stable and efficient operation of the converter. Crucial design considerations for the DC-SUB may involve the selection of startup timing parameters and control mechanisms to minimize deadtime during the startup phase.

The Enhanced Unbalanced-Input Pair Zero-Current Detector (EUIP-ZCD) is designed as an additional feature to enhance the detection and handling of unbalanced-input pairs, which can contribute to the elimination of reverse inductor current. Some noteworthy design considerations include the sensitivity and accuracy of the zero-current detection circuitry, as well as the incorporation of feedback mechanisms to dynamically adjust converter operation.

The overall control logic and timing parameters of the converter play a crucial role in achieving an optimized deadtime and eliminating RIC. Design considerations include the selection of appropriate control algorithms, feedback loops, and timing constraints to ensure precise control of switching events and minimize the occurrence of RIC. Design considerations related to output voltage regulation and ripple control are indispensable for achieving a stable and efficient operation of the converter. Parameters such as output capacitor values, feedback loop design, and modulation techniques can be optimized to minimize output voltage ripple and maintain tight regulation.

Finally, for optimization purposes, the design process involved extensive simulation and optimization to finely adjust various parameters for optimal performance. The evaluation of different design choices and the verification of performance under various operating conditions were conducted using the Cadence Virtuoso Spectre Circuit Simulator. Therefore, by considering these design factors and parameters, the proposed DC-DC converter achieves an optimized deadtime and eliminates reverse inductor current, thereby enhancing overall power efficiency and performance.

As shown in Table 4 above, our voltage ripple yields < 10mV and our proposed work achieves the lowest body-diode conduction interval of <3.0 ns as compared to past published DC-DC converters. Furthermore, our reverse inductor current has been minimized to almost negligible (~0.1 ns), which is far better than other published DC-DC converters. The fabricated dies have just been returned, and we have just completed the preliminary measurement at the time of writing this review. Initial measurement results show that the proposed SCD-DTC and EUIP-ZCD are performing as expected and the measured body-diode conduction and reverse inductor current is about 5.8 ns and <0.4 ns, respectively. This is just a slight degradation as compared to post-layout simulated results shown in Table 4. However, I must honestly admit that the power efficiency degrades more than what we expected and is estimated to be about 91.5% at a load current of 30mA. Our team is quite disappointed about it and more debugging work must be carried out in the coming weeks.

Table 4. FoM comparing our proposed post-layout simulated work with past published work.

	Units	TPEL [63]	TCAS I [71]	TPEL [72]	Proposed Work
Year	-	2017	2022	2014	2023
Technology Used	µm	0.13 (CMOS)	0.18 (BCD)	0.18 (CMOS)	0.18 (CMOS)
Input Voltage	V	2.2~3.3	2.7~4.7	0.9~1.4	2.8-3.3
Inductor Used	µH	3.0	4.7	1.0	10
Capacitor Used	µF	3.0	4.7	10.0	4.7
Output Voltage	V	1.7	1.6	2.5	1.8
Peak Efficiency @ Optimal Load Current	%	90.4@10 mA	92.1@10 mA	88@40 mA	95.8@30 mA
Frequency	kHz	2500	4000	800	250
Body Diode Conduction	ns	15.0	8.0	40.0	<3.0
Reverse Induction Current	ns	18.0	2.0	0.5	~0.1
Chip Silicon Area	mm^2	0.656	0.55	1.5	1.44

5. Conclusions

This proposed work introduces a DC-DC converter with Switched-Capacitor Delay Deadtime Controller (SCD-DTC), Digitally Controlled Startup Block (DC-SUB) and Enhanced Unbalanced-Input Pair Zero-Current Detector (EUIP-ZCD) that helps to improve the overall power efficiency. All the individual blocks of our proposed work have been

presented and analyzed in the different sections of this article. This includes the discussion of relevant signal waveforms and the two major optimization flowcharts. Finally, in Section 4, the post-layout simulation results show that our proposed work can simultaneously achieve optimized deadtime (body diode conduction < 3 ns) and almost fully eliminate the phenomenon of reverse inductor current. Furthermore, it also shows that it can achieve a well-regulated output voltage of 1.8 V with <0.01% of output ripple riding on it.

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