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A Behavior Model of SiC DMOSFET Considering Thermal-Runaway Failures in Short-Circuit and Avalanche Breakdown Faults

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Abstract: Accurate fault simulation and failure prediction have long been challenges for SiC MOSFETs users. This paper presents a behavior model of Silicon Carbide (SiC) double-implanted MOSFET (DMOSFET), considering thermal-runaway failures in short-circuit and avalanche breakdown faults on the basis of cell-level physical processes. The proposed model can simulate the faults with extremely high accuracy and precisely predict SiC DMOSFET's short-circuit withstand time and critical avalanche energy. By finite-element simulations, cell-level physical processes of short-circuit and avalanche breakdown faults are clarified. The mechanisms of thermal-runaway failures are deeply discussed with references to existing studies. Based on semiconductor and device physics mechanisms, the proposed model is constructed upon a traditional behavior model of SiC MOSFET with several parallel branches that are proposed to describe the thermal-runaway failures during both faults. The Cauer thermal network model is used for estimating junction temperature within it. The proposed model is constructed in Simulink, and it is validated using short-circuit and unclamped inductive switching (UIS) tests.

Keywords: silicon carbide (SiC) MOSFET; avalanche breakdown; short circuit; behavior model; failure prediction; thermal runaway

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1. Introduction

Silicon Carbide (SiC) is a kind of wide bandgap semiconductor material. Thanks to its excellent physical properties, SiC has advantages over Silicon (Si) in power electronics devices [1]. SiC metal-oxide semiconductor field-effect transistors (MOSFETs) are capable to perform well in high-frequency and high-temperature conditions with negligible tail currents and low switching oscillations [2,3]. SiC double-implanted MOSFET (DMOSFETs), also called planar-gate SiC MOSFETs, are the most mature type of SiC MOSFET and they are becoming more popular in the design of high-power-density and high-efficiency power electronics systems, such as motor drivers and charging piles of electric vehicles [4,5]. But in terms of reliability, especially the short circuit and avalanche ruggedness, they are far weaker than traditional Si IGBTs, which hinders them from large-scale applications [6,7].

Thermal runaway accounts for 38% of the causes of SiC MOSFET's failures in short-circuit faults [7], and it is also the main failure mechanism in avalanche breakdown faults [6,8,9]. Thus, for integrality and accuracy, thermal-runaway failures are necessary to be included in the fault simulations of SiC MOSFET. However, finite-element simulation, which is often used to evaluate faults and failure of power electronics devices, is inconvenient for circuit designers. Behavior models are widely used by researchers and engineers in the design, optimization, and faults diagnosis of power electronics systems and design

of protection circuits of power devices due to their fast simulation speed and considerable accuracy in circuit system simulations. However, the majority of behavior models of SiC MOSFETs focus on the accuracy of static and dynamic characteristics simulation at an operating temperature that is not extremely high [10–17]. They cannot simulate the devices under extreme operating conditions, like short-circuit and avalanche breakdown fault. For users of the devices and the circuit designer, if there exists a behavior model that can describe the faults and thermal-runaway failures of power devices, it is more convenient to carry out some simulations in extreme conditions, validate the design of protection circuit, and evaluate the reliability of the power devices in a power electronics system. For designers of power devices, if a behavior model is capable of reflecting the real cell-level parameters and the physical processes in faults and failures, it is easier to find out the key point in cell-level design to improve the device's reliability in faults.

In recent years, several papers have paid attention to modeling SiC MOSFET's faults [18–23]. The majority of them focus on fitting short-circuit characteristics of SiC MOSFETs without considering the physical mechanisms, therefore being less generic. Some models simulate short-circuit currents with equations entirely obtained using data fittings [18,19]. They cannot fully describe the physical processes of SiC MOSFET's short-circuit fault and cannot ensure accuracy in different working conditions due to a lack of physical basis. In [20,21], electrothermal models are established to simulate temperature-dependent characteristics during short-circuit faults, aiming to clarify the short-circuit failure mechanisms and achieve failure prediction. But they can only be used to calculate the short-circuit withstand time, not for circuit simulation. A physically based short-circuit model of SiC MOSFET is presented in [22]. It introduces several physical models into parameter calculations for more accurate simulation and can emulate the short-circuit failure, whereas other faults, such as avalanche breakdown, are not included in it. Michele Riccio et al. proposed a temperature-dependent model accounting for both short-circuit and avalanche breakdown faults [23]. This model is built based on the physical processes of both faults, but the key parameters are all calculated using data fittings, which reduces its physical meaning and may impact its universality.

In a word, the existing models still suffer from one or more of the following weaknesses: (1) the model includes only short-circuit fault and cannot describe avalanche breakdown fault at the same time; (2) it lacks a physical basis, which may decline universality and accuracy of the model; (3) it cannot characterize failure phenomena that occur during faults.

To overcome the aforementioned problems, this paper presents a behavior model of SiC DMOSFET considering thermal-runaway failure in short-circuit and avalanche breakdown faults. The proposed model is more complete and universal than the existing ones because it is built based on cell-level processes of short-circuit and avalanche breakdown faults and can describe thermal-runaway failures in both faults. It can help device users design the protection circuit and evaluate the ruggedness of SiC MOSFET in some to improve the reliability in application. Meanwhile, for designers of SiC DMOSFET, the proposed model can help them intuitively and quickly analyze the influence of the design of the device on the characteristics of it and improve the design.

This paper is organized as follows. Section 2 clarifies the physical basis of the proposed model: it analyzes the cell-level physical processes of both faults by finite-element simulation and further discusses the thermal-runaway failure mechanisms with reference to existing studies. On this basis, Section 3 then illustrates the working principles of the model. Section 4 presents the calculation of the parameters used in the model: junction temperature, carrier mobility, leakage current, and so on. In Section 5, the proposed model is validated using a short-circuit test and unclamped inductive switching (UIS) test experiments, and a commercialized SiC DMOSFET, C2M0080120D produced by Wolfspeed, is selected as the modeling object. Finally, Section 6 concludes this paper.

2. Physical Basis

The cell-level physical processes of short-circuit and avalanche breakdown faults and the failure mechanisms of both faults are the physical basis of the proposed model. However, the cell-level phenomena are microscopic and hard to observe. To clarify the physical basis of the proposed model deeply, in this section, a finite-element model of SiC DMOSFET is built and short-circuit and avalanche breakdown test simulations are carried out. Based on the simulation results, the cell-level physical processes of short-circuit and avalanche breakdown faults are analyzed. Furthermore, with reference to the existing studies, the failure mechanisms of SiC DMOSFET during both faults are discussed in depth.

2.1. Finite-Element Cell Model and Fault Simulations

Thus, in order to clarify the physical basis of the proposed model, as shown in Figure 1, a 2D finite-element cell model of SiC DMOSFET is established in Synopsys Sentaurus TCAD according to the practical structure of the modeling object. The doping distributions of the P-well, N+ and P+ regions are completed using ion implantation simulations, in which Nitrogen is set for the N-type doping and Phosphorus is set for P-type doping. The shape and boundary of the regions in the model are similar with those regions formed using ion implantation in real devices [24]. The key structure parameters of the cell are given in Figure 1.

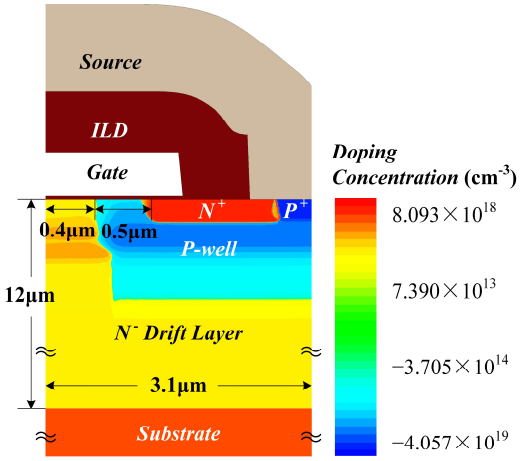


Figure 1. Two dimensional finite-element cell model of SiC DMOSFET.

Appropriate physical models are selected in the finite-element simulation to enable the simulated results to reveal the realistic cell-level physical processes. The default drift-diffusion model is used for carrier transportation calculation and Fermi statistics are chosen as the carrier distribution function here. In terms of carrier mobility calculation, the Masetti model describing doping-dependent mobility degradation is used and the high field saturation effect is taken into account. Furthermore, to calculate the electron mobility near SiC/SiO_2 interface, the University of Bologna mobility model and the interface charge model is included. Moreover, the combination of the exponential and uniform model, $N_0\exp(-(E - E_0)/E_S) + N_1$, is used, to fit the energetic distribution of both donor and acceptor interface traps, where $D_{IT,T} = 1.3 \times 10^{13}$/eV represents the energetic distribution of the interface state density near the band edge and $D_{IT,M} = 4.0 \times 10^{12}$/eV represents that near the middle of band. In the finite-element simulation, $E_S = 0.069$ eV describes the decay rate of the interface state density from band edge to the middle.

For the recombination model, the SRH, Auger and avalanche recombination are all considered and the Okuto–Crowell model is selected to calculate the impact ionization. Also, incomplete ionization and the anisotropy of 4H-SiC are considered. To emulate the lattice temperature variation during faults, the analytic thermoelectric powers model and

thermodynamic model are introduced, and the model's working temperature in static characteristics simulations and the initial temperature in fault simulations are set to 300 K.

The model's simulated on-resistance is 90.9 mΩ and the simulated breakdown voltage is 1686 V, whose relative error to the measured results of C2M0080120D is approximately 1.6% and 2.3%, respectively. The simulated static characteristics of the model cannot be identical to a realistic device, because they can be significantly influenced by the incomplete physical model and some unreasonable parameters sets in the simulation software. However, it does not prevent the model and simulation from showing the correct semiconductor-level physical processes. The convinced cell structure, doping distribution formed using process simulation, and the proper physical models selected according to realistic physical mechanisms all indicate that the model is able to describe the modeling object's cell-level physical processes during faults.

Then, short-circuit and UIS test circuits are built in Sentaurus TCAD and the cell model is put into it for fault simulations. In practical short-circuit and UIS test platforms, there may be some branches for protection between drain-gate or some branches between drain-source as buffer circuits. The aforementioned branches may affect the dynamic responses of the tests, but those factors do not actually influence the cell-level physical processes of SiC DMOSFET during faults. Hence, the simulation test circuit is simplified as shown in Figure 2, in which the inductance L here represents a small stray inductance of the power loop in the short-circuit test and a large load inductance in the UIS test.

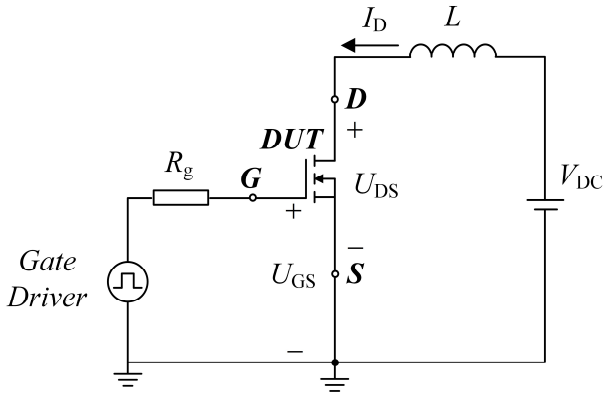


Figure 2. Short-circuit and UIS test circuit used in finite-element simulations.

By means of the fault simulations of the finite-element cell model, not only are the current and voltage waveforms obtained, but also the distributions of cell-level physical quantities, such as total current density, electric field, lattice temperature and so on, can be observed. These results may help to straightforwardly analyze the cell-level physical processes of SiC DMOSFET during faults as follows.

2.2. Cell-Level Physical Processes of Short-Circuit Fault and the Thermal-Runaway Failure in It

2.2.1. Cell-Level Physical Processes of Short-Circuit Fault

In Figure 3a, the solid blue lines and dotted orange line, respectively, represent the drain current I_D and the drain-source voltage U_{DS} waveforms in short-circuit fault test simulation when the failure does not occur. The process of SiC DMOSFET's short-circuit fault can be divided into three stages according to its working states, and the vertical black dashed lines show the boundaries between stages. Figure 3b gives the corresponding maximum lattice temperature T_{max} curve in short-circuit fault test simulation.

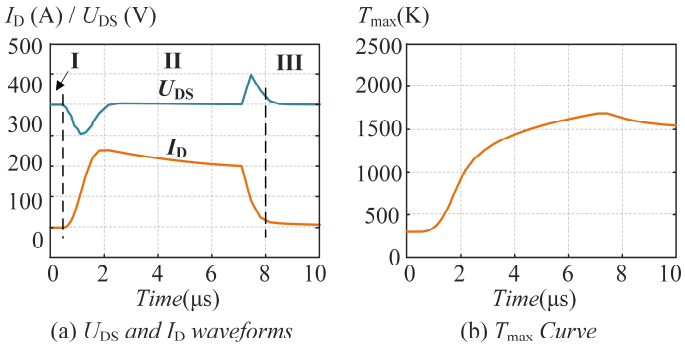


Figure 3. (**a**) Drain-source voltage U_{DS}, drain current I_D waveforms, and (**b**) maximum lattice temperature T_{max} curve obtained in the short-circuit test simulation where the thermal-runaway failure does not occur.

With reference to the waveforms and the typical cell-level total current density distributions of these stages obtained from the simulation, as given in Figure 4, the physical processes of SiC DMOSFET's short-circuit fault can be demonstrated:

- In stage I, gate drive voltage $U_{GS} = -5$ V and the SiC MOSFET is blocking. As shown in Figure 4a, the value of cell-level total current density is very low, which means almost no current flows through the device.
- In stage II, U_{GS} increases to 20 V and the device turns on. As shown in Figure 4b, the current begins to flow through the channel at the cell level. I_D increases and then falls because the channel electron mobility falls with increasing temperature.
- In stage III, U_{GS} turns to -5 V and the device turns off. I_D does not drop directly to zero, but first drops sharply to a small value and then slowly to zero, which is called tail current. At the cell level, as provided in Figure 4c, there is still leakage current flowing at the channel, but the value is far lower than that in stage II. The tail current is composed of the leakage current and it increases with the length of short-circuit pulse and maximum lattice temperature, indicating that high temperature is a main cause of non-negligible tail current [9,25,26].

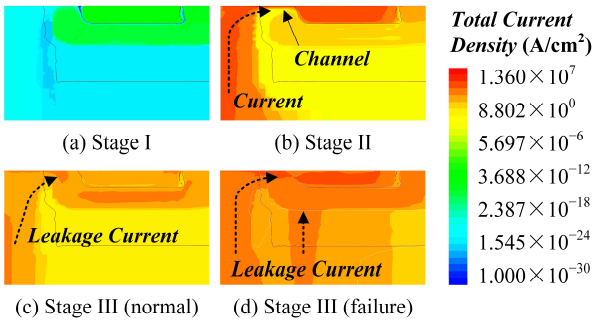


Figure 4. Typical cell-level total current density distributions of four stages in short-circuit test simulation that the thermal-runaway failures do not occur.

2.2.2. Discussion on the Short-Circuit Failure Mechanism

In the past few years, plenty of researchers have focused on SiC DMOSFET's failures in short-circuit faults. Most of them reach an agreement that there are two failure modes in SiC DMOSFET's short-circuit fault: thermal runaway and gate oxide breakdown [7,9,25–37]. As for the origin of thermal runaway failure, there are several different explanations.

On the one hand, some researchers find that the source metal will melt under high-temperature conditions, causing the incapacity of drain and source during fault, which may lead to the failure [32–34]. However, lots of experiment results can prove that delayed thermal runaway exists in SiC DMOSFET's short-circuit test [25,29]. As the I_D waveforms shows in the experiment results provided in those references, when U_{GS} returns to -5 V,

I_D maintains a low value at first and then increase sharply, which indicates that the gate driver can no longer control the device and the thermal-runaway failure happens. If the melting of the source metal is the origin of thermal-runaway failure in a short-circuit fault, the current should increase sharply, which therefore reflects that the melting of the source metal is not the failure mechanism but the result of a failure, and the failure occurs at the semiconductor level.

On the other hand, more studies agree that the main cause of thermal-runaway failure is a non-negligible leakage current generated by a high temperature during the fault, and the leakage current may consist of a channel leakage current, a thermal generation current, and a current generated by parasitic BJT [7,9,25,26,28,29,31]. When the leakage current is high enough to trigger a positive temperature feedback, the device is out of control and the thermal-runaway failure happens. This mechanism has been demonstrated by sufficient experimental results and elaborate simulation analysis [9,25,26,29], so leakage current seems to be the more convincing short-circuit failure mechanism.

To clarify the physical processes of thermal-runaway failure in SiC DMOSFET's short-circuit failure, we lengthen the short-circuit pulses in finite-element fault simulations and the U_{DS}, I_D and T_{max} curves in the case that the failure occurs can be obtained, as Figure 5 shows. The processes can also be divided into three stages. In stage I and II here, the physical processes obtained from the simulation results are essentially the same as the case that the failure does not occur. When the U_{GS} returns to zero at the beginning of stage III, I_D does not decline but increases rapidly, which implies that the gate driver can no longer control the device and the thermal-runaway failure happens. The total current density distribution of stage III is given in Figure 4d. It can be seen that the leakage current flows through not only the channel, but also the bottom of P-well region. Furthermore, compared with Figure 4c, the value is much higher.

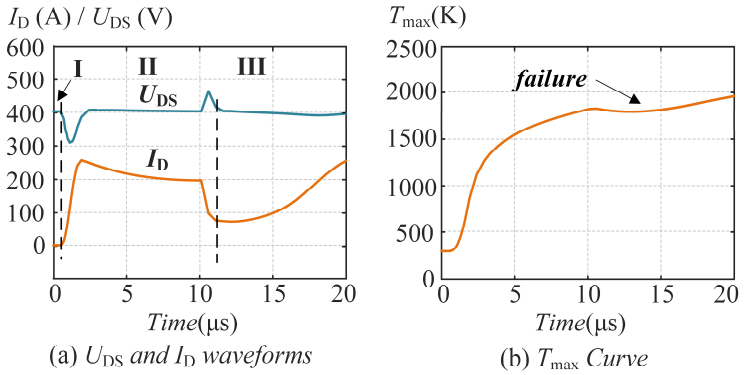


Figure 5. (**a**) Drain-source voltage U_{DS}, drain current I_D waveforms, and (**b**) maximum lattice temperature T_{max} curve obtained in the short-circuit test simulation where the thermal-runaway failure occurs.

Figure 6 compares the lattice temperature distribution of short-circuit faults before and after U_{GS} returns to −5 V for both cases that the failure does not occur and occurs. It is obvious that lattice temperature is much higher after U_{GS} returns to −5 V in the failure case, especially at the regions beside channel. As provided in Figure 5b, after the V_{GS} returns to −5 V, T_{max} does not decline like that in Figure 3b but still maintains the increasing trend. In Figure 6b, it can also be seen that the lattice temperature at channel does not decrease when short-circuit failure occurs. This means that there is a positive temperature feedback to hold the temperature. The results are the same with the existing studies [7,28,31].

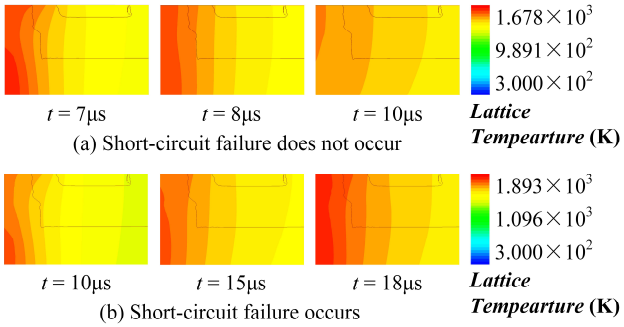


Figure 6. Lattice temperature distributions of short-circuit faults before and after U_{GS} returns to −5 V for both cases that (**a**) the failure does not occur and (**b**) it occurs.

According to the aforesaid illustrations and discussions, the short-circuit fault and failure part of the proposed model will be established based on the cell-level physical processes shown in simulation results and the failure mechanism discussed here; that a non-negligible leakage current generated by a high temperature leads to the thermal-runaway failure in SiC DMOSFET's short-circuit fault.

2.3. Cell-Level Physical Processes of Avalanche Breakdown Fault and the Thermal-Runaway Failure within It

2.3.1. Cell-Level Physical Processes of Short-Circuit Fault

Figure 7 gives the U_{DS}, I_D, and T_{max} waveforms in UIS test simulation when the failure does not occur in avalanche breakdown fault. According to the working state of the device, the processes of avalanche breakdown in UIS test can be divided into four stages and the vertical dashed lines represent the boundaries between stages.

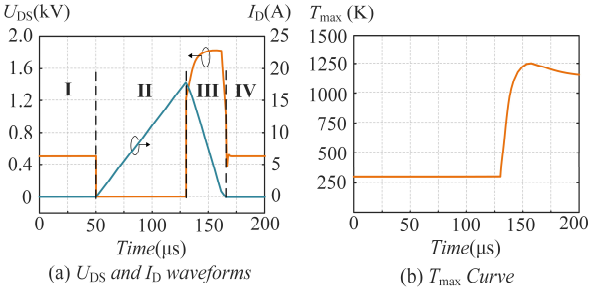


Figure 7. (**a**) Drain-source voltage U_{DS}, drain current I_D, and (**b**) maximum lattice temperature T_{max} curves obtained in UIS test simulation where the thermal-runaway failure does not occur.

Similarly, with reference to the waveforms and the cell-level total current density distributions of these stages obtained from the simulation, as given in Figure 8, the physical processes of SiC DMOSFET's avalanche breakdown fault can be demonstrated:

- In stage I, the device is in off-state. As shown in Figure 8a, at the cell level, there is only leakage current flow through the channel and the value is so small that it can be ignored.
- In stage II, the device turns on. I_D increases linearly because a large inductance is in series. At the cell level, the current flows through a thin channel closed to the SiC/SiO_2 interface, just like the stage II of short-circuit fault.
- In stage III, U_{GS} returns to −5 V and the device withstands very high voltage stress, causing an avalanche breakdown fault to occur at that moment. During a fault, U_{DS} is clamped to breakdown voltage, and it varies with increasing T_{max}. At the cell level, as shown in Figure 8c, it is obvious that the PN junction at the corner of the P-well region is broken down and the current path changes from the channel to the P-well region.

- In stage IV, I_D decreases to zero and U_{DS} drops to V_{DC}, which means the avalanche breakdown fault is over and the device returns to the blocking state. The cell-level total current density distribution is just the same as that in stage I.

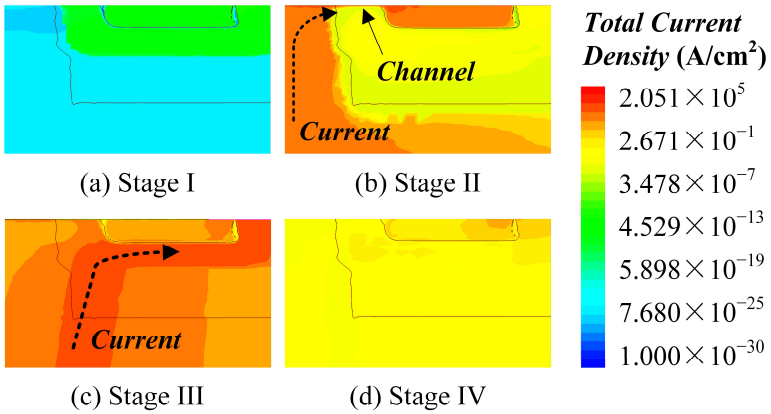


Figure 8. Typical cell-level total current density distributions of four stages UIS test simulation that the thermal-runaway failures do not occur.

2.3.2. Discussion on the Avalanche Breakdown Failure Mechanism

For the failure modes in SiC DMOSFET's avalanche breakdown faults, a lot of studies have been presented. All of them agree that high temperature causes the thermal-runaway failure. In terms of failure mechanisms, there are four mainstream views: (1) the device's junction temperature is so high that it will exceed the intrinsic limit of 4H-SiC; (2) the melting of the source metal; (3) the activation of the channel because the threshold voltage decreases with increasing junction temperature; (4) parasitic BJT latch-up at a high junction temperature [6,8,9,15,38–52].

The intrinsic carrier concentration of 4H-SiC is low because of its wide bandgap and it reaches 1.0×10^{16} cm^{-3} at 1270 °C [38,39,53]. Some researchers estimate SiC DMOSFET's junction temperature at the moment that avalanche failure occurs [38,40–42]. Though they give different estimated varying from 510 °C to 948 °C, which is a wide scale, it is obvious that the junction temperature during an avalanche breakdown fault cannot reach the intrinsic temperature limit of 4H-SiC. Hence, it seems that intrinsic limit is not likely to be SiC DMOSFET's avalanche failure mechanism.

In the past several years, the majority of researchers agree that the avalanche failure mechanism is that the melting of source metal, like aluminum, leads to a short circuit between source and drain [38,41,43]. The reason given by them is that the estimated junction temperature when an avalanche failure occurs will be close to or exceed aluminum's melting point and the temperature is not high enough to cause a latch-up of parasitic BJT and reach intrinsic limit. However, according to optical microscope diagram of failure devices shown in [8,43,44], the failure site steadily locates in the source pad near the bonding wire in different experiments. Figure 9 gives the schematic diagram of the cell-level structure in this area. At the location of source contact, there is a nickel (Ni) layer between the Al layer and 4H-SiC. The melting point of Ni is 1453 °C, which is much higher than that of Al and even 4H-SiC's intrinsic limit. And in other locations, Al and 4H-SiC are also isolated. Furthermore, as aforementioned, the junction temperature cannot reach the intrinsic limit and the device still have blocking characteristics. The above illustrations suggest that if only the Al melts, the Al cannot be in contact with 4H-SiC and the melting of the Al cannot lead to a short circuit of source and drain. Combined with the junction temperature estimations provided in [38,41], the melting of source metal is more likely to be an inducement but not the immediate cause of SiC DMOSFET's avalanche failure. Meanwhile, the immediate cause is more likely to occur at another site, maybe at the semiconductor level.

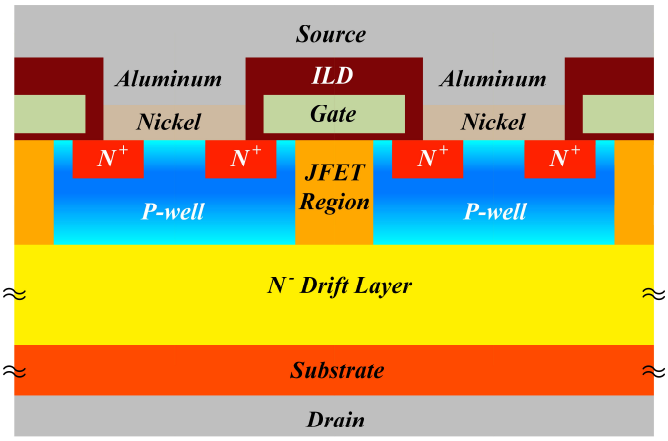


Figure 9. Schematic diagram of the cell-level structure of SiC DMOSFET at the failure site.

As for activation of the channel and parasitic BJT latch-up, failure mechanisms at the semiconductor level are also supported by several researchers [6,9,45,46]. Lots of researchers disagree with these opinions because they think the junction temperature during SiC DMOSFET's avalanche breakdown cannot reach the value required by these failure mechanisms at a semiconductor level. However, there is some compelling evidence supporting the fact that mechanisms at the semiconductor level exist in SiC DMOSFET's avalanche failure: ref. [46] gives some experiment results to show that SiC DMOSFET's avalanche failure is related to the turn-off voltage of U_{GS}; and by means of analytically modeling the parasitic BJT, ref. [6] indicates that the BJT can be triggered at a temperature that is possible to be reached during avalanche breakdown fault. Moreover, during avalanche breakdown fault, the temperature distribution is not uniform. There exists hot spots in the active area of a die [43] and the temperature at the hot spot can be much higher than the estimated average junction temperature. Thus, the failure caused by mechanisms at the semiconductor level seems possible to occur in SiC DMOSFET's avalanche breakdown fault. It may be the immediate cause of avalanche failure after the melting of the source metal. But confirming which of the correct avalanche failure mechanisms of SiC DMOSFET is correct still needs further verification.

To sum up the above discussions, the melting of the source metal seems more likely to be an inducement or a precursor of SiC DMOSFET's avalanche failure; the immediate cause of the failure is still undecided.

Because SiC DMOSFET's thermal-runaway failure may be related to the melting of source metal, which occurs out of the semiconductor, the finite-element simulation is not able to emulate this phenomenon. So measured results obtained from experiments, combined with the failure mechanisms discussed above, are used here to explain the physical processes of thermal-runaway failure in SiC DMOSFET's avalanche breakdown fault. Figure 10 gives measured U_{DS} and I_D waveforms in the UIS test experiment and it can also be divided into four stages. It is obvious that the waveforms in stage I, II, and III are almost identical with them in the stages shown in Figure 6, indicating that the physical processes of them are almost the same, too. In stage IV, the device reaches a critical threshold. Then, the voltage returns to a very low value and the current begins to rise again in accordance with the slope in stage I. From the perspective of external characteristics, the phenomenon is similar to a short circuit between source and drain.

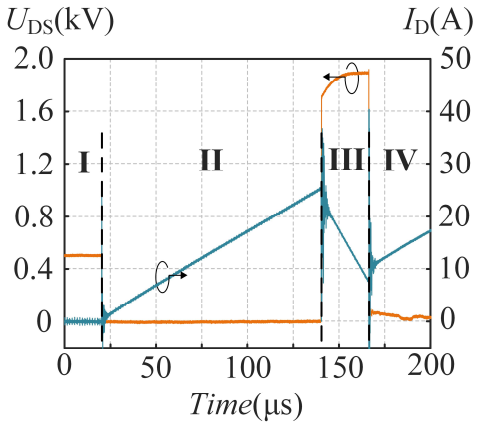


Figure 10. Measured U_{DS} and I_D waveforms in UIS test experiment.

On the basis of the aforesaid illustrations and discussions, the short-circuit fault and failure part of the proposed model will be established, based on the cell-level physical processes shown in simulation results and the failure mechanism discussed here that a non-negligible leakage current generated by a high temperature leads to the thermal-runaway failure in SiC DMOSFET's short-circuit fault. Also, the avalanche breakdown faults and thermal-runaway failure parts of the proposed can be built based on the above analysis. Critical threshold of the failure can be decided according to the thermal-runaway failure mechanisms discussed above, and it will be illustrated elaborately in Section III.

3. Working Principles of the Proposed Behavior Model

Based on the cell-level physical processes of both faults and thermal-runaway failures discussed in Section II, five working states can be defined to completely describe SiC DMOSFET's behaviors in short-circuit and avalanche breakdown faults: off-state (Figures 4a and 8a), on-state (Figures 4b and 8b), leakage current state (Figure 4c,d), avalanche breakdown state (Figure 8c), and avalanche failure state. The five states are explained as follows:

Off-state and on-state are two basic working states that describe SiC MOSFET's behaviors in conduction and blocking conditions, respectively. Leakage current is critical in tail current and thermal-runaway failure in short-circuit fault. Therefore, leakage current state is introduced. It is worth noting that according to semiconductor physics and the simulation results in Section II, leakage current exists in all working states of SiC MOSFET, but it can be ignored when the junction temperature is low. Hence, leakage current should be included in all five states, whereas it plays a leading role in the leakage current state (at a high junction temperature) and can be negligible in other working states. Because avalanche breakdown fault is caused by impact ionization and the thermal-runaway failure in it is induced by different mechanisms, two different working states, avalanche breakdown state and avalanche failure state, should be separately defined to characterize them. If a behavior model of SiC DMOSFET is able to take all five working states into consideration, it can completely describe all behaviors including short-circuit and avalanche breakdown faults and the thermal-runaway failures.

Figure 11 gives the circuit diagram of the proposed behavior model in this paper. It consists of two parts: a traditional behavior model of SiC MOSFET that describes on-state and off-state (the light blue part) and several extended parallel branches for describing leakage current, avalanche breakdown, and avalanche failure states (the pale golden part).

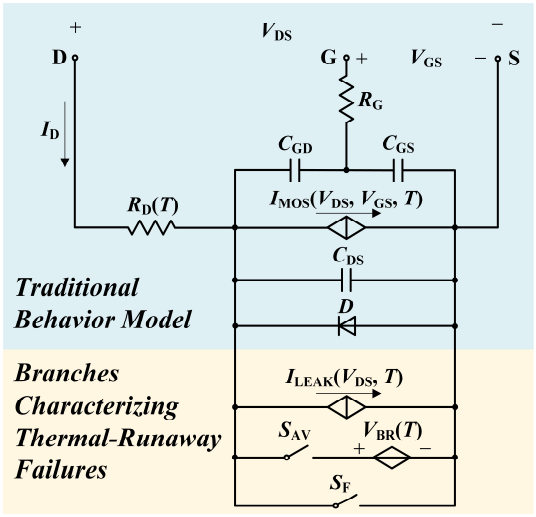


Figure 11. Circuit diagram of the proposed SiC DMOSFET's behavior model.

In the traditional behavior model, voltage-controlled current source I_{MOS} characterizes basic voltage-current relationships calculated in the metal-oxide-semiconductor (MOS) structure. C_{GS}, C_{GD}, and C_{DS} are parasitic capacitances between three terminals, which play critical roles in the dynamic responses of the model. D represents the body diode and R_G is the gate resistor integrated into the package. R_D represents the total resistance of the N^- drift layer and JFET region. Furthermore, because channel electron mobility varies with increasing junction temperature in short-circuit faults, it requires special calculations for carrier mobility used in I_{MOS} and R_D calculations according to semiconductor and device physics.

A controlled current source I_{LEAK} is included to describe the leakage current state. The physical mechanisms generating the current in leakage current state are totally different from that in on-state, so I_{LEAK} should be placed in a separate branch.

The physical mechanism of the PN junction's avalanche breakdown is the current amplification effect caused by a high electric field. The current increases very sharply when U_{DS} reaches a critical value, also called the breakdown voltage. According to the above physical basis, a separate branch made up of a temperature-controlled voltage source U_{BR} and a controlled switch S_{BR} is included to characterize SiC DMOSFET's avalanche breakdown state. Their working principles have been demonstrated in previous work [54].

As said in Section 2, from the perspective of external characteristics, the physical process of avalanche failure is similar to a short circuit happening between source and drain. Using the same idea of avalanche breakdown state modeling, as shown in Figure 11, the processes of an avalanche failure state are modeled as a separate branch consisting of a temperature-controlled switch S_F in the proposed behavior model. The avalanche failure mechanisms discussed in Section 2 suggests that the melting of Al seems to be an inducement or a precursor of thermal-runaway failure in SiC DMOSFET's avalanche breakdown fault, and the undecided mechanism occurs after that is more likely to be the immediate cause. Because the direct failure mechanism is still undecided, it can be simplified as a process spending a short period of time. Thus, the control logic of the switch can be defined as follows: after the junction temperature exceeds a critical threshold temperature T_{CRIT}, the melting of aluminum by a short time t_{FD}, enables the S_F to turn on and it cannot be turned off again. The T_{CRIT} characterizes the melting of the source metal, and the t_{FD} describes the undecided failure mechanism that occurs after the melting of the source metal. According to subsequent experimental verifications, this modeling approach for thermal-runaway failure in SiC DMOSFET's avalanche breakdown fault is accurate enough and it is easy to modify and improve if the failure mechanisms are clarified further.

The junction temperature T significantly influences SiC DMOSFET's characteristics in short-circuit and avalanche breakdown faults. So, the calculation of T should be included.

The models of all components and calculations of the key parameters in the proposed behavior model will be elaborated on in Section 4.

4. Models and Calculations

In this section, the modeling of all components and calculation methods of the key parameters in the proposed behavior model will be elaborated on, including the channel current, parasitic junction capacitances, the resistance of N-type drift layer and JFET layer, leakage current, junction temperature, and key physical parameters used in the above calculations such as intrinsic carrier concentration, threshold voltage and carrier mobility. A physically based and accurate methodology for avalanche breakdown voltage calculation has been explored in previous work [54] and it will not be repeated in this section.

Figure 12 displays the summary of parameters calculations in the proposed model. The parameters used in this section are listed in Table A1 in the Appendix A. The majority of the parameters related to device structure and fabrication can be obtained from the finite-element model of Section 2 and the open literature. Some fitting parameters can be obtained through curve fitting.

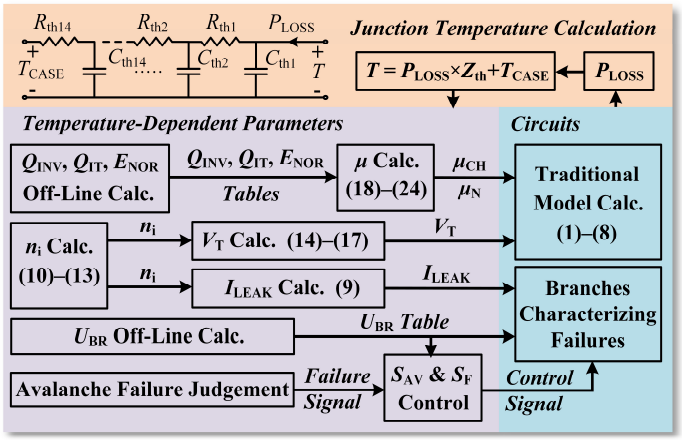


Figure 12. Summary of calculations in the proposed behavior model presented in this paper.

4.1. Channel Current I_{MOS}, Parasitic Junction Capacitance C_{GS}, C_{DS}, C_{GD}, and Body Diode D

In the proposed model, the channel current I_{MOS} is calculated using (1). The selected model is derived in an ideal N-channel enhanced MOS structure and takes the channel length modulation effect into account [19]. It is widely used in characterizing MOSFET's fundamental voltage–current relationship.

In (1), channel electron mobility μ_{CH} and threshold voltage V_T are the key parameters influencing the variation in current and the calculations of them will be presented later. C_{ox} is the capacitance of oxide per unit area; L_{CH} is the length of channel; L_{CELL} represents the equivalent total width of channel considering the number of cells; λ is the channel length modulation coefficient.

Models of parasitic junction capacitances are necessary for switching process simulations. In the proposed model, C_{GS} is modeled as a constant capacitance, C_{GD} and C_{DS} are, respectively, modeled as C_{rss} and ($C_{oss}-C_{rss}$), in which C_{rss} and C_{oss} is calculated using (2) and (3) [55]. C_{r0}, V_r, M_r, δ_r, γ_r, C_{rssFD}, V_o, M_o, δ_o, γ_o, and C_{ossFD} are all fitting parameters used for parasitic capacitance calculation. In (2) and (3), except U_{DS} which represents the drain-source voltage, all other parameters are obtained from data fitting according to the datasheet.

$$I_{MOS} = \begin{cases} 0 & U_{GS} \le V_T \\ \mu_{EFF} C_{ox} \frac{L_{CELL}}{L_{CH}} \left[(U_{GS} - V_T) \cdot U_{CH} - {U_{CH}}^2/2 \right] \cdot (1 + \lambda U_{CH}) & U_{GS} > V_T,\ U_{CH} < U_{GS} - V_T \\ \frac{\mu_{EFF} C_{ox}}{2} \cdot \frac{L_{CELL}}{L_{CH}} (U_{GS} - V_T)^2 \cdot (1 + \lambda U_{CH}) & U_{GS} > V_T, U_{CH} \ge U_{GS} - V_T \end{cases} \quad (1)$$

$$C_{\mathrm{rss}} = C_{\mathrm{r0}}\left(\frac{V_{\mathrm{r}}}{V_{\mathrm{r}} + U_{\mathrm{DS}}}\right)^{M_{\mathrm{r}}} + \delta_{\mathrm{r}}[1 - \tanh(\gamma_{\mathrm{r}} U_{\mathrm{DS}})] + C_{\mathrm{rssFD}} \tag{2}$$

$$C_{\mathrm{oss}} = C_{\mathrm{o0}}\left(\frac{V_{\mathrm{o}}}{V_{\mathrm{o}} + U_{\mathrm{DS}}}\right)^{M_{\mathrm{o}}} + \delta_{\mathrm{o}}[1 - \tanh(\gamma_{\mathrm{o}} U_{\mathrm{DS}})] + C_{\mathrm{ossFD}} \tag{3}$$

The parasitic body diode is an indispensable part of SiC DMOSFET, but it has almost no effect on the fault and failure characteristics of the device. Hence, the body diode is modeled as an anti-parallel ideal diode in the proposed model. The results shown in Section V can verify that the simplified model of the body diode does not influence the accuracy of the proposed model.

4.2. Drain Resistance R_D

The resistance of the N-type drift layer and the JFET region of SiC DMOSFET changes with increasing junction temperature, which can significantly influence the characteristics of the device during fault because the junction temperature increases sharply. Thus, the resistances are carefully modeled as follows and they are combined into a drain resistance, R_{D}, in the proposed model.

The resistance of the JFET region can be calculated using (4).

$$R_{\mathrm{JFET}} = \frac{1}{q\mu_{\mathrm{N}} N_{\mathrm{JFET}}} \cdot \frac{H_{\mathrm{JFET}}}{(W_{\mathrm{JFET}} - W_{\mathrm{SCR}}) L_{\mathrm{CELL}}} \tag{4}$$

In (4), the μ_{N} represents the electron mobility of the JFET region and the N-type layer, and its calculation will be presented in part E; q represents elementary charge; N_{JFET} is the equivalent doping concentration of the JFET region; W_{SCR} is the width of the space charge region between the JFET region and the P-well region and it can be calculated using (5).

$$W_{\mathrm{SCR}} = \sqrt{\frac{2\varepsilon_{\mathrm{SiC}}}{qN_{\mathrm{DR}}} \cdot \left[\frac{k_{\mathrm{B}} T}{q} \ln\left(\frac{N_{\mathrm{JFET}} N_{\mathrm{PWELL}}}{n_{\mathrm{i}}^2}\right) + U_{\mathrm{CH}}\right]} \tag{5}$$

In (5), n_{i}, the intrinsic carrier concentration, will be modeled physically in Section 4.5; $\varepsilon_{\mathrm{SiC}}$ is the permittivity of 4H-SiC; N_{DR} is the doping of the N-type drift layer; k_{B} represents the Boltzmann constant; N_{PWELL} is the equivalent doping of the P-well region; U_{CH} is the voltage on the channel.

According to the cell-level total current distribution obtained from the finite-element simulation, when SiC DMOSFET is in on-state, there is a trapezoid-like "current diffusion layer" located at the top of the N-type drift layer because the depletion region is blocked. Under the layer, the current distribution is uniform. So, the resistance of the N-type drift layer can be divided into two parts. The upper one, named as R_{DRU}, represents the resistance of the current diffusion layer and is modeled as a trapezoidal resistance. It can be calculated using (6).

$$R_{\mathrm{DRU}} = \frac{H_{\mathrm{DIFF}}/(W_{\mathrm{CELL}} - W_{\mathrm{JFET}} + W_{\mathrm{SCR}})}{q\mu_{\mathrm{N}} N_{\mathrm{DR}} L_{\mathrm{CELL}}} \ln\left(\frac{W_{\mathrm{JFET}} - W_{\mathrm{SCR}}}{W_{\mathrm{CELL}}}\right) \tag{6}$$

In (6), H_{DIFF} is the thickness of the current diffusion layer, W_{CELL} is the width of a cell, W_{JFET} is the width of the JFET region. The lower one, named as R_{DRL}, represents the resistance of the layer in which current flows uniformly and it can be calculated using (7).

$$R_{\mathrm{DRL}} = \frac{1}{q\mu_{\mathrm{N}} N_{\mathrm{DR}}} \cdot \frac{H_{\mathrm{EPI}} - H_{\mathrm{JFET}} - H_{\mathrm{DIFF}}}{W_{\mathrm{CELL}} L_{\mathrm{CELL}}} \tag{7}$$

In (7), H_{EPI} is the thickness of the epitaxial layer.

On this basis, the drain resistance in the proposed model can be defined as (8).

$$R_{\mathrm{D}} = R_{\mathrm{JFET}} + R_{\mathrm{DRU}} + R_{\mathrm{DRL}} \tag{8}$$

4.3. Leakage Current I_{LEAK}

The leakage current can be negligible in SiC DMOSFET under low-temperature conditions. But in high-temperature cases, it has a strong influence, which is a distinguishing feature of the SiC MOSFET's short-circuit fault and the main cause of short-circuit failure. Hence, the accurate calculation of the leakage current is necessary. For SiC DMOSFET, the leakage current usually consists of three components: thermal generation current I_{TH}, diffusion current I_{DIFF}, and avalanche leakage current $I_{\mathrm{AV(LEAK)}}$ [12,14]. According to previous calculations, in SiC DMOSFET's thermal-runaway failure in a short-circuit fault, the thermal generation current I_{TH} plays the leading role in total leakage current, and the other two components are miniscule, so they can be ignored in the total leakage current.

In the proposed model, a controlled current source I_{LEAK} is used to characterize the leakage current, and it is expressed by (9).

$$I_{\mathrm{L}} = I_{\mathrm{TH}} = S \cdot \frac{q n_{\mathrm{i}}}{\tau_{\mathrm{g}}} \sqrt{\frac{2\varepsilon_{\mathrm{SiC}} U_{\mathrm{CH}}}{q} \left(\frac{N_{\mathrm{DR}} + N_{\mathrm{CH}}}{N_{\mathrm{DR}} N_{\mathrm{CH}}} \right)} \tag{9}$$

In (9), S is the equivalent junction area generating leakage current; τ_{g} is the carrier lifetime.

4.4. Junction Temperature

During short-circuit and avalanche breakdown faults, SiC MOSFET generates high power dissipation, which causes the junction temperature to increase sharply and can considerably influence its behavior.

An *RC* thermal network is widely used for junction temperature evaluation in behavior models of power semiconductor devices. In the proposed model, a 14-order Cauer thermal network, shown in the red part of Figure 12, is included to calculate the junction temperature. As provided in Table 1, the values of the thermal resistance R_{thi} and thermal capacitance C_{thi} used in this paper are obtained from the SPICE models given via Wolfspeed, Durham, NC, USA.

Table 1. Values of thermal resistances and thermal capacitances in Cauer thermal network.

i	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
R_{thi} (mK/W)	13.3	13.3	37.8	36.9	83.6	58.4	43.2	51.2	51.9	47.5	46.6	58.7	40.8	10.4
C_{thi} (mJ/K)	0.424	0.341	1.32	1.58	1.88	2.64	8.50	14.2	26.0	47.8	102	165	282	2410

4.5. Physical Parameters

As mentioned above, some key physical parameters are introduced in the proposed model, such as intrinsic carrier concentration, threshold voltage, and carrier mobility. They have important effects on SiC DMOSFET's behaviors under fault and failure conditions, because they significantly change with the sharp increase in junction temperature. Thus, it is necessary to calculate them carefully. In this part, the models of intrinsic carrier concentration, threshold voltage, and carrier mobility are presented as follows.

4.5.1. Intrinsic Carrier Concentration

Intrinsic carrier concentration n_{i} is the key factor deciding the high-temperature characteristics of the power semiconductor devices. In this paper, n_{i} is calculated using its definition given in (10) [56].

$$n_{\mathrm{i}} = (N_{\mathrm{c}} N_{\mathrm{v}})^{1/2} \exp\left(\frac{E_{\mathrm{g}}}{2 k_{\mathrm{B}} T} \right) \tag{10}$$

In (10), E_g is the band gap of 4H-SiC, which can be calculated using (11) [57].

$$E_g = 3.267 - 6.5 \times 10^{-4} \frac{T^2}{T + 1300} \tag{11}$$

N_c and N_v, provided in (12) and (13) [56], represent the effective density of state in the conduction band and the valence band, respectively.

$$N_c = 2\left(\frac{2\pi \cdot 0.8 m_e \cdot k_B}{h^2}\right)^{3/2} T^{3/2} \tag{12}$$

$$N_v = 2\left(\frac{2\pi \cdot 1.2 m_e \cdot k_B}{h^2}\right)^{3/2} T^{3/2} \tag{13}$$

In (12) and (13), m_e is the electron mass, h is the Planck constant.

4.5.2. Threshold Voltage

Threshold voltage V_T is a temperature-sensitive parameter of SiC DMOSFET and it significantly influences the high-temperature behavior of the device. In this paper, modeling of the V_T is given in (14), which considers the fixed charges in gate oxide, the traps at the SiC/SiO_2 interface, and the correction of the surface potential in the flat-band voltage calculation [39].

$$V_T = \left[\frac{\Phi_{MS}}{q} - \frac{q n_F}{C_{ox}} - \frac{Q_{IT}(\Psi_S = 2\,\Psi_F)}{C_{ox}}\right] + 2\,\Psi_F + 2\sqrt{V_0 \Psi_F} \tag{14}$$

In (14), n_F is the density of the fixed charge at the SiC/SiO_2 interface; Φ_{MS} is the work function difference between the high-doped poly silicon gate and the P-type 4H-SiC at the channel. It can be defined as (15).

$$\Phi_{MS} = \Phi_M - \chi - \frac{E_g}{2} - \Psi_F \tag{15}$$

In (15), χ is the electronic affinity of 4H-SiC; Ψ_F represents the Fermi potential at the channel and it can be calculated using (16).

$$\Psi_F = \frac{k_B T}{q} \ln\left(\frac{N_{CH}}{n_i}\right) \tag{16}$$

V_0 is a constant related to the material properties and the design of device and it is defined as (17).

$$V_0 = \frac{q \varepsilon_{SiC} N_{CH}}{C_{ox}^2} \tag{17}$$

In (17), N_{CH} is the equivalent doping concentration of the channel.

As for Q_{IT}, the charge density of interface traps, is the key parameter influencing the value and high-temperature characteristics of V_T. It also has a significant influence on the channel electron mobility μ_{CH}. The modeling and calculation of it will be presented in the Appendix B.

4.5.3. Carrier Mobility

In SiC DMOSFET, the carrier mobility is one of the most important parameters affecting the electric conductivity and high-temperature characteristics. It is decided by multiple different physical mechanisms, and generally, it can be calculated using (18).

$$\mu_{TOTAL}^{-1} = \mu_1^{-1} + \mu_2^{-1} + \mu_3^{-1} + \cdots \tag{18}$$

In (18): μ_{TOTAL} is the carrier mobility that considers several physical mechanisms; μ_1, μ_2, μ_3 are the ones affected by only one physical mechanism. In general, there are four types of physical mechanisms and the corresponding carrier mobilities that should be taken into consideration are bulk mobility (μ_B), acoustic-phonon scattering (μ_{AC}), surface roughness scattering (μ_{SR}), and Coulomb scattering at interface traps (μ_C). The above four kinds of carrier mobility can be calculated using (19)–(22) [22,39,58–64].

$$\mu_B = \mu_{MIN} + \frac{\mu_L (T/300K)^{-2.4} - \mu_{MIN}}{1 + ((N_{CH} + N_{DR})/N_{REF})^{0.61}} \tag{19}$$

$$\mu_{AC} = \frac{K_1}{E_{NOR}} + \frac{K_2 (N_{CH} + N_{DR})^{0.0284}}{T E_{NOR}^{1/3}} \tag{20}$$

$$\mu_{SR} = \frac{\Gamma_{SR}}{E_{NOR}^2} \tag{21}$$

$$\mu_{Cit} = \frac{\Gamma_{Cit} T}{N_F + N_{IT}} \left(1 + \frac{n_{INV}}{n_{SCR}}\right)^{\zeta_C} \tag{22}$$

In the above equations, μ_{MIN}, μ_L, μ_{REF}, K_1, K_2, Γ_{SR}, Γ_{Cit}, n_{SCR}, and ζ_C are the physics-based parameters used in carrier mobility calculation; the effective perpendicular electric field E_{NOR} and the interface inversion charge n_{INV} are calculated utilizing the charge sheet model [60,65]; the interface trapped charge n_{IT} is calculated with references to [22,66,67]. The models and calculations of them are complex works and, therefore, will be elaborated in the Appendix B.

In the channel of SiC DMOSFET, limited by the technology of manufacturing, the quality of the SiC/SiO_2 interface is poor, which has a great impact on the channel electron mobility μ_{CH} [39,66]. Thus, as given in (23), the calculation of μ_{CH} should consider all four aforesaid physical mechanisms.

$$\mu_{CH} = \left(\mu_B^{-1} + \mu_{AC}^{-1} + \mu_{SR}^{-1} + \mu_{Cit}^{-1}\right)^{-1} \tag{23}$$

Because the JFET region and N-type drift layer is inside of the 4H-SiC, only bulk mobility should be considered in the calculation of electron mobility μ_N in R_D calculation. Hence, as given in (24), μ_N is equal to μ_B.

$$\mu_N = \mu_B \tag{24}$$

5. Model Validation

In this section, the proposed model is validated via comparing simulation results with experimental results, including static characteristic tests, short-circuit fault tests and UIS tests. All simulations are performed in MATLAB/Simulink and the modeling object, C2M0080120D produced by Wolfspeed, is chosen as the device under test (DUT) in both test experiments to verify the correctness and accuracy of the proposed model.

5.1. Static Characteristics

To validate the accuracy of the static characteristics, output curves under 300 K of C2M0080120D are measured via Keysight B1506A (manufactured by Keysight Technologies, Santa Rosa, CA, USA), and the corresponding curves of the proposed model under different gate-source voltages are simulated. Figure 13 gives the comparison between measured and simulated curves. The simulated on-resistance under V_{GS} = 20 V and I_D = 20 A is 95.8 mΩ, whose relative error is 6.4%. The simulated threshold voltage is 2.894 V at T = 300 K and 2.414 V at T = 423 K, whose relative error is only 0.2% and 0.5%, respectively. The results indicate that the model can correctly simulate the key static characteristics of SiC MOSFET.

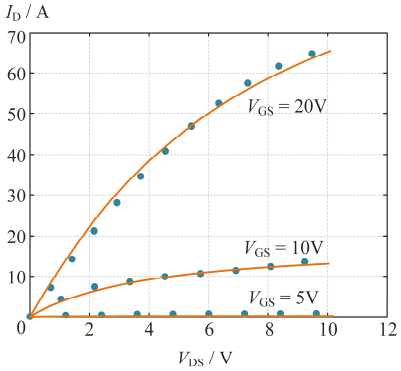


Figure 13. Measured (orange solid lines) and simulated (blue dotted lines) I_D-V_{DS} curves under different V_{GS}.

5.2. Short-Circuit Faults and Failures

To measure the behaviors of SiC DMOSFET in short-circuit faults, a short-circuit test experiment platform was built. Figure 14 gives the schematic circuit diagram: L = 231 nH is the stray inductance of the power loop; C_i = 35 nH and R_i = 4.7 kΩ are the input capacitance and resistance used to reduce gate oscillation; the gate resistance R_g equals 10 Ω for turning on and 20 Ω for turning off; the gate driver voltage is −5/+20 V. The room temperature is approximately 27 °C, so the T_{CASE} of SiC MOSFET is set to 300 K in the simulations. Figure 15 shows the test experiment platform, in which the load is replaced by a short wire for short-circuit test. The types and key parameters of instruments included in the platform are listed in Table 2.

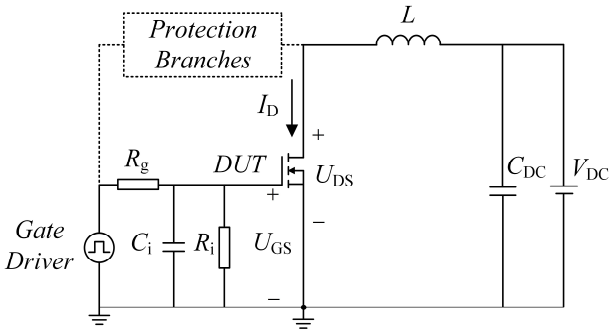


Figure 14. Equivalent circuit diagram of short-circuit test and UIS test platform.

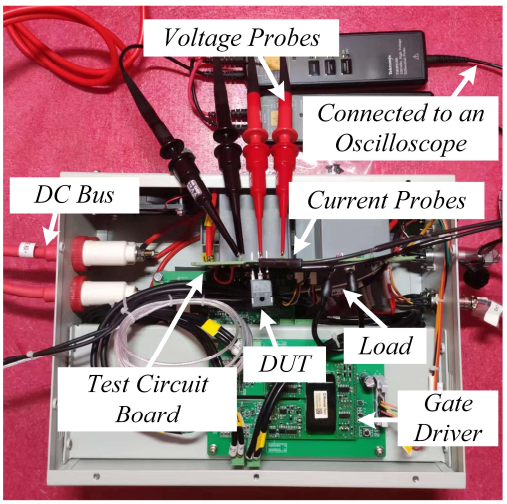


Figure 15. Short-circuit and UIS test experiment platform.

Table 2. Instruments used in short-circuit test experiment.

Instruments	Types	Parameters
DC power supply	Magna-Power XR6000	0~6000 V
Oscilloscope	Tektronix MSO58	500 MHz
Voltage probe	Tektronix THDP0100	6000 Vpk/600 Vpk
Current probe	CWTUM/06	120 A

Figure 16 reports the simulated and measured waveforms of the drain-source voltage U_{DS} and drain current I_D under the condition of V_{DC} = 400/500 V during a short-circuit pulse with a duration of 10 µs. The results show that the proposed model can accurately describe the short-circuit current that increases and then decreases. Also, the simulated peak current and the time to reach it are almost the same as the experimental results. These results can imply that the temperature characteristics of the channel electron mobility model, the drain resistances model, and the junction temperature calculation, are reasonable. Furthermore, it is worth noting that when V_{DC} = 500 V, the tail current can be directly observed, and the simulated tail current matches the experiments well. It can be seen that in the proposed model, the tail current is made up entirely of the leakage current I_{LEAK}, verifying that the calculation of I_{LEAK} is precise and the aforesaid composition of the tail current is correct. It also suggests that the cell-level physical basis of the short-circuit fault is correct. Figure 16a,b shows the results under different V_{DC}. In both conditions, the simulated waveforms match the experimental waveforms well, which validates the universality of the proposed model in different working conditions.

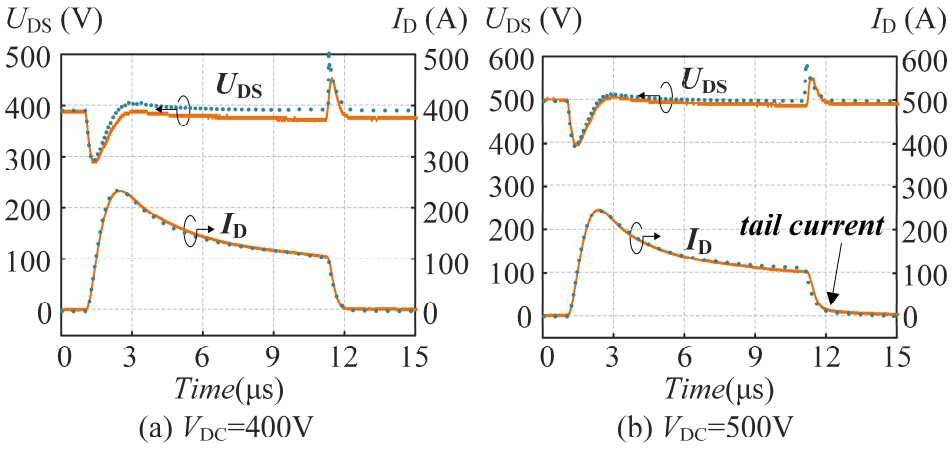


Figure 16. Measured (orange solid lines) and simulated (blue dotted lines) U_{DS} and I_D waveforms under different V_{DC} during short-circuit pulse with a duration of 10 µs.

As provided in Figure 17, The U_{DS} and I_D waveforms are measured when short-circuit failure occurs under long-pulse short-circuit faults. Short-circuit failure occurs at 28.5 µs when V_{DC} = 400 V and at 15.5 µs when V_{DC} = 500 V. The simulated waveforms match the measured results accurately and the short-circuit withstand time of the model perfectly matches that of the experimental results in both working conditions, indicating that the proposed can precisely predict the thermal-runaway failure in SiC MOSFET's short-circuit fault. Analyzing the composition of simulated I_D, compared with I_{MOS}, I_{LEAK} becomes non-negligible, which is the main cause of the thermal-runaway failure. This result can match the short-circuit failure mechanism shown in the physical basis.

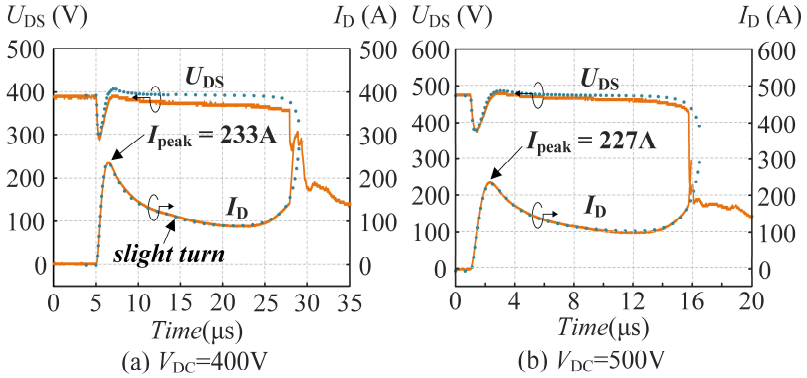


Figure 17. Simulated (orange solid lines) and measured (blue dotted lines) U_{DS} and I_D waveforms when short-circuit failure occurs under long-pulse short-circuit faults and different V_{DC}.

In addition, the proposed model can also reveal the physical mechanisms behind some details of the measured results. In Figure 17a, there is an abnormal slight turn in I_D waveform at the moment $t \approx 13.6$ μs. The proposed model can predict the inconspicuous phenomenon correctly and show the cause of it. The resistances of the N-type drift layer and JFET region increase with the increasing junction temperature, making the channel voltage drop. At the moment $t \approx 8.6$ μs, the channel voltage is so low that the device transitions from the saturation region to the linear region. In the linear region, it is the continuous lowing of the channel voltage that causes the slight drop of I_D.

Figure 18 gives the simulated junction temperature T curves under the above four different working conditions. It is obvious that when the thermal-runaway failure does not occur, T begins to drop after V_{GS} returns to −5 V, but when thermal-runaway failure occurs, T rises faster because of the increasing I_{LEAK}. The positive temperature feedback is obvious in the junction temperature curves when thermal-runaway failure occurs, which proves the thermal-runaway failure mechanisms discussed in Section II.

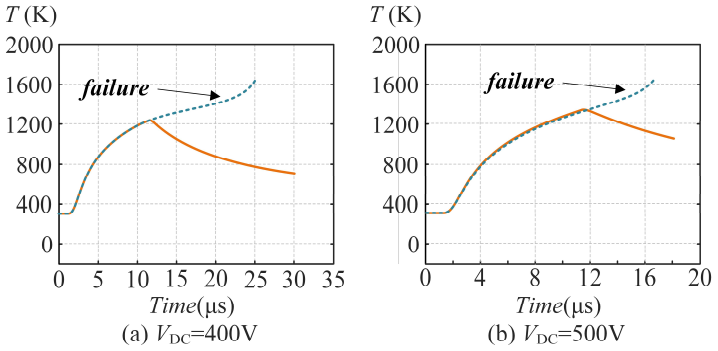


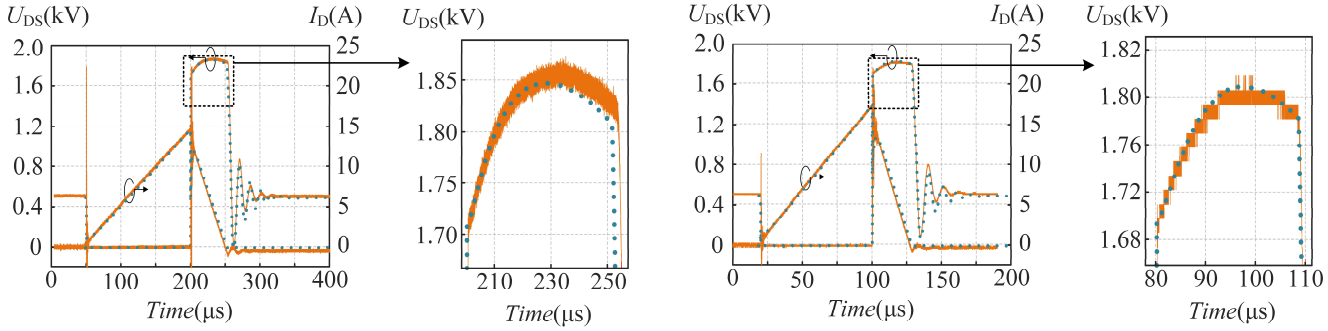
Figure 18. Simulated junction temperature T curves under the above four different working conditions.

5.3. Avalanche Breakdown Faults and Failures

Unclamped inductive switching (UIS) tests were performed to validate the model in avalanche breakdown fault. The schematic circuit diagram used for it can also be described in Figure 14 and the temperature conditions are the same. Compared with the short-circuit test platform, the inductance L here is a large load inductance, and there are several branches for protection between drain and source of the device. These branches can influence the dynamic responses of the device, but they do not change the physical processes of the avalanche breakdown faults in UIS test. Because the structure of these branches is complex, they are omitted in the circuit diagram, but they are carefully taken into consideration in the simulations. Figure 15 also shows the UIS test platform, in which the load is a line-frequency inductor for the UIS test.

Figure 19 displays U_{DS} and I_D waveforms measured in the UIS test under the condition of (a) L = 5.0 mH and the peak current $I_{peak} \approx 14.5$ A and (b) L = 2.3 mH and $I_{peak} \approx 17.1$ A,

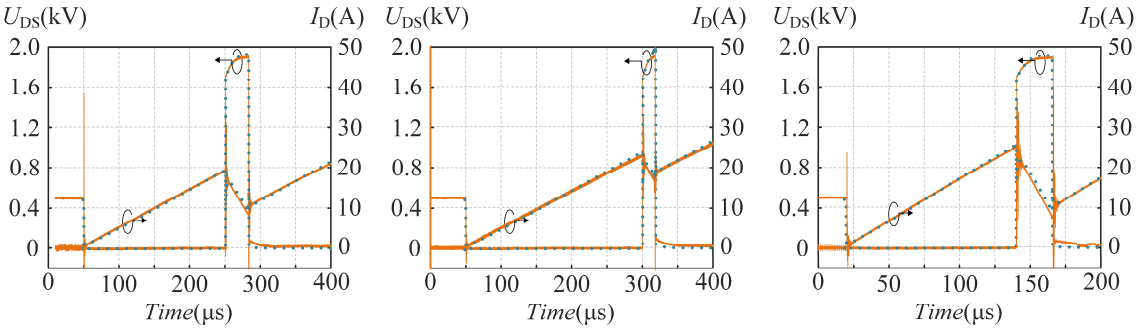
where the avalanche breakdown fault has occurred, but the thermal-runaway failure has not yet occurred. The simulated waveforms show great agreement with the measured results. It validates that the proposed model can correctly describe the working state changes in SiC MOSFET's avalanche breakdown fault, and also implies that the aforementioned cell-level physical processes of avalanche breakdown fault are shown to be correct. When the avalanche breakdown is over, there is an oscillation in U_{DS} waveform, which is mainly caused by the parasitic capacitances of the protection branches between drain and source. They are considered in the simulations, so the simulated and measured results can show a high degree of consistency. It can be seen that during avalanche breakdown, the simulated drain-source voltage U_{DS}, that is, the breakdown voltage U_{BR}, shows excellent agreement with the experimental waveform, which demonstrates that the model selected to calculate the breakdown voltage is accurate in a wide temperature range.



(a) L=5.0mH, I_{peak}≈14.3A (b) L=2.3mH, I_{peak}≈17.1A

Figure 19. Measured (orange solid lines) and simulated (blue dotted lines) U_{DS} and I_D waveforms measured in the UIS test under the condition of (**a**) L = 5.0 mH and the peak current I_{peak} ≈ 14.3 A and (**b**) L = 2.3 mH and I_{peak} ≈ 17.1 A.

As shown in Figure 20, under the condition of (a) L = 5.0 mH and I_{peak} ≈ 19.2 A, (b) L = 5.0 mH and I_{peak} ≈ 24.1 A, and (c) L = 2.3 mH and I_{peak} ≈ 25.1 A, avalanche failure occurs, and when avalanche breakdown is over, I_D does not drop to zero but begins to rise instead. In the proposed model, t_{FD} is set to 4.0μs for describing the undecided failure mechanism that occurs after the melting of source metal. The agreements between simulated and measured results validate that the proposed model can correctly describe the changes in working states during SiC MOSFET's avalanche failure. Table 3 gives the comparisons of the avalanche breakdown durations in three working conditions. The relative errors are very small in these working conditions, which verifies that the proposed model is universal in different conditions. It also suggests that using a short time t_{FD} to describe the undecided failure mechanism is advisable and it does not affect the model's accuracy.



(a) L=5.0mH, I_{peak}≈19.2A (b) L=5.0mH, I_{peak}≈24.1A (c) L=2.3mH, I_{peak}≈25.1A

Figure 20. Measured (orange solid lines) and simulated (blue dotted lines) U_{DS} and I_D waveforms when short-circuit failure occurs under long-pulse short-circuit faults and different V_{DC}.

Table 3. Comparisons of the avalanche breakdown durations.

Working Conditions	Measured	Simulated	Error
L = 5.0 mH, I_{peak} = 19.2 A	32.82 µs	32.75 µs	0.2%
L = 5.0 mH, I_{peak} = 24.1 A	17.47 µs	18.05 µs	3.3%
L = 2.3 mH, I_{peak} = 25.1 A	25.39 µs	25.80 µs	1.7%

Figure 21 provides the simulated curves of junction temperature T in the above four working conditions. It is obvious that when the avalanche breakdown is over, the junction temperature will decrease whether the thermal failure occurs or not. It can be explained as follows. When thermal-runaway failure occurs, the current is concentrated at the hot spots at the active area of a die, which causes junction temperature to rise near hot spots. However, the temperature will decrease in other areas far from the hot spots because the currents flowing through them will decrease. Therefore, the results do not contradict the avalanche breakdown failure mechanisms discussed in Section 2.

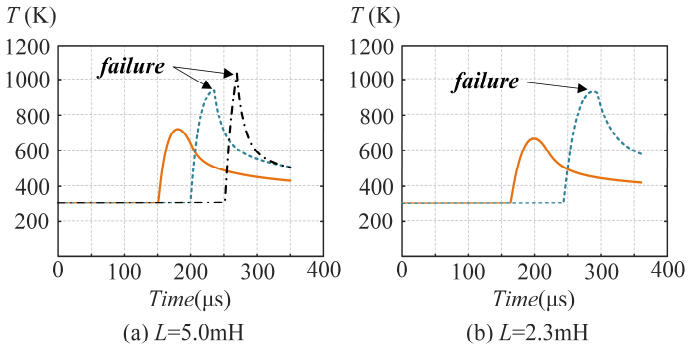


Figure 21. Simulated junction temperature T curves under the above five different working conditions.

In general, the critical avalanche energy E_{AV} is the key parameter to evaluate SiC MOSFET's avalanche ruggedness [15,40]. In our experiments, several DUTs are tested under different L for measuring E_{AV}. Because measured E_{AV} exists in small differences between devices, the average value will be regarded as the reference value here. Table 4 provided the comparisons between measured and simulated E_{AV} under the condition of (a) V_{DC} = 500 V, L = 5.0 mH, and (b) V_{DC} = 500 V, L = 2.3 mH. The relative errors are less than 5%, indicating that the proposed model is able to precisely predict SiC MOSFET's critical avalanche energy.

Table 4. Comparisons between measured and simulated E_{AV}.

Working Conditions	Measured	Simulated	Error
V_{DC} = 500 V, L = 5.0 mH	837.6 mJ	802.9 mJ	4.14%
V_{DC} = 500 V, L = 2.3 mH	727.4 mJ	749.7 mJ	3.06%

6. Conclusions

In this paper, a behavior model of SiC DMOSFET considering thermal-runaway failures in short-circuit and avalanche breakdown faults is presented. It is constructed based on cell-level physical mechanisms demonstrated through finite-element simulation and discussions on the existing studies. The models and parameters used in it are mostly physically based. To validate the proposed model, short-circuit and UIS test experiments are performed. In short-circuit and avalanche breakdown fault simulations, the model can simulate the current and voltage waveforms in different working conditions with extremely high consistency. In short-circuit fault simulation, the results indicate that it can accurately predict the short-circuit withstand time. In avalanche breakdown fault simulation, the model can accurately simulate the avalanche breakdown durations and the

maximum relative error is only 3.3% in the experiments. Moreover, the proposed model can precisely predict the critical avalanche energy, in which the maximum relative error is 4.14%. The results indicate that the proposed model can accurately predict SiC MOSFET's avalanche ruggedness.

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Conflicts of Interest: Authors L.W., W.Z. and Q.Z. were employed by the company Beijing Smart-Chip Microelectronics Technology Co., Ltd. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Appendix A

Table A1. Parameters used in Section 4.

Symbol	Quantity	Value	Symbol	Quantity	Value
C_{ox}	Capacitance of oxide per unit area	8.63×10^{-8} F/cm^2	W_{CELL}	Width of a cell	4.0 μm
L_{CH}	Length of channel	0.5 μm	W_{JFET}	Width of JFET region	0.8 μm
L_{CELL}	Total with of channel considering the number of cells	8.2×10^5 μm	q	Elementary charge	1.602×10^{-19} C
λ	Channel length modulation coefficient	5.44×10^{-5} V^{-1}	k_B	Boltzmann constant	1.38×10^{-23} J/K
C_{GS}	Gate-source, drain-source capacitance	1130 pF	ε_{SiC}	Permittivity of 4H-SiC	8.553×10^{-13} F/cm
C_{r0}	Parameters used for fitting parasitic junction capacitances C_{rss}	381.2 pF	S	Equivalent junction area generating leakage current	0.18 cm^2
V_r	Ditto	19.7 V	τ_g	Carrier lifetime	2.0 ns
M_r	Ditto	0.0084	N_{CH}	Equivalent doping concentration of the channel	8.0×10^{16} cm^{-3}
δ_r	Ditto	872.7 pF	m_e	Electron mass	9.1×10^{-31} kg
γ_r	Ditto	0.1861 V^{-1}	h	Planck constant	6.63×10^{-30} kg·cm^2/s
C_{rssFD}	Ditto	−363.3 pF	n_F	Density of fixed charge at the SiC/SiO_2 interface	1.3×10^{12} cm^{-2}
C_{o0}	Parameters used for fitting parasitic junction capacitances C_{oss}	1747.9 pF	Φ_M	Work function of the poly silicon gate	4.05 eV
V_o	Ditto	2.6 V	χ	Electronic affinity of 4H-SiC	3.60 eV
M_o	Ditto	0.79	μ_{MIN}	Parameters used in μ_B calculation	40
δ_o	Ditto	−91.8 pF	μ_L	Ditto	950

Table A1. *Cont.*

Symbol	Quantity	Value	Symbol	Quantity	Value
γ_o	Ditto	100 V^{-1}	N_{REF}	Ditto	1.94×10^{17} cm^{-3}
C_{ossFD}	Ditto	80.1 pF	K_1	Parameters used in μ_{AC} calculation	1.0×10^6 cm/s
N_{JFET}	Equivalent doping concentration of JFET region	5.0×10^{16} cm^{-3}	K_2	Ditto	3.23×10^6K·cm·s^{-1}·$(V/cm)^{-2/3}$
N_{DR}	Doping of N-type drift layer	9.0×10^{15} cm^{-3}	Γ_{SR}	Parameters used in μ_{SR} calculation	5.82×10^{14} V/s
N_{PWELL}	Equivalent doping of P-well region	1.0×10^{17} cm^{-3}	Γ_{Cit}	Parameters used in μ_{Cit} calculation	2.375 $eV^{-1}cm^{-2}$
H_{JFET}	Height of JFET region	1.0 μm	n_{SCR}	Ditto	1.4×10^{12} cm^{-2}
H_{EPI}	Thickness of epitaxial layer	12.0 μm	ζ_C	Ditto	0.8
H_{DIFF}	Thickness of current diffusion layer	4.0 μm			

Appendix B

The effective perpendicular electric field E_{NOR}, interface inversion charge $Q_{INV,}$ and the interface trapped charge Q_{IT} are critical parameters in the calculation of channel electron mobility. The detailed calculation procedures of them are shown below [22,60,65–68]. The quantities of parameters used in the Appendix are listed in Table A2 and the others not specified here are the same as those in Table A1.

Table A2. Parameters used in Appendix B.

Symbol	Quantity	Symbol	Quantity
N_A	Acceptor impurity doping concentration in the channel	WTA	The temperature-dependent band-tail energy parameter that governs the distribution of the states close to the edge of band
N_D	Donor impurity doping concentration in the channel	$D_{IT,MA}$	Band tails of acceptors distributed in the upper bandgap
E_A	Ionization energy of acceptor impurity	$D_{IT,T0}$	Deep-level trap distribution
E_D	Ionization energy of donor impurity	V_{FB}	Flat band voltage
E_V	Energy level of valence band	γ	Bulk coefficient
E_C	Energy level of conduction band	Φ_F	Fermi potential in the bulk

Q_{INV} and E_{NOR} are calculated by the charge sheet model [60,65]. As shown in (A1), Q_{INV} is a function of surface potential ψ_S and junctions temperature T, where Q_{SC} is space charge and Q_{DEP} is depletion charge.

$$Q_{INV}(\psi_S, T) = Q_{SC} - Q_{DEP} \tag{A1}$$

(A2) defines u_S. Q_{SC} and Q_{DEP} are both functions of u_S.

$$u_S = \frac{\psi_S}{k_B T/q} \tag{A2}$$

Q_{SC} can be expressed by:

$$Q_{SC}(u_S, T) = -c_B L_D \sqrt{2} H(u_S, T) \cdot \frac{v_S}{|v_S|}, \tag{A3}$$

and it can be calculated by (A3)–(A12). c_B is the concentration of free carriers in the bulk considering incomplete ionization:

$$c_B = \frac{2(N_A - N_{DR})}{1 + \alpha N_D + \left[(1 + \alpha N_D)^2 + 4\alpha(N_A - N_D)\right]^{1/2}}, \tag{A4}$$

where the coefficient α is defined as:

$$\alpha = \frac{2}{N_v} \exp\left(\frac{E_A - E_V}{k_B T/q}\right) \tag{A5}$$

L_D represents the Debye length:

$$L_D = \sqrt{\frac{k_B T \varepsilon_{SiC}}{q^2 c_B}} \tag{A6}$$

$H(u_S)$ is defined as (A7):

$$H(u_S, T) = \left\{ \frac{4F_{3/2}[\varpi(V,i) - u_S]}{3\sqrt{\pi}\exp[\varpi(V,i) + |u_B|]} + \frac{4F_{3/2}[\varpi(i,C) + u_S]}{3\sqrt{\pi}\exp[\varpi(i,C) + |u_B|]} + \frac{N_A \ln A}{c_B} + \frac{N_D \ln D}{c_B} - 1 \right\}^{1/2}, \tag{A7}$$

in which $\varpi(j,k) = (E_j - E_k)/k_B T$. A and D are given by:

$$A = \frac{2 + \exp[u_S - \varpi(A,i)]}{2 + \exp[u_B - \varpi(A,i)]} \tag{A8}$$

$$D = \frac{2 + \exp[\varpi(D,i) - u_S]}{2 + \exp[\varpi(D,i) - u_B]}, \tag{A9}$$

where u_B is the reduced Fermi energy in the bulk:

$$u_B = \frac{q}{k_B T}\psi_B = \frac{N_D - N_A}{|N_D - N_A|} \ln\left(\frac{c_B}{n_i}\right) \tag{A10}$$

$F_n[\eta]$ in (A7) represents the Fermi–Dirac integral:

$$F_n[\eta] = \int_0^\infty \frac{x^n}{1 + \exp(x - \eta)}\, dx \tag{A11}$$

v_S in (A3) can be expressed as the following equation:

$$v_S = u_S - u_B \tag{A12}$$

The depletion charge Q_{DEP} is defined as:

$$Q_{DEP}(u_S, T) = -c_B L_D \sqrt{2} H_{DEP}(u_S, T) \cdot \frac{v_S}{|v_S|}, \tag{A13}$$

where $H_{DEP}(u_S)$ is expressed by:

$$H_{DEP}(u_S, T) = \left\{ \frac{N_A \ln A}{c_B} + \frac{N_D \ln D}{c_B} - 1 \right\}^{1/2} \tag{A14}$$

In this way, the effective perpendicular electric field E_{NOR} can be calculated by:

$$E_{NOR}(u_S, T) = \frac{1}{\varepsilon_{SiC}} \left[\frac{1}{2} Q_{INV}(u_S, T) + Q_{DEP}(u_S, T)\right] \tag{A15}$$

n_{INV} in (22) can be expressed by:

$$n_{INV} = -Q_{INV}/q \tag{A16}$$

The interface trapped charge Q_{IT} can be expressed by:

$$Q_{IT}(\psi_S, T) = -q\int_{E_i}^{E_C} D_{IT}(E_t) \cdot f(\psi_S, T) dE_t, \tag{A17}$$

where $D_{IT}(E_t)$ is defined as:

$$D_{IT}(E_t) = D_{IT,TA}(E_t) + D_{IT,TD}(E_t) + D_{IT,MA} + D_{IT,MD} \tag{A18}$$

$D_{IT,TA}$ and $D_{IT,TD}$ characterize the band tails of acceptors and donors in the upper and lower half-gap, respectively. $D_{IT,MA}$ and $D_{IT,MD}$ characterize the distribution of deep-level density of states, assumed to be constant near the mid gap. Because the P-type channel region is considered here, $D_{IT,TD}$ and $D_{IT,MD}$ can be ignored.

In (A17), $f(\psi_S,T)$ is a probability distribution function used to describe the proportion of the interface traps occupied by charges:

$$f(\psi_S, T) = \left[1 + \frac{N_W}{n_i \exp(q\psi_S/k_B T)} \exp\left(\frac{E_t - E_i}{k_B T}\right)\right]^{-1} \tag{A19}$$

Solving (A17)–(A19), Q_{IT} can be expressed by [66]:

$$Q_{IT}(\psi_S, T) = Q_{IT,MA}(\psi_S, T) + Q_{IT,TA}(\psi_S, T), \tag{A20}$$

where $Q_{IT,MA}(\psi_S,T)$ and $Q_{IT,TA}(\psi_S,T)$ can be calculated by the following equations [66]:

$$Q_{IT,MA}(\psi_S, T) = -qD_{IT,MA} \cdot \left\{\frac{E_g}{2} - \frac{k_B T}{q} \ln\left[1 + \frac{N_c N_{CH}}{n_i^2} \exp\left(-\frac{\psi_S}{k_B T/q}\right)\right] + \frac{k_B T}{q}\left[1 + \frac{N_c N_{CH}}{n_i^2} \exp\left(-\frac{0.5E_g + \psi_S}{k_B T/q}\right)\right]\right\} \tag{A21}$$

$$\begin{aligned} Q_{IT,TA}(\psi_S, T) = -qD_{IT,T0} \cdot WTA \cdot \Bigg\{ & 2F1\left[1, \frac{k_B T/q}{WTA}; \frac{k_B T/q + WTA}{WTA}; -\frac{N_c N_{CH}}{n_i^2} \exp\left(-\frac{\psi_S}{k_B T/q}\right)\right] \\ & - \exp\left(\frac{E_V - E_C}{WTA}\right) \cdot 2F1\left[1, \frac{k_B T/q}{WTA}; \frac{k_B T/q + WTA}{WTA}; -\frac{N_c N_{CH}}{n_i^2} \exp\left(-\frac{0.5E_g + \psi_S}{k_B T/q}\right)\right]\Bigg\} \end{aligned} \tag{A22}$$

In (A22), $2F1[a, b; c; z]$ is the Gauss hypergeometric function.

By this point, E_{NOR}, Q_{INV}, and Q_{IT} have been expressed to functions of the surface potential ψ_S and junction temperature T. The relationship between ψ_S and gate source voltage U_{GS} can be expressed by [22,66].

References

1. Kimoto, T. Material Science and Device Physics in SiC Technology for High-Voltage Power Devices. *Jpn. J. Appl. Phys.* **2015**, *54*, 040103. [CrossRef]
2. She, X.; Huang, A.Q.; Lucía, Ó.; Ozpineci, B. Review of Silicon Carbide Power Devices and Their Applications. *IEEE Trans. Ind. Electron.* **2017**, *64*, 8193–8205. [CrossRef]
3. Millán, J.; Godignon, P.; Perpiñà, X.; Pérez-Tomás, A.; Rebollo, J. A Survey of Wide Bandgap Power Semiconductor Devices. *IEEE Trans. Power Electron.* **2014**, *29*, 2155–2163. [CrossRef]
4. Zhao, T.; Wang, J.; Huang, A.Q.; Agarwal, A. Comparisons of SiC MOSFET and Si IGBT Based Motor Drive Systems. In Proceedings of the 2007 IEEE Industry Applications Annual Meeting, New Orleans, LA, USA, 23–27 September 2007; pp. 331–335.
5. Srdic, S.; Liang, X.; Zhang, C.; Yu, W.; Lukic, S. A SiC-Based High-Performance Medium-Voltage Fast Charger for Plug-in Electric Vehicles. In Proceedings of the 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, USA, 18–22 September 2016; pp. 1–6.

6. Ren, N.; Wang, K.L.; Wu, J.; Xu, H.; Sheng, K. Failure Mechanism Analysis of SiC MOSFETs in Unclamped Inductive Switching Conditions. In Proceedings of the 2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD), Shanghai, China, 19–23 May 2019; pp. 183–186.
7. Ceccarelli, L.; Reigosa, P.D.; Iannuzzo, F.; Blaabjerg, F. A Survey of SiC Power MOSFETs Short-Circuit Robustness and Failure Mode Analysis. *Microelectron. Reliab.* **2017**, *76–77*, 272–276. [CrossRef]
8. Li, H.; Zhong, Y.; Wang, S.; Yu, R.; Chen, X.; Yao, R.; Wang, X.; Long, H. Failure Mechanism of SiC MOSFET under Different Avalanche Shocks Mode. *Proc. CSEE* **2019**, *39*, 5595–5603+5887. [CrossRef]
9. Zhao, X.; Li, T.; Liang, X.; Wu, Y.; Li, C.; Zheng, Z. Investigation on SiC MOSFET's Avalanche and Short-Circuit Failure Mechanism. In Proceedings of the 2022 IEEE 5th International Electrical and Energy Conference (CIEEC), Nangjing, China, 27–29 May 2022; pp. 3916–3921.
10. Sun, K.; Wu, H.; Lu, J.; Xing, Y.; Huang, L. Improved Modeling of Medium Voltage SiC MOSFET Within Wide Temperature Range. *IEEE Trans. Power Electron.* **2014**, *29*, 2229–2237. [CrossRef]
11. Mudholkar, M.; Ahmed, S.; Ericson, M.N.; Frank, S.S.; Britton, C.L.; Mantooth, H.A. Datasheet Driven Silicon Carbide Power MOSFET Model. *IEEE Trans. Power Electron.* **2014**, *29*, 2220–2228. [CrossRef]
12. Kraus, R.; Castellazzi, A. A Physics-Based Compact Model of SiC Power MOSFETs. *IEEE Trans. Power Electron.* **2016**, *31*, 5863–5870. [CrossRef]
13. Ji, S.; Zheng, S.; Wang, F.; Tolbert, L.M. Temperature-Dependent Characterization, Modeling, and Switching Speed-Limitation Analysis of Third-Generation 10-kV SiC MOSFET. *IEEE Trans. Power Electron.* **2018**, *33*, 4317–4327. [CrossRef]
14. Duan, Z.; Fan, T.; Wen, X.; Zhang, D. Improved SiC Power MOSFET Model Considering Nonlinear Junction Capacitances. *IEEE Trans. Power Electron.* **2018**, *33*, 2509–2517. [CrossRef]
15. DiMarino, C.; Hull, B. Characterization and Prediction of the Avalanche Performance of 1.2 kV SiC MOSFETs. In Proceedings of the 2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Blacksburg, VA, USA, 2–4 November 2015; pp. 263–267.
16. Ahmed, M.R.; Todd, R.; Forsyth, A.J. Predicting SiC MOSFET Behavior Under Hard-Switching, Soft-Switching, and False Turn-On Conditions. *IEEE Trans. Ind. Electron.* **2017**, *64*, 9001–9011. [CrossRef]
17. Zarebski, J.; Górecki, K. The Electrothermal Large-Signal Model of Power MOS Transistors for SPICE. *IEEE Trans. Power Electron.* **2010**, *25*, 1265–1274. [CrossRef]
18. Li, H.; Wang, Y.; Zhao, X.; Sun, K.; Zhou, Z.; Xu, Y. A Junction Temperature-Based PSpice Short-Circuit Model of SiC MOSFET Considering Leakage Current. In Proceedings of the IECON 2019—45th Annual Conference of the IEEE Industrial Electronics Society, Lisbon, Portugal, 14–17 October 2019; Volume 1, pp. 5095–5100.
19. Xiang, P.; Hao, R.; You, X.; Liu, S.; Jiao, H.; Li, F. Analytical Modeling of SiC MOSFETs Short-Circuit Behavior Considering Parasitic Parameters. In Proceedings of the 2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 11–15 October 2020; pp. 2835–2841.
20. Wang, Z.; Shi, X.; Tolbert, L.M.; Wang, F.; Liang, Z.; Costinett, D.; Blalock, B.J. Temperature-Dependent Short-Circuit Capability of Silicon Carbide Power MOSFETs. *IEEE Trans. Power Electron.* **2016**, *31*, 1555–1566. [CrossRef]
21. Hofstetter, P.; Bakran, M.-M. Predicting Failure of SiC MOSFETs under Short Circuit and Surge Current Conditions with a Single Thermal Model. In Proceedings of the 2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe), Riga, Latvia, 17–21 September 2018; pp. P.1–P.9.
22. Zhou, Y.; Liu, H.; Mu, S.; Chen, Z.; Wang, B. Short-Circuit Failure Model of SiC MOSFET Including the Interface Trapped Charges. *IEEE J. Emerg. Sel. Top. Power Electron.* **2020**, *8*, 90–98. [CrossRef]
23. Riccio, M.; d'Alessandro, V.; Romano, G.; Maresca, L.; Breglio, G.; Irace, A. A Temperature-Dependent SPICE Model of SiC Power MOSFETs for Within and Out-of-SOA Simulations. *IEEE Trans. Power Electron.* **2018**, *33*, 8020–8029. [CrossRef]
24. Lixin, T.; Fei, Y.; Xiping, N.; Yunlai, A.; Wenting, Z.; Rui, L.; Zechen, D.; Junmin, W. Development and Analysis of 6500V SiC Power MOSFET. In Proceedings of the 2021 18th China International Forum on Solid State Lighting & 2021 7th International Forum on Wide Bandgap Semiconductors (SSLChina: IFWS), Shenzhen, China, 6–8 December 2021; pp. 6–9.
25. Unger, C.; Pfost, M. Particularities of the Short-Circuit Operation and Failure Modes of SiC-MOSFETs. *IEEE J. Emerg. Sel. Top. Power Electron.* **2021**, *9*, 6432–6440. [CrossRef]
26. Han, K.; Kanale, A.; Baliga, B.J.; Ballard, B.; Morgan, A.; Hopkins, D.C. New Short Circuit Failure Mechanism for 1.2kV 4H-SiC MOSFETs and JBSFETs. In Proceedings of the 2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Atlanta, GA, USA, 31 October–2 November 2018; pp. 108–113.
27. Jiang, X.; Wang, J.; Lu, J.; Chen, J.; Yang, X.; Li, Z.; Tu, C.; Shen, Z.J. Failure Modes and Mechanism Analysis of SiC MOSFET under Short-Circuit Conditions. *Microelectron. Reliab.* **2018**, *88–90*, 593–597. [CrossRef]
28. Chen, X.; Chen, H.; Shi, B.; Wang, Y.; Li, X.; Zhou, C.; Li, C.; Deng, X.; Luo, H.; Wu, Y.; et al. Investigation on Short-Circuit Characterization and Optimization of 3.3-kV SiC MOSFETs. *IEEE Trans. Electron. Devices* **2021**, *68*, 184–191. [CrossRef]
29. Unger, C.; Pfost, M. Investigation of Gate and Drain Leakage Currents During the Short Circuit of SiC-MOSFETs. In Proceedings of the 2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD), Vienna, Austria, 13–18 September 2020; pp. 238–241.

30. Reigosa, P.D.; Iannuzzo, F.; Ceccarelli, L. Failure Analysis of a Degraded 1.2 kV SiC MOSFET after Short Circuit at High Temperature. In Proceedings of the 2018 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), Singapore, 16–19 July 2018; pp. 1–5.
31. Romano, G.; Maresca, L.; Riccio, M.; d'Alessandro, V.; Breglio, G.; Irace, A.; Fayyaz, A.; Castellazzi, A. Short-Circuit Failure Mechanism of SiC Power MOSFETs. In Proceedings of the 2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD), Hong Kong, China, 10–14 May 2015; pp. 345–348.
32. Riccio, M.; Castellazzi, A.; De Falco, G.; Irace, A. Experimental Analysis of Electro-Thermal Instability in SiC Power MOSFETs. *Microelectron. Reliab.* **2013**, *53*, 1739–1744. [CrossRef]
33. Pulvirenti, M.; Cavallaro, D.; Bentivegna, N.; Cascino, S.; Zanetti, E.; Saggio, M. Thermal Model Development for SiC MOSFETs Robustness Analysis under Repetitive Short Circuit Tests. In Proceedings of the 2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe), Lyon, France, 7–11 September 2020; pp. P.1–P.10.
34. Kakarla, B.; Ziemann, T.; Stark, R.; Natzke, P.; Grossner, U. Short Circuit Ruggedness of New Generation 1.2 kV SiC MOSFETs. In Proceedings of the 2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Atlanta, GA, USA, 31 October 2018–2 November 2018; pp. 118–124.
35. Reigosa, P.D.; Iannuzzo, F.; Ceccarelli, L. Effect of Short-Circuit Stress on the Degradation of the SiO2 Dielectric in SiC Power MOSFETs. *Microelectron. Reliab.* **2018**, *88–90*, 577–583. [CrossRef]
36. Yao, K.; Yano, H.; Tadano, H.; Iwamuro, N. Investigations of SiC MOSFET Short-Circuit Failure Mechanisms Using Electrical, Thermal, and Mechanical Stress Analyses. *IEEE Trans. Electron. Devices* **2020**, *67*, 4328–4334. [CrossRef]
37. Liu, J.; Zhang, G.; Wang, B.; Li, W.; Wang, J. Gate Failure Physics of SiC MOSFETs Under Short-Circuit Stress. *IEEE Electron. Device Lett.* **2020**, *41*, 103–106. [CrossRef]
38. Kelley, M.D.; Pushpakaran, B.N.; Bayne, S.B. Single-Pulse Avalanche Mode Robustness of Commercial 1200 V/80 mΩ SiC MOSFETs. *IEEE Trans. Power Electron.* **2017**, *32*, 6405–6415. [CrossRef]
39. Kimoto, T.; Cooper, J. *Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications*; John Wiley & Sons: Hoboken, NJ, USA, 2014.
40. Fayyaz, A.; Yang, L.; Riccio, M.; Castellazzi, A.; Irace, A. Single Pulse Avalanche Robustness and Repetitive Stress Ageing of SiC Power MOSFETs. *Microelectron. Reliab.* **2014**, *54*, 2185–2190. [CrossRef]
41. An, J.; Namai, M.; Okamoto, D.; Yano, H.; Tadano, H.; Iwamuro, N. Investigation of Maximum Junction Temperature for 4H-SiC MOSFET During Unclamped Inductive Switching Test. *Electron. Commun. Jpn.* **2018**, *101*, 24–31. [CrossRef]
42. Gao, Z.; Cao, L.; Guo, Q.; Sheng, K. Experimental Investigation of the Single Pulse Avalanche Ruggedness of SiC Power MOSFETs. In Proceedings of the 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, 15–19 March 2020; pp. 2601–2604.
43. Liu, S.; Tong, X.; Wei, J.; Sun, W. Single-Pulse Avalanche Failure Investigations of Si-SJ-Mosfet and SiC-Mosfet by Step-Control Infrared Thermography Method. *IEEE Trans. Power Electron.* **2020**, *35*, 5180–5189. [CrossRef]
44. Dchar, I.; Zolkos, M.; Buttay, C.; Morel, H. Robustness of SiC MOSFET under Avalanche Conditions. In Proceedings of the 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, USA, 26–30 March 2017; pp. 2263–2268.
45. Nida, S.; Kakarla, B.; Ziemann, T.; Grossner, U. Analysis of Current Capability of SiC Power MOSFETs Under Avalanche Conditions. *IEEE Trans. Electron. Devices* **2021**, *68*, 4587–4592. [CrossRef]
46. Fayyaz, A.; Romano, G.; Urresti, J.; Riccio, M.; Castellazzi, A.; Irace, A.; Wright, N. A Comprehensive Study on the Avalanche Breakdown Robustness of Silicon Carbide Power MOSFETs. *Energies* **2017**, *10*, 452. [CrossRef]
47. Luo, H.; Zhang, J.; Wu, H.; Zheng, F.; Qian, J.; Chen, X. Reliability and Failure Investigation of SiC MOSFET Under Avalanche. In Proceedings of the 2022 23rd International Conference on Electronic Packaging Technology (ICEPT), Dalian, China, 10–13 August 2022; pp. 1–5.
48. Jiao, Y.; Zhang, J.Q.; Liu, P. Review of Avalanche Tolerance of Silicon Carbide Power MOSFETs. In Proceedings of the 2022 19th China International Forum on Solid State Lighting & 2022 8th International Forum on Wide Bandgap Semiconductors (SSLCHINA: IFWS), Suzhou, China, 7–10 February 2023; pp. 8–12.
49. Yu, R.; Li, H.; Zhong, Y.; Lai, W.; Wang, X.; Yao, R.; Liu, R.; Yu, Y. Improved Temperature Estimation Model of 4H-SiC MOSFET under Avalanche Condition. In Proceedings of the 2020 4th International Conference on HVDC (HVDC), Xi'an, China, 6–9 November 2020; pp. 874–879.
50. Ren, N.; Hu, H.; Wang, K.L.; Zuo, Z.; Li, R.; Sheng, K. Investigation on Single Pulse Avalanche Failure of 900V SiC MOSFETs. In Proceedings of the 2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Chicago, IL, USA, 13–17 May 2018; pp. 431–434.
51. Fayyaz, A.; Castellazzi, A.; Romano, G.; Riccio, M.; Irace, A.; Urresti, J.; Wright, N. UIS Failure Mechanism of SiC Power MOSFETs. In Proceedings of the 2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Fayetteville, AR, USA, 7–9 November 2016; pp. 118–122.
52. Alexakis, P.; Alatise, O.; Hu, J.; Jahdi, S.; Gonzalez, J.O.; Ran, L.; Mawby, P.A. Analysis of Power Device Failure under Avalanche Mode Conduction. In Proceedings of the 2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia), Seoul, Republic of Korea, 1–5 June 2015; pp. 1833–1839.

53. Pala, V.; Hull, B.; Richmond, J.; Butler, P.; Allen, S.; Palmour, J. Methodology to Qualify Silicon Carbide MOSFETs for Single Shot Avalanche Events. In Proceedings of the 2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Blacksburg, VA, USA, 2–4 November 2015; pp. 56–59.
54. Wu, Y.; Li, C.; Zheng, Z.; Wang, L.; Liu, T.; Liu, G. A Behavior Model of Planar SiC MOSFET Considering Avalanche Breakdown. In *ICWPT 2022: The Proceedings of 2022 International Conference on Wireless Power Transfer (ICWPT2022)*; Ma, C., Zhang, Y., Li, S., Zhao, L., Liu, M., Zhang, P., Eds.; Springer Nature: Singapore, 2023; pp. 748–765.
55. Hsu, F.-J.; Hung, C.-C.; Chu, K.-T.; Lee, L.-S.; Lee, C.-Y. A Dynamic Switching Response Improved SPICE Model for SiC MOSFET with Non-Linear Parasitic Capacitance. In Proceedings of the 2020 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia), Suita, Japan, 23–25 September 2020; pp. 1–4.
56. Neamen, D.A. *Semiconductor Physics and Devices: Basic Principles*; Publish House of Electronics Industry: Beijing, China, 2018.
57. Goldberg, Y.; Levinshtein, M.; Rumyantsev, S. *Properties of Advanced Semiconductor Materials: GaN, AIN, InN, BN, SiC, SiGe*; John Wiley & Sons: Hoboken, NJ, USA, 2001; Volume 25.
58. Arnold, E.; Alok, D. Effect of Interface States on Electron Transport in 4H-SiC Inversion Layers. *IEEE Trans. Electron. Devices* **2001**, *48*, 1870–1877. [CrossRef]
59. Masetti, G.; Severi, M.; Solmi, S. Modeling of Carrier Mobility against Carrier Concentration in Arsenic-, Phosphorus-, and Boron-Doped Silicon. *IEEE Trans. Electron. Devices* **1983**, *30*, 764–769. [CrossRef]
60. Pérez-Tomás, A.; Brosselard, P.; Godignon, P.; Millán, J.; Mestres, N.; Jennings, M.R.; Covington, J.A.; Mawby, P.A. Field-Effect Mobility Temperature Modeling of 4H-SiC Metal-Oxide-Semiconductor Transistors. *J. Appl. Phys.* **2006**, *100*, 114508. [CrossRef]
61. Zeng, Y.A.; White, M.H.; Das, M.K. Electron Transport Modeling in the Inversion Layers of 4H and 6H–SiC MOSFETs on Implanted Regions. *Solid-State Electron.* **2005**, *49*, 1017–1028. [CrossRef]
62. Tilak, V.; Matocha, K.; Dunne, G. Electron-Scattering Mechanisms in Heavily Doped Silicon Carbide MOSFET Inversion Layers. *IEEE Trans. Electron. Devices* **2007**, *54*, 2823–2829. [CrossRef]
63. Dhar, S.; Haney, S.; Cheng, L.; Ryu, S.-R.; Agarwal, A.K.; Yu, L.C.; Cheung, K.P. Inversion Layer Carrier Concentration and Mobility in 4H–SiC Metal-Oxide-Semiconductor Field-Effect Transistors. *J. Appl. Phys.* **2010**, *108*, 054509. [CrossRef]
64. Powell, S.K.; Goldsman, N.; McGarrity, J.M.; Bernstein, J.; Scozzie, C.J.; Lelis, A. Physics-Based Numerical Modeling and Characterization of 6H-Silicon-Carbide Metal–Oxide–Semiconductor Field-Effect Transistors. *J. Appl. Phys.* **2002**, *92*, 4053–4061. [CrossRef]
65. Arnold, E. Charge-Sheet Model for Silicon Carbide Inversion Layers. *IEEE Trans. Electron. Devices* **1999**, *46*, 497–503. [CrossRef]
66. Licciardo, G.D.; Di Benedetto, L.; Bellone, S. Modeling of the SiO_2/SiC Interface-Trapped Charge as a Function of the Surface Potential in 4H-SiC Vertical-DMOSFET. *IEEE Trans. Electron. Devices* **2016**, *63*, 1783–1787. [CrossRef]
67. Haasmann, D.; Dimitrijev, S. Energy Position of the Active Near-Interface Traps in Metal–Oxide–Semiconductor Field-Effect Transistors on 4H–SiC. *Appl. Phys. Lett.* **2013**, *103*, 113506. [CrossRef]
68. Potbhare, S.; Goldsman, N.; Lelis, A.; McGarrity, J.M.; McLean, F.B.; Habersat, D. A Physical Model of High Temperature 4H-SiC MOSFETs. *IEEE Trans. Electron. Devices* **2008**, *55*, 2029–2040. [CrossRef]