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Research on Implementation of a PWM Generation Algorithm for Train Stationary Stopping Frequency

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Abstract: In industrial electronic equipment or communication equipment, a reference clock should be generated for stable operation of the equipment, which requires precise and stable reference frequency generation. As a method for generating this reference frequency, an analog method called PLL (phase locked-loop) has been devised and widely used. However, in order to make a more precise and stable reference frequency simple and economical, a DDS (direct digital synthesizer) has been developed. In this paper, we propose a stable and accurate method to generate a low frequency of the PWM method via pure logic circuit configuration without a microprocessor for digital reference frequency generation. Depending on the electronic communication equipment, the required reference frequency varies from a low frequency to a very high frequency. The reference frequency synthesis required in these frequency bands has been studied in various ways, but in industries such as railways, the low-frequency band based on the DDS method is used. In particular, it is very important to operate without a single operating error or failure in order to obtain information for stopping the train. Therefore, it is necessary to design a pure logic method that excludes a stored program type processor that minimizes the possibility of temporary interruption due to disturbance such as surge or high voltage. Therefore, through this study, the algorithm is implemented so that the duty ratio is output at 50:50, the circuit is configured so that two target frequencies are generated at the same time, and the performance is verified by generating the low-frequency band used for stopping the railway train. It was confirmed that the accuracy and stability were improved compared to the analog method used for stopping the railway train, and it was verified that the frequency resolution was superior to the similar results obtained in the digital frequency synthesis field so far.

Keywords: phase locked loop; direct digital synthesizer; hardware description language; pulse width modulation

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1. Introduction

Typically, the frequency used in the train berthing system to judge whether or not a railway train stops at the right position in North America or Europe has been used among low-frequency bands. In this case, the frequency used is composed of a circuit using an analog component such as an inductor. However, due to the characteristics of the frequency-generating device, it is difficult to freely change the frequency or to realize the frequency deviation with a precision of 5% or more. In addition, as the digitalization of the electronic communication system gradually introduces a digital stationary train system, it is necessary to convert the frequency generation to a digital method. For this purpose, digital methods such as DDS have been known to be more suitable for mutual application than analog methods such as PLL. However, as the number of electric trains

used as electric power sources for railway trains has increased, digital frequency generation has also been hampered by disturbances such as high voltage and various surges. In order to solve this problem, it is necessary to synthesize the frequency by means of digital DDS, but it is necessary to utilize a durable method that does not disturb the frequency failure or precision caused by the surrounding environment. In this study, we attempted to verify the performance of the prototype by applying the ultra-precision frequency generation algorithm of the pulse width modulation method, which generates two frequencies simultaneously in the low-frequency band using an FPGA, which is a pure logic device, instead of a program controlled by a program such as a microprocessor. The accuracy of the implemented algorithm and the generated frequency is verified and proven to be superior to the related research.

2. Related Research

2.1. Frequency Generation by PLL Synthesizer

In the block diagram in Figure 1, the RO (reference oscillator) is a crystal oscillator that creates a frequency 1/N times the desired frequency and inputs it into the PD (phase detector), and the output of the VCO (voltage-controlled oscillator) is divided by N into the PD's signal. It generates and outputs a pulse current equal to the phase difference compared with other inputs, and this is input into the pulse-to-voltage converter and converted to voltage through the internal charge pump circuit and low-pass filter. As shown in Figure 2, this voltage is converted into voltage at the VCO. The frequency is determined according to the output. When the PD's average output becomes zero (locked), the VCO's output stabilizes. In other words, a frequency corresponding to N times the PD input is output by a division ratio of N [1,2].

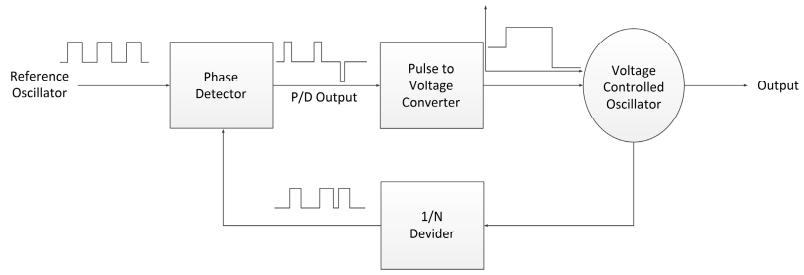


Figure 1. PLL Synthesizer Block Diagram.

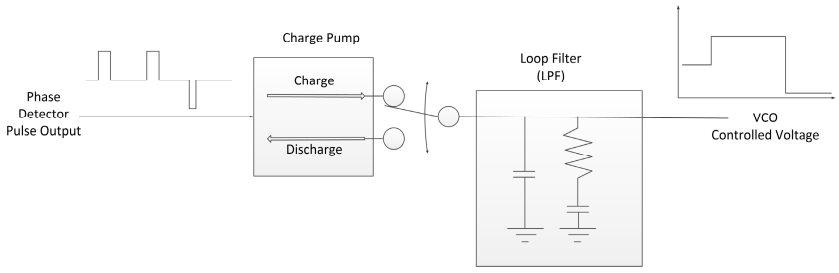


Figure 2. Pulse-to-voltage converter architecture.

K. M. Pisolkar [3] applied PLL technology by creating a low frequency in a PV (photo voltaic) grid-connected system and inputting PV power by synchronizing it with 60 Hz transmitted from a power plant. As shown in Figure 3 below, an oscillator was used to track the frequency and phase of three phases. The frequency of the oscillator was adjusted by the control system to eliminate phase difference. The three-phase input signal abc was converted to a dq0 value by comparing the phase with the exact angular velocity of the oscillator. The signal corresponding to the phase difference between the abc signal and the oscillator rotation frame was filtered into

the averaging block. A PID (proportional integraldifferential) controller maintained the phase difference at 0 according to the controlled oscillator.

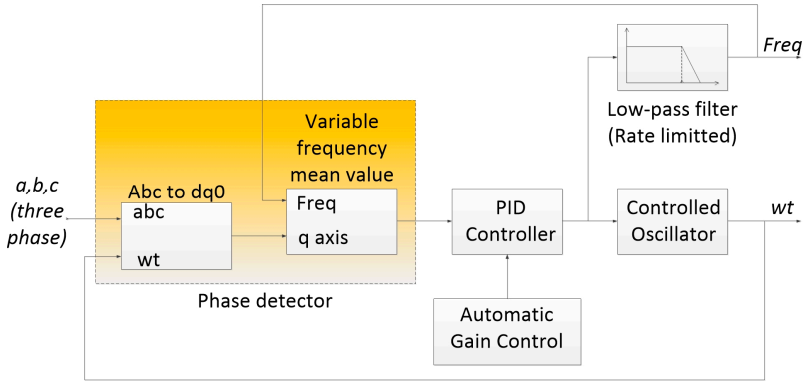


Figure 3. PLL block diagram in 3-phase inverter.

K. Balakier [4] used an optical PLL based on a foundry photonic integrated circuit. Tingbing Ouyang [5] proposed a multi-phase detection method to eliminate spurious noise due to the nonlinearity of the time-to-digital converter and digital-to-time converter in ADPLL (all-digital PLL), and M. Tang [6] proposed a three-phase PLL using feedback RC. Based on the multi-phase clock detection technique, the transfer function was derived by analyzing the multi-phase detection theory in the time domain and the frequency domain. This method significantly removes partial spurious while maintaining adaptability to the frequency variations of the partial spurious. The principle of multi-phase detection is shown in Figure 4. It was assumed that the nonlinearity of the DTC included only the fundamental harmonics and that the oscillator had a differential clock 180° out of phase with CKV and CKV180°. Reference CKR was delayed by DTC until it was aligned with CKV and CKV180°. After the reference clock was delayed, it became CKR1 and CKR2, and the two new difference delays were TDCO/2. When the respective phases were sensed as CKV and CKV180°, the two outputs of the TDC were reversed. Averaging the two outputs eliminated nonlinearity. The average output was as follows:

$$\mathrm{Y(n)} = \frac{1}{2}(X(n) + X(n-1)) \tag{1}$$

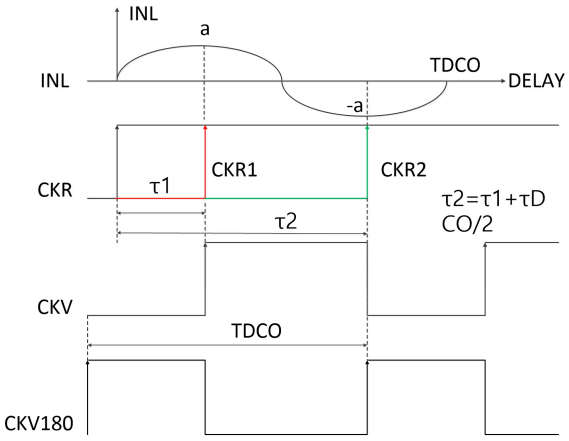


Figure 4. Basic timing diagram of multiphase detection technology.

Also, because this is an FIR (finite impulse response) system, the transfer function in the Z domain was as follows.

$$H(z) = 1/N\left(1 + Z^{-1}\right) \quad (2)$$

In Equation (2), harmonics from the 1st to the N – 1th order can be filtered out. Therefore, we emphasize that even if the frequency of the fractional spurious changes, the filter sampling clock frequency of the intrinsic FIR follows the change in the same way as the FIR filter.

2.2. Frequency Generation by DDS

DDS (direct digital synthesizer) refers to a circuit that uses a single fixed high-speed clock to repeatedly output sinusoidal waveform data, which is a time-varying signal, to a D-A converter and filter it to generate a sinusoidal wave.

Figure 5 shows the configuration of DDS.

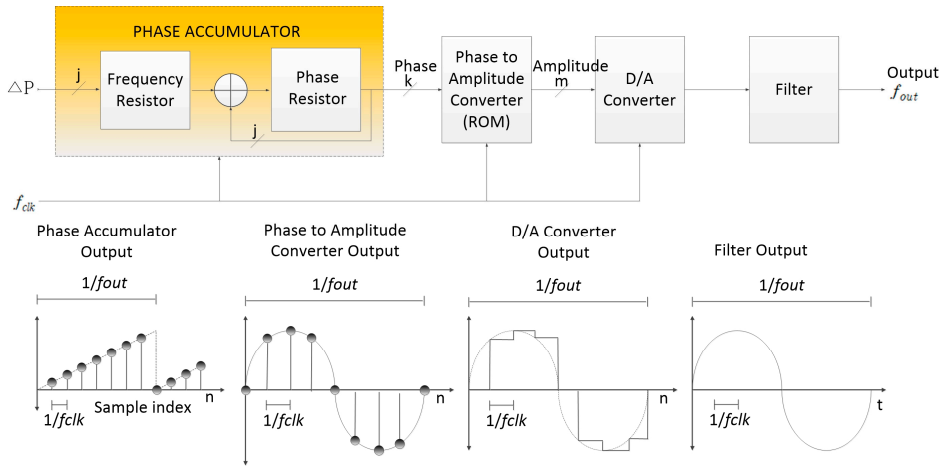


Figure 5. DDS architecture.

The main components of DDS are the phase accumulator, phase-to-amplitude converter (sine lookup table), digital-to-analog converter, and filter. DDS generates a sine wave at a given clock frequency. The frequency depends on three variables: the reference clock frequency, the binary number programmed into the phase register (frequency control word or tuning word), and the length of the n-bit accumulator. J. Tierney [7] and Hemanth Kumar S N [8] implemented the 0 to 150 kHz range in 5 Hz steps using FPGA. Snigdha Madhab Ghosha [9] used this technique for frequency hopping. The binary number in the phase register provides the primary input to the phase accumulator. I. V. Strelnikov [10] implemented DDS using phase-manipulated signals. Han Liu [11] used a 5th-order elliptic function filter to filter the sinusoidal driving signal of DDS to improve the driving performance of a two-dimensional MEMS scanning mirror. When a sine lookup table is used, the phase accumulator calculates the phase address of the lookup table, which outputs a digital value of the amplitude corresponding to the sine of the corresponding phase angle to the DAC. The DAC converts those numbers into corresponding values of analog voltage or current. To generate a fixed-frequency sine wave, a phase increment determined by the binary number M is added to the phase accumulator at each clock cycle. When the phase increment is large, the phase accumulator quickly counts the sine lookup table and generates a high-frequency sine wave. Smaller phase increments cause the phase accumulator to count more slowly, producing a low-frequency sine wave.

The Vedic Multiplier Vedic Synthesizer (VMVS) system proposed by Shanthi K G [12] implements a low-latency technique in DDS connected to the Vedic multiplier output. The heart of the system is a phase accumulator whose contents are updated each clock cycle. Each time the PA is updated, the digital number stored in the phase register is added

to the number in the phase accumulator register. The phase accumulator is updated by 1 each clock cycle. The output of the phase accumulator serves as the address of the phase-to-amplitude converter in the sine lookup table. Muhammad Nadir khan [13] presented a DDFS architecture using a compressed ROM technique.

$$\sin(\alpha + \beta) = \sin\alpha \cos\beta + \cos\alpha \sin\beta \tag{3}$$

In Equation (3), we split the phase into two numbers, α and β, to split the N-bit phase word into $\alpha + \beta + 2$ (MSB), which uses only 2α and 2β ROMs and a single multiplication block to reduce power without compromising spurious results. Methods to reduce consumption were introduced. Ashwitha Baikady [14] designed technologies such as quarter-wave symmetry, memoryless ROM, and the phase accumulator to reduce power consumption and achieve efficient performance in terms of circuit usage area by using the Kogge–Stone adder. Therefore, the lookup table maps the phase of the phase accumulator to the digital word that drives the DAC. For $n = 32$ and M = 1, the phase accumulator passes through each of the 2^{32} outputs in one cycle. The corresponding output frequency is equal to the clock frequency divided by 2^{32}.

M, the digital word of the phase register, is the amount by which the phase accumulator increases with each clock cycle. If f_{clk} is the clock frequency, the output frequency is as follows.

$$f_{out} = M^k \frac{f_{clk}}{2^n} \tag{4}$$

The above equation is the DDS tuning equation. The frequency resolution is as follows.

$$\frac{f_{clk}}{2^n} \tag{5}$$

Hemanth Kumar S N [8] announced that the DDS output frequency was designed in the range of 0 Hz to 150 kHz in 5 Hz increments.

2.3. PWM Output of Frequency Generation Using DDS

When designing an inverter, Liang Yi Yang [15] used technology to output PWM parallel data into serial data using a triangular carrier wave in a DDS configuration, thereby simplifying the circuit by not using a D/A converter, and presented a three-phase SPWM generator for commercial electricity and synchronization [16].

3. PWM-Based Algorithm Design and Generation

In the configuration of DDS, if PWM is implemented by arranging lookup table values in series instead of parallel, the D/A converter can be eliminated, simplifying the circuit and freeing up space for use. With this idea, this study presents an algorithm for generating frequencies using PWM.

3.1. Frequency Generation Using PWM

The logic to generate two frequencies simultaneously creates two circuit blocks using the same logic and outputs them simultaneously. It uses a reference frequency of 2^n, $n = 26$, and a crystal oscillator with a frequency of 67.108864 MHz. It is used as an industrial component (TCXO) and implements a frequency generation algorithm using HDL.

The main hardware configuration is the circuit shown in Figures 6 and 7. The circuit in Figure 6 is the FPGA logic circuit for frequency generation. In the circuit, PWM_OU1, which is the FPGA output, is the PWM output of AA (alignment antenna), PWM_OU2 is the PWM output of 8M (8 m position antenna), and they are 3.3V logic.

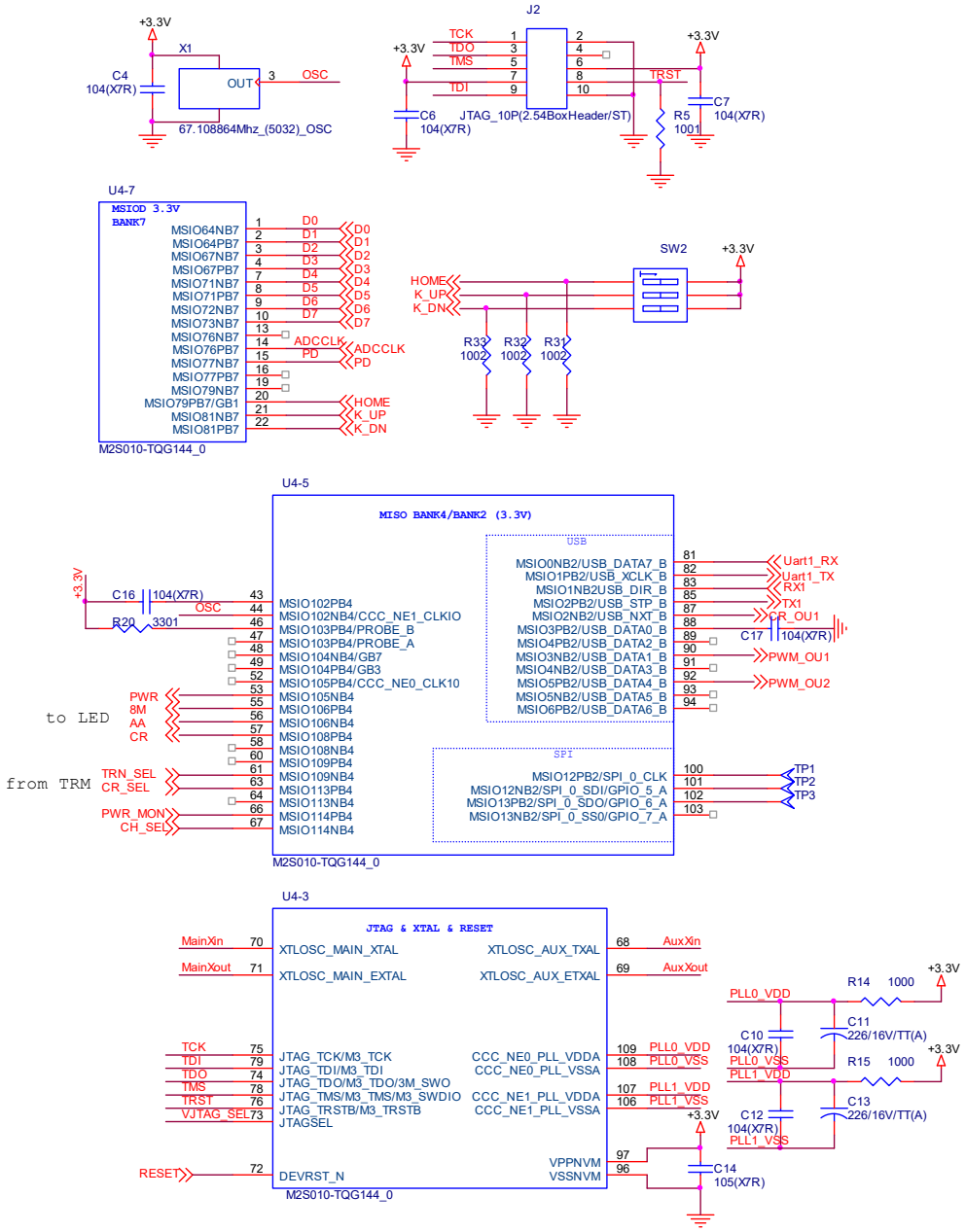


Figure 6. Frequency generator FPGA circuit (PWM_OU1:8M PWM, PWM_OU2:AA PWM).

In the circuit in Figure 7, the PWM input, which is the FPGA output, was used as two inputs with a comparison value of 2.0 V and applied to the 5V comparator circuit. After pulling up the output and performing low-frequency filtering, a sine wave was output. The relationship between R, C, and frequency for filtering was as follows.

$$\omega_c = \frac{1}{RC} \tag{6}$$

Therefore, we configured the circuit by appropriately selecting R and C according to the equation.

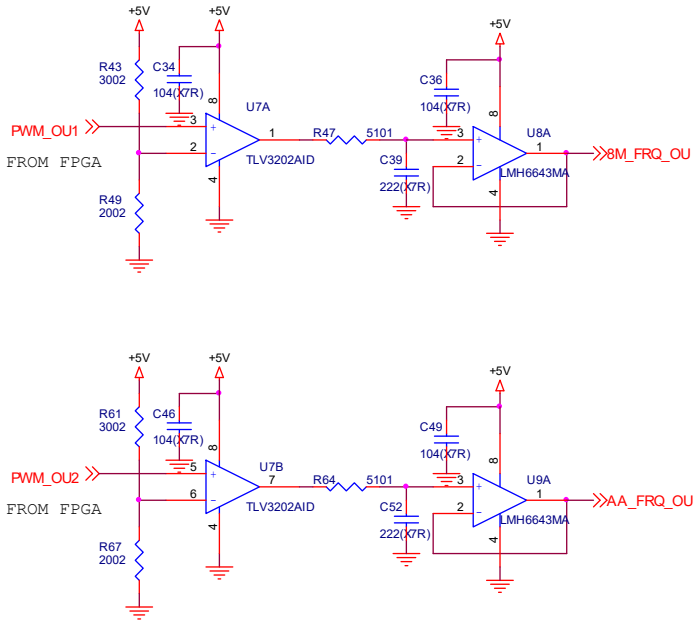


Figure 7. Circuit for PWM input and sine wave output.

3.2. PWM-Based Algorithm Design

The frequency of 67.108864 MHz generated by the crystal oscillator was multiplied by 4 in the internal PLL block of the FPGA to achieve a frequency of 2^n to 268.435456 MHz, where n = 28. If this is expanded and arranged in binary, it becomes a 28-bit array, and the logic corresponding to the frequency is implemented using the following equation.

$$Y = \frac{1}{CK} \times 2^{13} \times 2^{28} \times F_q \tag{7}$$

where:

Y: value for frequency calculation;
CK: 268.435456 MHz clock;
Fq: actual carrier frequency to be used.

3.3. Frequency Generation Implementation

Using Equation (5), we substituted 14,351 Hz and 13,235 Hz into Fq, respectively; expressed the two calculated Y values in binary; and then changed the msb-lsb array to an lsb-msb array. This value was named R_Y. We calculated the Y value by substituting the carrier frequencies of 14.351 kHz, to be transmitted to the 8M antenna, and 13.235 kHz, to be transmitted to the AA antenna, respectively, into Equation (1).

$$Y_{8M} = 16{,}384 \times 14{,}351 = 235{,}126{,}784(\text{dec}) \Rightarrow 1110{,}0000{,}0011{,}1100{,}0000{,}0000{,}0000\ (\text{bin})$$

$$Y_{AA} = 16{,}384 \times 13{,}235 = 216{,}842{,}240(\text{dec}) \Rightarrow 1100{,}1110{,}1100{,}1100{,}0000{,}0000{,}0000\ (\text{bin})$$

To apply this to digital logic, if the binary values of Y_{8M} and Y_{AA} are swapped from msb to lsb, the values are as follows.

$$\text{R_}Y_{8M} \Rightarrow 0000{,}0000{,}0000{,}0011{,}1100{,}0000{,}0111\ (\text{bin})$$

$$\text{R_}Y_{AA} \Rightarrow 0000{,}0000{,}0000{,}0011{,}0011{,}0111{,}0011\ (\text{bin})$$

We created a binary down counter of 2^{28} using the reference clock.

The down-counted value of 2^{28} corresponding to 268.435456 MHz, the inverted value, and the R_Y value were taken as the count enable signal of the algorithm by taking the logic end.

The up-counter was used again to obtain the carrier frequency. In order to increase the accuracy of the output, a 13-bit counter larger than the 8 bits to be used was used to accurately output the upper 7 bits as the bits for generating the final PWM output, and the remaining 6 bits were up-counted using a D-flip-flop circuit.

PWM was implemented using the upper seven bits of this counter output. The PWM conversion lookup table was created using values from Hex 80 to Hex FF for the upper limits of quadrant 1 and 2 based on Hex 80, and values from Hex 00 to Hex 80 for use in the upper limits of quadrant 3 and 4. The PWM algorithm proposed in this paper operates in the following structure: First, since the power source of the FPGA chip used as a logic device uses 3.3 VDC, a logic circuit is constructed so that a sine wave is output around 1.65 VDC. In this case, the frequency, including the PWM signal in the register for generating the frequency, was designed and inputted as 13 bits, and this was set as Ref_Cnt. The upper 6 bits among 13 bits were configured as a lookup table. The upper two bits of these six bits were determined as the 1,2,3,4 quadrants of the Cartesian coordinates, and the remaining four bits were configured as the PWM signal area. Then, if the value X is "80" through the comparator (compA), the duty ratio becomes 50:50. If the value is greater than "80", the duty ratio becomes smaller. If the value is less than "80", the duty ratio becomes larger. The algorithm is designed to operate in a logic structure. The HDL representation of the lookup table used herein is shown in Table 1 (Table_Sel).

Table 1. HDL expressions of PWM look-up table.

```
Entity PWM_8M is
   Port(clr : in std_ logic;
      CLK : in std_logic;
         Ref_Value : in std_logic_vector(12 downto 0);
         PWM_P : out std_logic;
         PWM_N : out std_logic
         )
   Architecture behaves like PWM_8M
signal Table_Sel :std_logic_vector(5 downto 0);
signal Ref_Cnt: std_logic_vector(6 downto 0);
signal compA: std_logic_vectoe(7 downto 0);
signal compB: std_logic_vectoe(6 downto 0);
 begin
Table_Sel <= Ref_Value(12 downto 7);
Ref_Cnt <= Ref_Value(6 downto 7);
compB <= compA(7 downto 1);
process(Table_Sel)
 begin
    if(clr = '0')then compA <= X"80";
    elsif(CLK'event and CLK='1')then
      case Table_Sel is
       when "00" & X"0" => compA <= X"80"; 1 Quadrant-
--Descript from "00" & X"1" to "00" & X"E" by upper method--
   when "00" & X"F" => compA <= X"FE";
   when "01" & X"0" => compA <= X"FF"; 2 Quadrant
--Descript from "01" & X"1" to "01" & X"E" by upper method--
   when "01" & X"F" => compA <= X"8C";
   when "10" & X"0" => compA <= X"80"; 3 Quadrant
--Descript from "10" & X"1" to "10" & X"E" by upper method--
   when "10" & X"F" => compA <= X"02";
   when "11" & X"0" => compA <= X"01"; 4 Quadrant
--Descript from "11" & X"1" to "11 & X"E" by upper method--
   when "11" & X"F" => compA <= X"74";
   when others => compA <= X"80";
 end case;
 end if;
end process;
```

In this way, the tables from the 1st quadrant to the 4th quadrant were sequentially stored in "compA" (8M). Similarly, "compB" (AA) also used the same table values, and the middle table values from X"1" to X"E" were as shown in Table 2 below, written from X"0" to X"F". It was completed by inserting this value in the same format into the middle.

Table 2. Look-up table value.

1Quadrant-80, 8C, 99, A5, B1, BC, C7, D1, DA, E2, EA, F0, F5, FA, FD, FE,
2Quadrant-FF, FE, FD, FA, F5, F0, EA, E2, DA, D1, C7, BC, B1, A5, 99, 8C,
3Quadrant-80, 74, 67, 5B, 4F, 44, 39, 2F, 26, 1E, 16, 10, 0B, 06, 03, 02,
4Quadrant-01, 02, 03, 06, 0B, 10, 16, 1E, 26, 2F, 39, 44, 3F, 5B, 67, 74

The HDL expression of the PWM generation process is shown in Table 3.
Here, the PWM frequency by the table of 2^7 bits becomes X.

$$f_{8M_{PWM}} = 14,351 \times 2^7 = 1,836,928 \text{ Hz} \quad (8)$$

$$f_{AA_{PWM}} = 13,235 \times 2^7 = 1,694,080 \text{ Hz} \quad (9)$$

PWM output is generated when two outputs of '+' and '−' are combined and output.

Table 3. HDL description for PWM output.

```
process(clr, CLK, Ref_Cnt,compA)
begin
if(clr='0') then
            PWM_PO <= '0';
            PWM_NE <= '0';
   elsif(CLK'event and CLK='1')then
         if(Ref_Cnt >= compA)then
               PWM_PO <= '1';
               PWM_NE <= '0';
         else
               PWM_PO <= '0';
               PWM_NE <= '1';
         end if;
      end if;
end process;
```

PWM output is generated by creating two outputs of '+' and '−' and combining them. Like compA, compB is written in the same way to complete the PWM output of the AA frequency. The circuit block that compiles this is shown in Figure 8 below.

The logic of PWM_8M and PWM_AA was also structured in the same format, and the compilation block of PWM_AA was also omitted, as it was similar to PWM_8M. By configuring the PWM logic like this, implementing it on FPGA, compiling and comparing the output waveform in a comparator, converting it to a DC 5V circuit, and passing it through the R-C filter circuit, a sine wave frequency of 8M and AA was output.

In the circuit shown in Figure 7, a PWM signal of 8M frequency generation was output at pin 1 of U7A, and a sine wave of 8M frequency generation was output at pin 1 of U8A. The measured waveforms are shown in Figure 9.

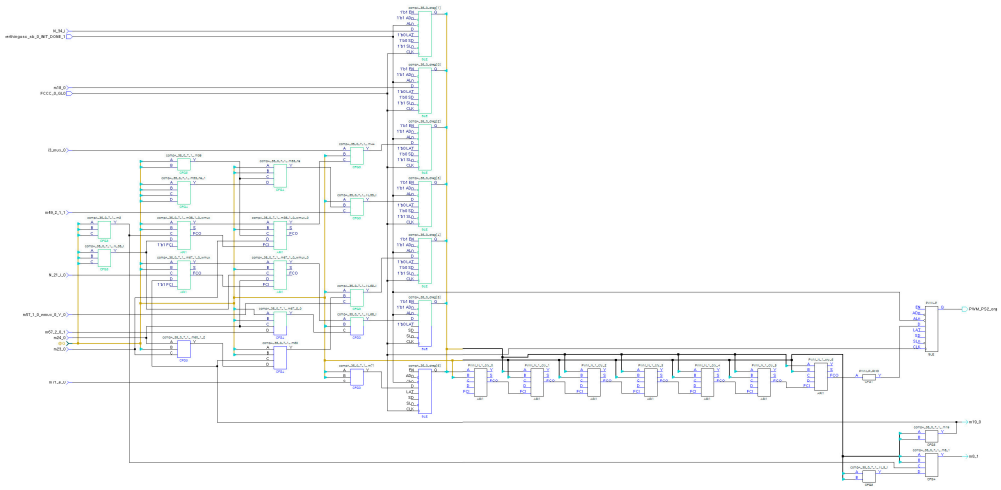


Figure 8. PWM 8M compilation circuit block diagram.

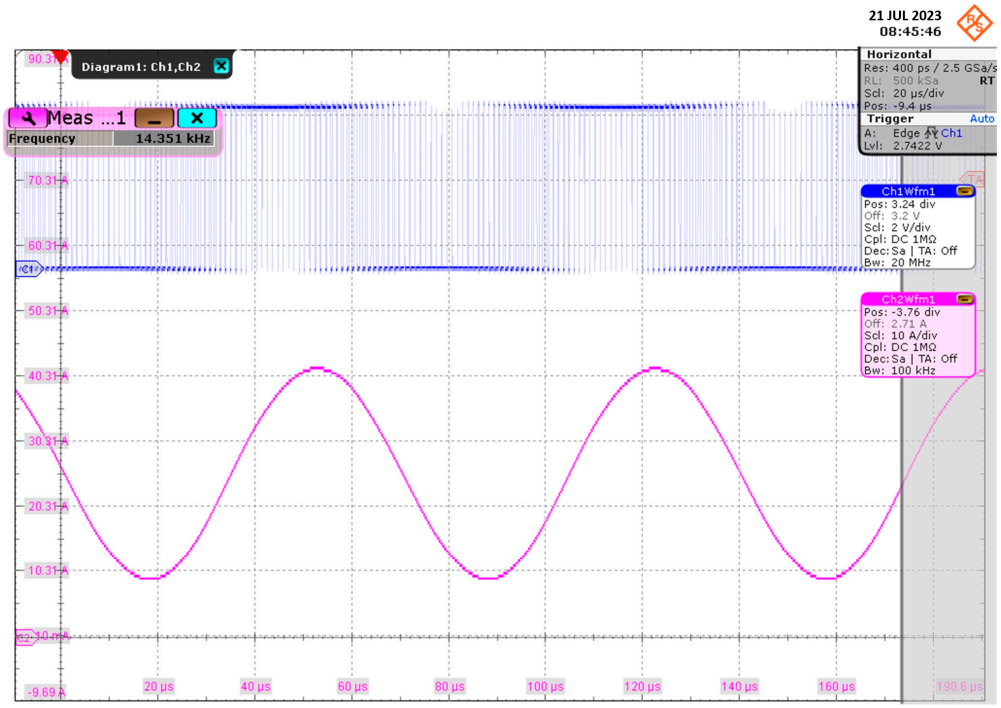


Figure 9. PWM and sine wave measurement waveforms at 8M frequency.

It can be seen that the waveform measurement result is displayed at 14.351 kHz at the top of the left side of Figure 9.

In the circuit shown in Figure 7, the PWM signal of AA frequency was output at the 7th pin of U7B, and the sine wave of AA frequency was output at the 1st pin of U9A. The measured waveform is shown in Figure 10.

It can be seen that the waveform measurement result is displayed at 13.235 kHz at the top of the left side of Figure 10.

Figure 11 shows the oscillator module where the PCB was manufactured using the above circuit and the components were attached. The block A portion of Figure 11 is a circuit diagram of Figure 5, and the block B portion is a circuit diagram of Figure 6.

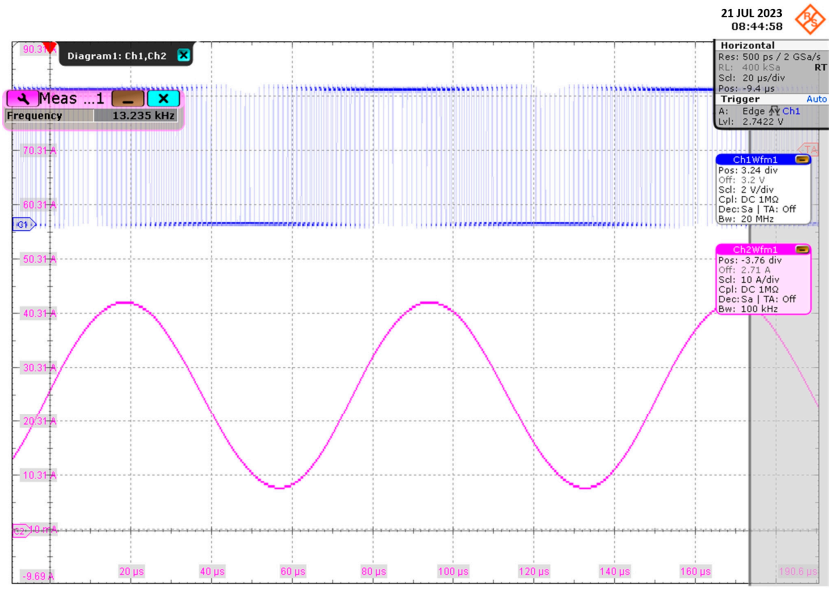


Figure 10. PWM and sine wave measurement waveforms at AA frequency.

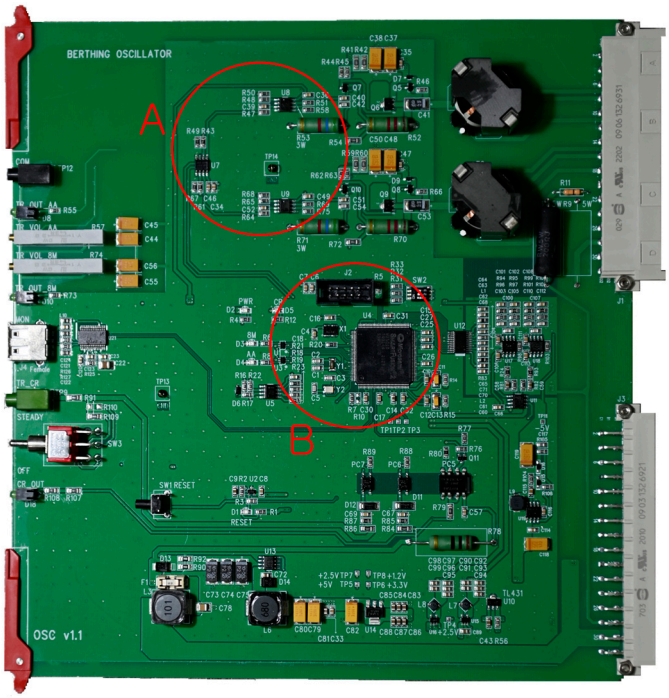


Figure 11. Photo of the manufactured oscillator module.

4. System Design and Fabrication

4.1. Train Stationary Stopping System Design

The system receives a signal (14.351 kHz) from 8M (8M Marker Coil) at a position of 8 m before the train stops at the station, recognizes that it is 8 m before the stop, and then stops at the position of the alignment antenna (AA) after 8 m and receives the signal (13.235 kHz). When the train receives the signal of AA, it transmits a receive acknowledgement signal (21.945 kHz) to AA in response. Therefore, the system can design the transmitter to generate, amplify, and transmit the frequencies to be transmitted to 8M and AA, respectively, and design a receiver to receive the AA confirmation signal.

The configuration diagram of the fixed position stopping system is shown in Figure 12, specifically in the orange-colored area.

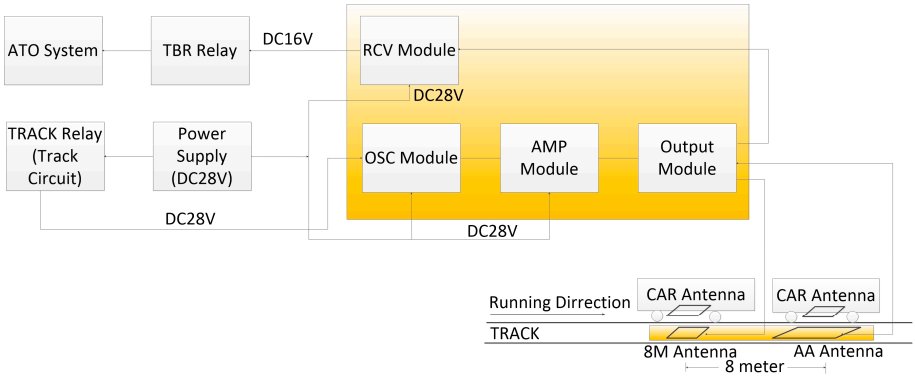


Figure 12. Configuration diagram of fixed-position stopping system.

The specifications were set as follows according to the required functions and performance. The functional requirements are listed in Table 4.

Table 4. Functional requirements.

No.	Item	Function
1	Power supply	DC 28 V 4Amax
2	AA Carrier Transmit Frequency	13.235 kHz
3	AA Carrier Transmit Output	4~10 Vrms, 50 Ω
4	8M Carrier Transmit Frequency	14.351 kHz
5	8M Carrier Transmit Output	4~10 Vrms, 50 Ω
6	AA Confirmation Carrier Transmit Frequency	21.945 kHz
7	AA Confirmation Modulation Transmit Frequency	77 Hz
8	Receiving Relay Coil Spec.	2100 Ω BN Relay

The performance requirements are listed in Table 5.

Table 5. Performance requirements.

No.	Module	Item	Performance
1	Oscillator Module	AA Carrier Transmit Frequency with Tolerance	13.235 kHz ± 5%
		8M Carrier Transmit Frequency with Tolerance	14.351 kHz ± 5%
2	Amplifier Module	Input voltage and impedance	2.76~5.4 Vrms, 1 kΩ
		Output voltage and impedance	11.5~23.4 Vrms, 50 Ω
3	Receive Module	AA Confirmation Carrier Receive Frequency with Tolerance	21.945 kHz ± 5%
		AA Confirmation Modulation Receive Frequency with Tolerance	77 Hz ± 5%
		BN Relay coil Drive Voltage	DC28 V, 2100 Ω

4.2. Design and Fabrication

The design block diagram and main circuit diagram for each module of the device designed according to "Functional requirements" and "Performance requirements", as well as the manufactured PCB and module, were as follows.

4.2.1. Oscillator Module

The design block diagram of the module was as follows, and the internal FPGA part output two types of PWM frequency generation to implement a sine wave with a filter.

The main circuit is shown in Figures 8 and 9, and the manufactured module is shown in Figure 11. The oscillator module in which the PCB was manufactured using the above circuit and to which the component was attached is shown in Figure 13.

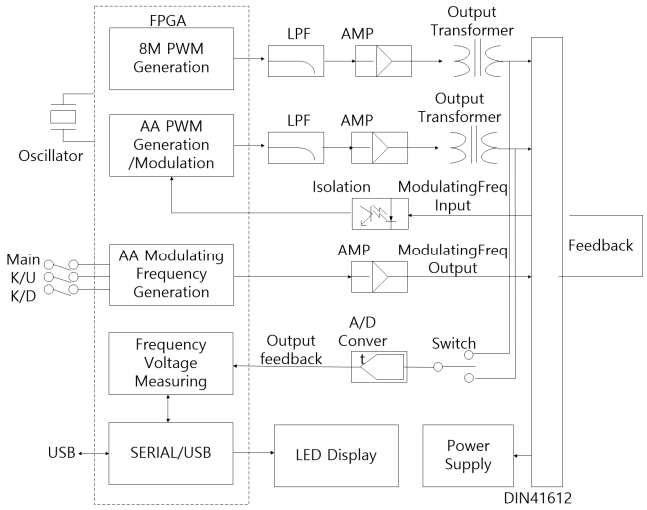


Figure 13. Oscillator module design block diagram.

4.2.2. Amplifier Module

This is a module that amplifies 8M and an AA frequency generated in the oscillator module and transmits them to 8M and AA antennas located at the station. Since the distance between the machine room, where the device is to be installed, and the two antennas is different for each station, the output must be varied, and the variable position must be remembered in order to facilitate the maintenance and management of the device. Therefore, in the amplifier module, the digital input unit is connected to the switch using the D/A converter, and the frequency used is input into the reference voltage terminal to adjust the amplitude to the switch instead of the volume, so that the convenience of maintenance and management is increased.

Oscillator. The adjusted output was filtered through a class D amplifier circuit and output through an output transformer, as shown in Figure 14.

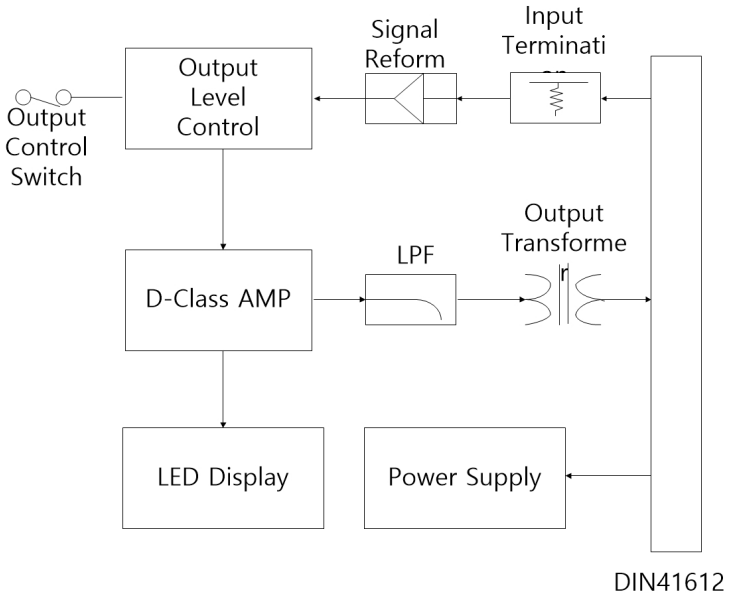


Figure 14. Amplifier module design block diagram.

The main circuit of the designed amplifier is shown in Figure 15.

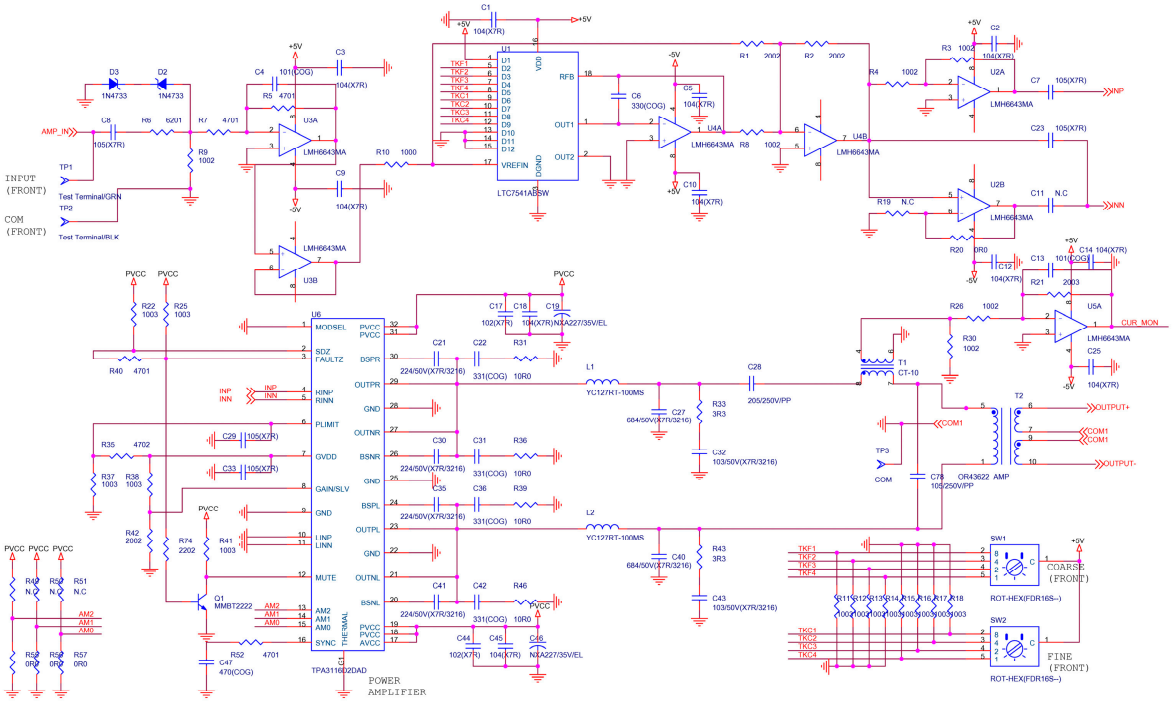


Figure 15. Amplifier module design main circuit.

The manufactured amplifier PCB and module are shown in Figure 16. In Figure 16, Block A is the input control part and B is the D-class power amplifier part.

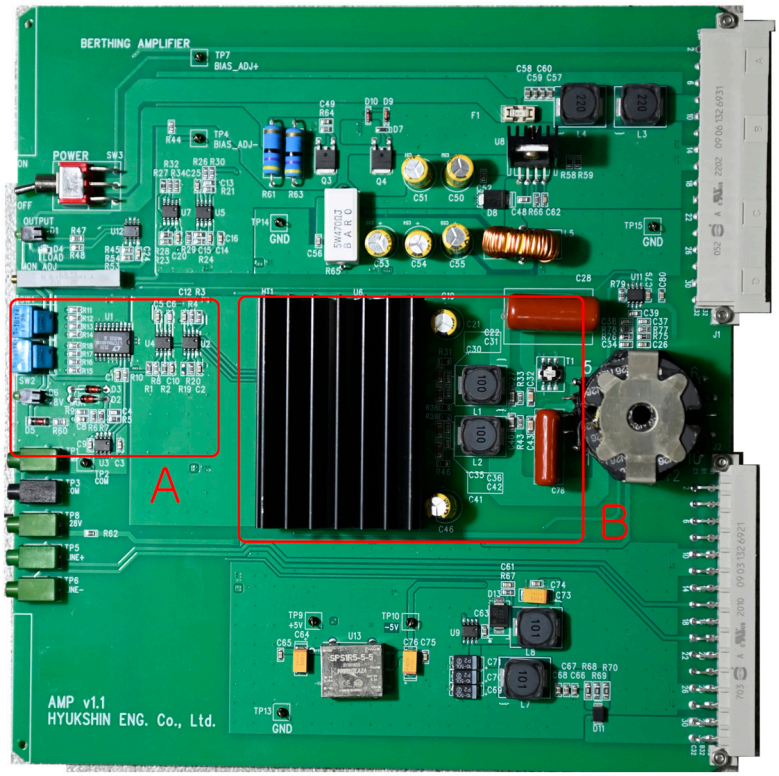


Figure 16. Photo of the manufactured amplifier module.

4.2.3. Receive Module

The transmission signal of 21.945 kHz, which is the acknowledgement signal from the train, is delivered to AA. The received signal is overlapped with the AA transmission signal in the output module, and then input into the receive module.

The design block diagram of the module is shown in Figure 17. The input part was insulated to prevent direct exposure to external electric shock or noise, and a transformer and voltage limiting circuit were configured to prevent direct current or alternating current voltage above a certain voltage from flowing in. After reproducing the carrier frequency with a band-pass filter, it was demodulated, and the signals above the reference value and below the maximum value were compared to determine whether the demodulation was normal in the FPGA again. If it was correct, the frequency for generating the voltage to drive the relay coil was output.

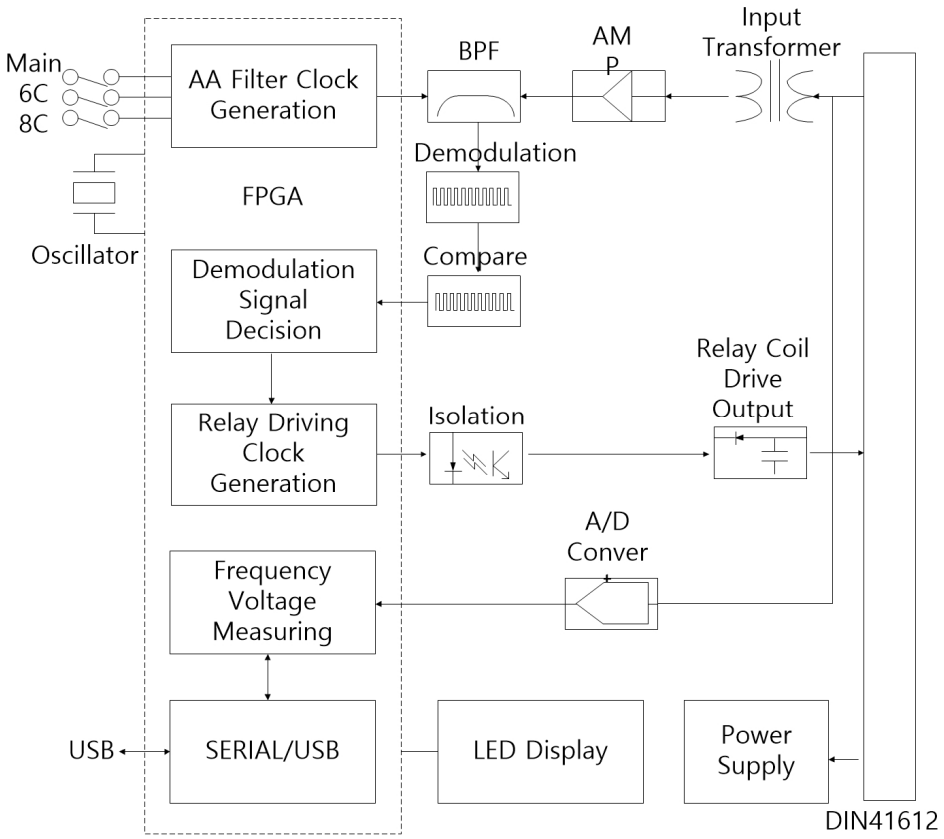


Figure 17. Receive module design block diagram.

The main circuit of the designed receiver is shown in Figure 18.

The red rectangles A, B, C, and D in Figure 19 represent the input control part, the FPGA logic and SCF(switched capacitor filter) clock oscillation part, and the demodulation and signal comparison part.

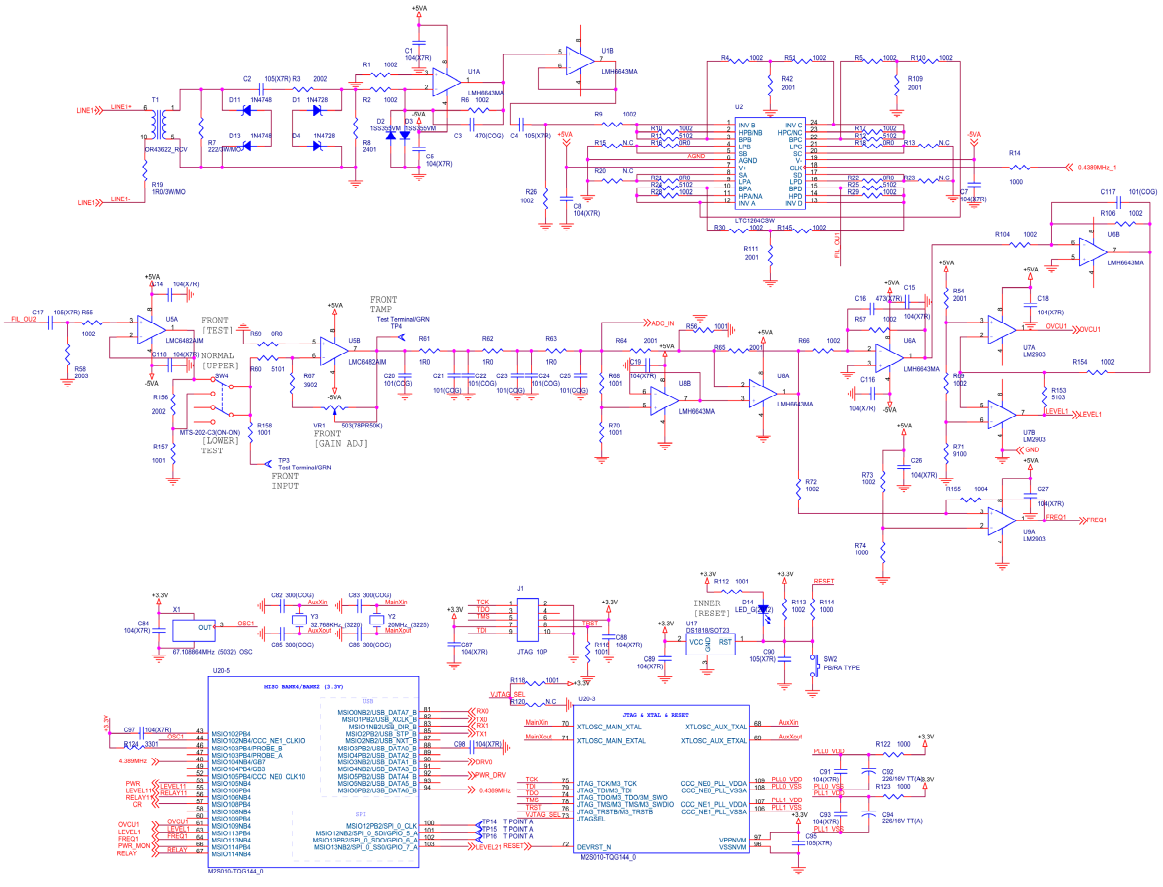


Figure 18. Receive module design main circuit.

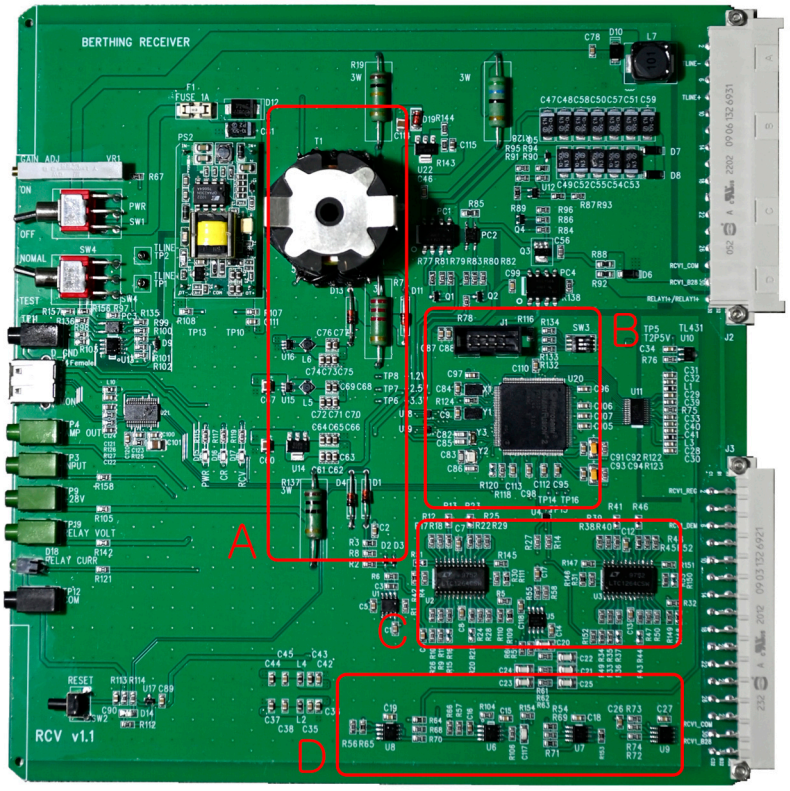


Figure 19. Photo of the manufactured receive module.

4.2.4. Completely Assembled Equipment

Figure 20 shows a system in which each completed module listed above is mounted on a sub-rack. It is a structure in which two systems are mounted on one sub-rack. From the left, the AA amplifier module, 8M amplifier module, oscillator module, and reception module are shown. The red letters A, B, C, and D in Figure 20 represent an AA amplifier module, an 8M amplifier module, an oscillator module, and a receiver module.

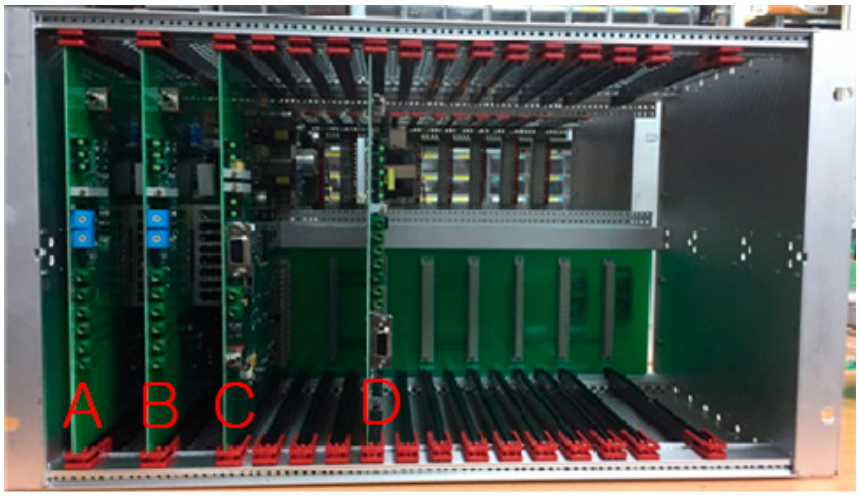


Figure 20. Completed equipment.

5. Experimentation and Verification

5.1. Laboratory Experiment

(1) Oscillator module experiment

The carrier frequencies for 8M and AA were implemented as PWM outputs, and the low-frequency filtered waveforms were measured as exactly 13.235 kHz and 14.351 kHz, respectively, as shown below, all within an error range of 0.1%. The measurement details are shown in Figure 21. A full diagram of the oscillator part in the appendix of this paper is shown in Figure A1.



(a) (b)

Figure 21. Filtered output waveform (**a**,**b**). (**a**) AA carrier frequency of 13.235 kHz is measured. (**b**) 8M carrier frequency of 14.351 kHz is measured.

(2) Amplifier module experiment

The waveform of the signal input from the oscillator module is shown in Figure 22. In the upper left corner of Figure 22, 14.351 kHz and 13.235 kHz are measured.

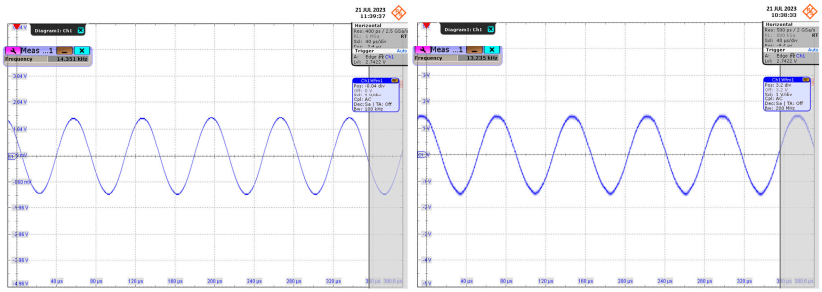


Figure 22. Amplifier input waveforms of 8M and AA signals.

The 8M and AA waveforms, output through the output transformer after the D-class amplifier through the output variable circuit, are shown in Figure 23. In Figure 23, at the upper left, it is shown that the frequency was measured at 14.352 kHz and 13.236 kHz, and the amplitude was measured at 30 Vpp and 28 Vpp.

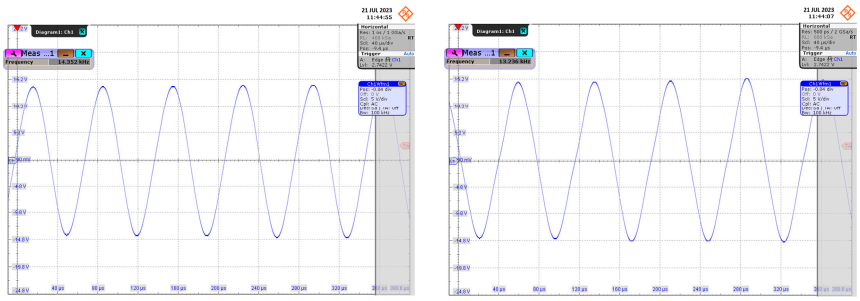


Figure 23. Amplifier output waveforms of 8M and AA signals.

(3) Receive module experiment

The signal that the AA confirmation signal generated on the car, input into the receive module through the AA antenna, was as follows. The AA transmission signal (7~10 Vrms) and the AA confirmation signal (0.2~0.5 Vrms) were overlapped and input into the receiver for isolated reception, then input into the transformer. The superimposed receive input waveform is shown in Figure 24.

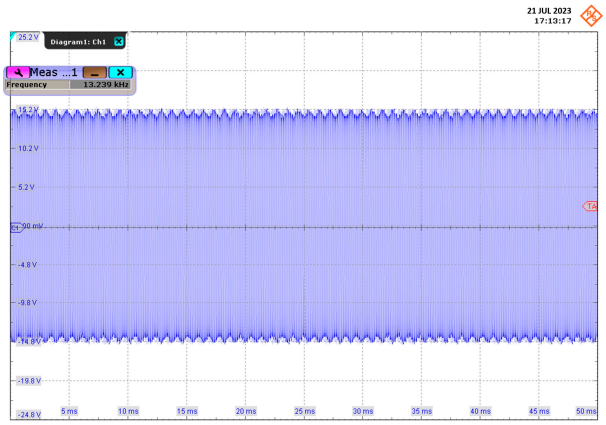


Figure 24. Receive input waveform.

The output of the AA confirmation frequency, filtered using a band pass filter in the receiving module, is shown in Figure 25. As shown in the upper left corner of Figure 25, 21.944 kHz was measured.

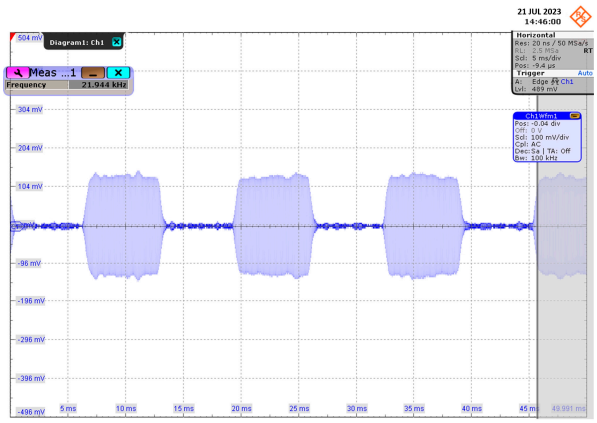


Figure 25. Filtered output waveform.

The waveform output by demodulating the above signal is shown in Figure 26. As shown in the upper left corner of Figure 26, 77.033 Hz was measured.

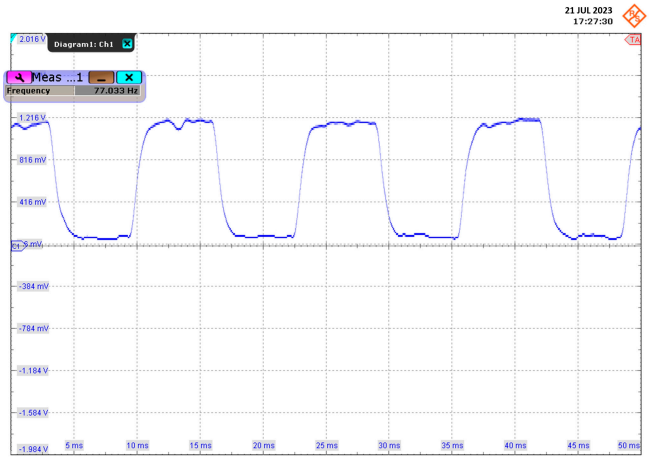


Figure 26. Demodulated AA confirmation output waveform.

The output compared to the normal level after demodulation is shown in Figure 27, and the main line AA confirmation demodulation frequency was measured at 77.00 Hz, within an error range of 0.1%.

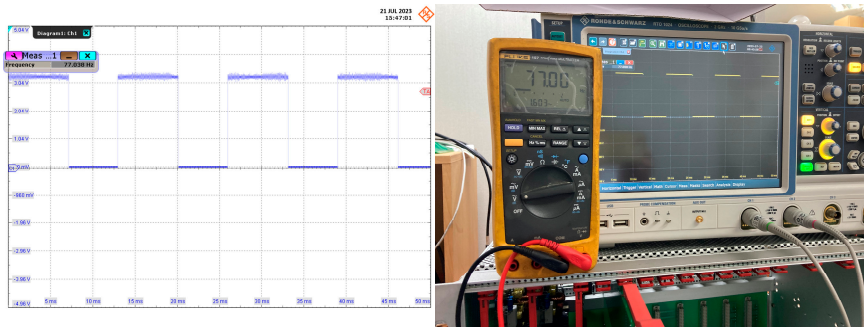


Figure 27. Main line AA confirmation demodulation frequency: 77 Hz.

The determination of a correct signal was implemented with logic to correctly judge whether the demodulation frequency was within 10% of the specified value and whether the duty ratio was within the range of 25 to 75%, taking into account the field situation and the demodulation characteristics of the circuit. In this case, in order to drive the relay

coil, a frequency of about 20 kHz was generated to drive the charge pump circuit, and an output of −28 V DC was made to generate a negative voltage through the rectification and smoothing circuit. The voltage at both ends of the DC24 V relay was −16 V. A resistor was inserted serially to enable DC to alleviate chattering and ensure smooth operation. The purpose of lowering the voltage was to alleviate the chattering that occurs when the relay operates, to ensure smooth operation and to extend the life span.

5.2. Field Experiment

Testing the actual application of a product in the field is more important than anything else. This is because it is an important experiment that allows researchers to determine whether a product can actually be used by directly operating it at the actual use site.

The experiment was first applied to a test ship at the depot, and this lasted for a period of more than 3 months to determine whether the first application would be possible. If it were judged to be in normal operation, the applicability would be tested for a period of more than 6 months using the same method as the main line experiment. Upon performance, the product would be judged to have succeeded, and it would be put into operation on the route.

It was installed on an actual main line and tested for operation. The block mark in Figure 28 denotes a newly designed module that is being experimented with in order to replace existing modules.

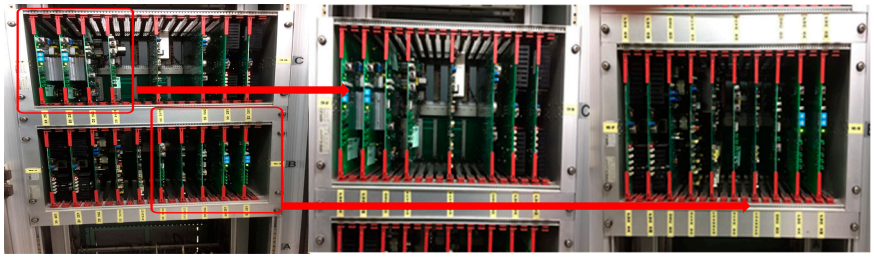


Figure 28. Main line XX station machine room experiment scene.

5.3. Comparison with Related Research and Existing Devices

5.3.1. Comparison with Related Studies

DDS can be implemented from a frequency of 1/2 of the reference clock to a decimal frequency of less than 1 Hz, depending on the number of bits of the PCW, and larger frequencies can be generated using DDS and PLL. In the paper by Hemanth Kumar S N [8], the frequency was generated in 5 Hz units, and the PWM generation logic implemented in this paper can set the frequency in 1 Hz units, as shown in Table 6. The PWM frequency generation method was designed as a method to generate audio frequencies, so they are difficult to compare, but it can be implemented from 1 Hz to 6000 Hz.

Table 6. Composition of PWM research with existing research.

Item	Frequency Generation Range	Frequency Used	FPGA Implementation	Implementation Unit (Hz)	Note
DDS	$1 \sim \frac{f_{clk}}{2}$	Low frequency~High frequency	Some possible	5	[8]
PLL	$2^n f_{clk}$	Low frequency ~ High frequency	Some possible with add component	2	
PWM	$1 \sim \frac{f_{clk}}{12000}$	Audio frequency	All possible	1	

5.3.2. Comparison with Existing Equipment

The existing device was manufactured by Company A and is operating on the city railway. As a result of measuring the frequency precision by replacing the existing device with the newly manufactured device, the existing device showed an error in the range of 0.45 to 0.75%, and the manufactured device showed an error of 0.009%, as shown in Table 7.

Table 7. Comparison measurements with existing equipment compared to target frequency.

No.	Item	Unit	Target Rating	Existing Equipment Measurements	Development Equipment Measurements
Transmitter	8M	kHz	14.351	14.361 (0.69%)	14.351 (0.009%)
	AA	kHz	13.235	13.245 (0.75%)	13.235 (0.009%)
Receive	AA Confirmation	kHz	21.945	21.935 (0.45%)	21.945 (0.009%)

6. Conclusions

A frequency generation algorithm based on PWM was devised and implemented in HDL, and two frequencies were generated simultaneously using the FPGA logic method. In the paper by Hemanth Kumar S N [8], the frequency was generated in 5 Hz units, but it was confirmed that the method using the PWM generation algorithm, which is the focus of this paper, is excellent in terms of performance, achieving frequency setting in 1 Hz unit. The hardware space was reduced by removing the separately configured sine wave generation, D/A converter, and R-C filtering, and the measurement result of the generation frequency was very accurate to within 0.001%. The design method proposed in this paper shows that the design costs are higher than that of the existing method, but the product's cost is lower. If the reliability and accuracy level of the existing method is 5%, that of this method is 0.001%, which is incomparably superior. In addition, the engineering method of the RAMS system was introduced to make it a necessary system in the field, and it was confirmed that the system operated normally until the design, manufacturing, and development experiment; the railway vehicle base experiment; and the railway main line field experiment. Excellent results were confirmed in the cross-comparison test with the existing equipment. In traditional frequency generation, which mainly uses physical devices such as inductors, devices such as inductors and capacitances are bulky and expensive to manufacture if they are to have mechanical durability. As in this study, the digital method incurs development preparation costs such as compilers for initial development, but the production cost is much lower than that of the conventional analog method, and it is economical because it produces stable and reliable products. The PWM implementation algorithm designed and tested in this study is expected to contribute to the development of related technologies if it is applied to fields requiring low-frequency reference frequencies. This study verified its quality and performance, demonstrating that it can be immediately applied in the industrial field.

Author Contributions: Conceptualization, C.P. and E.H.; methodology, E.H.; software, E.H.; validation, C.P. and E.H.; formal analysis, C.P.; investigation, C.P.; resources, C.P.; data curation, C.P.; writing—original draft preparation, C.P.; writing—review and editing, I.K.; visualization, D.S.; supervision, D.S.; project administration, D.S. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: Data are contained within the article.

Conflicts of Interest: Euntaek Han is employed by the Hyukshin Engineering Co., Ltd, Changsik Park is employed by the Juyoung Electronic Co., Ltd. The remaining authors declare that the research

was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Appendix A

In this section, to help readers to understand this thesis, we include a full layout demonstrates the implementation of the design of the oscillator module with the core principles of frequency generation, which is the ultimate goal of this study, as an FPGA.

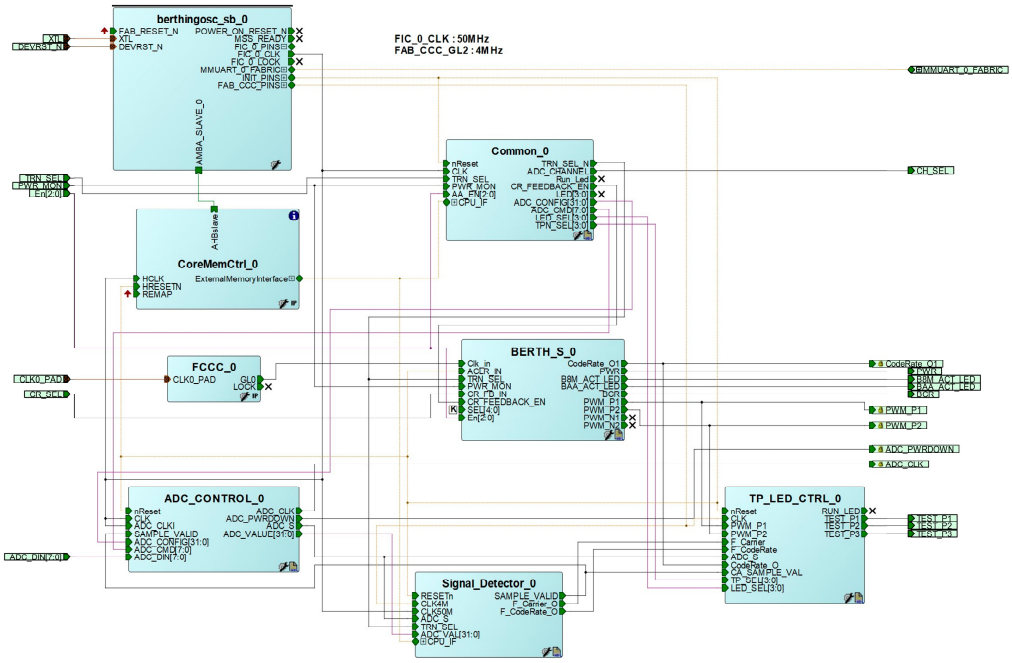


Figure A1. Oscillator module whole diagram.

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