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A High ENOB 14-Bit ADC without Calibration

Costas Laoudias [1,*], George Souliotis [2,*] and Fotis Plessas [3]

[1] Nanozeta Technologies, Larnaca CY-6043, Cyprus
[2] Department of Electrical and Computer Engineering, University of the Peloponnese, 26334 Patras, Greece
[3] Department of Electrical and Computer Engineering, University of Thessaly, 38334 Volos, Greece; fplessas@e-ce.uth.gr
* Correspondence: kostas@nanozetatech.com (C.L.); gsoul@uop.gr (G.S.)

Abstract: This paper presents an implementation of a 14-bit 2.5 MS/s differential Successive-Approximation-Register (SAR) analog-to-digital converter (ADC) to be used for sensing multiple analog input signals. A differential binary-weighted with split capacitance charge-redistribution capacitive digital-to-analog converter (CDAC) utilizing the conventional switching technique is designed, without using any calibration mechanism for fast power-on operation. The CDAC capacitor unit has been optimized for improved linearity without calibration technique. The SAR ADC has a differential input range 3.6 V_{pp}, with a SNDR of 80.45 dB, ENOB of 13.07, SFDR of 87.16 dB and dissipates an average power of 0.8 mW, while operating at 2.5 V/1 V for analog/digital power supply. The INL and DNL is +0.22/−0.34 LSB and +0.42/−0.3 LSB, respectively. A prototype ADC has been fabricated in a conventional CMOS 65 nm technology process.

Keywords: SAR ADC; split capacitor array; differential topology; sample-and-hold circuit; dynamic comparator

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1. Introduction

Analog-to-digital converters (ADCs) are key blocks in many systems that need to acquire analog signals and convert them to a digital form. Typical applications that employ ADCs with a resolution of 12 bits or greater are medical devices, sensor acquisition systems, laboratory equipment, automotive radars, etc. Depending on the application, ADCs with different specifications may be used. Usually, the specifications are defined in terms of resolution, speed, power consumption and accuracy, whereas some of them cannot be satisfied simultaneously and must be compromised.

Other parameters also, affect the final design and the performance of ADC, although they are not taken into account in their evaluation. For example, the maximum input range dictates the design of input stages and a different design approach may be followed depending on it. A higher input voltage range needs circuits with a higher supply voltage, resulting in higher power consumption.

Among others, the Successive Approximation Register (SAR) ADC is a widely used architecture, as it can operate at high speed, with relatively low power [1]. Some additional terms of the performance of an ADC are related to the linearity, expressed as the integral non-linearity (INL), the differential non-linearity (DNL), and the effective number of bits (ENOB) which may be significantly reduced compared with the nominal resolution.

The main building blocks of the SAR ADC are the charge-redistribution capacitive DAC (CDAC), the comparator, and the SAR logic. The CDAC employs a capacitor array based on a capacitor unit. The total number of the capacitor units required in a differential conventional capacitor array is equal to 2×2^N, where N is the number of bits of the ADC. For high N, the exponential increase of the capacitor units results in a large input load capacitance and a layout area, with too many issues due to the insertion of many interconnection parasitic elements. Furthermore, there is a need for high driving capability

of the large CDAC array which increases the power consumption. The split capacitor topology [2,3] can be used to decrease the number of capacitor units to almost $2 \times 2^{1+N/2}$, in cost of linearity. However, the split capacitor should be designed with a fractional value [4–6]. The value of the capacitor unit is also an important trade-off between mismatch, linearity, ENOB, and power. A larger capacitor unit improves the mismatch variations and helps to improve linearity without other calibration schemes [7].

Furthermore, the capacitive DAC for SAR ADC is mostly designed for INL and DNL to be within ± 1 LSB. The INL and DNL directly affect the performance of SAR ADC. The main sources of these errors in the CDAC are the parasitic capacitances, which can be alleviated by increasing the capacitance of the unit capacitor in the CDAC array and also with a proper layout technique. On the other hand, increasing the capacitance of the unit capacitor size increases power consumption and reduces speed.

Another approach to eliminate CDAC nonlinearities is the use of calibration schemes [8–16]. The main drawbacks in calibrating CDAC are the barely higher circuit complexity and most important, the testing cost and time [10]. A mismatch error shaping and analog range compensation method are applied in [17]. However, SAR ADCs with improved performance without calibration have been reported [18,19]. To increase the speed, a combined architecture has been used in [20,21].

In this paper, a 14-bit split-capacitor SAR ADC is presented with a fast settling time, improved ENOB, and high input voltage range. To keep the circuit complexity and the power-on time low, no calibration circuit is employed. To achieve a robust and competitive performance without calibration, various design tradeoffs related to the unit and the split capacitors have been weighed and settled. The value of the unit capacitor has been carefully selected and layout placement considerations have been taken into account for increased linearity. The optimum value of the split capacitor has been determined as it is critical in final DNL and INL values. Two supply domains have been used making the ADC able to accept high input voltage. The input driver and the CDAC operate at 2.5 V, whereas the ADC logic and all the rest circuitry operate at 1 V. Thus, a 3.6 V_{pp} differential input signal can be applied, without the need for voltage scaling which would introduce further non-linearity and dc offset.

In what follows, in Section 2 the SAR ADC architecture is presented evaluating the unit capacitor and the split capacitor sizes, in Section 3 the results are provided and discussed, and in Section 4 the conclusions are presented.

2. SAR ADC Architecture

The SAR ADC operates by using a binary search algorithm to converge to the input signal. A simplified block diagram of a differential 14-bit SAR ADC is shown in Figure 1, where the main components of the core are depicted: (i) a charge-redistribution CDAC comprised of binary-weighted capacitor array and switches, (ii) a comparator that compares the voltages generated from the two DACs, (iii) a SAR logic that controls the DACs, (iv) the internal generation of multiple clocks and phases. The total implementation is shown in Figure 2.

In addition to the aforementioned main functional blocks, the complete system includes some key peripheral blocks which are also very critical for the accurate operation of the ADC. A Sample-and-Hold Amplifier (SHA) is used as an input buffer to realize multiple functions i.e., sufficient driving capability, linearity enhancement, offset cancellation, signal gain, etc. An accurate, low-noise, fast-settling reference voltage is provided by the reference buffer block. Thus, the reference voltage must remain stable and settle to less than 1 LSB resolution, otherwise, linearity degradation and missing code errors will occur. The internal generation of multiple clocks and phases operates in synchronous mode aligned with the external clock (clk), and thus has no impact on the noise of the ADC. Finally, a conventional analog multiplexer block (MUX) is utilized in this 8-channel recording system. At last, the bias currents are provided by the IBIAS block.

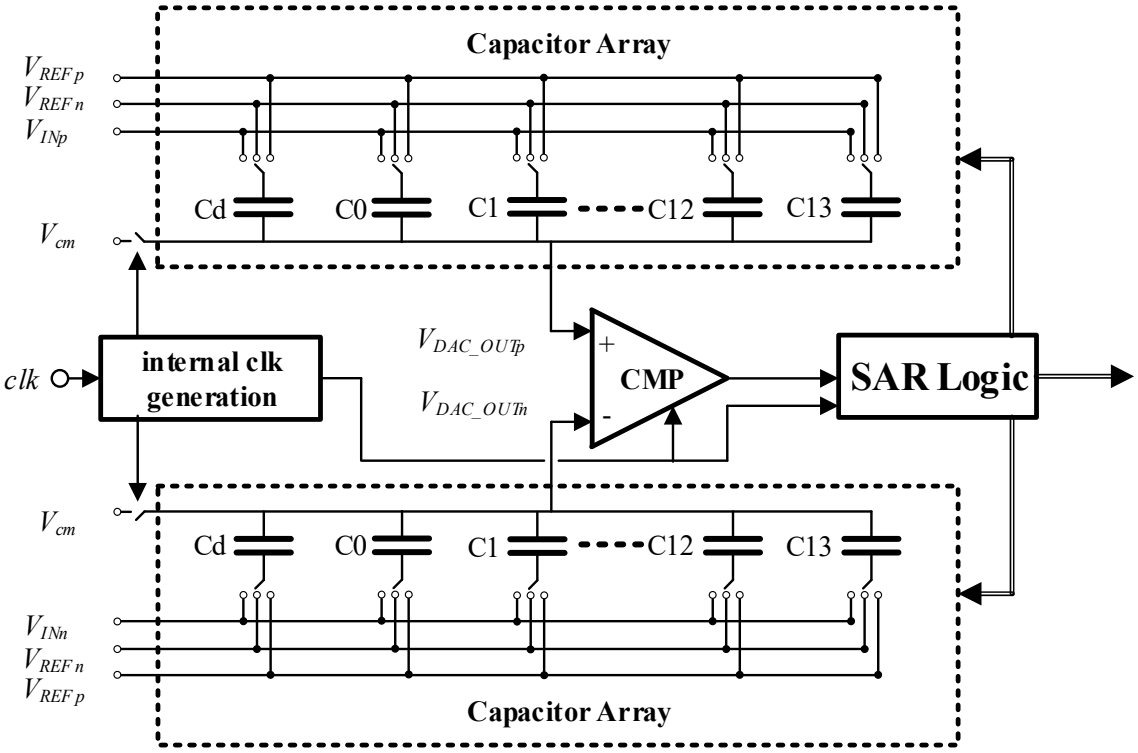


Figure 1. A generic 14-bit SAR ADC block diagram.

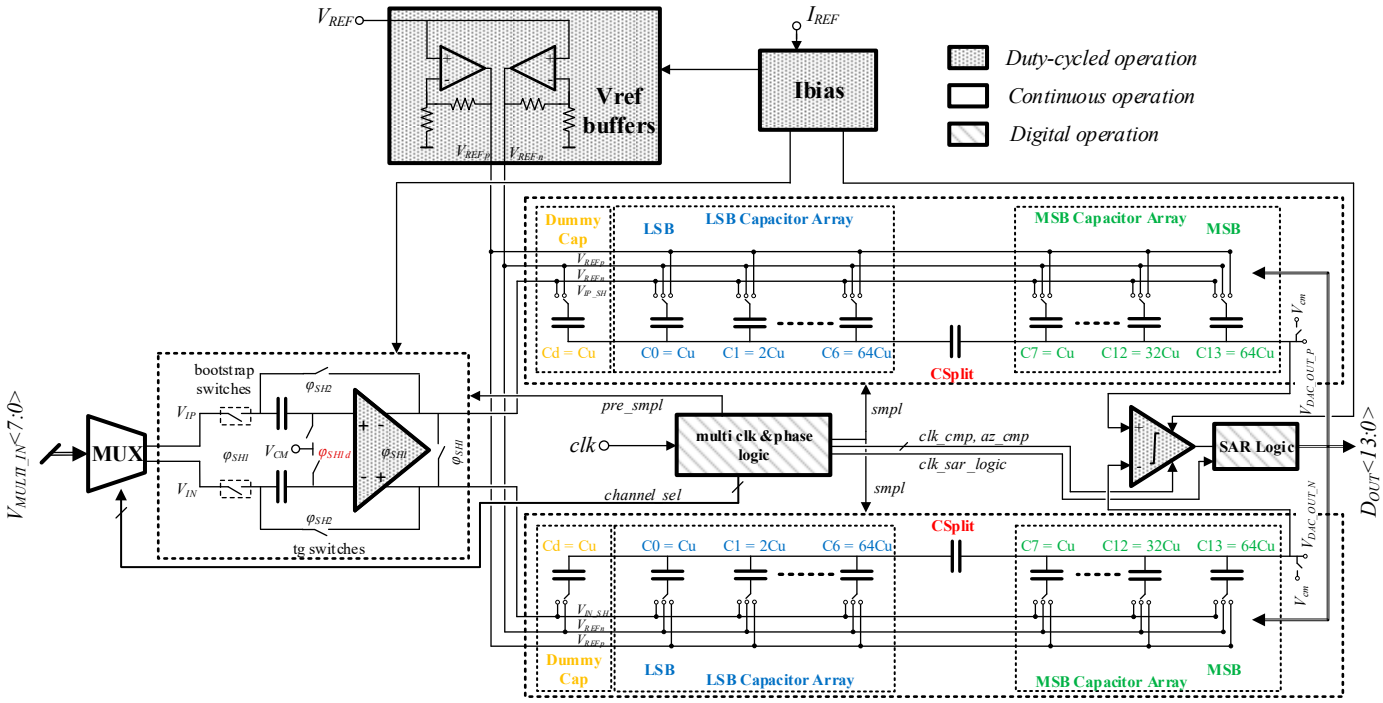


Figure 2. The complete implementation of ADC.

The high differential input voltage of 3.6 V_{pp} requires an increased power supply which results in increased total power consumption. As the digital part of the ADC is designed in standard cell technology, level shifters are required to allow the cross-connections between the voltage domain from 2.5 V to 1 V and vice versa. Due to the employment of level shifters, the dynamic power consumption is increased.

The power consumption of the DAC and the comparator dominates the total power consumption of an ADC. Static power consumption of reference voltage and input signal buffer is comparable to or even higher than the core ADC topology. Thus, to reduce the power consumption of the whole ADC, duty-cycling technique is adopted [19,22,23]. The blocks that are operating in the power-switching regime are remarked in Figure 2.

The input SHA driver needs to provide an accurate replica of the input signal at the end of the tracking phase. Therefore, the driver output is more critical at the sampling phase, whereas it can be powered down during the conversion phase. The sampling phase is equal to 6.25% of the total conversion time. In this implementation, however, a duty cycle of about 10% is adopted to ensure the proper settling of the internal voltages, so that the performance of the ADC is not affected by the power switching. The reference voltage buffer and bias current generator are also duty-cycled, in a similar way.

2.1. ADC Design Considerations

As shown in Figure 1, to maintain the high precision and linearity of the system, a differential architecture is utilized. Differential structures benefit from the improved common-mode rejection, as disturbances from ground, substrate, and reference voltage are seen as common-mode signals, the doubling of the input signal range and the less even-order distortion.

The most common solution for DAC function is the charge-redistribution technique which is implemented by an array of binary-weighted capacitor units. The array is used to sample the input voltage. During the SAR conversion process, by means of the switch array, charge redistribution is taking place to sequentially determine the residue voltages V_{DAC_OUTn} and V_{DAC_OUTp}. The capacitive arrays are identical for both sides and their switching operation is complementary. The upper capacitive DAC samples the positive input signal, whereas the lower capacitive DAC senses the negative input signal.

The conventional bottom-plate sampling scheme is adopted for higher linearity due to its mitigation of charge injection [24,25]. Input signal and reference voltages are connected to bottom plates, whereas top plates are switched on the common-mode voltage V_{cm}.

As shown in the timing diagram in Figure 3, in brief, the operation is the following: during the first two cycles the input signal is pre-sampled and held in SHA (pre-sample). At the next cycle (sample), the bottom plates of all capacitors in the upper and lower capacitive DAC are connected to the input signal provided by SHA, and all the top plates are connected to the common-mode voltage V_{cm}. By the end of the sampling cycle, the top plate switches are open. The next cycle is the first step in the binary search algorithm, where MSB is evaluated by setting the code of SAR logic D_{OUT} < 13:0 > at midcode. In the following 13 cycles, the algorithm continues successively until all the bits are determined. The SAR logic is comprised of a 15-bit shift register and an asynchronous up/down counter reducing the dynamic power consumption [26].

To significantly reduce the area of CDAC, a split capacitor is placed in the middle to divide the capacitor array into the MSB and LSB binary-weighted sub-arrays [2], as shown in Figure 4. For a 14-bit SAR ADC, the conventional binary-weighted DAC array requires 2^{14} C_u, where C_u is the unit capacitance. In the case of a split array, where each sub-array is chosen equal to a 7-bit binary-weighted CDAC, MSB array has $(2^7 - 1)$ C_u, LSB array has 2^7 C_u and the theoretical value of split capacitor is (128/127) C_u.

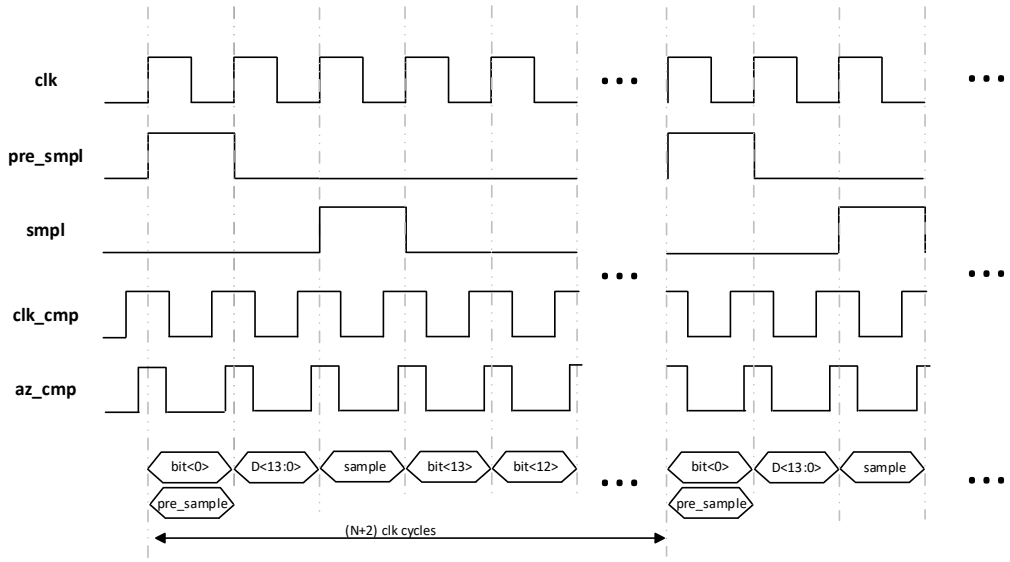


Figure 3. Timing diagram of the critical signals.

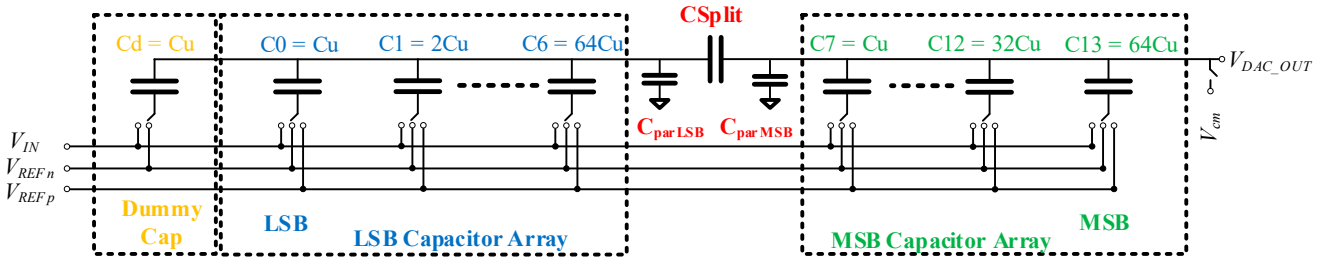


Figure 4. The DAC capacitor array (single-ended).

2.2. Capacitor Unit Value C_u

The value of the capacitor unit C_u is a critical choice for the overall performance of ADC. The capacitor mismatch is minimized by increasing the size of the capacitor [7]; however, this slows down the conversion speed and unfortunately increases the chip area and power. One of the targets in this implementation is the highest ENOB and linearity without the employment of any complicated calibration/redundancy scheme, while the power consumption was on lower priority.

The Equation (1) is providing the Signal-to-Noise-and-Distortion ratio (SNDR) for the most dominant noise contributions in an ADC [27]

$$\text{SNDR} = 10log_{10}\left(\frac{P_{signal}}{P_Q + P_{ji} + P_{kT/C} + P_n + P_{dist}}\right) \quad (1)$$

where P_Q, P_{ji}, $P_{kT/C}$, P_n and P_{dist} are the quantization noise, jitter noise, sampling noise, noise from other blocks and distortion, respectively. SNDR is a good indication of the overall dynamic performance of an ADC and is often converted to ENOB using the relationship for the theoretical SNR of an ideal N-bit ADC, SNR = 6.02N + 1.76 dB, where the equation is solved for N and the value of SNDR is substituted for SNR [27,28],

$$\text{ENOB} = \frac{\text{SNDR} - 1.76\ \text{dB}}{6.02} \quad (2)$$

For an initial estimation of the capacitor unit value, the considerations followed in [1] are also applied in this work, implying that the SNDR should be noise limited and not limited by distortion. The reduction of noise typically requires increased power consumption. For a SAR ADC with very low noise contribution from peripherals (i.e.,

sampling clock jitter, input signal buffer, reference voltage), its noise is dominated by the sampling noise $\overline{v_{n,out}^2} = kT/C_{DAC}$ and the comparator thermal noise, where C_{DAC} is the total capacitance of capacitive DAC array. The jitter noise becomes more dominant in high sampling-rate ADCs since it has a strong dependency on the input signal frequency fin. Therefore, this noise source can be disregarded in this design.

In a 14-bit ADC, a kT/C_{DAC} noise limited SNR is 86.04 dB. With a single-ended input signal of 1.8 V_{pp}, the total sampled noise is $\overline{v_{n,out}^2}$ = 31.73 uV, which results in a total capacitance of C_{DAC} = 4.11 pF, at room temperature of 300K. For this implementation, where the total number of capacitor units in split-array CDAC is about 256, this corresponds to a capacitor unit value of $C_u \approx 16$ fF.

As already mentioned, the linearity of ADC is improved by increasing the value of C_u. This is shown in Figure 5, where simulated ENOB is plotted against values of C_u.

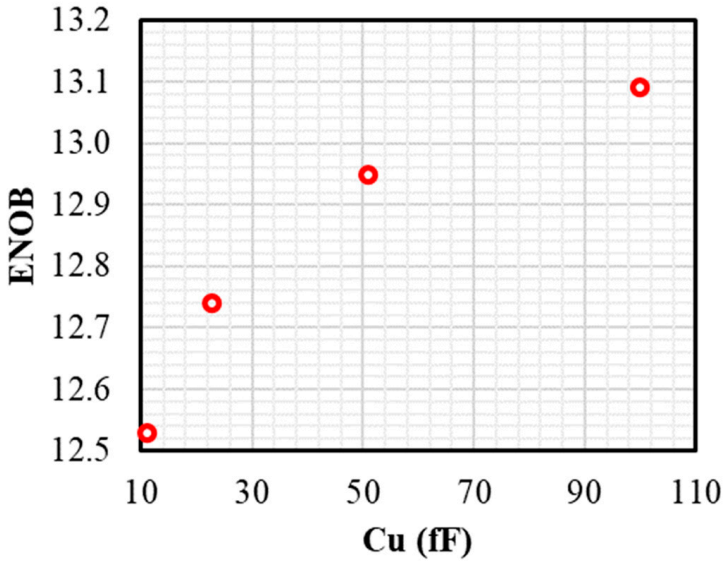


Figure 5. Simulation results of ENOB versus C_u value.

From this plot, it can be concluded that for C_u values larger than 50 fF, ENOB is only improved by about 0.1. Thus, taking into account the results of Figure 5 and the trade-offs between the effective resolution, the power consumption and the area, the unit capacitance C_u has been chosen as a ~50 fF metal-oxide-metal (MOM) capacitor. The capacitor units were built by using only higher metal levels (M4 to M6) to reduce the parasitic capacitance to the ground, at the cost of a greater layout area.

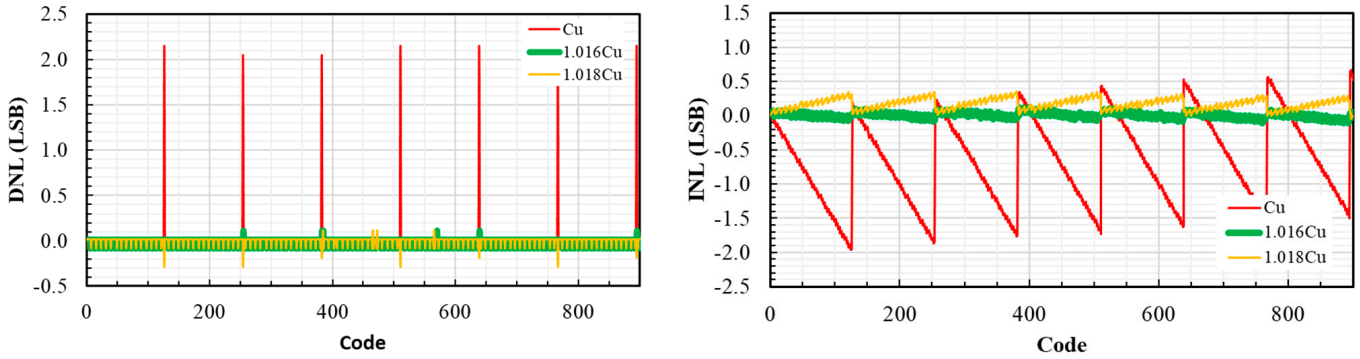
2.3. Split Capacitor Value C_{split}

Another important factor that affects the performance of ADC is the parasitic capacitances in CDAC. Among others, the two most crucial parasitic elements that need to be considered are the top-plate parasitic capacitances of the MSB and LSB sub-arrays, denoted in Figure 4 as $C_{par,MSB}$ and $C_{par,LSB}$, respectively. The parasitic $C_{par,MSB}$ introduces only a gain error, whereas parasitic $C_{par,LSB}$ degrades the linearity since its effect on the V_{DAC_OUT} value is not constant for different input signal levels. Because of the $C_{par,LSB}$, the DNL will have a deterministic pattern at every $2^{N/2}$ codes, where the peak value is approximately given by [29]

$$DNL_{peak} \approx \frac{\left(2^N - 2^{N/2}\right)C_{par,LSB} + C_u}{2^N C_u} \quad (3)$$

In this implementation, N = 14 and $C_u \approx 50$ fF. Also, from layout extraction, the top-plate parasitic capacitance of each unit is found ~0.8fF. Thus, for 127 units in the LSB sub-array the total top-plate parasitic capacitance is $C_{par,LSB} \approx 102$ fF. Applying these

numbers in Equation (3), the DNL_{peak} is around 2 LSB and appears at every 128 codes. This is confirmed by the simulation results shown in Figure 6, for the case of $C_{split} = C_u$. To eliminate this error, the split capacitance C_{split} value is chosen to be different than the theoretical value of (128/127) C_u. As shown in Figure 6, by increasing the C_{split} the DNL peaks are decreasing where the optimum value is $C_{split} \approx 1.016C_u$. For a further increase of C_{split}, the peaks are becoming more negative which again degrades the linearity. The exact theoretical ratio cannot be applied practically, due to the physical constraints, so, a minimum, non-zero DNL, is always expected.



(**a**) (**b**)

Figure 6. Simulation results (**a**) DNL and (**b**) INL for various C_{split} values.

A careful layout methodology in DAC capacitor array has been followed to keep a good linearity. For minimal mismatching effects, the placement of the capacitor units is implemented in a kind of common centroid technique, as shown in Figure 7. The placement shown in Figure 7 was chosen to keep a balance between matching techniques of the capacitor units and connectivity complexity. The capacitor units associated with the least significant bits of MSB and LSB array are placed in the center of each array because they consist of small numbers, and they are more sensitive to mismatches. The capacitor units of the most significant bits of each separate MSB and LSB array are located at the outer place of the layout and surround the rest of the sensitive units. Also, the capacitor units composing the positive and negative arrays associated with the same bits are placed closed in pairs, to minimize mismatches. Finally, the split capacitor units are placed in the center, between the MSB and LSB array.

Other layout considerations have been taken into account to improve the overall performance, in terms of linearity and ENOB. Firstly, the capacitor units have been placed at a certain distance to minimize the parasitic capacitance between each other. Secondly, the levels and the dimensions of the interconnection metal are important, and the suitable selection is taken depending on the number and the distance of the interconnected units. Finally, a shielding consisting of dummy capacitors is applied for the periphery units and a shielding is applied, where possible, for the interconnecting metals. The split capacitor C_{split} can easily fit in the space of one C_u as it is only slightly greater than C_u. So, its specific placement also provides a good matching with the rest of the capacitor units.

# Bit	unit cap representation		# Units
0	0p	0n	1
1	1p	1n	2
2	2p	2n	4
3	3p	3n	8
4	4p	4n	16
5	5p	5n	32
6	6p	6n	64
	Splitp	Splitn	1
7	7p	7n	1
8	8p	8n	2
9	9p	9n	4
10	10p	10n	8
11	11p	11n	16
12	12p	12n	32
13	13p	13n	64
	Sparep	Sparen	4
	Dum		110

(**a**)



(**b**)

Figure 7. Placement of capacitor units in the MSB and LSB array: (**a**) Representation of bits and capacitors; (**b**) The placement of the capacitor units.

2.4. The Comparator

The comparator is the key circuit block that plays a significant role in defining the SAR ADC performance. The requirements of the comparator are speed and accuracy. Comparator offset does not affect overall linearity, as it appears as an offset in the overall transfer characteristic [30]. Offset-cancellation techniques are usually applied to reduce the comparator offset. Noise, however, is a concern, and the comparator is usually designed to have input-referred noise less than 1 LSB [31,32].

Additionally, the comparator needs to resolve voltages within the accuracy of the overall system. For a 14-bit ADC with an input signal within a range up to 3.6 V_{pp}, LSB is about 220 uV.

The architecture selected for the design of the comparator is the combination of three low-gain amplifiers with high BW in cascade as pre-amplifying stages followed by a fast latch comparator stage that uses positive feedback to resolve the final decision. The topology of the comparator is shown in Figure 8. The number of the used stages is a tradeoff between delay, bandwidth, power and input referred offset.

Pairs of offset canceling capacitors are inserted between the three pre-amplifiers. The pre-amplifiers aim to reduce the equivalent offset of the comparator and isolate the latch from DAC to reduce the kickback noise effect.

A simple NMOS differential pair with passive resistors, which has a moderate gain and high bandwidth, is employed as the pre-amplifier, as shown in Figure 8b. Employed in cascade three of them, a high kickback noise isolation together with a high bandwidth are offered. Also, the overall gain allows the signal to reach an adequate level at the input of the dynamic latch comparator and to overcome the possible dc-offset, usually generated by the mismatch. The dynamic latch comparator shown in Figure 8c [28] is employed for the sake of high final gain. This comparator provides a return-to-zero (RTZ) output, as it is reset when *rst* signal is low. As *rst* goes high, the latch begins to regenerate. A final SR latch keeps the output constant over the clock period, eliminating the RTZ operation and driving the output to SAR logic.

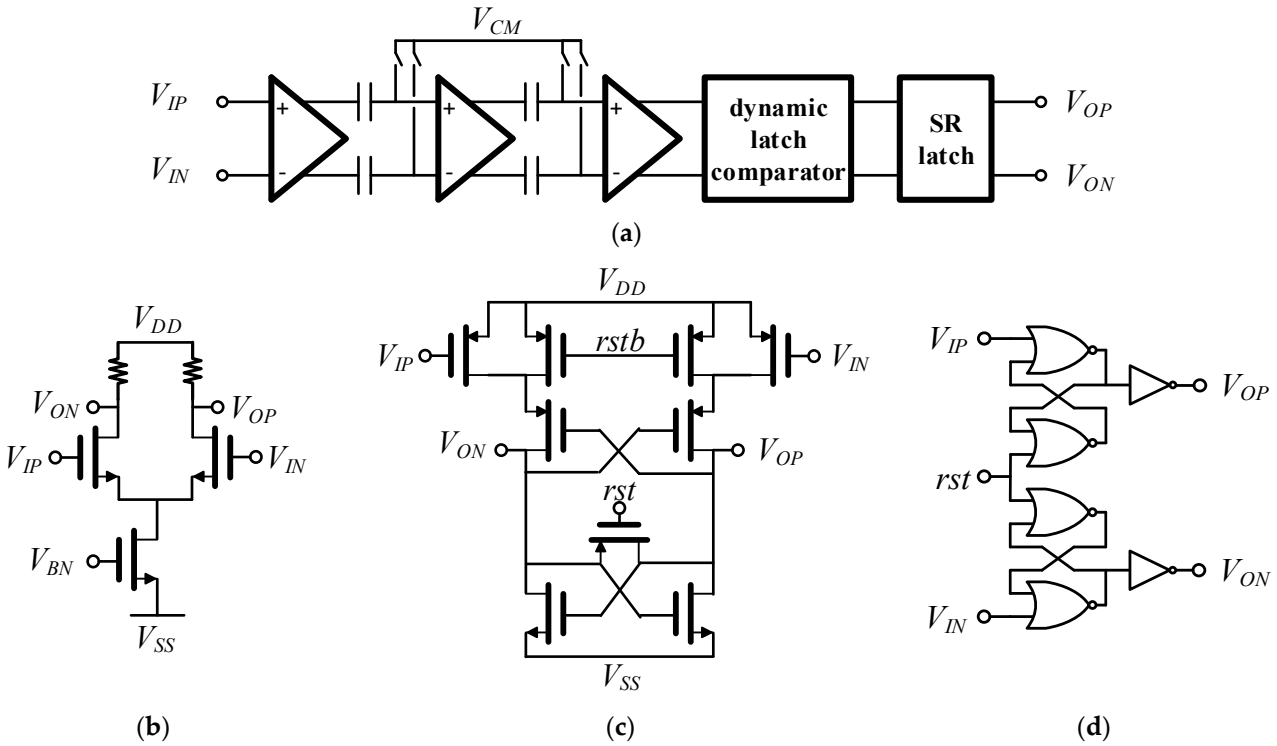


Figure 8. Comparator in SAR ADC: (**a**) three stage preamplifiers and one latch; (**b**) preamplifier stage; (**c**) dynamic latch comparator; (**d**) SR latch.

2.5. The Input Signal Buffer

A Sample-and-Hold Amplifier (SHA) is chosen to drive the input of ADC [33]. The scope of using SHA block as the driving stage is twofold: Firstly, it is used as a buffer to drive properly the input load of SAR ADC. Secondly, it provides an offset cancellation.

The topology used for this purpose is the so-called Flip-Around SHA [34], shown in Figure 9a. This design has the advantages of improved linearity because of the bottom-plate sampling of the input signal and the inherent offset cancellation. It is a non-inverting topology and the amplifier operates in a unity-gain configuration. The design of the amplifier is a two-stage folded-cascode with nmos input differential-pair followed by a simple common-source stage, thus achieving the required open-loop gain and output current driving capability. To further improve the linearity of SAR ADC, bootstrap technique is utilized for the input switches.

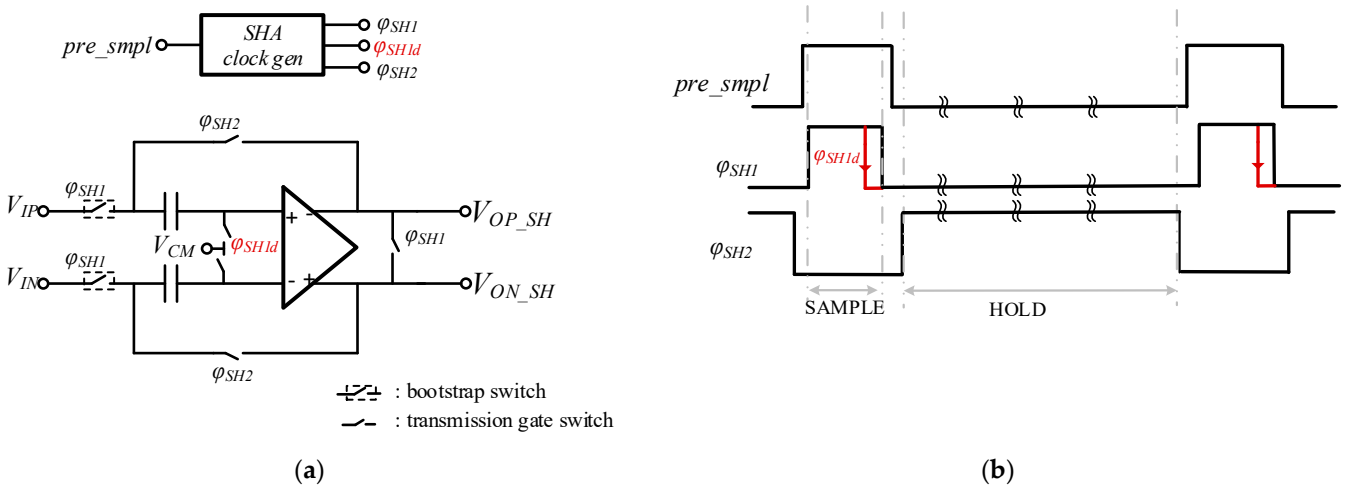


Figure 9. Flip-around SHA: (**a**) topology; (**b**) timing diagram.

Based on the analysis for the calculation of sampling noise presented in Section 2.2, the value of the sampling capacitor inside SHA is selected as 4pF. Thus, the sampling noise introduced by the SHA is negligible. As shown in the time diagram in Figure 9b, during the sampling phase the differential input signal ($V_{IP,N}$) is pre-sampled by the sampling capacitor. During the holding phase, the sampled capacitor is flipped in order to achieve the signal transmission and provide the pre-sample (V_{OP,N_SH}) to the SAR ADC.

3. Simulation Results and Discussion

The ADC has been designed and fabricated in a conventional CMOS 65 nm technology node. The important specs in this ADC were the high linearity and high ENOB. Therefore, two supply voltages have been used, as described in the previous section, one at 2.5 V and one at 1 V. Even though the supply of 2.5 V increases the overall consumption, this is the key point to manage the 3.6 V_{pp} differential input voltage, keeping an improved performance in terms of linearity, ENOB, and accuracy. The 1 V supply voltage was used mainly for the digital circuits and some analog blocks, wherever it was possible, without affecting the ADC performance. A scaling down of the input signal could allow the absence of the 2.5 V domain, but at the same time, it would add more non-linearities and noise to the overall system performance.

The differential input voltage $V_{I,DIFF}$ is depicted in Figure 10a, where the peak-to-peak value is 3.6 V_{pp}. In Figure 10b the levels of the single-ended signals are shown. A common problem in ADCs is the gain error which is usually issued from the rail-to-rail limitations.

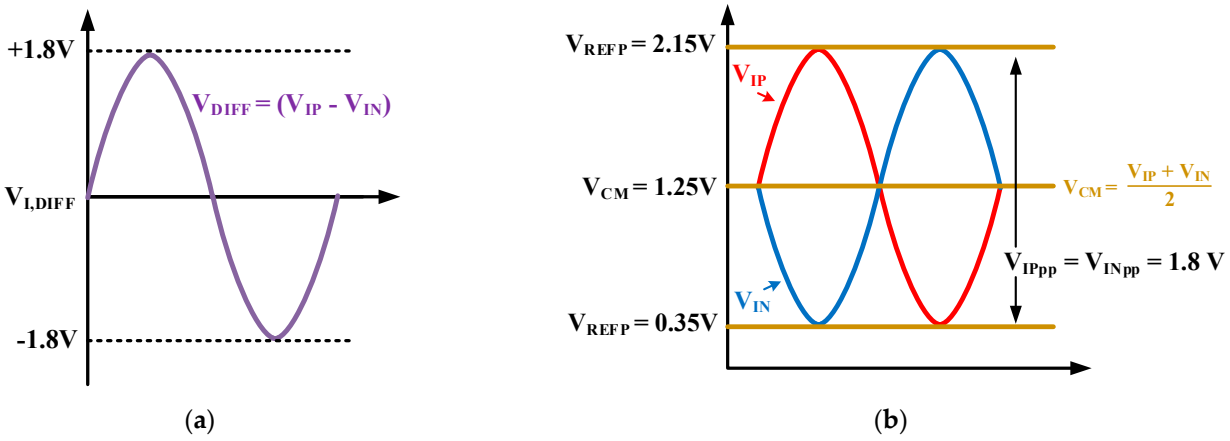
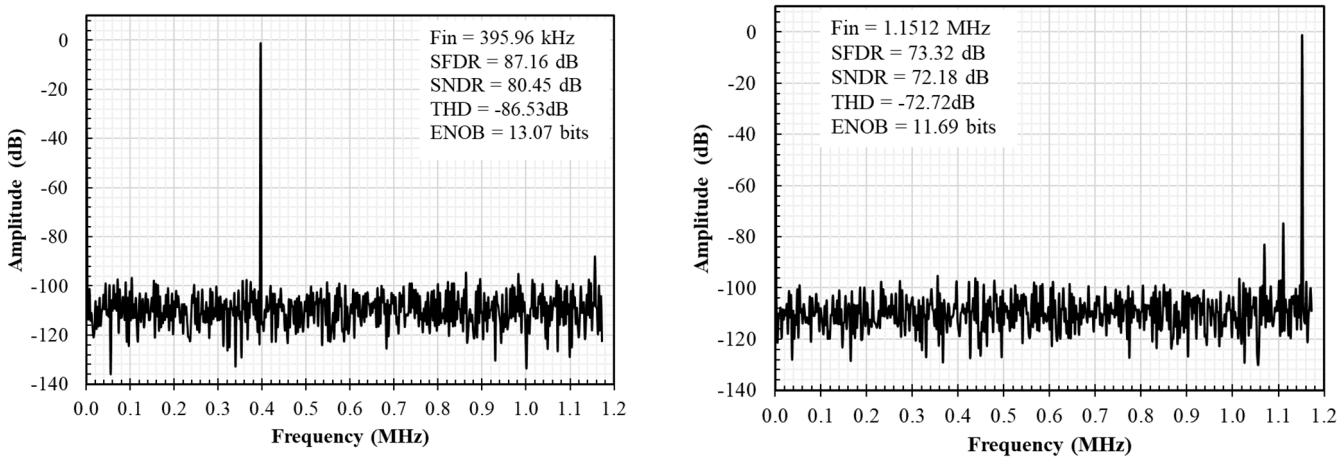


Figure 10. Input voltage of ADC: (**a**) Differential and (**b**) single-ended representation.

As shown in Figure 10, the internal reference voltages V_{REFp}, V_{REFn} are set as $V_{REFp} = V_{cm} + V_{REF}/2$, $V_{REFn} = V_{cm} - V_{REF}/2$, where the reference voltage is V_{REF} = 1.8 V to be equal to the full-scale range of the single-ended input signal. The common-mode voltage is set as $V_{cm} = (V_{REFp} + V_{REFn})/2$ = 1.25 V. The V_{cm} voltage is selected to be higher than the usual value of $V_{REF}/2$, for optimum performance of the input driver and comparator blocks. The power supply for analog and digital blocks is 2.5 V and 1 V, respectively.

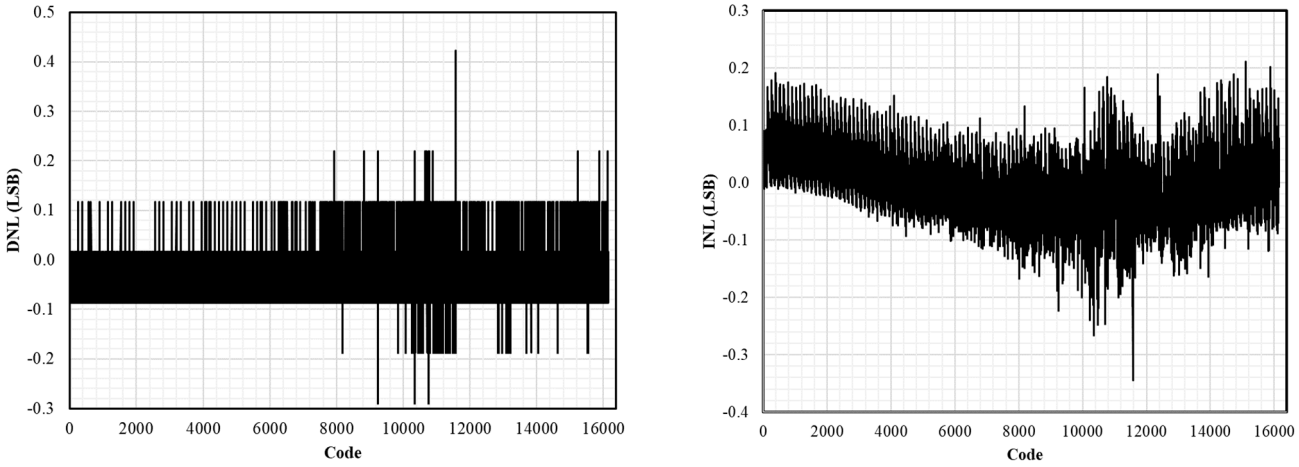
It is worth noting that all simulation results have been performed by running transient noise analyses. This ensures that the noise impact on the final ADC performance has been considered in the final plotted and numerical results presented in this section.

For input frequency equal to 395.96 KHz the SFDR is 87.16 dB, the SNDR is 80.45 dB, the THD is −86.53 db and the ENOB is 13.07 bits, as shown in Figure 11a. For input frequency equal to 1.1512 MHz the SFDR is 73.32 dB, the SNDR is 72.18 dB, the THD is −72.72 db and the ENOB is 11.69 bits, as shown in Figure 11b. The INL and DNL is +0.22/−0.34 LSB and +0.42/−0.3 LSB, respectively, as shown in Figure 12a,b. The power consumption of the ADC core, not including the reference buffers, is 0.8 mW: 0.38 mW for the SHA (47.83%), 0.3 mW for the comparator (37.76%), 0.1 mW for the DAC including the level shifters (12.59%) and 0.014 mW for the digital logic blocks (1.83%).



(**a**) (**b**)

Figure 11. ADC output spectrum: (**a**) fin = 395.9 kHz; (**b**) f_{in} = 1.1512 MHz.



(**a**) (**b**)

Figure 12. (**a**) DNL; (**b**) INL diagrams.

ADC performance is usually limited by the mismatch errors and specifically by the local mismatch of the capacitor units. As shown in Figure 13, Monte Carlo simulations, for input frequency equal to 395.96 KHz, verify that ENOB remains almost invariant by mismatches. The mean value of ENOB for 15 samples is 13.00 and the standard deviation is 0.0749. The small variation is explained by the selected value of C_u and C_{split} as studied in detail in Section 2.

In Table 1, a summary of the ADC performance is given and compared with the performance of other SAR ADCs. From this table is shown that the proposed ADC shows a competitive performance without the calibration. Obviously, the commercial AD7610 and ADS8504 dissipate significantly increased power compared with the other ADCs. This implementation also shows a relatively higher power consumption due to the larger capacitor value used in the CDAC. However, the employment of a larger capacitor gives sufficient results in terms of SNDR, SFDR, and ENOB, without any calibration and so the proposed ADC can be used in applications requiring fast power-on, without needed time for calibration.

The layout of ADC is shown in Figure 14 where the consisting blocks are annotated. The total area is 300 μm × 465 μm. The level shifters from 1 V to 2.5 V occupy a significant part of the layout, but they are required due to the high input voltage and the dual supply

voltage. They are placed between the SAR logic and the switches of the capacitor array. As depicted in the figure, the first preamplifier is positioned close to the capacitor array to reduce the parasitic capacitances of the interconnections and also to reduce any injected noise in the input of the comparator.

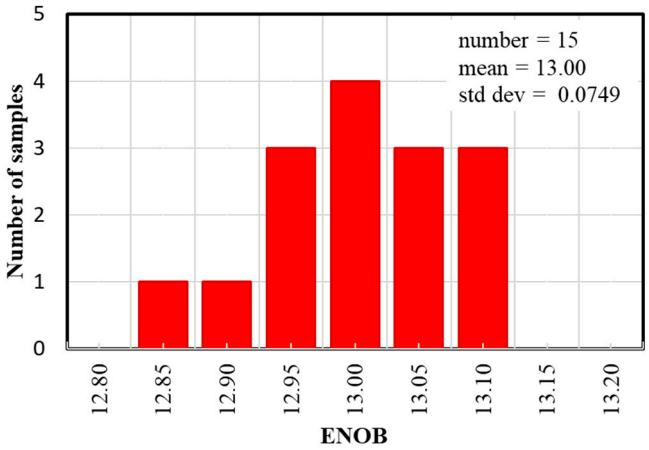


Figure 13. Monte Carlo simulation results of ENOB.

Table 1. Performance summary and comparison results.

	This Work	AD7610	ADS8504	[7]	[8]	[16]	[17]	[19]	[26]	[31]
Resolution (bits)	14	16	12	14	12	14	14	12	12	14
CMOS tech. (nm)	65	NA	600	NA	28	600	65	65	65	40
Supply Voltage (V)	2.5/1	5	5	NA	0.9	±15	0.8	1.2	1	2.5/1.2
Input range (V)	±1.8	±10	±10	NA	NA	±12	NA	0.18	0.6	±0.9
Power (mW)	0.8	90	70	NA	0.86	90	0.00066	1.1	0.47	38
Sampl. rate (MS/s)	2.5	0.25	0.25	1	100	0.4	0.128	40	20	30
SNDR @LF (dB)	80.45	94	NA	NA	61.46	73.32	80.4	64.7	65.44	77.2
SNDR @Nyquist (dB)	72.18	NA	NA	NA	58.82	NA	NA	NA	NA	75.7
SFDR @LF (dB)	87.16	NA	NA	NA	82.7	89	93	81.6	NA	97.48
SFDR @Nyquist (dB)	73.32	NA	NA	94.9	79.1	NA	NA	NA	NA	NA
ENOB @LF (bit)	13.07	15.2 @2KHz	11.8 @45KHz	NA	9.95	11.9 @ 5KHz	NA	NA	10.98	12.52
ENOB @Nyquist (bit)	11.69	NA	NA	NA	9.51	NA	NA	NA	10.58	NA
Area (mm^2)	0.14	NA	NA	NA	0.0023	9.76	0.034	0.0448	0.14	0.2365
DNL (LSB)	+0.42/−0.3	NA	±0.45	NA	+0.75/−0.56	0.92	NA	NA	+0.46/−0.48	NA
INL(LSB)	+0.22/−0.34	±1.5	±0.45	0.66	+0.83/−0.85	0.95	NA	NA	+0.50/−0.58	NA
Calibration	No	Yes	Yes	Redundancy	Yes	Yes	Yes	No	Yes	Yes

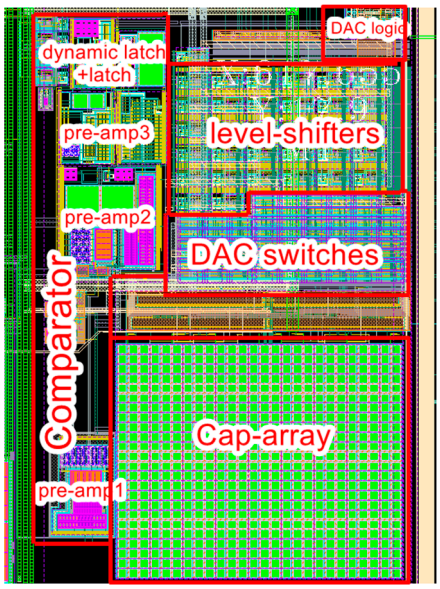


Figure 14. The ADC layout.

4. Conclusions

A 14-bit 2.5 MS/s differential SAR ADC has been presented in this paper offering high linearity without calibration. A differential binary-weighted with split capacitance array has been used to reduce the total area. The ADC has been designed in a 65 nm CMOS technology node. The values of the CDAC unit and split capacitors have been carefully evaluated and selected for improved linearity. For further improvement of ENOB without calibration, a multistage autozeroing comparator has been utilized. The ADC achieves an ENOB of 13.07 bits at low frequency and 11.69 bits at Nyquist frequency, with an input differential voltage range 3.6 V_{pp}. The INL and DNL is +0.22/−0.34 LSB and +0.42/−0.3 LSB, respectively.

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