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A Full-Duplex 60 GHz Transceiver with Digital Self-Interference Cancellation

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Abstract: This paper presents the design and measurement of an IEEE 802.11ad standard compatible RF transceiver for 60 GHz wireless communication systems. In addition to the traditional half-duplex (HD) mode, this work supports full-duplex (FD) operations to deliver better channel utilization and faster response times for the system. The isolation between the transmitter and receiver from the architecture design to system integration for FD operations has been fully considered. A digital self-interference cancellation (DSIC) is implemented in MATLAB to verify the FD performance. The super-heterodyne architecture with an intermediate frequency (IF) of 12 GHz is designed to suppress the image frequencies without using extra filters. A flexible phase-locked loop (PLL) synthesizer provides a local oscillator (LO) frequency with a 2 kHz resolution. Other than the time division duplex (TDD) mode used in the conventional 60 GHz system, a wide-bandwidth baseband digital variable-gain amplifier (DVGA) with a 3 dB bandwidth of more than 4 GHz also supports frequency division duplex (FDD) operations. The transceiver chip is fabricated using the Tower Jazz 0.18 μ m SiGe BiCMOS process. With an on-board antenna, the transceiver covers all four channels in the 802.11ad standard, with MCS-12 (7.04 Gbps under 1.76 GSym/s and 16-QAM) under 1.5 m. In the proposed system design, the RF frontend-based self-interference (SI) suppression from the local transmitter to receiver LNA is around 54 dB. To achieve a practical FD application, the SI is further suppressed with the help of a digital SI compensation. The measured power consumption for the transmitter and receiver configurations are 194 mW and 231 mW, respectively, in HD mode and 398 mW for the FDD or FD operation mode.

Keywords: 60 GHz communication; 802.11ad; digital self-interference cancellation (DSIC); frequency division duplex (FDD); full duplex (FD); low power consumption; self-interference (SI); transceiver SoC; SiGe BiCMOS



Citation: Wang, Y.; Thangarasu, B.K.; Mahalingam, N.; Ma, K.; Meng, F.; Huang, Y.; Yeo, K.S. A Full-Duplex 60 GHz Transceiver with Digital Self-Interference Cancellation. *Electronics* **2024**, *13*, 483. <https://doi.org/10.3390/electronics13030483>

Academic Editors: Antonio Vincenzo Radogna and Stefano D'Amico

Received: 10 December 2023

Revised: 18 January 2024

Accepted: 19 January 2024

Published: 24 January 2024



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1. Introduction

The increasing demand for high-speed communication has urged researchers to develop new communication systems. Currently, wireless data transmission with a data rate that is higher than one gigabit per second (Gbps) is essential due to the proliferation of internet-enabled devices. The spectrum at 60 GHz, reserved internationally for the industrial, scientific, and medical (ISM) bands with an available 9 GHz unlicensed bandwidth, draws much attention. There have been significant research efforts toward the 60 GHz applications related to high-data-rate wireless communications.

The high-performance, high-data-rate 60 GHz transceivers are reported in [1–4]. The designs [1,2] target the next generation of WiFi standard 802.11ay with a wider bandwidth and higher-order modulation. The work in [1] presents an area-efficient bidirectional

transceiver that utilizes a bidirectional amplifier to entirely share the mixer and LO between the transmitter and receiver modes. The measured link error vector magnitude (EVM) for a single channel is -24.3 dB for 16-QAM at 0.12 m. In [2], a single transceiver with 50.1 Gbps with 8.35 GSym/s in 64-QAM and 3.52 GSym/s with a 128-QAM modulation is reported. The reported single-channel communication with 64-QAM in 0.15 m achieves an EVM of -28.2 dB. In [3], a low-power, small-size on–off keying (OOK) transceiver is reported with 12.5 Gbps and an energy efficiency of 2.65 pJ/bit. All the reported works in [1–3] suffer from shorter communication distances limited by the noise floor bandwidth, and they all rely on half-duplex (HD) operation only. The work in [4] presents 2×64 - and 2×256 -element dual-polarization transceiver arrays with maximum equivalent isotropic radiated power (EIRP) values of 38 dBm and 44 dBm, respectively, which provide good signal coverage but consume a large chip area and power consumption.

The FD operation is another way to deliver a high data rate by doubling the system's achievable spectrum efficiency [5,6]. Moreover, the ultra-low latency demand for the upcoming wireless communication system [7] is another benefit for the FD system. With optical communication-like propagation characteristics and a narrow beamwidth, the FD system is a good candidate for a 60 GHz transceiver to work in FD mode. However, the FD system suffers from an enormous RF signal power difference between the power imposed by its transmission and that received from the remote transmitter.

Self-interference (SI) suppression or cancellation is critical for an FD system. The work in [8] presents a 60 GHz transceiver with a polarization-based antenna with RF cancellation. It achieves an SI suppression of 70 dB from the transmitter to its receiver. The work in [9] involves SI cancellation for an FD transceiver in a single-antenna system. It achieves 40 dB SI cancellation by using an RF circulator to separate the transmitter and receiver and a reconfigurable impedance mismatched circuit to modify the frequency response of the SI channel. The work in [10] demonstrates an E-band backhaul solution achieving 8 Gbps under the frequency division duplex (FDD) mode. The isolation between the transmitter and receiver is greater than 50 dB. However, the active RF frontend cancellation-based FD systems involve a complex circuit design and work for a specified bandwidth only.

This paper proposes a low-power 60 GHz transceiver prototype that is fully compatible with the IEEE 802.11ad wireless standard. Other than the traditional IEEE 802.11 WiFi standards, which work in HD mode, this work supports both FDD and FD operations. Additionally, the system supports hybrid schemes with reconfigurable switching between the HD, FDD, and FD operation modes. The proposed system's SI requirements are relaxed compared to the works in [8,11] due to a low transmission power for a comparable communication distance.

The organization of this paper is as follows: Section 2 describes the design challenges of the proposed transceiver through the link budget estimation. Section 3 introduces the design and implementation of some critical components in the prototype system. In Section 4, the integrated transceiver measurement is shown. Finally, in Section 5, a conclusion is presented.

2. System Requirement

Figure 1 shows the simplified diagram of the proposed system with two transceiver sets. In the HD mode, one transceiver is configured as the transmitter and the other as the receiver. Since they are always working in opposite modes, there is only one RF stream available all the time, which is also named time division duplexing (TDD). While in the frequency division duplex (FDD) mode or the in-band full-duplex (FD) mode, both transceiver sets act as transmitters and receivers simultaneously. Two RF streams are available in the opposite direction, and they can be configured with either the same or different carrier frequencies. In FDD, different carrier frequencies are used, while in FD, the same carrier frequency is used. Figure 2a,b shows the spectrum conversion for both the FDD and FD modes.

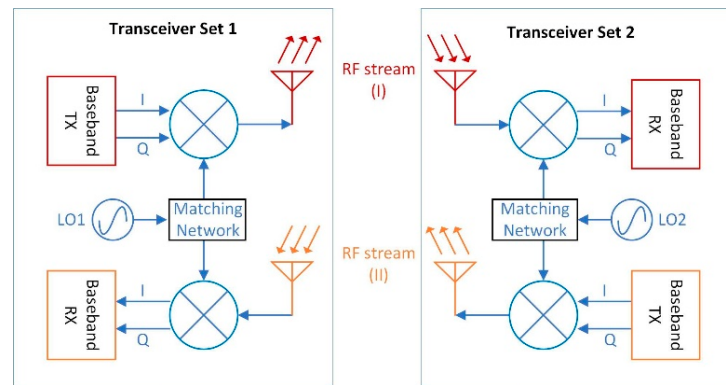


Figure 1. Simplified diagram for the dual-stream system.

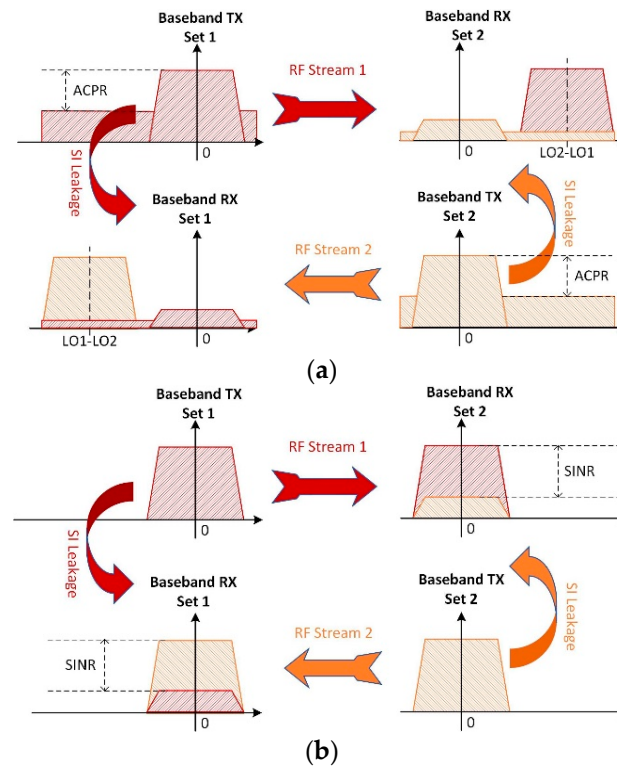


Figure 2. Frequency spectrum for the proposed dual-stream operation of the (a) frequency division duplex (FDD) and (b) full-duplex (FD) modes.

In the FDD operation mode shown in Figure 2a, the LO frequencies are set at LO1 and LO2 so that the transmitter and receiver are separated in the frequency domain. This is achieved by adopting wide-bandwidth amplifiers in the receiver chain to cover its adjacent band. The wanted signals are separated from the SI signal in the frequency domain, and they can be recovered using a high-pass filter. The adjacent channel power ratio (ACPR) and SI isolation are the dominant considerations for FDD operation. However, the channel utilization is low, as both transceivers occupy separate physical channels. The digital baseband processor needs to handle the signal with an IF carrier, which will increase the complexity of the data processing units. In the FD mode, as shown in Figure 2b, both transceivers work simultaneously using the same channel, such that two RF streams share the same physical channel but are in opposite directions. In this mode, a frequency reuse strategy can theoretically double the spectral efficiency. The technical difficulties for such an approach are the requirement for SI suppression or cancellation, as the SI and the wanted signal overlap at the baseband. An excessive SI may even result in a reduced capacity for the FD system that falls below the HD systems. As shown in Figure 2b, the signal-to-

interference and noise ratio (SINR) is the key parameter to estimate the capability of the FD system. In principle, the SI can be perfectly regenerated and compensated since the transmitted data are known inside the transceiver. However, the realistic SI is also affected by the non-linear effects of the transmitter and receiver chain and the unpredictable LO phase noise that makes it far from the estimation.

2.1. Link Budget Model

The proposed transceiver is targeted for the IEEE 802.11ad wireless standard up to a communication distance of 3 m. It can support the MCS12 scheme under traditional WiFi operation. The highest raw data rate is 7.04 Gbps under 1.76 GSym/s of 16-QAM with the EVM at -21 dB. A wideband signal results in an increased in-band noise floor and reduces the SNR. The noise floor can be estimated by using the thermal noise for the given channel's bandwidth together with the additional receiver's noise figure and some implementation losses. Considering a 2.16 GHz channel bandwidth, an additional 5 dB budget for the receiver chain's noise figure, and 5 dB implementation losses, the noise floor of the receiver system will be -70.6 dBm theoretically.

Table 1 lists the EVM requirements for some of the key modulation schemes defined in the WiFi standard [12], with the receiver sensitivity level for the system based on the estimated noise floor. As listed in the table, the received signal power at the LNA input must be higher than -49.6 dBm because of the 21 dB minimal EVM requirement for the targeted modulation scheme at MCS12. To further increase the systems' data rate, either a higher-order modulation scheme or a lower error code rate is required, as can be seen for MCS12.1 to MCS12.6, but with an increased SNR requirement.

Table 1. EVM and sensitivity requirements.

MCS Index	Modulation Type	Code Rate	EVM Requirements (dB) ¹	Receiver Sensitivity (dBm) ²
5	$\pi/2$ BPSK	13/16	-12	-58.6
6	$\pi/2$ QPSK	1/2	-11	-59.6
7	$\pi/2$ QPSK	5/8	-12	-58.6
8	$\pi/2$ QPSK	3/4	-13	-57.6
9	$\pi/2$ QPSK	13/16	-15	-55.6
9.1	$\pi/2$ QPSK	7/8	-16	-54.6
10	16-QAM	1/2	-19	-51.6
11	16-QAM	5/8	-20	-50.6
12	16-QAM	3/4	-21	-49.6
12.1	16-QAM	13/16	-22	-48.6
12.2	16-QAM	7/8	-23	-47.6
12.3	64-QAM	5/8	-26	-44.6
12.4	64-QAM	3/4	-27	-43.6
12.5	64-QAM	13/16	-29	-41.6
12.6	64-QAM	7/8	-31	-39.6

¹ EVM requirements from IEEE Standard 802.11-2016 [12]. ² Estimated based on a 2.16 GHz channel bandwidth, a 5 dB receiver chain noise figure, and 5 dB implementation losses.

The reference-free space loss for the 60 GHz signal is around 68 dB at a 1 m distance [13,14]. In this estimation, the additional attenuation items can be ignored because the multipath fading effect is insignificant due to the short communication distance, narrow beamwidth, and good alignment of the antennas. A pair of narrow-beam directional antennas are designed and integrated on the RF-printed circuit board (PCB) to simplify the system's integration and reduce the prototype cost. The integrated antenna provides a 12 dBi antenna gain for both the transmitter and receiver with 17° half-power beam coverages. The propagation loss for the system reduces to 53.6 dB with the help of such directional antennas. As mentioned in Table 1, the EVM requirement for MCS-12 is -21 dB and the received power must be larger than -49.6 dBm. With a 53.6 dB propagation loss,

the transmitter's output power should be larger than +4 dBm to satisfy the minimum received power requirements.

To support a higher modulation scheme with variable amplitude, such as 16-QAM and 64-QAM, a peak-to-average power ratio (PAPR) budget is needed to ensure the linearity of the modulated signal. This can be realized by either increasing the output power of the transmitter or reducing the communication distance to support those high-order modulation schemes.

2.2. System Architecture

The transceiver architecture of the proposed system is shown in Figure 3 [15]. It is a super-heterodyne transceiver with two stages of frequency conversion. The sufficiently high intermediate frequency (IF) helps the low-noise amplifier (LNA) and power amplifier (PA) to suppress the image components by their bandwidth characteristics. This architecture also requires only one phase-locked loop (PLL) synthesizer to complete all frequency conversions and achieve low power consumption.

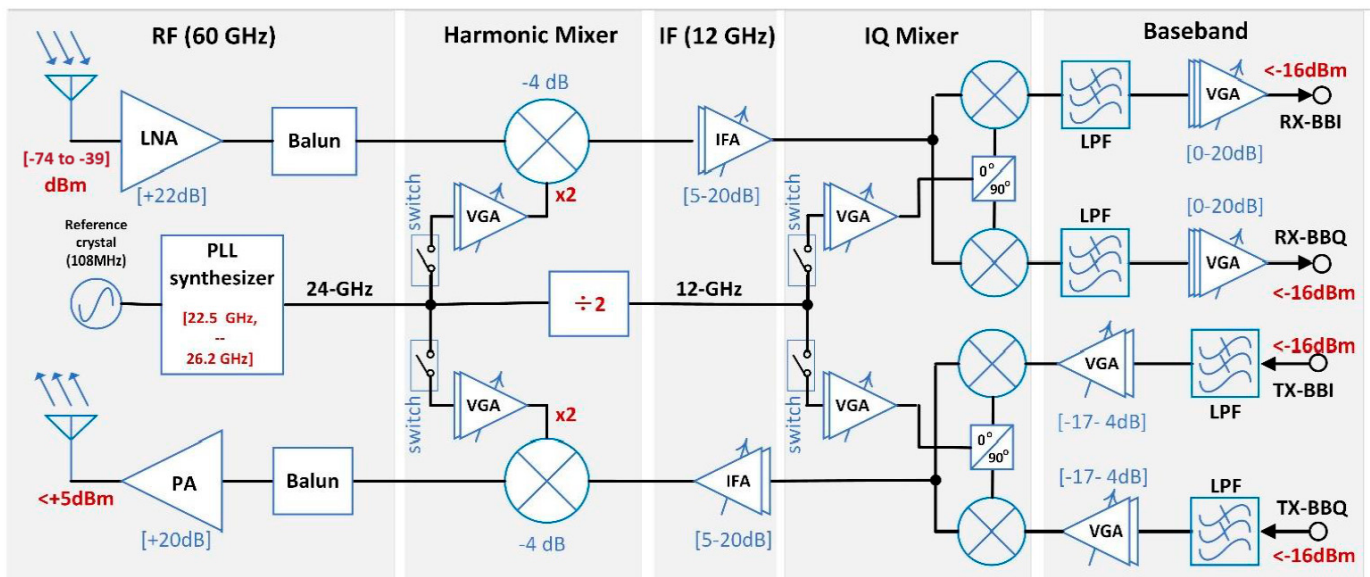


Figure 3. A block diagram of the proposed transceiver SoC.

In the receiver chain, a sub-harmonic mixer is used as the first stage of the down-conversion mixer. The input signal is mixed with a local oscillator at 4/5 of the RF frequency to generate the down-converted IF signal to 1/5 of the RF frequency. The second stage is a quadrature I/Q mixer to further down-convert the IF signal to the quadrature baseband. A 90° hybrid is utilized to generate the orthogonal LO signal. Finally, the I/Q mixer's output passes through a low-pass filter and a dB-linear digital variable-gain amplifier (DVGA) before passing through the digital baseband for further processing. The amplitude imbalance can be compensated by fine-tuning the gain of the baseband DVGA, and the matched hybrid minimizes the phase imbalance across the frequency bands of interest. The overall variable gain in the receiver chain is from 23 dB to 58 dB. The saturation output power of the baseband DVGA in the receiver chain is -16 dBm for both the I and Q paths. The input power range for the receiver should be chosen between -74 dBm and -39 dBm.

The transmitter chain of the proposed system is an inverse frequency conversion scheme as the receiver. It shares the same LO sources as the receiver from the on-chip PLL synthesizer. The input baseband signal should be less than -16 dBm, and the baseband DVGA may attenuate or amplify the baseband input for the quadrature mixer. A programmable IF amplifier (IFA) amplifies the IF signal in the transmitter chain. This IFA provides a gain of 5 dB to 20 dB with good linearity for a wideband modulated signal with

a 3 dB bandwidth up to 7 GHz. The transmitter is suitable for a variable power range, with good linear modulation performance.

The transceiver frequency synthesizer can generate frequencies from 22.5 GHz to 26.2 GHz, with a 400 Hz frequency resolution step size. This corresponds to LO frequencies from 56.25 GHz to 65.5 GHz, to fully cover all four channels in the 802.11ad wireless standard. A 108 MHz crystal is selected as an external reference for the PLL. The divider chain in the PLL can be operated in the integer mode for better phase noise. The PLL employs a fractional frequency divider chain and can also support other reference frequencies between 33 MHz and 40 MHz or 100 MHz and 120 MHz [15]. To provide the mode switch between the different operation types, the LO network with a high-efficiency switch supports the LO power distribution to the transmitter chain, receiver chain, or both. In the FDD and FD operation modes, the LO power feed to the transmitter chain drops by half compared to the HD mode, and the output power of the transmitter drops at the same time.

2.3. FDD and FD Modes of Operation

Unlike the traditional TDD mode, the transmission and reception happen simultaneously in the FDD and FD modes, which are supported in the proposed system. The FDD operation mode is achieved by adopting a wider bandwidth baseband DVGA, IFA, and LNA. The proposed transceiver supports an offset frequency operation up to 2.16 GHz, such that the carrier frequency difference between the two local oscillators is 2.16 GHz. In such a condition, the transmitter up-converts the signal to the specified RF frequency band, while the received signal down-converts it to a 2.16 GHz IF band. The DVGA design reported in [16] with a 0.3 dB gain step using a 6-bit digital gain control is employed here. The optimization for bandwidth extension in [16] achieves a 3 dB bandwidth of more than 4 GHz. To cover all possible FDD operation bands, which satisfy the 802.11ad standard, the IFA requires a vast bandwidth of 6 GHz, centered from 12.096 GHz to 12.48 GHz, where the receiver works using channel 2 or channel 3, respectively, because the received IF signal may locate on either side of the IF LO with a 2.16 GHz carrier offset for those channels. For channels 1 and 4, the received IF signal will be located at certain bandwidths within the band mentioned above. The IFA design has a 3 dB bandwidth from 9.0 GHz to 15.5 GHz that completely covers the signal band. The SI signal in the FDD mode is important, as the SI is always located at zero carrier frequency. The low-frequency noise may degrade the system's performance by reducing the DVGA's operation range or even failing the system when the DVGA is saturated. However, a physical separation in the spectrum enables the FDD system to achieve a level of performance close to the HD system. The performance is not affected even with the strong SI leakage when the DVGA is ensured to work in the linear range.

In the FD operation, the SI and the wanted signal overlap at the baseband. Recently, RF-related active cancellation [8,17,18], pure digital cancellation [19,20], or a hybrid of both RF and digital cancellation [11] was introduced. The RF frontend-related cancellation approach achieves good performance, usually for a specified frequency range and limited bandwidth with a complex circuit design and area [8,21]. In this work, RF isolation and digital cancellation are used due to the low design complexity and acceptable performance across the interested frequency band. Since the received signal power must be higher than -49.6 dBm for MCS12 with an EVM better than -21 dB, it is harder to achieve an SI signal power that is lower than the noise floor just by using RF frontend isolation [8]. The digital-based SI cancellation is involved in increasing the SINR and reducing the FD's performance degradation. The FD with a lower SINR loss can be assumed to be approximately double the spectral efficiency, whereas with a high SINR loss, the effective spectral efficiency might be even lower than the HD mode. An SINR loss of 3 dB illustrates the point at which the FD mode can still be expected to provide a capacity gain compared to the HD transceiver [22,23]. Hence, the system's SI power should be lower than -67.6 dBm to make the FD mode meaningful.

3. Design and Implementation

Some of the detailed sub-block circuit designs for the proposed transceiver are presented in previously published works [15,16,24–26]. In this work, the proposed transceiver needs to additionally support FDD and FD operations. The optimized DVGA with a bandwidth extension is presented in [16]. An updated PLL synthesizer with a power distribution network to provide LO signals to the transmitter and receiver chains at the same time is introduced and presented in [26]. The optimized matching network, including high-isolation switches for efficient power delivery, and both the HD and FD modes are described in it. Compared to the HD mode, the maximum LO power to the transmitter chains in the FDD and FD modes drops by 3 dB, and it degrades the transmitter's maximum output power by 6 dB.

To achieve a similar SINR requirement that fulfills the specifications, we can either increase the received signal power or reduce the unwanted noise power, including the SI. However, in the FD mode, the transmitter power is in direct proportion to the received power for a given communication distance, and the SI isolation factor is fixed for a given system. The receiver chains will amplify both the received signal and the SI signal simultaneously. In other words, the transmission power determines the SI noise power, regardless of the communication distance. A shorter communication distance can relax the transmission power required while maintaining the received signal power, and the reduced transmission power will simultaneously scale down the SI noise. For the shortest distance, e.g., the line-of-sight (LoS) channel in this work, it provides a 6 dB power gain when reducing the communication distance by half.

3.1. RF Isolation from the Transmitter Chain to the Receiver

The SI can occur at any stage in the transmitter chain. It may come from the 60 GHz band within the transceiver chipset, PCB, antennas, and reflected signal. The 12 GHz IF signals and the direct baseband leakage from the transmitter chain may also be available at the receiver system as the SI. Some efforts are made at the level of chip design to reduce the on-chip leakages for the 60 GHz signals. The floor plan is optimized to maximize the distance between the PA and LNA layouts with additional guard rings and isolation wells around them. In addition, isolated power, ground, and I/O pads are used for transmitter and receiver chains to avoid signal coupling. At the circuit level, all the sub-blocks except the PA and LNA are implemented using a fully differential architecture to minimize the effects of the coupling signal in the common mode or supply networks. The 0.18 μm BiCMOS can achieve a signal isolation of around 60 dB for a distance of 50 μm [27], and it is good enough for the proposed low-power, short-distance design without extra active cancellation.

Two adjacent antipodal Fermi antennas are embedded on the FR4 RF PCB separately for the transmitter and receiver. The antenna has a half-power beamwidth of 17° and 24° in the E plane and H plane, respectively [25]. Figure 4 shows the top view of the fabricated PCB with a pair of antennas and corresponding interconnection transmission lines. The quadrature baseband signals are placed on the sides of the PCB as shown in Figure 4. The double-row 40-pin connector is placed on the right side for power supply and control signals from the motherboard. The left cross-sectional view of the PCB with antenna beams is shown in Figure 4 and marks the thickness of the different materials used in the PCB design. Two separate antennas avoid the difficulties of signal isolation within the antenna, unlike the single-antenna FD in [11]. For the antenna design, a pair of conducting arms are placed symmetrically on both sides of the RO4003 substrate layer. Moreover, the whole antenna is placed on a slot of the FR4 board that is much thicker than the antenna.

The narrow-beam antenna is designed to deliver maximum energy in the direction of the antenna tip, pointing with a small-angle coverage. The TX and RX antennas will send power in the marked direction, and the energy propagated between them is minimized. The measurement shows around a 30 dB drop for the energy propagation in the orthogonal direction compared with the beam direction [25]. The thick FR4 board between the two

antennas also blocks the direct propagation path between them to further reduce power transfer. The board-level measurement is performed to extract the energy leakage through the near-field of the antenna and the mutual coupling. A Keysight PNA-N5247 network analyzer is used to analyze the board-level leakage signal across the interested band. The measurement is performed with a 5 dBm input signal fed to one of the antennas, and the received signal power in the other antenna is measured. The measured S21 shows more than 80 dB of attenuation in the interested frequency ranges from 57 GHz to 67 GHz. The SI leakage in the board is lower than the noise floor, and it can be ignored.

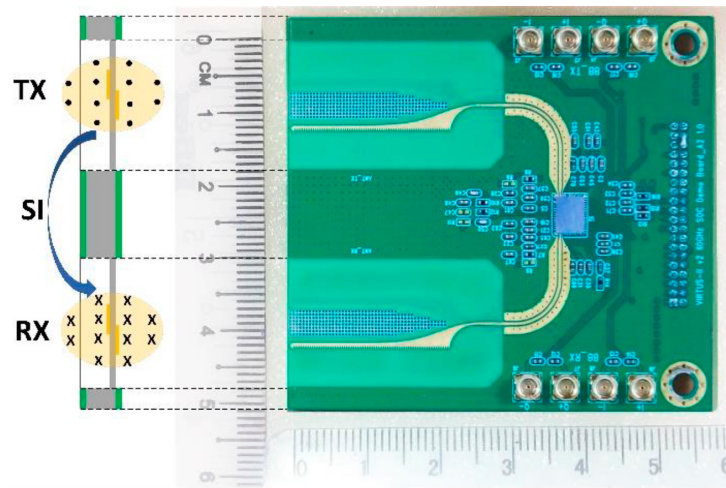


Figure 4. The fabricated PCB with two antennas.

3.2. Digital SI Cancellation Scheme

The SI power should be less than -67.6 dBm to ensure the FD operation has benefits compared to the HD operation for a 3 m communication distance. This is challenging to achieve using only the RF isolation approach. This section focuses on a digital SI cancellation scheme to relax the RF-related leakage optimization requirement. To simplify the digital SI cancellation (DSIC) scheme, only a linear transformation is adopted in this work, and the dominant SI leakage source considered is from the PA's output to the LNA's input. So, the transmitter signal S_{tx} can be expressed as in (1), where I and Q are the baseband signals, ω_0 is the LO carrier frequency, and φ_{tx} and θ_{tx} are the phase noise and the initial phase of the transmitter LO, respectively.

$$S_{tx} = I \cdot \cos((\omega_0 + \varphi_{tx})t + \theta_{tx}) + Q \cdot \sin((\omega_0 + \varphi_{tx})t + \theta_{tx}) \quad (1)$$

The transmitted RF signal S_{tx} loops back to the LNA's input through an undesired SI leakage path and will be down-converted through the receiver chain by using the same LO ω_0 but with the phase noise φ_{rx} and an initial phase θ_{rx} . The received I/Q baseband signal is captured by an analog-to-digital converter (ADC) in the baseband processor. The captured baseband signal before the ADC can be expressed as follows:

$$I_{rx} = 1/2[(I \times \cos((\varphi_{trx})t - \theta_{trx}) - Q \times \sin((\varphi_{trx})t - \theta_{trx}) \quad (2)$$

$$Q_{rx} = 1/2[(Q \times \cos((\varphi_{trx})t - \theta_{trx}) - I \times \sin((\varphi_{trx})t - \theta_{trx})] \quad (3)$$

where $\varphi_{trx} = \varphi_{tx} - \varphi_{rx}$ and $\theta_{trx} = \theta_{tx} - \theta_{rx}$. It is clearly seen that the SI signal is related to the LO phase noise, and it is rotated depending on the initial phase θ_{trx} . Equations (2) and (3) shows that the phase noise is effectively doubled as φ_{tx} and φ_{rx} are not related to each other, and there is a constant phase rotation in the received I/Q signal. At the same time, the propagation delay of the signal causes an offset between the sampling time of the receiver's ADC and the ideal sampling time. The time-domain equalization filter is used after the phase rotation and symbol synchronization to minimize the error

between the received leakage signal and the estimated value. Here, the propagation delay and channel effect of the SI leakage channel are assumed to be fixed across the time and input signals. Figure 5 shows the block diagram of the proposed DSIC scheme. The design is implemented in MATLAB with four times the oversampling data captured by an oscilloscope. I_{rx} and Q_{rx} are received as baseband signals, and I_{tx} and Q_{tx} are the original signals from the transmitter. The data sequence is separated into a training period and an SI cancellation period as shown in Figure 5. During the training period, only the SI leakage signal is available in the receiver chains. The IEEE 802.11ad-based frame packages are used as training sequences. Firstly, the I/Q data-related correlation is calculated in the phase rotation module to detect the package and estimate the initial phase simultaneously. Then, the Gardner filter is used for symbol synchronization after the phase rotation. It helps to correct the sampling time offset. Finally, a symmetrical filter with 21 multipliers is implemented as a 41-tapped finite impulse response (FIR) filter to do time-domain equalization among 10 symbols. The FIR-based recursive least squares (RLS) algorithm is used as an adaptive filter to optimize the equalization filter. The FIR filter coefficients are calculated during the training period and maintained for the SI cancellation period. A 3rd-order LaGrange interpolation module is used to regenerate the symbol data based on the estimated sampling time offset. Then, the SI leakage signal is regenerated after the phase rotation, and it is subtracted from the received baseband signal. In the proposed system, the DSIC is executed in MATLAB. The transmission baseband signals I_{tx} and Q_{tx} must be synchronized to the received sequence again before the SI cancellation runs. The evaluation of the DSIC assumes that the SI signal is 12 dB lower than the wanted signal with a given phase rotation and sampling offset. The concept simulation runs based on the ideal test patterns with a few specified effects, including phase rotation, sampling offset, and additional Gaussian white noise. The phase noise and channel flatness degradation are not included in the DSIC simulation. The simulation achieves more than a 20 dB SI cancellation by using a 6-bit ADC, with perfect alignment of the phase and sampling time. The finer ADC resolution achieves better performance based on a 6 dB improvement per bit. However, the performance is sensitive to the symbol's sampling time offset. It will drop to 5 dB with the worst estimated sampling timing offset. The DSIC module achieves an 8 dB SNR improvement by using the 41-tapped FIR filter with an 8-bit ADC at four times over-sampling with measured data. The SINR of the input signal is around 12 dB and the input signal is fully occupied by the 10-bit ADC's input range. Detailed information is introduced in the next section.

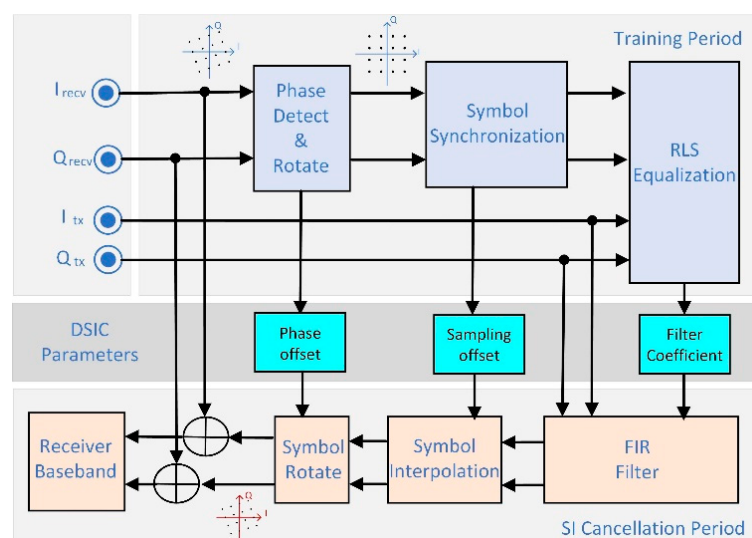


Figure 5. A block diagram of the digital SI cancellation.

4. System Measurement

Figure 6a shows the evaluation platform with a die photo of the fabricated transceiver chipset in Figure 6b. The transceiver's die size is 4 mm × 5 mm, including 64 ESD-protected I/O pads. As shown in Figure 6b, the transmitter and receiver sub-systems are placed on the bottom and top sides of the chip for maximum signal isolation, and the PLL is placed in between. Figure 6a shows the PCB with the transceiver chip assembled on the RF board and is integrated with two on-board antennas. A motherboard powered with an NXP 8-bit MC9S08JM60 MCU controls the RF front end's working conditions and monitors its power consumption. Windows-based software is used to configure the working condition of the RF chipset through a GUI interface. A mini-USB port works as both the control bus and the power supply of the platform. There are two quadrature differential baseband interfaces matched to 100 Ω impedance, and they are available on the RF board as the transmitter input and receiver output. A 108 MHz TCXO crystal board works as a reference for the RF platform.

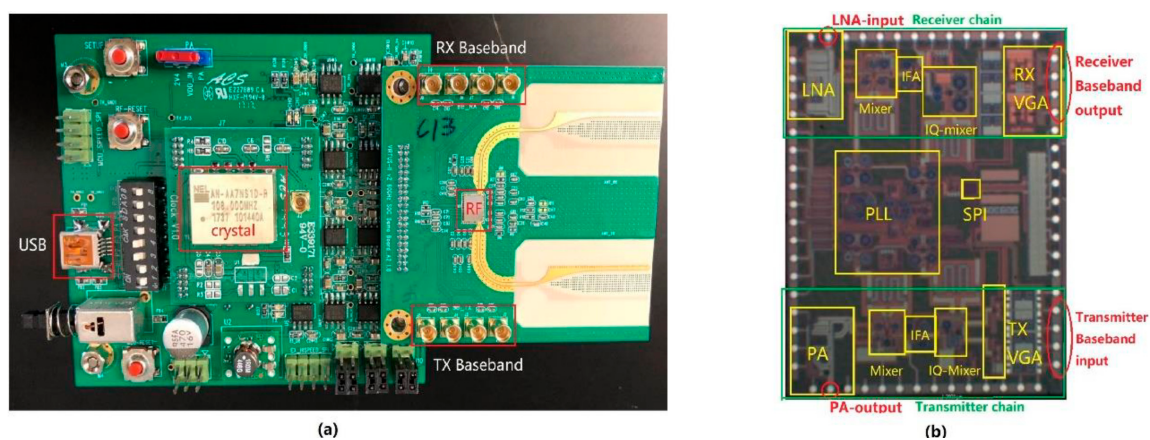


Figure 6. Photos of the fabricated chip die with the RF platform: (a) the 60 GHz RF platform with the motherboard and (b) the transceiver die.

Figure 7 shows the measurement setup of the transceiver system. One set of DUTs is configured as the transmitter. A Keysight M8199 arbitrary waveform generator (AWG) with corresponding software features (81199A) is used to generate a baseband test pattern. A horn antenna is connected to the Rohde and Schwarz FSW67 spectrum analyzer to check the transmitter power. The single-tone baseband signal is used to measure the maximum output power of the PA and channel flatness over the specified frequency band. The power plot is calculated based on the measured power, amending with the estimated setup losses.

Another set of DUTs is configured in the full-duplex mode to down-convert the RF signal transmitted by the first set of DUTs with its own local leakage. The single-tone signal helps analyze the relationship between the received signal and local SI from the transmitter. Furthermore, the 802.11ad-based package frame support measures the signal quality through the demodulated EVM. A Tektronix AWG 7122C is used as the second baseband source. The AWG has dual-channel 12 GSym/s digital-to-analog converters (DACs) to support the 802.11ad standard. A Rohde and Schwarz RTO 1044 oscilloscope captures the baseband signal for further analysis and calculates the EVM. It captures the received baseband data at 10 GSyms/s. MATLAB is used to resample the data to four times oversampling and remove the out-band noise as well. The virtual storage-extended (VSE) software V1320.7500.06 with 802.11ad features from Rohde and Schwarz was used to demodulate the received baseband quadrature signal and plot the EVM. For the full-duplex mode, the captured data are filtered by a digital filter in MATLAB to reduce the SI signal power through the DSIC module. The generated data are demodulated and analyzed by Keysight VSA software version V2019.1.3.

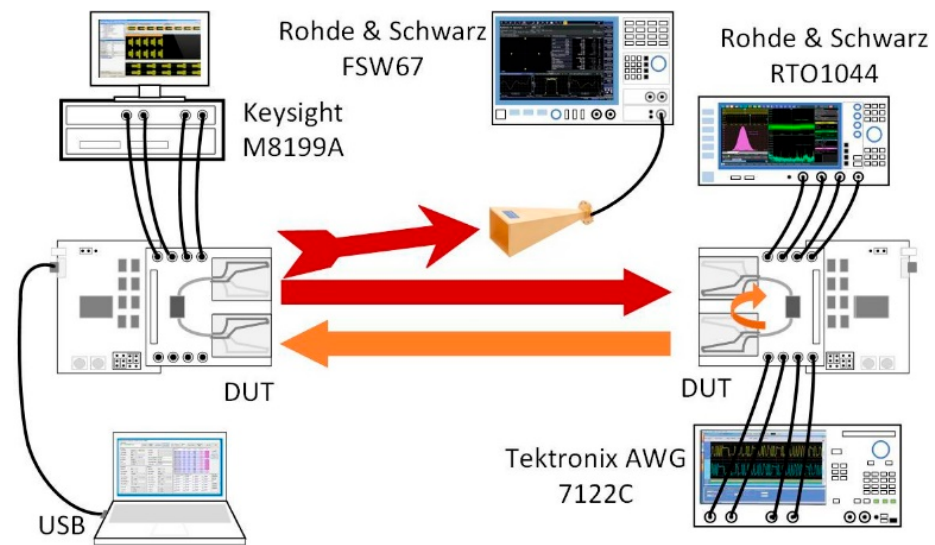


Figure 7. Measurement setup of the proposed system.

4.1. Transmitter Power

The transmitter power is measured by using a single-tone quadrature signal, varying frequencies from 100 MHz to 1.3 GHz, with a 100 MHz frequency step. The measured power is plotted based on four-channel modulation and mirrors for the same frequency offset, as shown in Figure 8. The measurement is taken at a 1 m distance with an additional 3 dB amplifier G_{PA} between the receiver horn antenna and the FSW67 spectrum analyzer. An additional 60 GHz amplifier is added, as the received signal power is too low for FSW67 to demodulate. Based on the setup and considering the free-space link loss G_{pl} to be 68 dB, the gain of the onboard transmitter antenna G_{tx} and horn antenna G_{rx} are 12 dBi and 17 dBi, respectively. Also, the total loss for the 60 GHz cables and adaptors G_{cable} is 8.7 dB. The transceiver output power is 16.7 dB higher than the directly measured value, as estimated in (4). Figure 8 plots the transmission power of the transceiver chip based on measurement results.

$$G_{loss} \text{ (dB)} = (G_{PA} + G_{tx} + G_{rx}) - G_{pl} - G_{cable} = -16.7 \text{ (dB)} \quad (4)$$

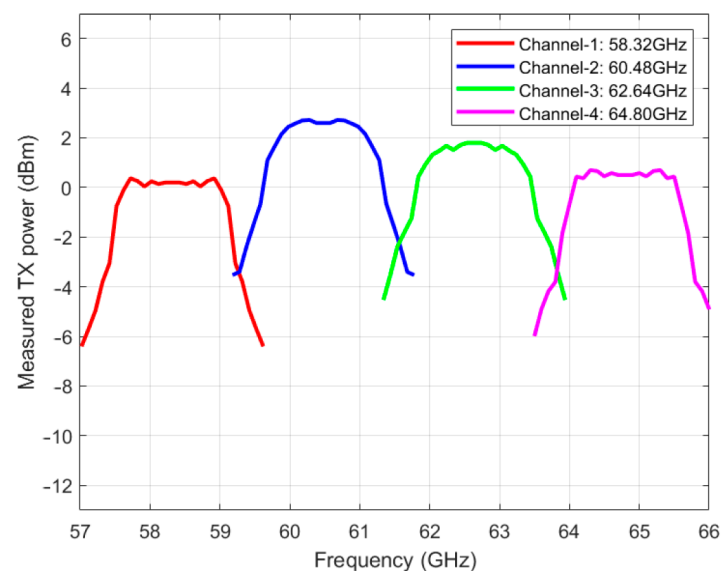


Figure 8. The transmission power on measurement.

It clearly shows that channel 2 has the highest output power compared with other channels, and all four channels have less than 1 dB channel flatness within the 1.76 GHz bandwidth. The saturated output power for the transceiver is around 2.7 dBm. The power significantly drops for out-band signals because the baseband DVGA in the transmitter chain filters the unwanted baseband to meet the spectrum mask requirements.

4.2. HD Link Measurement

The half-duplex 802.11ad modulation is measured at a 1.5 m communication distance for all four channels and is shown in Figure 9. It is defined based on the measured maximum output power, with a 6 dB peak-to-average power ratio (PAPR) linear protection range for the modulated signals. In this HD measurement, the transmission powers for MCS9 and MCS12 are set at 3 dB and 6 dB, respectively, lower than the maximum output power to have good linearity of the modulated signal. As shown in Figure 9, the measured EVM is very close to -21 dB for all channels, which is the basic EVM requirement for MCS12 of the IEEE 802.11ad standard. In the constellation diagram, the measured average EVM across the four channels for 1000 symbols under MCS12 are -21.7 dB, -21.5 dB, -20.5 dB, and -21.3 dB, respectively, for the 16-QAM-modulated data symbols, and -22.4 dB, -22.1 dB, -21.4 dB, and -22.4 dB, respectively, for pilot symbols modulated using $\pi/2$ -BPSK. The proposed transceiver fulfills the EVM requirement of MCS12 for channels 1, 2, and 4 and the 0.5 dB margin for channel 3. The QPSK-modulated signal is plotted in the same figure, which is better than the EVM specification requirements of -16 dB defined in MCS9.1.

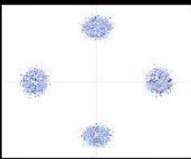
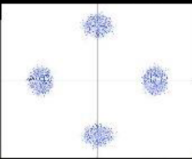
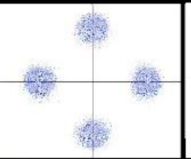
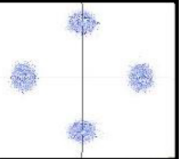
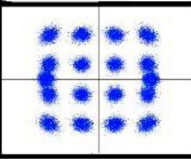
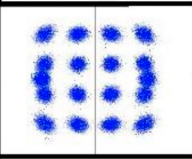
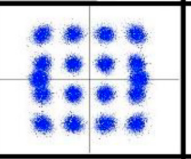
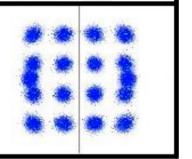
	ch1 - 58.32GHz		ch2 - 60.48GHz		ch3 - 62.64GHz		ch4 - 64.80GHz	
PPDUs	Average	Unit	Average	Unit	Average	Unit	Average	Unit
EVM All	-20.090	dB	-19.848	dB	-17.861	dB	-19.672	dB
EVM Data Symbols	-20.062	dB	-19.812	dB	-17.807	dB	-19.642	dB
EVM Pilot Symbols	-20.895	dB	-20.892	dB	-19.577	dB	-20.528	dB
MCS9								
PPDUs	Average	Unit	Average	Unit	Average	Unit	Average	Unit
EVM All	-21.743	dB	-21.536	dB	-20.558	dB	-21.324	dB
EVM Data Symbols	-21.699	dB	-21.500	dB	-20.506	dB	-21.259	dB
EVM Pilot Symbols	-22.427	dB	-22.105	dB	-21.381	dB	-22.366	dB
MCS12								

Figure 9. The measured link EVM for the IEEE 802.11ad standards.

MCS12.3 to 12.6 were added to the WiFi standard in 2016 to support a higher data rate by introducing 64-QAM support in a single carry modulation. Figure 10 shows the 64-QAM-modulated signal with a symbol rate of 1.5 GSym/s and a raw data rate of 9 Gbps. Figure 10a shows the raw data demodulation without a frame header, and Figure 10b is the constellation plot for an MCS12.6 frame package. The reported EVM value is 23.16 dB for the raw data. Other than the frame-based measurement for the 802.11ad standard, the raw data in Figure 10a without a package header may degrade the measured EVM value because of poor synchronization and equalization. Figure 10b captured a frame package with a $\pi/2$ -BPSK-modulated header and guide symbols. Figure 10b shows symbol gathering better, especially for high-power symbols located at the constellation diagram corner. However, the EVM result here is 21.88 dB, as the VSE software cannot separate the guide symbols from the data symbols correctly in the current release.

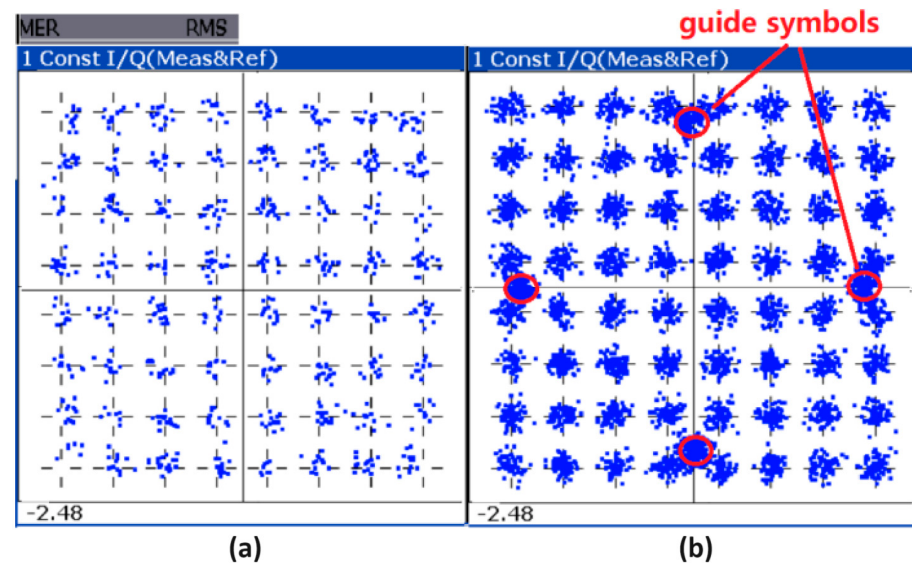


Figure 10. The measured EVM for (a) 64-QAM raw data and (b) the MCS12.6 frame.

The power consumption values of the transmitter and the receiver are 194.1 mW and 231.4 mW, respectively. Here, the power consumption is measured at a 1.5 m communication distance using the MCS12 of the 802.11ad standard. The communication distance can be further increased for a constant amplitude modulation, such as BPSK and QPSK, with the PA's saturated output. The maximum transmitter power consumption is 312.7 mW when using a 2.4 V power supply.

4.3. Frequency Division Duplex Measurement

For the FDD measurement, the communication distance is set to 0.8 m, as the measured transmitted power drops around 6 dB for the FDD operation mode compared to the HD. The reason for such a power drop is the output power of the LO signal feed to the 12 GHz I/Q mixer and the 24 GHz harmonic up-mixer are dropped when the loading network changes to drive both the transmitter and receiver chains. The performance measurement is performed with four different test conditions: firstly, the signal is transmitted from channel 2 and received at channels 1 and 3, and secondly, data are sent from channels 1 and 3 and received at channel 2. For all the measurements, the received baseband output signal 'I' is taken by the oscilloscope and then demodulated directly using VSE software. Here, the Rohde and Schwarz RTO 1044 is used as a baseband oscilloscope that samples the received signal at 10 GSym/s. The SI signal here is removed by the bandpass digital filter in VSE software directly. Figure 11 shows the measured constellation diagram with the average EVM results. The performance is better than the HD measurement, and it meets the EVM requirement of MCS12.2.

Such an EVM improvement occurred due to three reasons. Firstly, the reduced communication distance increases the received signal power by 5.5 dB. In other words, the power drop of the transmitter in the FDD mode is compensated by the communication distance. Secondly, the smaller input signals improve the linearity of the VGA, mixer, and PA. Finally, the high resolution and high sampling rate of the oscilloscope completely removed the SI noise in the digital baseband processor. The measured average EVM across the four test conditions for 500 symbols under 16-QAM are -23.2 dB, -23.27 dB, -22.78 dB, and -22.83 dB, respectively, and -21.65 dB, -21.26 dB, -20.97 dB, and -20.59 dB, respectively, for the QPSK data symbols.

		ch 2 --> ch 1		ch 2 --> ch 3		ch 1 --> ch 2		ch3 --> ch 2	
PPDUs		Average	Unit	Average	Unit	Average	Unit	Average	Unit
MER	RMS	21.65	dB	21.26	dB	20.97	dB	20.59	dB
QPSK									
									
PPDUs		Average	Unit	Average	Unit	Average	Unit	Average	Unit
MER	RMS	23.10	dB	23.27	dB	22.78	dB	22.83	dB
QAM 16									
									

Figure 11. The measured EVM for the frequency division duplex operation.

4.4. Full-Duplex Measurement

Figure 12 shows the single-tone signal's power spectrum received together with the local SI at 0.8 m. The measured transmission power is -3 dBm. The 450 MHz is the received signal from the antenna, and the 550 MHz is the SI from the local transmitter. Here, both transmitters are configured at the same condition with similar PA output power, and both the transmitter and receiver are operated on channel 2. The transmission loss here is 42 dB as calculated in (4), where the antenna gains for the transmitter G_{tx} and receiver G_{rx} are all 12 dBi.

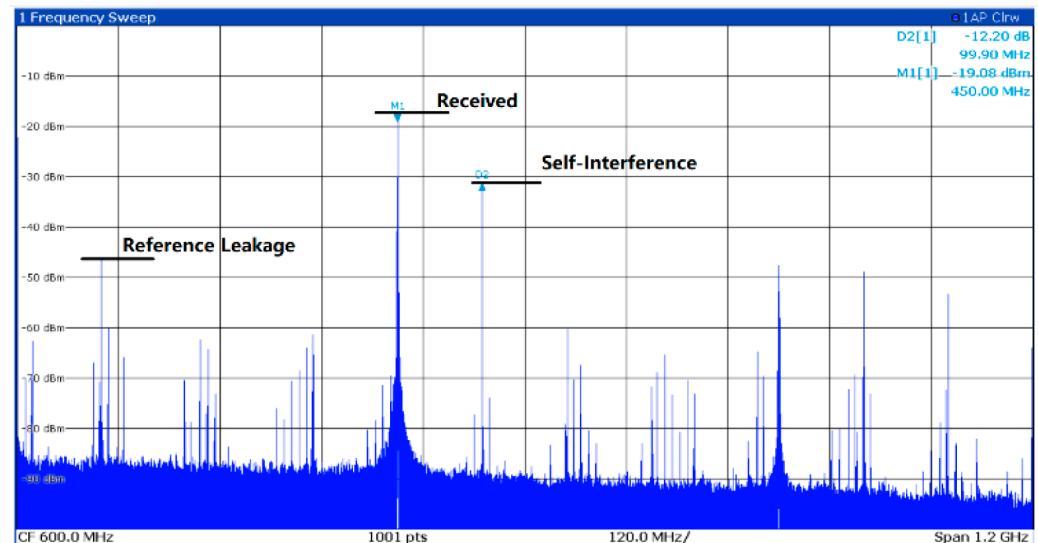


Figure 12. The received power versus the SI power at 0.8 m.

The received power achieves the maximum peak-to-peak output voltage V_{pp} of the DVGA. The measured receiver chain gain G_{rec} here is 26.08 dB as calculated in (5), where P_{rec_out} is the output power of the receiver chain and P_{rec_in} is the input power to the LNA.

$$G_{rec} \text{ (dB)} = P_{rec_out} \text{ (dBm)} - P_{rec_in} \text{ (dBm)} = -19.08 - (-3 - 42) = 25.92 \text{ dB} \quad (5)$$

As plotted in Figure 12, the estimated isolation between the output of the PA and the input of the LNA is 54.2 dB based on the measured SI power level of -31.28 dBm, as shown in (6); when the $P_{rec_in_SI}$ is the input SI power at the receive chain, P_{PA_out} is the output power from the PA. The $P_{rec_in_SI}$ is calculated based on the output power of the

receiver chain and the gain of the chain. The maximum isolation for the FD mode can be achieved at around 35 dB when setting the programmable amplifier (DVGA and IFA) to the minimal gain condition. However, the communication distance must be reduced to 0.45 m to compensate for gain drops.

$$G_{iso} \text{ (dB)} = P_{rec_in_SI} \text{ (dBm)} - P_{PA_out} \text{ (dBm)} = (-31.28 - 25.92) - (-3) = -54.2 \text{ dB} \quad (6)$$

For the modulated signal measurement, the RF isolation is around 30 dB, as a 5 dB gain is set at the receiver's DVGA to attain enough baseband signal amplitude. Figure 13 shows the time domain signal before and after DSIC processing. Two frame packages available with a 2 μ s gap between them are captured in Figure 13a. The SI signal is available all the time, and it can be observed easily during the 2 μ s package gap. The I and Q signals are captured by the oscilloscope in channels 1 and 2, as shown in Figure 13a. Figure 13b plots the received package data after the DSIC module. Here, the Rohde and Schwarz RTO 1044 oscilloscope captured data at 10 GSym/s, with 8 bits of valuable ADC output. The symbol rate of the test sequence is 1 GSym/s for both transmitters. The captured data are resampled at 4 GHz, and the out-band noise is removed before sending them to the DSIC.

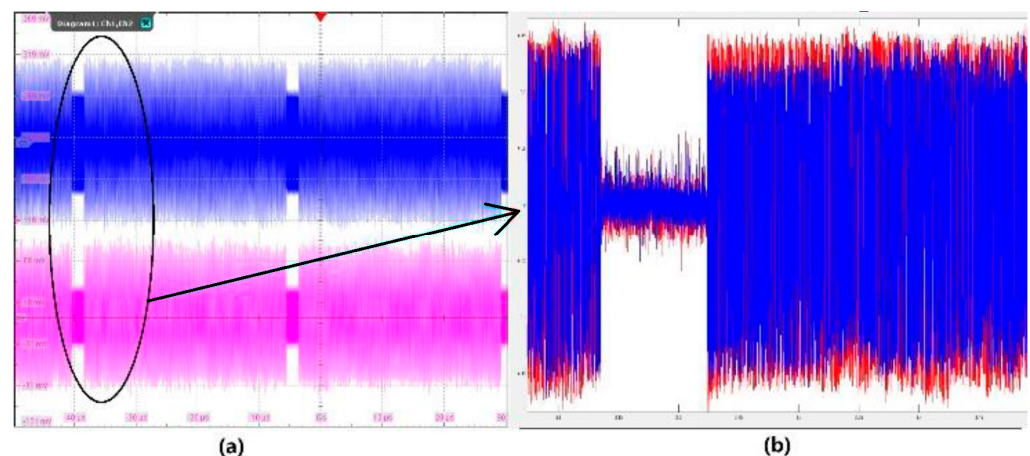


Figure 13. The time domain signal before and after the DSIC: (a) the signal captured by the oscilloscope and (b) the MATLAB output after the DSIC.

The dominant SI signal in the system comes from the 60 GHz domain before the LNA input. To measure the isolation between the transmitter and the receiver chain, the gain of the receiver's IFA is set to a minimum, and the DVGA gain is set to 5 dB. The output data from the DSIC are demodulated by a Keysight 89,600 VSA as shown in Figure 14. The reported EVM values for QPSK and 16-QAM are -17.05 dB and -17.8 dB, respectively. Here, the 16-QAM-based EVM is worse than the actual value, as 1/8 of the symbols are piloted and modulated by $\pi/2$ -BPSK. It is not mapping correctly. Assuming all the pilot symbols have a similar vector error as the data symbols, the amended EVM for all symbols should be -18.7 dB in 16-QAM. As the VSA software cannot decode the original package before the DSIC, we assume the EVM is the same as the received SINR, which is 12 dB, as shown in Figure 12. Hence, the MATLAB-based DSIC in this measurement achieved a 6.7 dB EVM improvement.

The super-heterodyne architecture is the key contributor to canceling the image frequency. For the receiver side, the image frequency is located at $2 \times \text{IF}$, which is beyond the working frequency band of the receiver baseband DVGA. The detailed performance of the integrated receiver baseband DVGA is provided in [16], which suggests that the baseband DVGA has a low pass filter response with a stopband suppression better than 50 dB at $2 \times \text{IF}$ frequency. Furthermore, in the transmitter chain, the differential sub-harmonic modulator, as illustrated in [24], indicates an image rejection of -15 dBc, which together helps to reduce the image signal component.

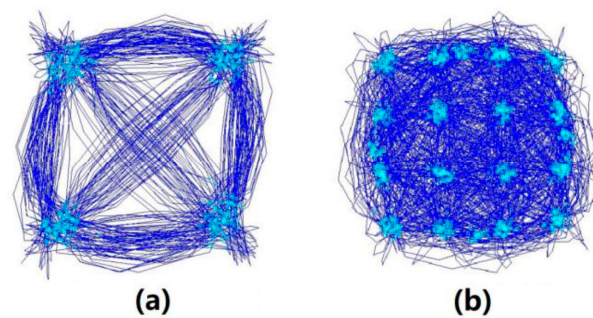


Figure 14. A constellation diagram in the FD measurement for the (a) QPSK MCS9 data symbols and (b) the QAM16 MCS12 data symbols.

The received signal is a combination of the signal received from the wireless channel and the leakage signal from the transmitter. The process technology is the standard BiCMOS process, and the leakage power from the transmitter to the receiver is quite large. Figure 12 shows the measured received signal against the local leakage signal, resulting in an SINR of 12.2 dB, which is not enough for the QAM16 operation. After introducing a digital filter to suppress the leakage signal by 6.7 dB, the system is made operable.

The above measurement covers three different working modes: HD, FDD, and FD. Firstly, based on the measurement results, the design satisfies the specification to support the 802.11ad communication standard at 1.5 m up to MCS12. The transceiver covers the design specifications of 3 m for MCS9, as the power can further increase, and the PA linearity is not an issue for the QPSK-modulated signal. Secondly, the FDD and FD measurements are completed at a 0.8 m communication distance, as the maximum transmitter power is 6 dB lower than that in the HD. Thirdly, the FD is measured at 0.8 m to fulfill the 12 dB SINR before the DSIC processing. The FD baseband data cannot be demodulated directly by using Keysight VSA software without the DSIC. The MATLAB-based DSIC is introduced to suppress the SI, and it achieves a 6.2 dB SINR gain. Table 2 summarizes and compares the measured performance of the proposed design with the state-of-the-art works. As can be seen in Table 2, this work realizes the fully integrated low-power 802.11ad-compatible RF transceiver with FDD and FD support, which simultaneously achieves 7.04 Gbps and 4 Gbps for both the transmitter and receiver in the FDD and FD modes, respectively. The system can achieve a simulated interference cancellation of 6.7 dB.

Table 2. A performance summary and comparison of state-of-the-art designs.

	This Work			[1]	[2]	[3]	[8]	[10]	[11]
Process technology	180 nm SiGe BiCMOS			40 nm CMOS	65 nm CMOS	65 nm CMOS	45 nm SOI CMOS	—	45 nm SOI CMOS
Operation mode	HD	FDD	FD	HD	HD	HD	FD	FDD	FD
SIC Mode	RF	RF	RF + DSIC	—	—	—	Antenna + RF	RF	Antenna + RF
SIC (dB)	54	54	60.7	—	—	—	70	50	60
Silicon Area RF (mm ²)	20			0.96	6.0	0.36 + 0.25	4.5	—	7.3
Antenna Gain Tx + Rx (dBi)	12 + 12			14 + 14	14 + 14	4.2 + 4.2	5.0 + 5.0	31 + 31	—
P_{sat} (dBm)	2.7	−3	−3	5.5	7.3	1.6	15	14/16 ^s	18.5
Tx + Rx Power Consumption (mW)	194 (Tx mode) / 231 (Rx mode)	398	398	94 (Tx mode) / 105 (Rx mode)	169 (Tx mode) / 139 (Rx mode)	12.1 (Tx mode) / 21 (Rx mode)	206 (Tx mode) / 111 (Rx mode)	—	— (Tx mode) / 108 (Rx mode)

Table 2. Cont.

	This Work			[1]	[2]	[3]	[8]	[10]	[11]
Modulation Type	16-QAM 1.76 GHz	16-QAM 1.76 GHz	16-QAM 1.0 GHz	64-QAM 7.04 GHz	64-QAM 10.44 GHz	OOK 12.5 GHz	BPSK 5.0 GHz	32-QAM 1.6 GHz	16-QAM 1.0 GHz
Data Rate (Gbps)	7.04	7.04 #	4 #	28.16	50.1	12.5	5 #	8 #	4 #
Distance (m)	1.5	0.8	0.8	0.01	0.04	0.05	0.7	25	0.5

It can support such a data rate in both directions. \$ Dual band at 74 GHz and 84 GHz with different powers.

5. Conclusions

This paper presents a low-power 60 GHz BiCMOS transceiver fully compatible with the IEEE 802.11ad wireless standard. In contrast to the traditional mode, the proposed transceiver allows FDD operation with -22.78 dB and -20.97 dB and FD operation with -18.7 dB and -17.05 dB EVM at a 0.8 m communication distance for 16-QAM and QPSK, respectively. The maximum data rate is 7.04 Gb/s for both the transmitter and receiver. The FD operation mode in the proposed system works only in $\pi/2$ -BPSK without a DSIC and works in 16-QAM with a DSIC. Moreover, with the 4 GHz and 3 dB bandwidth of the I/Q baseband DVGA, together with the 6 GHz and 3 dB bandwidth of the IF amplifier, the transceiver can also support the operation of the two-channel bonding receiver defined in IEEE 802.11ay with a doubled data rate of 14.08 Gb/s.

Author Contributions: Conceptualization, Y.W., and B.K.T.; methodology, Y.W., B.K.T., and N.M.; formal analysis, F.M., and Y.H.; investigation, Y.W., B.K.T., and N.M.; writing—original draft preparation, Y.W., and K.S.Y.; writing—review and editing, Y.W., B.K.T., N.M., K.M., and K.S.Y.; supervision, K.M.; project administration, K.S.Y. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: Data are contained within the article.

Acknowledgments: This research was supported by the Singapore National Research Foundation, award number NRF-CRP20-2017-0003 and project number CRP20-2017-0006. The authors would also like to thank the Tower Jazz Semiconductors Inc., Newport Beach, CA, USA, for providing fabrication service of the design.

Conflicts of Interest: The authors declare no conflicts of interest.

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