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A Hysteresis Current Controller for the Interleaving Operation of the Paralleled Buck Converters Without Interconnecting Lines

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Abstract: Paralleled buck converters have garnered significant attention for fulfilling the increasing demands of power supplies in modern applications. They have the advantages of increased current capacity and reduced current ripple. Under this architecture, applying distributed control brings the benefits of reliability and scalability. However, the interconnecting lines between the converters are required for achieving the interleaving operation, which reduces the reliability and scalability. To eliminate the interconnecting lines, this paper proposed a hysteresis current controller to achieve the symmetric interleaving operation. First, the parallel structure with a common output filter was proposed to provide the hardware basis for the proposed control method. Then, the hysteresis current controller was constructed based on the inductor voltage of each buck module to achieve the interleaving operation. The experiment of the three-module-paralleled buck converter was conducted. The experimental results show that the symmetric interleaving was achieved with a maximum phase shift error of 4.1%; the output of the parallel system can recover within 2.60 ms after the load transitions from 50% to 100%; and the parallel system can recover within 1.96 ms after one module removal. The simulation results of the six-module-paralleled buck converter show that the parallel system can recover within 1.00 ms after one module addition, which illustrates the scalability of the proposed method.

Keywords: interleaving; hysteresis controller; distributed control method; decentralized control; paralleled dc–dc converters

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1. Introduction

The buck converter is one of the most popular topologies for voltage step-down applications [1,2]. The buck converter typically consists of a switching network (a switch and a diode, or two switches) and a filter (an inductor and a capacitor), and the output voltage can be adjusted by the pulse width modulation (PWM). Due to the simple structure, low cost, and high reliability, buck converters have been applied in many applications. For example, servers [3], microgrids [4], and electric vehicles [5] utilize a buck converter as the front-end stage to pre-regulate the voltage to a suitable level [6], and AI engines (Artificial Intelligence Engines) also require buck converters to supply a regulated voltage [7]. However, a single buck converter may struggle to meet high current demands, and thus, several buck modules in parallel are required to share the total current and reduce the total current ripple [7–10].

The modular structure of paralleled buck converters is well suited for implementing distributed control. In contrast to centralized control, the distributed control disperses the control function into local controllers located within each module. The local controllers cooperate with each other to achieve the coordination and optimization of the paralleled system, and the exit of a module will not affect the operation of the entire system. Therefore, the distributed control methods can enhance the reliability and scalability of the paralleled

system [11,12]. Furthermore, the expansion of the parallel converter may bring challenges to stability. However, the stability can be analyzed with an electromagnetic transient simulation platform, e.g., MATLAB Simulink, and frequency-domain stability analysis methods, e.g., impedance-based modeling method [13–15]. In addition, the stability can be enhanced according to the results of a simulation or sensitivity analysis to ensure that the system can operate stably after expansion. Therefore, the parallel converters with the distributed control methods have been widely used in microgrids [16,17], traction systems [18,19], etc. However, to achieve the current sharing and total ripple reduction, communications between the modules are required for exchanging the current and phase information. Communications are often achieved by interconnecting lines, which increases the system's complexity and reduces reliability.

To achieve current sharing without interconnecting lines, a well-established method, i.e., the voltage droop control, is usually utilized [20–22]. It adjusts the voltage reference of the module according to its own current, and thus, it does not require information from other modules. However, to reduce the total current ripple, the interconnecting line, which carries the phase information or the synchronous signals, is still required to achieve the interleaving operation. In references [23–25], the adjacent modules were connected by the interconnecting lines to transfer the phase angles of the neighboring modules or generate the clock signal, so the local module could generate its carrier to achieve the interleaving operation. Reference [26] reduced the interconnecting lines to a single line. The single signal bus carried the number of modules and sequential number at the same time, enabling the module to generate its control signal with the corresponding phase shift.

However, the interleaving line for ripple reduction still introduces the risk of a single point of failure, reducing the system's reliability. Therefore, some research has been dedicated to eliminating the interconnecting lines. Reference [27] proposed to use the spike signals on the output voltage to extract the action moment of other modules. Then, the phase-locked loop was used to realize the interleaving operation. It can achieve the interleaving automatically; however, it is noise-sensitive. Reference [28] used the local module current to construct an oscillator circuit for control, so that the system could converge to the interleaving state. However, it required a high sampling rate. References [29,30] constructed a gradient-descent-based controller by sampling the ripple of the module current at a specific time, reducing the requirements for sampling rate. References [31,32] utilized the phase of the module current and voltage to adjust the module phase. Although the interconnecting lines were eliminated, the aforementioned methods are relatively complicated, requiring high-speed analog-to-digital conversion (ADC) and high-performance digital controllers, which distinctly increases the cost.

To achieve the current sharing and current ripple reduction without interconnecting lines, while also ensuring simpler control and lower cost, this paper proposes an analog hysteresis current control method for the paralleled buck converter. The innovations are as follows:

(1) As shown in Figure 1, this paper proposes a modified parallel structure with the common output filter (L_t, C_o). The common filter can be implemented by the differential-mode filters, which are required in most of the parallel systems, and thus do not significantly increase the cost. With this structure, the state transition information of other modules can be integrated into the inductor voltage v_{Li} of each module. This configuration provides the hardware basis for the proposed control method.
(2) An analog hysteresis current controller is constructed by utilizing the inductor voltage to generate the hysteresis band. Since the waveform of v_{Li} is correlated with the state transition of other modules, such a hysteresis controller can naturally achieve the interleaving operation, and no interconnecting lines are required.
(3) The proposed hysteresis current controller can achieve the interleaving and the current control simultaneously. Additionally, the cooperation methods of the proposed current controller with the voltage droop control and the voltage outer loop are given.

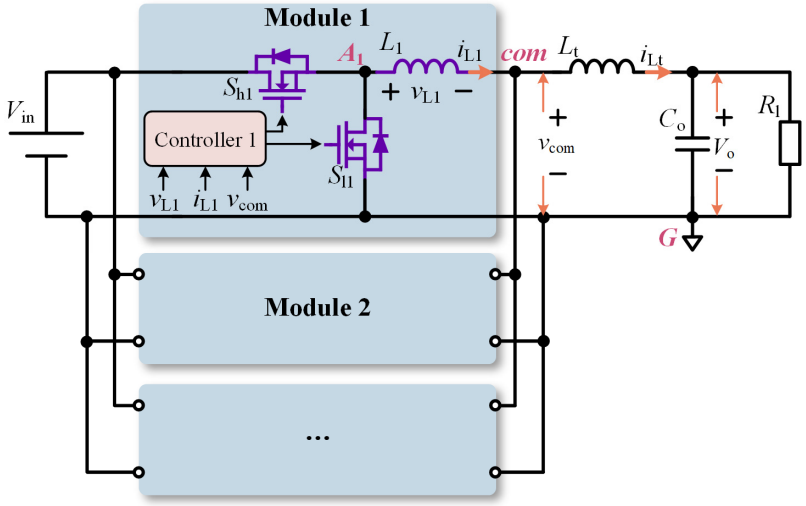


Figure 1. Structure of the paralleled buck converters with the common output filter.

This paper is organized as follows: Section 2 introduces the proposed structure of the paralleled buck converters. Next, Section 3 describes the proposed hysteresis current controller based on the shaped-inductor-voltage for the interleaving operation, and the simulation results are given. Section 4 gives the implementation methods of the proposed controller. Experimental verifications are given in Section 5. Finally, Section 6 gives the conclusions.

2. The Proposed Structure of the Paralleled Buck Converters

2.1. Structure Specification and Design Considerations

Figure 1 shows the proposed structure of the paralleled buck converters. The main design considerations are as follows:

Each module contains a control switch S_{hi}, a synchronous switch S_{li}, and an inductor L_i, and all of these buck modules are connected together at the point *com*. Then, the common output filter, consisting of the inductor L_t and the capacitor C_o, is connected to power the load R_l. The existence of L_t enables the state transitions of other modules to affect the inductor voltage v_{Li}, which is the hardware basis of the proposed controller to achieve the interleaving operation without interleaving lines. Moreover, the ripple of the total output current i_{Lt} flowing through L_t is small, which benefits the magnetic design of L_t.

For each module, a current sensor is used to sample i_{Li} for the inner hysteresis current control. A voltage sensor is used to sample the terminal voltage v_{com} to realize the outer voltage droop control. In addition, an independent winding is added on L_i to sample v_{Li}. Since v_{Li} contains the information of the state transition of other modules, it will be used to construct the hysteresis band for the current control, as well as to achieve the interleaving operation.

It is emphasized that both the current sharing and interleaving operations are achieved by fully utilizing the information of i_{Li}, v_{com}, and v_{Li}, and thus, no interconnecting lines are required.

2.2. Modeling and Analyses of the Inductor Voltage

For illustration purposes, the following analysis is conducted with the three-module-paralleled buck converter.

The equivalent circuit of the three-module-paralleled system is given in Figure 2a and v_{Ai} (i = 1, 2, 3) is the switching node voltage. The switching function for module i (i = 1, 2, 3) is defined as s_i. When S_{hi} is on and S_{li} is off, module i is in the on-state, and thus s_i = 1. On the contrary, when S_{hi} is off and S_{li} is on, module i is in the off-state and thus s_i = 0. Therefore, v_{Ai} can be expressed as

$$v_{Ai} = s_i V_{in}. \tag{1}$$

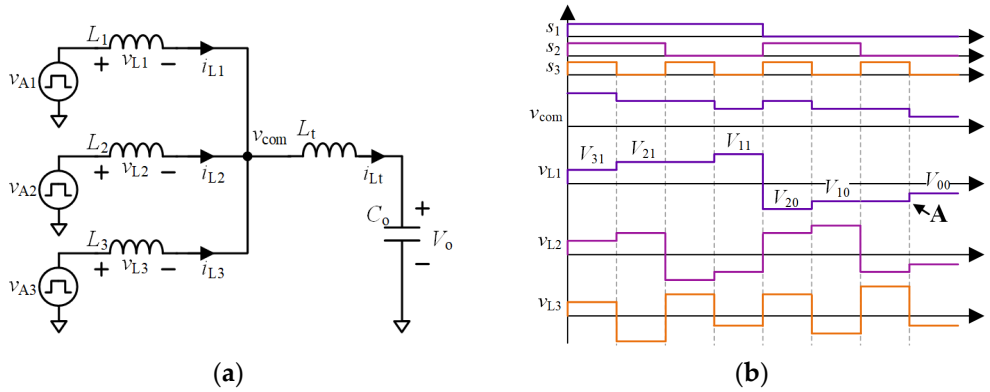


Figure 2. (**a**) Equivalent circuit of the paralleled buck converters with common output filter and (**b**) its voltage waveforms.

Considering that the modules are identical, $L_1 = L_2 = L_2 = L$ is satisfied. According to the superposition theorem, v_{com}, the voltage of the common point *com*, can be obtained as

$$v_{com} = \frac{LV_o + s_1 L_t V_{in} + s_2 L_t V_{in} + s_3 L_t V_{in}}{L + 3L_t}. \tag{2}$$

According to Equations (1) and (2), the voltage of inductor L_1, L_2, and L_3 can be calculated as:

$$v_{L1} = \frac{(L + 2L_t)V_{in}s_1 - L_t V_{in}(s_2 + s_3) - LV_o}{L + 3L_t}, \tag{3}$$

$$v_{L2} = \frac{(L + 2L_t)V_{in}s_2 - L_t V_{in}(s_1 + s_3) - LV_o}{L + 3L_t}, \tag{4}$$

$$v_{L3} = \frac{(L + 2L_t)V_{in}s_3 - L_t V_{in}(s_1 + s_2) - LV_o}{L + 3L_t}. \tag{5}$$

From Equations (3)–(5), it can be observed that v_{Li} is related to the input voltage V_{in}, the output voltage V_o, and the states (the on-state or off-state expressed by the switching function s_i) of the three modules. Figure 2b gives the voltage waveforms of v_{L1}, v_{L2}, and v_{L3} when s_1, s_2, and s_3 take different values. Taking v_{L1} as an example, Equation (6) gives the value of v_{L1} with different s_i:

$$v_{L1} = \begin{cases} V_{11} = \alpha[V_{in}(L + 2L_t) - LV_o] & (s_1 = 1, \Sigma s_i = 1) \\ V_{21} = \alpha[(L + L_t)V_{in} - LV_o] & (s_1 = 1, \Sigma s_i = 2) \\ V_{31} = \alpha(LV_{in} - LV_o) & (s_1 = 1, \Sigma s_i = 3) \\ V_{00} = -\alpha LV_o & (s_1 = 0, \Sigma s_i = 0) \\ V_{10} = \alpha(-L_t V_{in} - LV_o) & (s_1 = 0, \Sigma s_i = 1) \\ V_{20} = \alpha[-2L_t V_{in} - LV_o] & (s_1 = 0, \Sigma s_i = 2) \end{cases}, \tag{6}$$

where $\alpha = 1/(L + 3L_t)$, and $\Sigma s_i = s_1 + s_2 + s_3$. For the voltage value V_{ij} with different s_i, the subscript i represents Σs_i (the number of modules that are in the on-state), and the subscript j represents the state of the local module. For example, $v_{L1} = V_{20}$ means that two modules in the system are in the on-state and module 1 is in the off-state. Furthermore, V_{ij} satisfies the relation $V_{11} > V_{21} > V_{31} > 0 > V_{00} > V_{10} > V_{20}$.

From (6), several interesting features can be observed. Firstly, v_{L1} is related to s_i. Therefore, when s_i changes, v_{L1} changes. For example, as point A in Figure 2b, when $s_1 = 0$, $s_2 = 0$, and s_3 jump from 1 to 0, v_{Li} jumps synchronously from V_{10} to V_{00}. This means that v_{L1} contains the switching states of the other modules, i.e., the phase information. Similarly, the inductor voltages of the other modules exhibit the same characteristics. Therefore, it is possible to utilize v_{Li} to achieve the interleaving operation using appropriate methods.

3. Hysteresis Current Controller Based on Shaped-Inductor-Voltage

Based on the above structure, this paper proposes a hysteresis current controller based on the shaped-inductor-voltage, which utilizes the integrated phase information in v_{Li} to achieve symmetric interleaving without the interleaving line. The subsequent analysis is conducted based on the case of $D < 1/3$ to illustrate the proposed idea.

3.1. Construction of the Proposed Current Controller

The proposed method is based on the hysteresis current controller. It is one of the classical control methods [33]. Figure 3a shows the waveforms of the traditional hysteresis current controller, which has a fixed hysteresis band with the upper limit h_H and the lower limit h_L. The voltage v_{iei} is the converted current error, which satisfies $v_{iei} = k_{iv} i_{ei} = k_{iv}(i_{Li} - I_{refi})$ (k_{iv} denotes the current–voltage ratio, i_{ei} denotes the error between the inductor current value i_{Li} and the current reference I_{refi}). When v_{iei} exceeds the preset limit h_H or h_L, the control signal g_i changes to alter the operating state of module i, thereby limiting v_{iei} within the hysteresis band. The hysteresis current controller has the advantages of being simple, fast, and stable. However, since the operations of the three modules are independent when this method is directly utilized without communicating the phase information, the frequencies of the three modules are likely to be different, and it is challenging to achieve the interleaving operation.

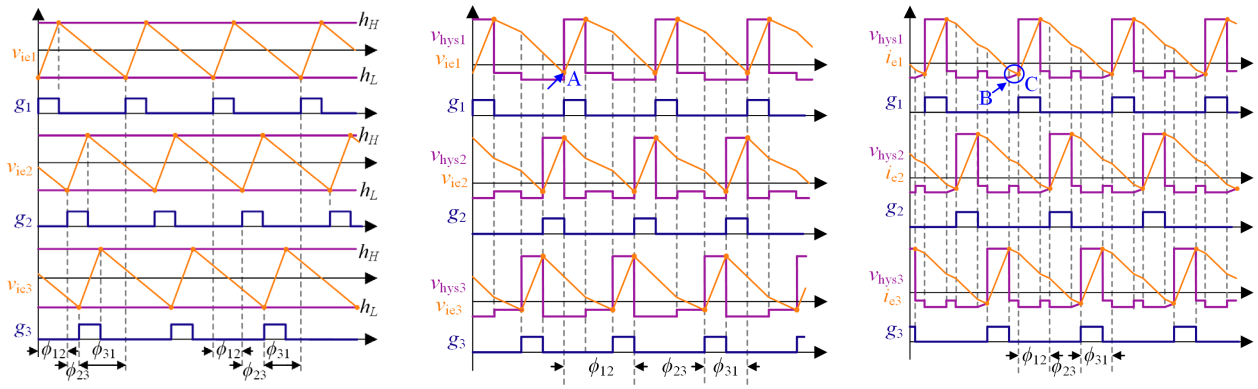


Figure 3. Construction of the hysteresis current controller. (**a**) Traditional hysteresis current controller, (**b**) hysteresis current controller with v_{Li} directly constructing the hysteresis band and (**c**) the proposed hysteresis current controller based on the shaped-inductor-voltage.

Therefore, the inductor voltage v_{Li}, which contains the phase information, is directly used to construct the hysteresis band, as illustrated in Figure 3b. This hysteresis band produces the correction of the control signals for the modules. For example, as point A shows in Figure 3b, when g_2 changes from 1 to 0, v_{hys1} simultaneously steps upward, causing v_{ie1} to exceed v_{hys1}; hence, g_1 jumps to 1. This correction enables the three modules to operate at the same switching frequency without interconnecting lines.

However, the phase angle ϕ_{12}, ϕ_{23}, and ϕ_{31} between these modules are not the desired value (i.e., $\phi_{12} = \phi_{23} = \phi_{31} = 120°$). This is because the voltage step resulting from the state transition of other modules causes an immediate step in the hysteresis band, which may immediately change the module state. To fix this problem, the voltage jump (as shown in point B in Figure 3c) is modified as a ramp (as shown in region C in Figure 3c). This modification delays the switching moment. (As shown in region C. After g_3 jumps to 0, v_{hys1} does not follow the inductor voltage, instead, it gradually attenuates until it equals v_{ie1}, and subsequently, g_1 jumps to 1). Based on the designs above, a hysteresis current controller based on the shaped-inductor-voltage is proposed in this paper. The proposed hysteresis current controller can automatically converge to the symmetric interleaving operation state. The detailed analysis is given as follows.

3.2. Analysis of Interleaving Operation

The steady state waveforms of the proposed controller are given on the left of Figure 4 (see the "steady state" region). The errors of the waveform transformation process and the delay and error of the current sampling are neglected in the analysis. The upper and lower limits of the hysteresis band v_{hysi} can be expressed as

$$h_{\max i} = k_i V_{10}, \tag{7}$$

$$h_{\min i} = k_i V_{01}, \tag{8}$$

where i = 1~3, and k_i is the voltage adjustment coefficients of module i, which are constant and determined by the hardware. Since the modules are the same, $k_1 = k_2 = k_3 = k$, and $h_{min}1 = h_{min}2 = h_{min}3 = h_{min}$, $h_{max}1 = h_{max}2 = h_{max}3 = h_{max}$ are satisfied.

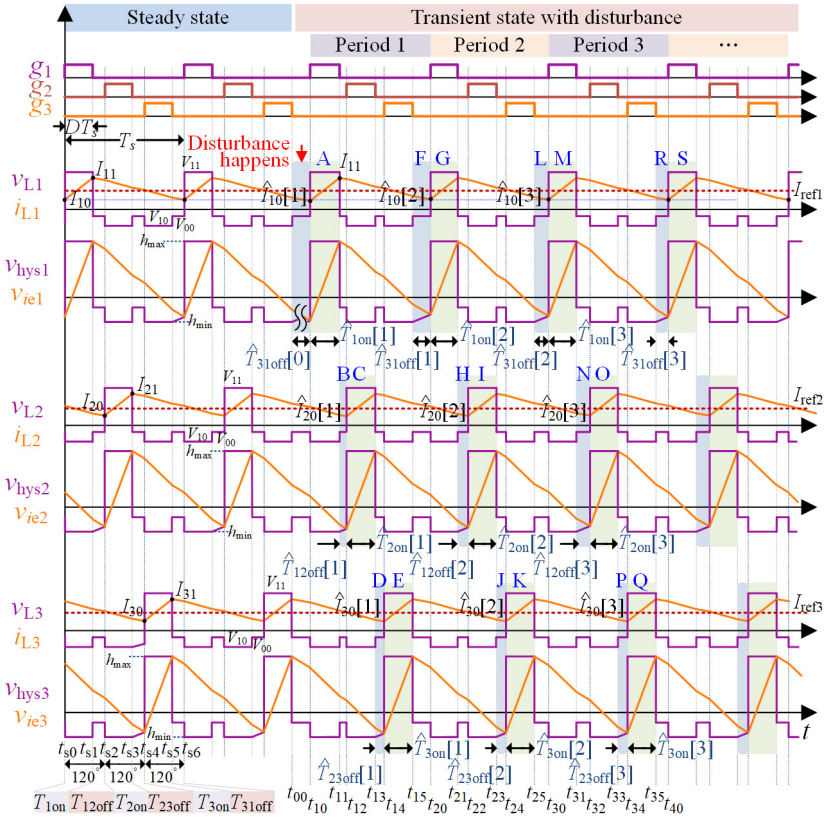


Figure 4. Key waveforms of the steady state and the transient state for $D < 1/3$.

According to the waveforms of the inductor current and the hysteresis band, the minimum and maximum inductor currents in the steady state satisfy the following relationships:

$$\begin{aligned} I_{10} &= (h_{\min} + \lambda_1 T_{31off})/k_{iv} + I_{ref1} \\ &= h_{\max}/k_{iv} + a_{00}(T_{12off} + T_{23off} + T_{31off}) + a_{10}(T_{2on} + T_{3on}) + I_{ref1} \end{aligned}, \tag{9}$$

$$\begin{aligned} I_{20} &= (h_{\min} + \lambda_2 T_{12off})/k_{iv} + I_{ref2} \\ &= h_{\max}/k_{iv} + a_{00}(T_{23off} + T_{31off} + T_{12off}) + a_{10}(T_{3on} + T_{1on}) + I_{ref2} \end{aligned}, \tag{10}$$

$$\begin{aligned} I_{30} &= (h_{\min} + \lambda_3 T_{23off})/k_{iv} + I_{ref3} \\ &= h_{\max}/k_{iv} + a_{00}(T_{31off} + T_{12off} + T_{23off}) + a_{10}(T_{1on} + T_{2on}) + I_{ref3} \end{aligned}, \tag{11}$$

$$I_{11} = h_{\max}/k_{iv} + I_{ref1} = I_{10} + a_{11} T_{1on}, \tag{12}$$

$$I_{21} = h_{\max}/k_{iv} + I_{ref2} = I_{20} + a_{11} T_{2on}, \tag{13}$$

$$I_{31} = h_{\max}/k_{iv} + I_{ref3} = I_{30} + a_{11}T_{3on}, \tag{14}$$

where I_{i0} and I_{i1} are the minimum and maximum current of module i, respectively; I_{refi} is the current reference of module i; a_{00}, a_{10}, and a_{11} are the current changing rates, and $a_{00} = V_{00}/L$, $a_{10} = V_{10}/L$; and $a_{11} = V_{11}/L$ are satisfied. λ_i is the attenuation rate of the ramp in v_{hysi}. λ_i and k_{iv} are determined by the hardware design and considering that the parameters of the three modules are the same, $\lambda_1 = \lambda_2 = \lambda_3 = \lambda$ are satisfied. T_{1on}, T_{2on}, and T_{3on} are the periods when module 1, module 2, and module 3 are in the on-state, respectively. T_{12off}, T_{23off}, T_{31off} are the periods of t_{s1}~t_{s2}, t_{s3}~t_{s4}, t_{s5}~t_{s6}, respectively, as shown in Figure 4.

Considering a small disturbance happens during t_{00}~t_{11} on module 1, which breaks the steady state, I_{refi} is assumed to be constant and equal to its steady-state value during this process. Since I_{refi} is generated by the voltage outer loop with a relatively slow response speed compared to the current inner loop, this assumption is reasonable. The small disturbance causes a deviation of $\Delta T_{31off}[0]$ from the steady-state value T_{31off}, and the length of this time interval $\hat{T}_{31off}[0]$ is

$$\hat{T}_{31off}[0] = T_{31off} + \Delta T_{31off}[0]. \tag{15}$$

With the analysis in Appendix A, the expressions of $\Delta T_{31off}[k]$ can be derived as

$$\Delta T_{31off}[1] = \frac{\alpha a_{00}(a_{11} - a_{10})[(2a_{11} - a_{10}) \cdot \lambda_{iv} - a_{00}a_{11}]}{a_{11}^2(\lambda_{iv} - a_{00})^2}\Delta T_{31off}[0], \tag{16}$$

$$\Delta T_{31off}[2] = (\alpha^3 + 2\alpha^2)\Delta T_{31off}[1] + \frac{\alpha^2(\alpha+1)a_{00}\lambda_{iv}(a_{11} - a_{10})^2}{a_{11}^2 \cdot (\lambda_{iv} - a_{00})^2}\Delta T_{31off}[0], \tag{17}$$

$$\Delta T_{31off}[k] = (\alpha^3 + 3\alpha^2)\Delta T_{31off}[k-1] + \alpha^3\Delta T_{31off}[k-2]\ (k \geq 2)\Big), \tag{18}$$

where the coefficient α is

$$\alpha = -\frac{a_{10}\lambda_{iv} - a_{00}a_{11}}{a_{11}(\lambda_{iv} - a_{00})}, \tag{19}$$

where λ_{iv} satisfies $\lambda_{iv} = \lambda/k_{iv}$.

The coefficients are relatively complex. Therefore, to demonstrate that the system can return to the steady state under the disturbance, the hardware parameters in Table A1 are substituted into Equations (16)–(18). Figure 5 shows the variation curve of $\Delta T_{31off}[k]/\Delta T_{31off}[0]$ with respect to the number of recurrences. It can be seen that $\Delta T_{31off}[k]/\Delta T_{31off}[0]$ reduces rapidly when $k \geq 2$, $\Delta T_{31off}[k]/\Delta T_{31off}[0] \approx 0$ holds when the recurrence number $k \geq 17$. This demonstrates that $\Delta T_{31off}[k]$ gradually approaches zero after several periods, i.e., $\hat{T}_{31off}[k]$ can converge to the corresponding steady-state value T_{31off}. Similarly, the deviations of other intervals can also converge to zero. Therefore, the system can recover to a steady state after the small disturbance, which indicates that the proposed controller exhibits good stability. Figure A1 in Appendix A gives more numerical results with different V_{in}, V_o, or λ. The curves show that $\Delta T_{31off}[k]$ can also gradually approach zero under these conditions. This further validates that the proposed controller can recover to the steady state.

When the modules are working under the steady state, the three modules in the system have the same period T_s (frequency), i.e., $T_s = T_{1on} + T_{2on} + T_{3on} + T_{12off} + T_{23off} + T_{31off}$. Therefore, according to the volt-second balance principle, these modules satisfy

$$V_{00}(T_{12off} + T_{23off} + T_{31off}) + V_{10}T_{1on} + V_{01}(T_{2on} + T_{3on}) = 0 \tag{20}$$

$$V_{00}(T_{12off} + T_{23off} + T_{31off}) + V_{10}T_{2on} + V_{01}(T_{3on} + T_{1on}) = 0 \tag{21}$$

$$V_{00}(T_{12off} + T_{23off} + T_{31off}) + V_{10}T_{3on} + V_{01}(T_{1on} + T_{2on}) = 0 \tag{22}$$

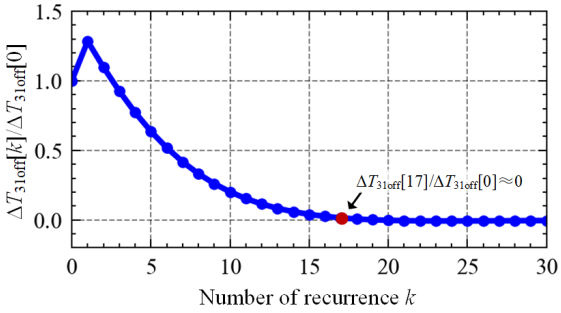


Figure 5. Variation curve of $\Delta T_{31off}[k]/\Delta T_{31off}[0]$.

The difference between (20) and (21) yields $(V_{10} - V_{01})(T_{1on} - T_{2on}) = 0$. Since $V_{10} > 0 > V_{01}$ holds, it is established that $V_{10} - V_{01} > 0$ consistently holds. Therefore, $T_{1on} = T_{2on}$ can be derived. With the similar method, it can be derived that

$$T_{1on} = T_{2on} = T_{3on}, \tag{23}$$

which indicates that the duty cycles of the three modules in the system are the same for the steady state.

This represents that the three modules have the same duty cycle D in the steady state. With (23), the difference between (9) and (10) yields $T_{12off} = T_{31off}$. With similar method, the following expression holds

$$T_{12off} = T_{23off} = T_{31off}. \tag{24}$$

Therefore, based on Equations (23) and (24), it can be derived that

$$T_{1on} + T_{12off} = T_{2on} + T_{23off} = T_{3on} + T_{31off} = T_s/3, \tag{25}$$

in other words, the phase angles between the three modules satisfy the relationship of $\phi_{12} = \phi_{23} = \phi_{31} = 120°$. The above analyses prove that with the proposed hysteresis current controller, the three modules can realize the symmetric interleaving in the steady state.

The steady-state waveforms for the cases of $1/3 \leq D \leq 2/3$ and $D \geq 2/3$ are shown in Figure 6. Although the position of the ramp in v_{hysi} is slightly different, it can also demonstrate that the symmetric interleaving operation can be achieved using a similar analysis method.

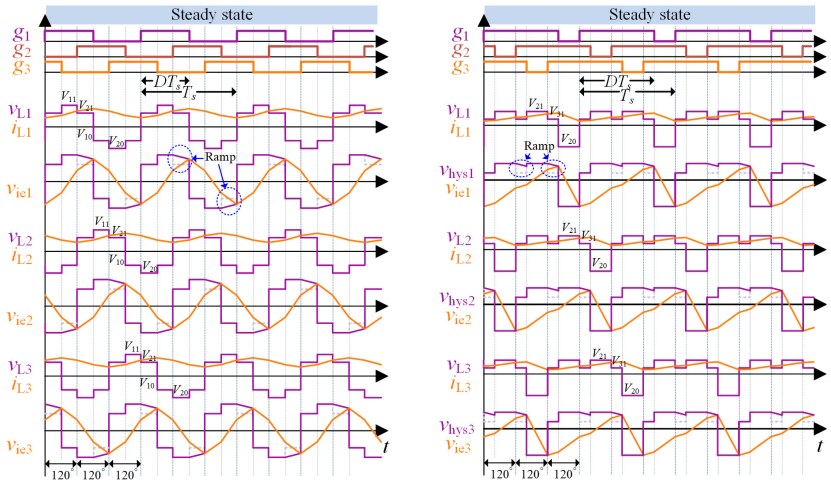


Figure 6. Steady-state waveforms for the case of (**a**) $1/3 \leq D \leq 2/3$ and (**b**) $D > 2/3$.

Although the above analysis is based on the three-module-paralleled system, the proposed method can be utilized in the system with two or more modules, and the analysis methods above and the conclusions still hold.

3.3. Simulation Verification

To validate the above analysis, the paralleled buck converters are built in MATLAB Simulink with the parameters in Table A1.

Figure 7a depicts the dynamic process with the disturbance of the current reference I_{ref}, with V_{in} = 48 V. During the simulation, $I_{ref1} = I_{ref2} = I_{ref3} = I_{ref}$ are given, and I_{ref} is set to change from 1.8A to 0.9A. Before the disturbance, the three modules achieve the symmetric interleaving operation with phase angles of 120°, as shown in Figure 7b. When the disturbance occurs, the phase angles are affected but the system can gradually converge to the steady state with the phase angle of 120°, as shown in Figure 7c. This verifies that the three-module-paralleled system can automatically adjust the phase after disturbance and can converge to the symmetric interleaving state. Furthermore, Figure 7d shows the key waveforms of the proposed hysteresis current controller in module 1, with I_{ref} = 1.8A. A hysteresis delay of 0.05 V for realizing the comparison of v_{ie1} and v_{hys1} is used to enhance the anti-interference capability. The waveforms well match the analysis waveforms in Figure 4. It can be observed that several voltage jumps exist on v_{L1}, which are introduced by the actions of other modules in the system, and these voltage jumps are adjusted to the voltage ramps on v_{hys1}, e.g., region A in Figure 7d.

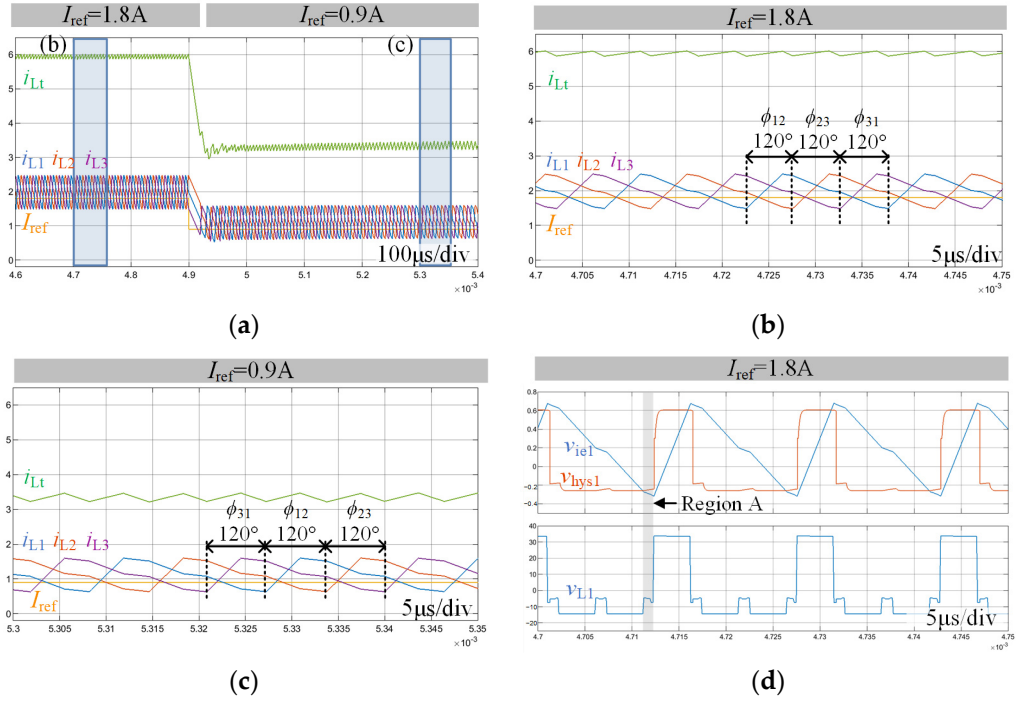


Figure 7. Simulation results of (**a**) the dynamic process with the disturbance of I_{ref}, (**b**,**c**) the zoomed views of the steady states and (**d**) the key waveforms of the proposed hysteresis current controller.

Figure 8a,b give the simulation results of the steady state waveforms for $1/3 \leq D \leq 2/3$ (with V_{in} = 24 V and I_{ref} = 2A) and $D > 2/3$ (with V_{in} = 16 V and I_{ref} = 2A), respectively. The waveforms also match those in Figure 6 and the symmetric interleaving can also be achieved in both cases.

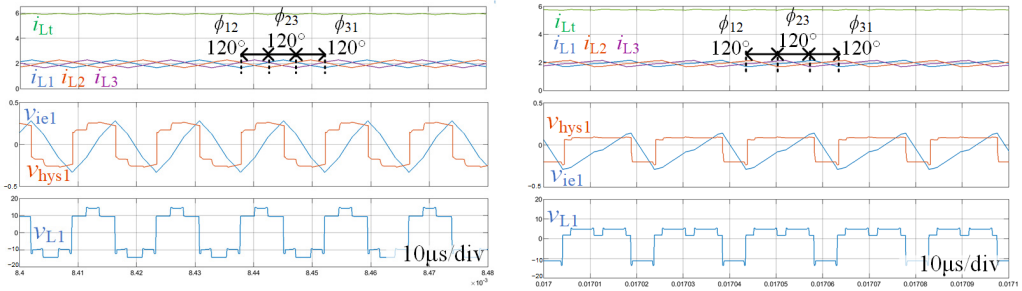


Figure 8. Steady-state waveforms for (**a**) $1/3 \leq D \leq 2/3$ and (**b**) $D > 2/3$.

Figure 9a gives the simulation results of a six-module-paralleled system and it shows that the system can restore stability after module addition. The zoomed views in Figure 9b,c show that both the five-module-paralleled system and the six-module-paralleled system can operate in the symmetric interleaving states, with phase angles of 72° (360°/5) and 60° (360°/5), respectively. The proposed method is effective for the system with more modules. In addition, it has hot-plug capability and the phase angles can automatically adjust.

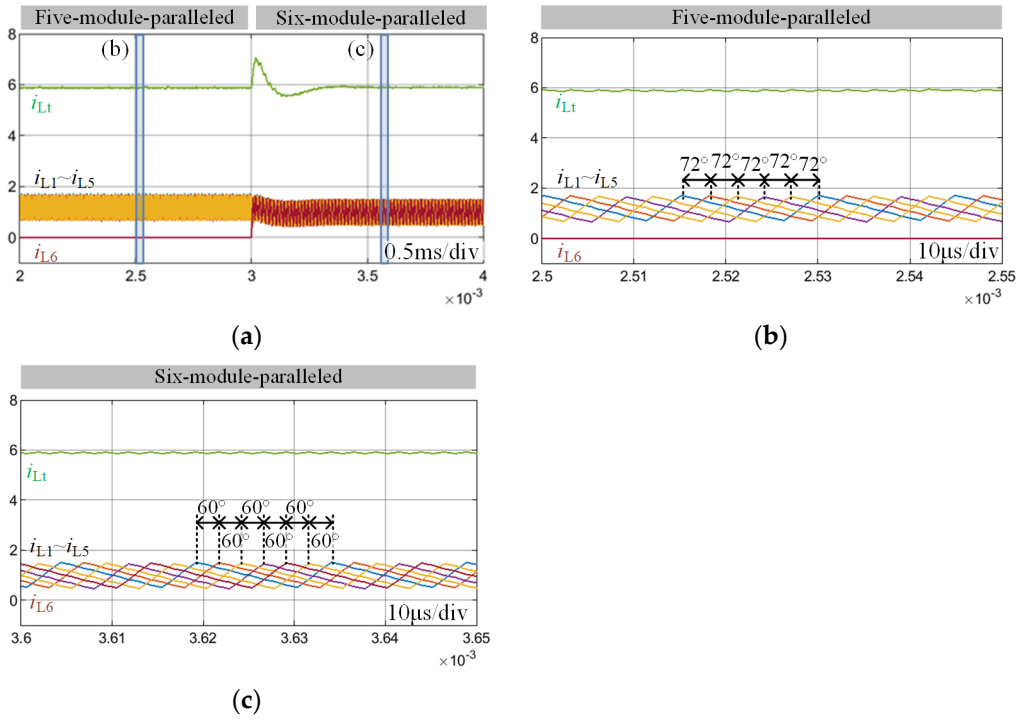


Figure 9. Simulation results of the module addition. (**a**) The dynamic process and the zoomed views of the stable state of (**b**) the five-module-paralleled system and (**c**) the six-module-paralleled system.

4. Implementation of the Proposed Hysteresis Current Controller

4.1. Hardware Design of the Proposed Hysteresis Current Controller

The proposed hysteresis current controller is implemented by analog methods.

According to the analysis above, the proposed hysteresis current controller has integrated the phase information into the waveform of v_{Li} to eliminate the interconnecting lines. However, the actions of the switches result in high-frequency noise on v_{Li}, and the noise increases with the increase in the operating voltage and current. Therefore, when implementing the proposed hysteresis current controller, it is necessary to use some methods, such as isolated sampling and filtering, to cope with the noise and to guarantee the stability of control.

Figure 10 shows the circuit diagram of the controller in module i. An independent winding of W turns is added to the inductor to sample v_{Li} and the isolated sampling method ensures strong noise immunity. The sampled signal v_{seci} is proportional to v_{Li} and is used to construct the hysteresis band v_{hysi}. Furthermore, the low-pass filter with a bandwidth of 1.06 MHz is employed to filter out the high-frequency noise while not affecting the voltage jump information (i.e., phase information) in v_{seci}. To generate the ramp, the positive part and negative part of the waveforms of v_{seci} are separately shaped.

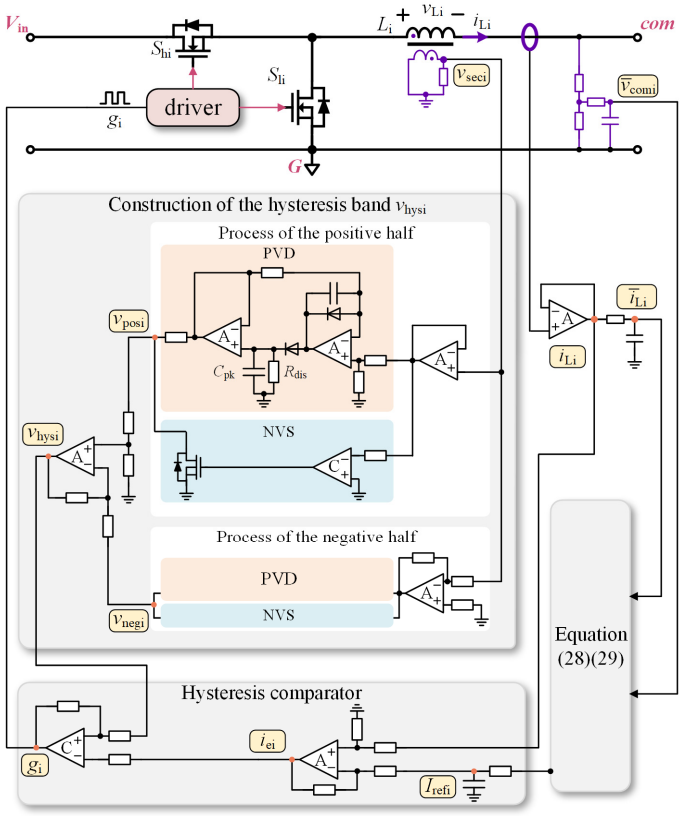


Figure 10. The circuit diagram of module i.

For the positive part shaping, a peak voltage detection (PVD) circuit is utilized to detect and maintain the maximum value. The discharging resistor R_{dis} is paralleled across the capacitor C_{pk} of the PVD circuit to form the required ramp. When v_{seci} falls, C_{pk} discharges through R_{dis}, converting the voltage jump into the slowly discharging voltage. Moreover, during the period when v_{seci} is less than zero, the output of the PVD circuit is clamped to 0 by the negative voltage shielding (NVS) circuit, avoiding its influence on the shaping of the negative part. Thereout, the shaped voltage v_{posi} for the positive part is obtained. The values of C_{pk} and R_{dis} need to be chosen carefully. C_{pk} should not be too large so that the PVD circuit can track the peak value quickly, while R_{dis} needs to be carefully chosen to ensure that the ramp always exists before the next state transition of this module. Furthermore, the low-pass filter is added to each stage of the operational amplifier to avoid noise interference.

For the negative part shaping, v_{seci} is firstly inverted by the phase inverter, and then v_{negi} can be obtained using the same method of processing v_{posi}. Subsequently, v_{posi} and v_{negi} are combined by the subtractor to obtain v_{hysi}. Both v_{hysi} and the current error i_{ei} of module i are fed into the hysteresis comparator to generate the control signal g_i for module i. The hysteresis comparator can suppress noise and enhance the stability of the comparison.

From the implementation process of the proposed hysteresis current controller, it can be seen that to construct v_{hysi} with v_{Li}, the analog basis method is the most convenient and cost-efficient way (in the digital method, the high-speed ADC and digital controller are

required to realize hysteresis operation, leading to an increase in implementation costs). Furthermore, due to the simple structure of the proposed hysteresis control, only the voltage adjustment coefficients k_i (voltage divider resistors) and attenuation rate λ (C_{pk} and R_{dis}) need to be tuned.

4.2. Cooperation with the Voltage Outer Loop and the Voltage Droop Control

Furthermore, the proposed current hysteresis controller can achieve both the interleaving and the inner loop current control. The required current reference I_{refi} comes from the voltage droop control for current sharing and the voltage outer loop, which can be implemented with common methods.

To realize the voltage outer loop, the output voltage V_o is rebuilt from the terminal voltage v_{comi} of each module. v_{comi} of module i can be expressed with

$$v_{comi} = v_{Lt} + v_o, \tag{26}$$

where v_{Lt} is the transient voltage across the common inductor L_{t}, and v_{o} is the transient output voltage. Filtering the signal v_{comi} with a simple *RC* filter, the low-frequency components of v_{comi}, namely $\bar{v}_{comi}$, can be obtained (the time constant of the *RC* filter should be much smaller than that of the outer voltage loop). Mathematically, $\bar{v}_{comi}$ is

$$\overline{v}_{comi} = \overline{v}_{Lt} + \overline{v}_o \approx V_o, \tag{27}$$

In (27), the average inductor voltage $\bar{v}_{Lt}$ converges to zero due to the volt-second balance principle; therefore, $\bar{v}_{comi}$ is dominated by the filtered average voltage $\bar{v}_o$, i.e., V_o. Therefore, $\bar{v}_{comi}$ can be used to estimate V_o as the feedback in the outer voltage loop. The expression of the voltage outer loop based on the PI (Proportional-Integral) controller can be expressed as

$$I_{refi} = K_p(V_{refi_dr} - \overline{v}_{comi}) + K_i \int (V_{refi_dr} - \overline{v}_{comi}), \tag{28}$$

where K_p and K_i are the proportional and integral coefficients, respectively. Moreover, V_{refi_dr} is the voltage reference with a droop feature. The output of the controller is treated as the current reference I_{refi} of the inner hysteresis controller.

For voltage droop purpose, V_{refi_dr} is obtained by introducing the average of the sampled current value $\overline{I}_{Li}$ as feedback

$$V_{refi_dr} = V_{ref} - k_{dr}\overline{I}_{Li}, \tag{29}$$

where k_{dr} represents the droop coefficient and V_{ref} represents the voltage reference value. With (29), the goal of the voltage droop is to achieve the balance of $\overline{I}_{Li}$. Since $\overline{I}_{Li}$ equals the output current I_{oi}, the output currents can also be naturally shared.

5. Experimental Verification and Discussion

To experimentally validate the proposed hysteresis current controller, a three-module system prototype was built with the parameters in Table A1, as shown in Figure 11. It can be seen that there are only power connections among the modules, and no interconnection lines exist for signal transmission.

Figure 12a,b show the dynamic processes of the load transitions while maintaining V_o at 12 V. It can be seen that the paralleled system can achieve the regulation of V_o. After the load addition in Figure 12a, the steady-state value of V_o decreased from the original value of 11.99 V to 11.85 V due to the voltage droop control, and after the load removal in Figure 12b, V_o recovered from 11.85 V to 11.99 V. Meanwhile, the inductor currents of the three modules, i_{L1}, i_{L2}, and i_{L3}, are always overlapped, which indicates that the

current sharing can be achieved even in the dynamic processes. The current sharing error is within 4.0%.

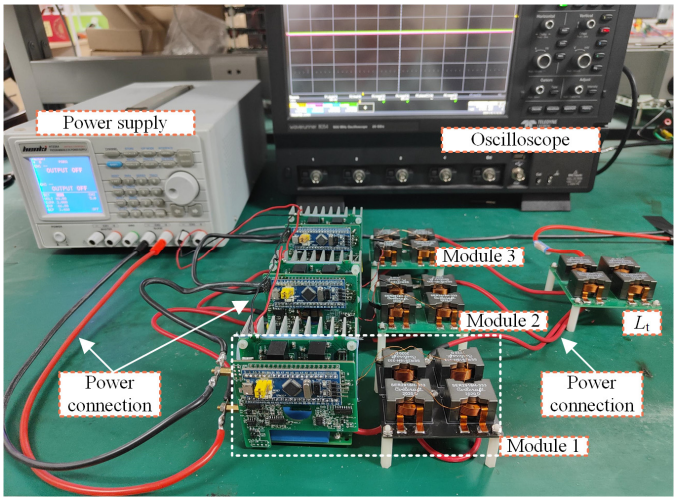


Figure 11. Prototype of the three-module-paralleled buck converter.

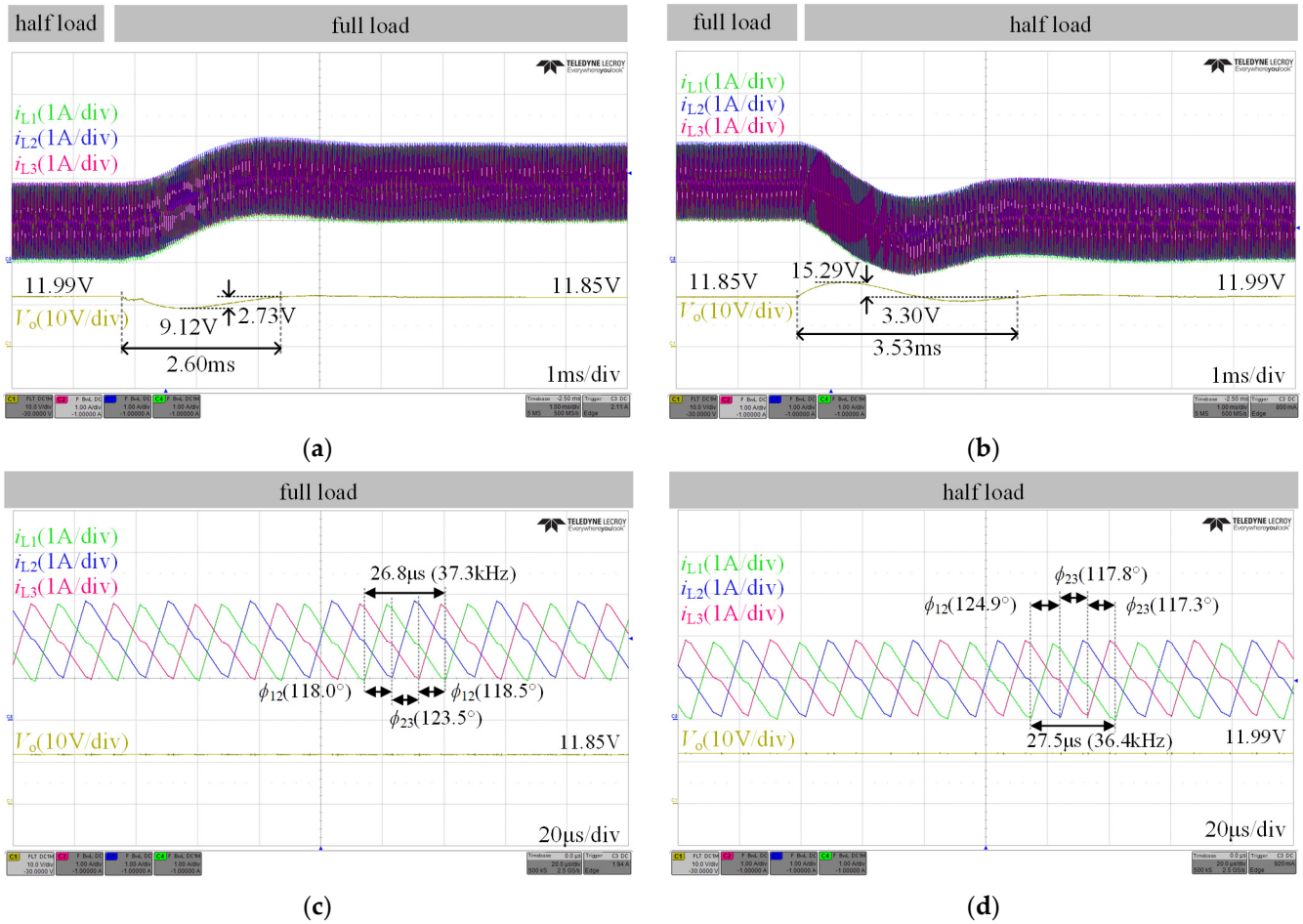


Figure 12. Measured waveforms of the dynamic process of (**a**) the load addition and (**b**) the load removal, and the zoomed views of the steady states of (**c**) full load and (**d**) half load.

The interleaving operation can be further observed in Figure 12c,d. Figure 12c shows the zoomed view of the steady state with the full load, and the phase angles ϕ_{12}, ϕ_{23}, and ϕ_{31} were 118.0°, 123.5°, and 118.5°, respectively. Figure 12d shows the zoomed view of

the steady state with the half load, and the phase angles ϕ_{12}, ϕ_{23}, and ϕ_{31} were 124.9°, 117.8°, and 117.3°, respectively. The phase angles of both states were close to the desired value of the symmetric interleaving 120° (360°/3), with a maximum relative error of 4.1%. This demonstrates that the proposed method can automatically achieve the symmetric interleaving operation.

From the experimental results above, it can be seen that for the proposed method, the phase shift error and the current sharing error exist. The phase shift error results from the inconsistencies of the hardware parameters, including the delay of the comparator, and the accuracy of the resistors. These inconsistencies are inherent problems of using the analog circuits for generating the control signals. For the methods with interconnecting lines, the information on the lines is always generated by the digital controllers. Therefore, the phase shift error and the current sharing error result from the accuracy of the phase lock loop (PLL) and the ADC. For example, [26] utilizes one interconnecting line to carry a synthetic signal generated by the operating modules. With the synthetic signal, each module can decode the total number of operating modules and its sequential number, thereby achieving the interleaving and current sharing. The phase shift error results from the PLL, e.g., the phase shift error of the method in [26] is about 5.4%. Furthermore, the error of the proposed method can be further decreased by selecting the resistors with higher precision and analog devices with more consistent characteristics or integrating the circuits by using integrated circuit technology to improve the consistency.

Figure 13 gives the waveforms of two extreme situations, i.e., the module removal and addition. Figure 13a gives the waveforms of the dynamic process when removing module 3 from the three-module-paralleled system. After the removal of module 3, V_{o} stabilized at 11.77 V after 1.96 ms. Furthermore, i_{L1} and i_{L2} increased simultaneously and maintained the current sharing throughout the dynamic process. Figure 13b gives the zoomed view of the module removal. It can be observed that when module 3 was removed, the phase angles of the remaining modules automatically adjusted and gradually approached the values under the symmetric interleaving state. The zoomed view of the steady state is given in Figure 13c and it shows that the two remaining modules could also achieve the symmetric interleaving operation with the phase angles of 177.9° and 182.1°, which are close to 180° (360°/2) with a relative error of 1.2%.

Figure 13d gives the dynamic waveforms of the module addition. The addition of module 3 to a two-module-paralleled system resulted in the fluctuations of V_{o}; nevertheless, V_{o} could stabilize at 11.84 V with a settling time of 2.41 ms. As i_{L3} increased, i_{L1} and i_{L2} decreased, and the current sharing among the three modules was achieved after about 30 ms. The transient of module addition is shown in Figure 13e, and it shows that when module 3 was added, the phase angles adjusted automatically. Figure 13f shows the zoomed view of the steady state, where the two-module-paralleled system could also achieve the symmetric interleaving operation with the maximum relative error of 1.2%.

The above experimental results demonstrate that the proposed hysteresis current controller has the hot-plug capability, which enhances the modularity, scalability and redundancy of the system.

Most of the hot-plug methods are achieved based on digital controllers. Therefore, these methods require detection of the circuit state to determine whether the module is added or removed. Then, the controller can adjust the phase shift cycle by cycle based on the detection results, and the system recovers to a stable state after multiple periods. On the contrary, the proposed method uses the analog hysteresis current controller to achieve both the current sharing and the interleaving. Consequently, once the module is added or removed, the waveform of v_{Li} is immediately changed, resulting in the synchronous changes in the hysteresis band v_{hysi}. Furthermore, the inductor current can quickly respond to the change in v_{hysi}. Therefore, the dynamic processes can be faster.

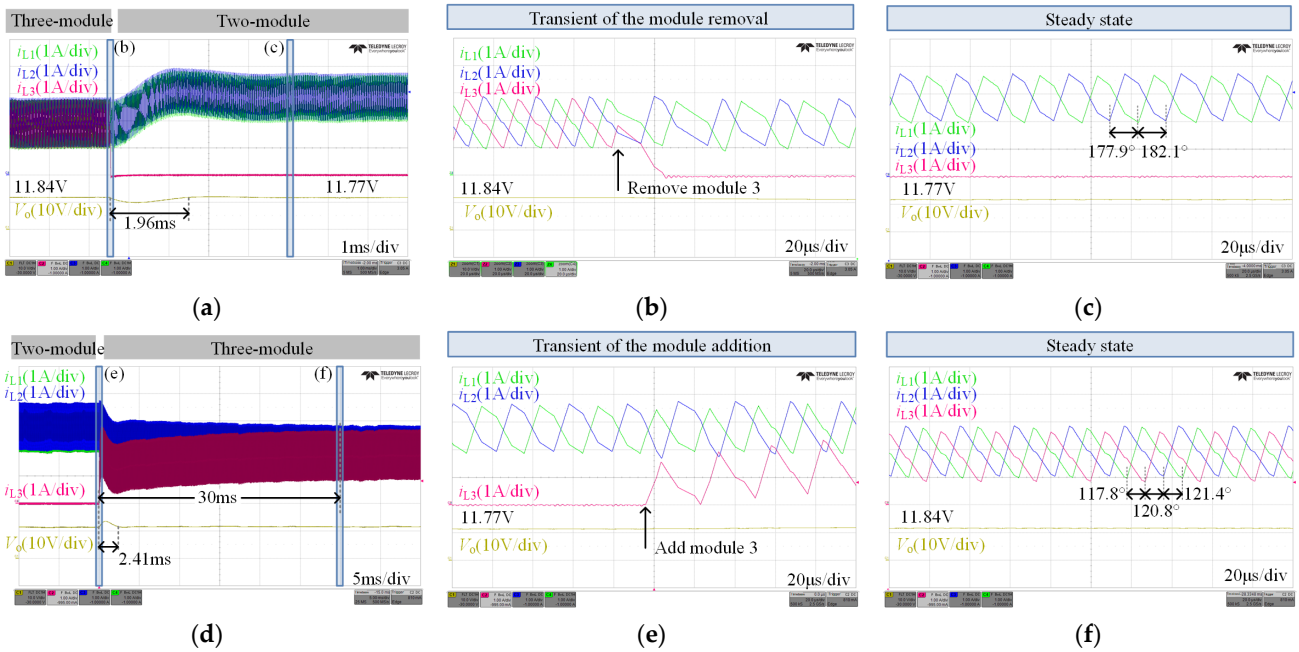


Figure 13. Dynamic processes of (**a**) the module removal and its zoomed views (**b**,**c**), and (**d**) the module addition and its zoomed views (**e**,**f**).

To compare the hot-plug performance, the simulation of the proposed method under similar conditions of the method in [31] (It is realized with digital controllers without the interleaving lines) was conducted. The parameters are given in Table A2 and the results are given in Figure 14. It can be seen that after the module addition, V_o recovered to the stable value after 731 μs. Additionally, the symmetric interleaving and current sharing were achieved after 348 μs and 3 ms, respectively. In contrast, for the method in [31], the dynamic process lasted for 13 ms. In addition, for the module removal process, the current sharing is always achieved. V_o recovered to the stable value after 447 μs and the symmetric interleaving was achieved after 316 μs. These times are much shorter than those of the method in [31] (13 ms). Therefore, the dynamic processes of both the module addition and removal are much faster than the method in [31].

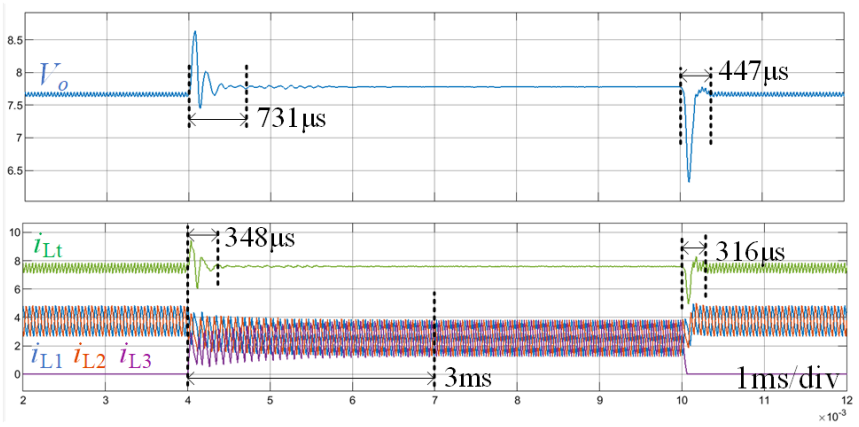


Figure 14. Simulation of the dynamic processes of module addition and removal.

6. Conclusions

This paper proposes a hysteresis current controller for the paralleled buck converters to achieve the interleaving operation without the need for interconnecting lines. Firstly, the paralleled structure is slightly modified to integrate the phase information into the

inductor voltage in the module. Then, the hysteresis current controller based on the shaped-inductor-voltage is designed and with the controller, the symmetric interleaving is automatically achieved. The effectiveness of the proposed control method is validated through simulations and experiments. The results confirm the following:

(1) The proposed hysteresis control can achieve symmetric interleaving of the modules, with the maximum phase angle error of 4.1%;
(2) The current sharing can be achieved by combining the proposed controller with the voltage drop control, and the error of current sharing is within 4.0%;
(3) The hot-plug capability is verified. The modules can achieve the current sharing after adding the new module for 30 ms and can keep the current sharing after removing one module. At the same time, the phase angles can automatically adjust to the symmetrical interleaving state.
(4) The output voltage can recover within 2.60 ms after the load transitions from 50% to 100% and recover within 3.53 ms after the load transitions from 100% to 50%. In addition, the output voltage can recover within 1.96 ms after one module removal and recover within 2.41 ms after one module addition.

The proposed method utilizes an additional winding to sample the inductor voltage for constructing the hysteresis band, thereby eliminating the need for isolated voltage sensors. Furthermore, the construction of the hysteresis band and the generation of the control signals are implemented by analog circuits, thereby eliminating the need for high-speed ADC and a high-performance digital controller. These characteristics demonstrate that the proposed method has the merits of low cost and simplicity. Additionally, the results of the load transitions and hot-plug demonstrate the robustness. Therefore, the proposed controller can reliably achieve the desired control objectives without the need for interconnecting lines, making it highly potential for those applications that require reliability, modularity, and scalability.

The proposed method is hysteresis-control-based, which suffers from frequency variation with voltage variation. Hence, one of the future research opportunities will be to reduce the frequency variation range of the proposed control to facilitate the filter design. In addition, future research will extend this method to other paralleled DC–DC converters. Moreover, the proposed idea is currently verified by the circuit with discrete components, however, such a circuit is suitable for being made into integrated chips so as to further reduce costs and improve reliability and consistency.

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Data Availability Statement: Data are contained within the article.

Conflicts of Interest: The authors declare no conflicts of interest.

Appendix A

1. Derivation of Equations (16)–(18)

With the voltage-current relationship of the inductor, the resulting current disturbance $\hat{I}_{10}[1]$ is

$$\begin{aligned} \hat{I}_{10}[1] &= I_{10} + \Delta I_{10}[1] \\ &= h_{\max}/k_{iv} + a_{00}(T_{12off} + T_{23off} + \hat{T}_{31off}) + a_{10}(T_{2on} + T_{3on}) + I_{ref1} \end{aligned} . \quad \text{(A1)}$$

Combining Equation (9), the current deviation $\Delta I_{10}[1]$ can be solved as

$$\Delta I_{10}[1] = a_{00}\Delta T_{31off}[0]. \tag{A2}$$

(1) [t_{10}~t_{11}]: As range A in Figure 4 shows, for module 1, i_{L1} increases to the maximum current I_{11}, and I_{11} is determined by h_{max1} which is not affected by the disturbance. I_{11} can be expressed as

$$I_{11} = \hat{I}_{10}[1] + a_{11}\hat{T}_{1on}[1], \tag{A3}$$

where $\hat{T}_{1on}[1]$ is the length of this time interval, and $\hat{T}_{1on}[1] = T_{1on} + \Delta T_{1on}[1]$ is satisfied. Combining Equations (12) and (A2), $\Delta T_{1on}[1]$ can be solved as

$$\Delta T_{1on}[1] = -\Delta I_{10}[1]/a_{11} = -a_{00}\Delta T_{31off}[0]/a_{11}. \tag{A4}$$

(2) [t_{11}~t_{12}]: As range B in Figure 4 shows, for module 2, i_{L2} decreases to the minimum current $\hat{I}_{20}[1]$ and it can be expressed as

$$\begin{aligned} \hat{I}_{20}[1] &= \Delta I_{20} + \Delta I_{20}[1] \\ &= (h_{\min} + \lambda\hat{T}_{12off}[1])/k_{iv} + I_{ref2} \\ &= h_{\max}/k_{iv} + a_{00}(T_{23off} + \hat{T}_{31off}[0] + \hat{T}_{12off}[1]) + a_{10}(T_{3on} + \hat{T}_{1on}[1]) + I_{ref2} \end{aligned}, \tag{A5}$$

where $\hat{T}_{12off}[1]$ is the length of this time interval. Therefore, combining Equation (10), $\Delta T_{21off}[1]$ and the current deviation $\Delta I_{20}[1]$ can be solved as

$$\Delta T_{12off}[1] = \frac{a_{00}\Delta T_{31off}[0] + a_{10}\Delta T_{1on}[1]}{\lambda_{iv} - a_{00}}, \tag{A6}$$

$$\Delta I_{20}[1] = \lambda_{iv}\Delta T_{12off}[1], \tag{A7}$$

where the coefficient λ_{iv} satisfies $\lambda_{iv} = \lambda/k_{iv}$.

(3) [t_{12}~t_{13}]: As range C shows, for module 2, i_{L2} increases to the constant maximum current. I_{21} can be expressed as

$$I_{21} = h_{\max}/k_{iv} + I_{ref2} = \hat{I}_{20}[1] + a_{11}\hat{T}_{2on}[1], \tag{A8}$$

where $\hat{T}_{2on}[1]$ is the length of this time interval. According to Equation (13), the time deviation from T_{2on} is

$$\Delta T_{2on}[1] = -\lambda_{iv}\Delta T_{12off}[1]/a_{11}. \tag{A9}$$

(4) [t_{13}~t_{14}]: As range D shows, for module 3, i_{L3} decreases to the minimum current $\hat{I}_{30}[1]$, and it can be calculated as

$$\begin{aligned} \hat{I}_{30}[1] &= \Delta I_{30} + \Delta I_{30}[1] \\ &= (h_{\min} + \lambda\hat{T}_{23off}[1])/k_{iv} + I_{ref3} \\ &= h_{\max}/k_{iv} + a_{00}(\hat{T}_{31off}[0] + \hat{T}_{12off}[1] + \hat{T}_{23off}[1]) + a_{10}(\hat{T}_{1on}[1] + \hat{T}_{2on}[1]) + I_{ref3} \end{aligned}, \tag{A10}$$

where $\hat{T}_{23off}[1]$ is the length of this time interval. $\hat{T}_{23off}[1]$ and the current deviation $\Delta I_{30}[1]$ can be solved combining Equation (11):

$$\Delta T_{23off}[1] = \frac{a_{00}(\Delta T_{31off}[0] + \Delta T_{12off}[1]) + a_{10}(\Delta T_{1on}[1] + \Delta T_{2on}[1])}{\lambda_{iv} - a_{00}}. \tag{A11}$$

$$\Delta I_{30}[1] = \lambda_{iv}\Delta T_{23off}[1]. \tag{A12}$$

(5) [t_{14}~t_{15}]: As range E shows, for module 3, the maximum current I_{31} is

$$I_{31} = h_{\max}/k_{iv} + I_{ref3} = \hat{I}_{30}[1] + a_{11}\hat{T}_{3on}[1]. \tag{A13}$$

where $\hat{T}_{3on}[1]$ is the length of this interval. Combining Equation (14), the deviation from T_{3on} can be solved as

$$\Delta T_{3on}[1] = -\lambda_{iv}\Delta T_{23off}[1]/a_{11}. \tag{A14}$$

(6) [t_{15}~t_{20}]: As range F shows, for module 1, similar to the analysis of range D, the deviation $\Delta T_{31off}[1]$ from the steady-state value T_{31off} is

$$\Delta T_{31off}[1] = \frac{a_{00}(\Delta T_{12off}[1] + \Delta T_{23off}[1]) + a_{10}(\Delta T_{2on}[1] + \Delta T_{3on}[1])}{\lambda_{iv} - a_{00}}. \tag{A15}$$

Substituting Equations (A9) and (A14), Equation (A15) can be modified as:

$$\begin{aligned}\Delta T_{31off}[1] &= \frac{-(\lambda_{iv}a_{10} - a_{00}a_{11})}{a_{11}(\lambda_{iv} - a_{00})}(\Delta T_{12off}[1] + \Delta T_{23off}[1]) \\ &= \alpha(\Delta T_{12off}[1] + \Delta T_{23off}[1])\end{aligned}. \tag{A16}$$

Hence, the relationship between $\Delta T_{31off}[1]$ and $\Delta T_{31off}[0]$, i.e., Equation (16), can be obtained by substituting Equations (A4), (A6), (A9) and (A11).

Additionally, the current deviation $\Delta I_{10}[1]$ is

$$\Delta I_{10}[1] = \lambda_{iv}\Delta T_{31off}[1]. \tag{A17}$$

(7) [t_{20}~t_{21}]: As range G shows, for module 1, similar to the analysis of range E, the deviation $\Delta T_{1on}[2]$ has a similar form of Equation (A14), that is,

$$\Delta T_{1on}[2] = -\lambda_{iv}\Delta T_{31off}[1]/a_{11}. \tag{A18}$$

(8) Then, sequentially analyze range H~R in Figure 4 with the same method. The recurrence equations between different intervals can be derived as

$$\Delta T_{12off}[k] = \alpha(\Delta T_{23off}[k-1] + \Delta T_{31off}[k-1])(k \geq 2), \tag{A19}$$

$$\Delta T_{23off}[k] = \alpha(\Delta T_{31off}[k-1] + \Delta T_{12off}[k])(k \geq 2), \tag{A20}$$

$$\Delta T_{31off}[k] = \alpha(\Delta T_{12off}[k] + \Delta T_{23off}[k])(k \geq 1). \tag{A21}$$

Based on the above equations, when k = 2, $\Delta T_{31off}[2]$ can be calculated. In addition, combining Equations (16), (A4), (A6), (A9), (A11), and (A16)–(A18), the relationship between $\Delta T_{31off}[2]$, $\Delta T_{31off}[1]$ and $\Delta T_{31off}[0]$, i.e., Equation (17), can be obtained.

Additionally, when k > 2, substituting $\Delta T_{12off}[k]$ and $\Delta T_{23off}[k]$ into $\Delta T_{31off}[k]$, Equation (A21) is

$$\Delta T_{31off}[k] = 2\alpha^2\Delta T_{31off}[k-1] + \alpha^2(\Delta T_{23off}[k-1] + \Delta T_{12off}[k])(k > 2). \tag{A22}$$

Subsequently, substituting $\Delta T_{23off}[k-1]$ and $\Delta T_{12off}[k]$ yields

$$\Delta T_{31off}[k] = (\alpha^3 + 2\alpha^2)\Delta T_{31off}[k-1] + \alpha^3\Delta T_{31off}[k-2] + \alpha^3(\Delta T_{23off}[k-1] + \Delta T_{12off}[k-1])(k > 2). \tag{A23}$$

According to Equation (A21), when k > 2, $(\Delta T_{12off}[k-1] + \Delta T_{23off}[k-1]) = \Delta T_{31off}[k-1]/\alpha$ is satisfied; therefore, Equation (18) can be obtained by substituting this relationship into Equation (A23).

2. Variation curves of $\Delta T_{31off}[k]/\Delta T_{31off}[0]$

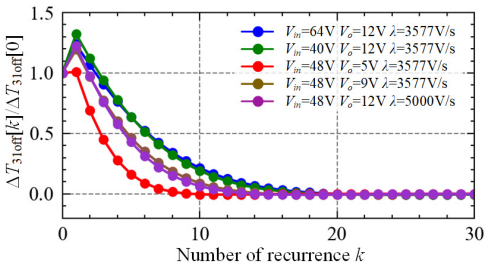


Figure A1. Variation curves of $\Delta T_{31off}[k]/\Delta T_{31off}[0]$ with different parameters.

3. Parameters

Table A1. Parameters for the simulations and experiments.

Parameter	Value
Inductor inside the module L_i	132 µH
Common inductor L_t	60 µH
Common capacitor C_o	250 µF
Rated input voltage V_{in}	48 V
Output voltage V_o	12 V
Rated load R_l	2 Ω
Voltage adjustment coefficients k_i	0.018 V/V
Attenuation rate λ	3577 V/s
Current–voltage ratio k_{iv}	1.0 V/A

Table A2. Parameters for the simulations of Figure 14.

Parameter	Value
Inductor inside the module L_i	180 µH
Common inductor L_t	60 µH
Common capacitor C_o	50 µH
Rated input voltage V_{in}	24 V
Output voltage V_o	8 V
Rated load R_l	1 Ω
Voltage adjustment coefficients k_i	0.1 V/V
Attenuation rate λ	20,000 V/s
Current–voltage ratio k_{iv}	1.0 V/A

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