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Integrated Junction Barrier Schottky Diode and MOS-Channel Diode in SiC Planar MOSFETs for Optimization of Reverse Performances

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Abstract: A novel planar silicon carbide (SiC) MOSFET integrated with both MOS-channel diode (MCD) and junction barrier Schottky diode (JBS) on the same chip (MCD-JBSFET) is proposed and investigated through Technology Computer-Aided Design (TCAD) simulations in this paper. The proposed device features the lowest turn-on voltage and the best current conduction capability under the reverse-biased conditions, allowing it to achieve the same reverse conduction capability with fewer MCDs compared to conventional MOSFET with MCD structures (MCDFET). This reduction in the number of MCDs enables more channels to operate under forward-biased conditions, thereby improving power density. Compared to a conventional MOSFET integrated with JBS structure (JBSFET), the reverse current in the MCD-JBSFET flows through both the MCD and JBS, which suppresses the peak lattice temperature at Schottky contact and enhances the high-temperature robustness, especially under surge current conditions. In addition, the split-gate structure in the proposed structure optimizes the reverse capacitance and the figure of merit $R_{on,sp} \times Q_g$ by factors of 0.65 and 2.15, respectively. Finally, the switching losses are reduced by 40.2%, indicating the suitability of MCD-JBSFET for high-frequency and high-current applications.

Keywords: integrated Schottky diode; MOSFET channel diode; reverse characteristic; high-temperature robustness; dynamic performances

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1. Introduction

The superior properties of silicon carbide (SiC) material, such as wide bandgap, high critical breakdown electric field, and high saturation drift velocity, make SiC MOSFET attract great attention for next-generation power semiconductor applications [1]. Since the development of the first SiC MOSFET, researchers have explored a range of novel structures and fabrication techniques, including planar gate, trench gate, super-junction designs [2–7]. However, the wide bandgap of SiC introduces challenges for the body diode when operated in reverse conduction mode, such as bipolar degradation, higher turn-on voltage, increased on-state dissipation, and suboptimal reverse recovery characteristics [8,9]. Using anti-parallel junction barrier Schottky diode (AP-JBS) is one of the most popular methods to mitigate these problems, but it increases package volume, complicates circuit design, and introduces parasitic elements [10,11]. Particularly, when a high current is concentrated in a single chip, AP-JBS may not provide sufficient protection in SiC modules. Over the past few years, various methods have been proposed to solve these problems and improve reverse characteristics, with MOSFET featuring MOS-channel diodes (MCDFET) and those

integrated with junction barrier Schottky diode (JBSFET) emerging as two particularly effective solutions [12–27]. The MCDFET was initially proposed as a Si-based split-gate trench MOSFET in Ref. [16] and later adapted for SiC MOSFET in Ref. [12]. This structure partitions a segment of the gate polysilicon into source polysilicon and employs variable oxide layer thicknesses beneath the polysilicon for the improvement of reverse characteristics. However, this structure sacrifices the number of MOSFET channels, deteriorating output characteristic and power density [11–16]. The JBSFET, on the other hand, mitigates the parasitic parameters and packaging issues associated with AP-JBS [17–24]. Nevertheless, the integrated structure also enables the device to function under high-current conditions both as a MOSFET in forward conduction mode and as a freewheeling diode under reverse-biased conditions, which might elevate the operating temperature and threaten long-term reliability. Therefore, it is necessary to find a way to improve the reverse characteristics of the device while ensuring the forward electrical parameters and reliability.

A novel structure integrated with junction barrier Schottky diode (JBS) and MOS-channel diode (MCD) within the same chip (MCD-JBSFET) is proposed and simulated through Sentaurus Technology Computer-Aided Design (TCAD) in this paper. Compared to conventional MCDFETs, the MCD-JBSFET shows a significantly lower reverse turn-on voltage and conduction dissipation, supporting a higher channel current density for forward conduction while maintaining equivalent reverse capabilities, which is beneficial for power density. Additionally, compared to conventional JBSFETs, the MCD-JBSFET achieves more uniform reverse conduction current and lattice temperature distribution under reverse conduction operations, along with improved capacitance, gate charge and switching characteristics. These advantages indicate the practicality of the proposed device for high-current and high-frequency applications.

2. Device Structure and Simulation Model

Figure 1 illustrates schematic cross-sections for MCDFET, JBSFET, and MCD-JBSFET. The proposed device can be fabricated on an N+ type substrate, followed by the growth of a 10 μm thick n-drift layer with a doping concentration of 1.3×10^{16} cm^{-3} to achieve a breakdown voltage higher than 1200 V [12–14]. To balance breakdown voltage (BV) and on-state resistance (R_{on}), the current spread layer (SL) is introduced by selectively implanting nitrogen ions, forming a 0.6 μm deep layer with a doping concentration of 1×10^{17} cm^{-3}. Multiple aluminum implantations were conducted to form P-base regions at a depth of 0.8 μm from the surface. High-doped N+ and P+ regions are then formed through implantation and activation at 1650 °C for 30 min [28]. Considering lateral diffusion of Al ions caused by implantation-induced defects, the half-width of the JFET region under the Schottky contact is set at 0.4 μm to ensure sufficient space for reverse current flow [29]. Then, a sacrificial oxidation process is performed after annealing to improve the SiC/SiO_2 interface quality. A 30 nm oxide layer is thermally grown at 1200 °C in dry O_2 and annealed in NO [30], followed by lithography etching, as shown in Figure 2c. Subsequently, a 20 nm oxide layer is thermally grown with similar processing, patterned to yield real and dummy gate oxide thickness of 50 nm and 20 nm, respectively. Due to varying doping levels in SiC, the oxide thickness above the strongly implanted region (N+ region) is slightly higher than that above the lightly doped regions (CSL and P-base regions). In situ-doped polysilicon is deposited and segmented into gate and source polysilicon. The channel under gate polysilicon (CUGP) and MCD under the dummy gate are formed, as depicted in Figure 2d. The former is mainly operated in the first quadrant, which represents the forward conduction state of the device, and both V_{ds} and I_{ds} are positive, while the latter is primarily utilized in the third quadrant, which corresponds to the reverse conduction state, and both V_{ds} and I_{ds} are negative. An interlayer dielectric is deposited and etched to expose ohmic and Schottky regions. Finally, nickel is deposited on both front and back sides, followed by annealing at 900 °C for 2 min to establish ohmic contacts with N+/P+ regions and Schottky contacts with n-drift regions [18]. Detailed structural parameters and a simplified process diagram are exhibited in Table 1 and Figure 2, respectively.

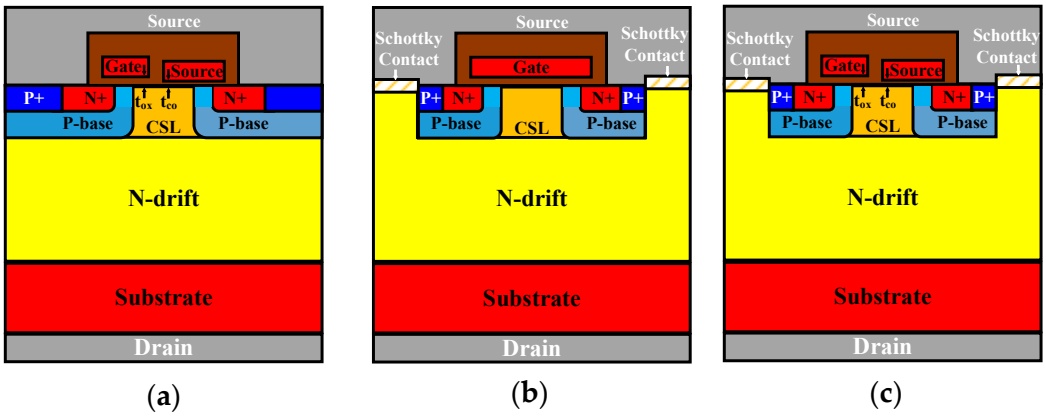


Figure 1. Schematic cross-sections for the (**a**) JBSFET, (**b**) MCDFET, and (**c**) JBS-MCDFET, respectively.

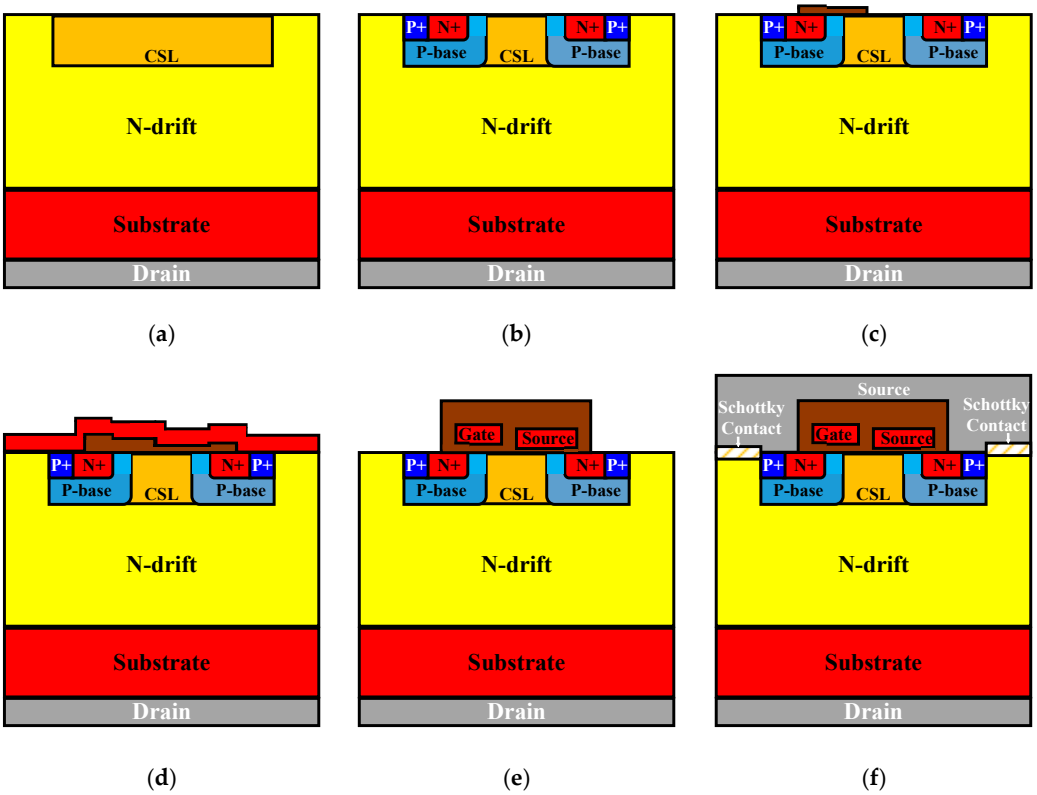


Figure 2. The schematic fabrication processes of MCD-JBSFET: (**a**) forming CSL by nitrogen implantation; (**b**) forming N+/P+/P-well regions by ion implantation; (**c**) growing and etching to obtain 30 nm oxide layer; (**d**) growing and patterning 20 nm oxide layer, and then depositing polysilicon; (**e**) split-gate polysilicon and source polysilicon, and etching to form metal contact windows; and (**f**) depositing metal to form ohmic and Schottky contact (not in size).

For accurate simulation of static and dynamic characteristics, a comprehensive set of physical models should be incorporated, such as the e-Barrier-Tunneling model for Schottky contact, the van Overstraeten model for avalanche, the anisotropic and incomplete ionization models for carriers, Shockely–Read–Hall and Auger-recombination models for doping dependence, and fixed charge with a value of 1×10^{12} cm^{-3} between the SiO_2 and SiC interface. The area factor in the +z direction is set to 2×10^7 μm to obtain an active area of 1 cm^2.

Table 1. Device structural parameters for simulation.

Device Parameters	MCDFET	JBSFET	MCD-JBSFET	Unit
Cell pitch	5.0	5.0	5.0	μm
Epitaxy thickness	10	10	10	μm
Epitaxy doping	1.3×10^{16}	1.3×10^{16}	1.3×10^{16}	cm^{-3}
CSL width	1.0	1.0	1.0	μm
CSL depth	0.6	0.6	0.6	μm
CSL doping	1×10^{17}	1×10^{17}	1×10^{17}	cm^{-3}
t_{ox}	50	50	50	nm
t_{co}	10~50	-	10~50	nm
Channel length	0.5	0.5	0.5	μm
Schottky contact width	-	0.4	0.4	μm
Schottky metal work function	-	4.7	4.7	eV
Spacer *	0.1	-	0.1	μm
P-base width	2.0	1.6	1.6	μm
P-base depth	0.8	0.8	0.8	μm
P-base top doping	1×10^{16}	1×10^{16}	1×10^{16}	cm^{-3}
P-base bottom doping	1×10^{18}	1×10^{18}	1×10^{18}	cm^{-3}
P-plus doping	1×10^{19}	1×10^{19}	1×10^{19}	cm^{-3}
N-plus doping	1×10^{20}	1×10^{20}	1×10^{20}	cm^{-3}

* The distance between gate poly and source poly.

3. Simulation Results and Discussion

3.1. Forward and Blocking Characteristics

In this section, critical electrical parameters of three types of devices are simulated and investigated by Sentaurus TCAD tools. Figure 3 presents the characteristic curves and distributions of the maximum oxide electric field (E_{m_ox}) for the devices with MCD structures under varying thicknesses of dummy gate oxide (t_{co}) conditions. As depicted in Figure 3a, E_{m_ox} decreases significantly with increasing t_{co}. Figure 3b reveals that E_{m_ox} primarily occurs at the bottom corner of the source polysilicon, adjacent to the gate polysilicon. The notably higher E_{m_ox} in MCDFET and MCD-JBSFET compared to JBSFET can be attributed to the increased electric field strength due to a thinner dummy oxide layer, and reduced shielding capability in the JFET region under the spacer between two polysilicon types with similar reverse bias conditions. This explains why, even at t_{co} = 50 nm, E_{m_ox} values of devices with MCD structures remained higher than those in JBSFET. However, at t_{co}= 10 nm, the E_{m_ox} exceeded 4 MV/cm with 1200 V drain bias, threatening oxide layer reliability and making it unsuitable for practical applications. Therefore, a t_{co} of 20 nm was temporarily chosen for subsequent investigations and the reason will be explained in Section 3.2.

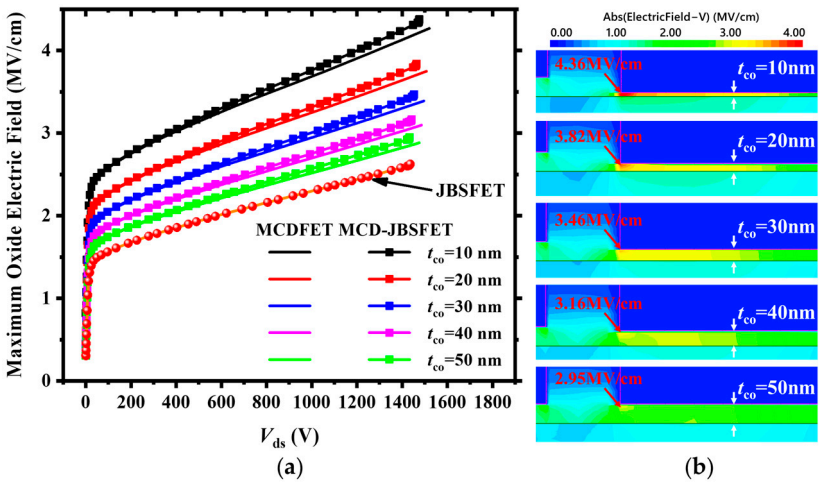


Figure 3. The E_{m_ox} (**a**) characteristic curves and (**b**) distributions for MCDFET and MCD-JBSFET with different t_{co}.

As shown in Figure 4a, breakdown voltages extracted at I_{ds}= 5 mA/cm^2 were 1495 V, 1434 V, and 1451 V for MCDFET, JBSFET, and MCD-JBSFET, respectively. These values are closed and all above 1200 V, ensuring reliable device performances. Meanwhile, avalanche points occurred at P-base/N-drift interface corners, while E_{m_ox} did not exceed 4 MV/cm, indicating the good protection for both oxide and Schottky contact due to the narrow P-base regions, as shown in Figure 4b–d [12].

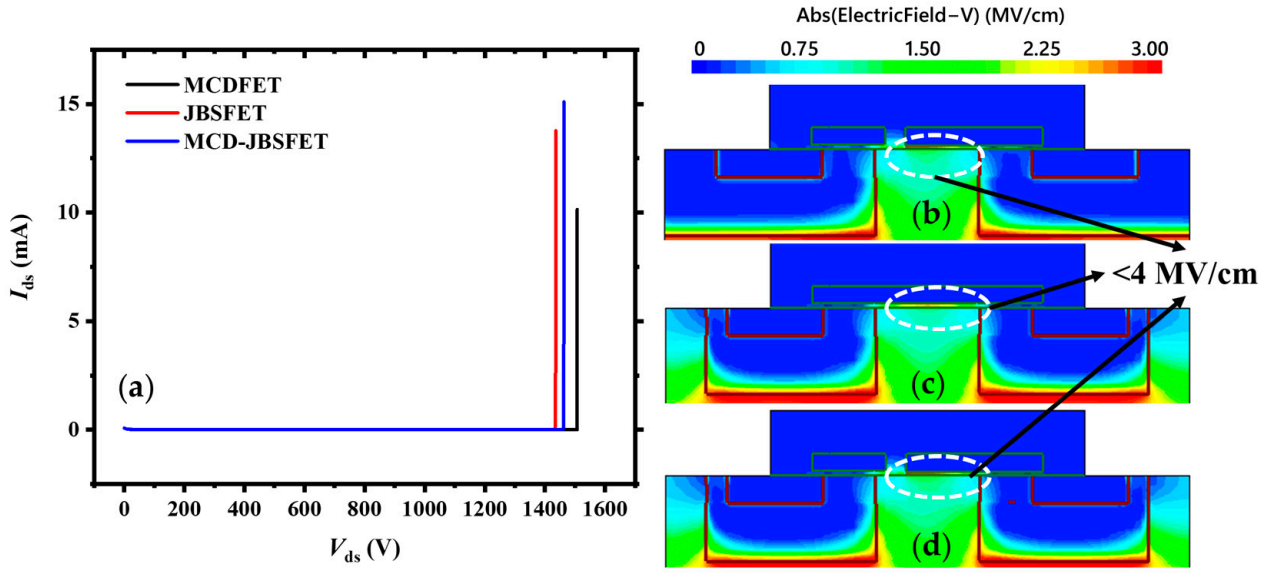


Figure 4. (**a**) The blocking characteristic curves and (**b**–**d**) the E_{m_ox} distributions of MCDFET, JBSFET, and MCD-JBSFET, respectively.

The on-state resistance, a crucial characteristic of SiC MOSFETs, was also investigated in this paper. Due to lower channel mobility, channel resistance typically contributes about 30% of total on-state resistance, resulting in resistance degradation in MCD structures due to the lower channel current density. Therefore, a channel mobility of 30 cm^2/V·s was adopted, based on measurements from the fabricated device.

Figure 5a,b display the output and blocking characteristic curves for three types of devices at CSL doping concentration of 1×10^{16} cm^{-3}, 5×10^{16} cm^{-3}, and 1×10^{17} cm^{-3}, respectively. In Figure 5a, the current conduction in devices with MCD structures improves as CSL doping concentration increases. When the doping concentration reached 1×10^{17} cm^{-3}, the R_{on} measured at I_{ds} = 100 A/cm^2 was 1.07 mΩ·cm^2, 0.98 mΩ·cm^2 and 1.03 mΩ·cm^2 for MCDFET, JBSFET, and MCD-JBSFET, respectively, with differences less than 10%. This can be attributed to the ability of CSL to horizontally stretch the current to flow across the JFET region uniformly, with this effect enhanced by the increase in the doping concentration, as shown in Figure 6a,b. Nevertheless, *BV*s exhibited a significant reduction with increasing CSL doping concentrations, as shown in Figure 5b. When CSL doping concentration reached 1.5×10^{17} cm^{-3}, *BV*s for all devices dropped below 1200 V, no longer meeting design requirements. Thus, the 1×10^{17} cm^{-3} doping concentration of CSL is selected to obtain a favorable trade-off between *BV* and R_{on}.

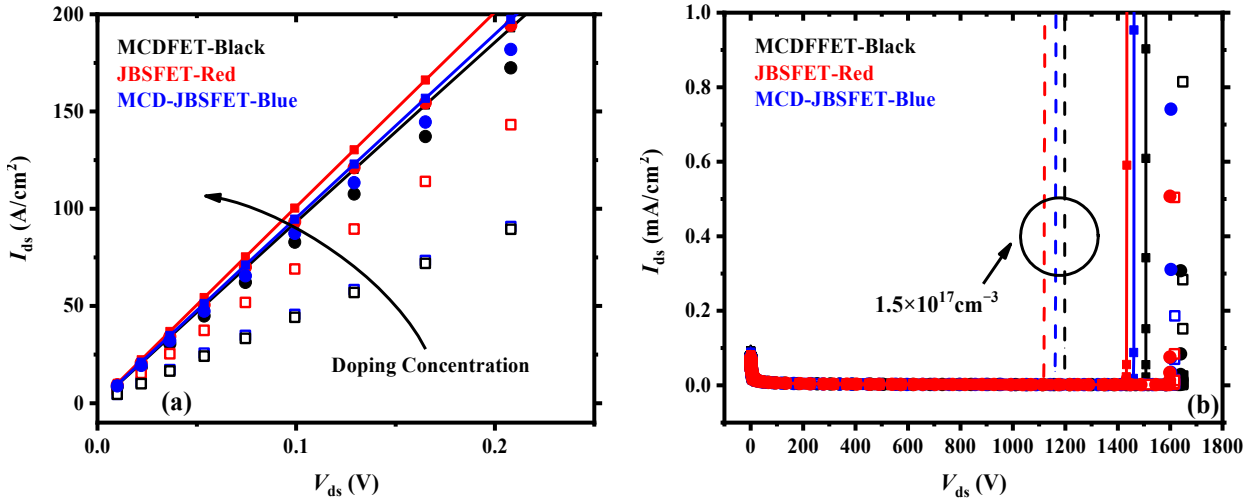


Figure 5. (**a**) The output and (**b**) blocking characteristic curves of MCDFET, JBSFET and MCD-JBSFE with CSL doping concentrations of 1×10^{16} cm^{-3} (hollow square), 5×10^{16} cm^{-3} (solid circle) and 1×10^{17} cm^{-3} (solid square-line), respectively. Meanwhile, the curves with doping concentration of 1.5×10^{17} cm^{-3} are also illustrated with dotted lines.

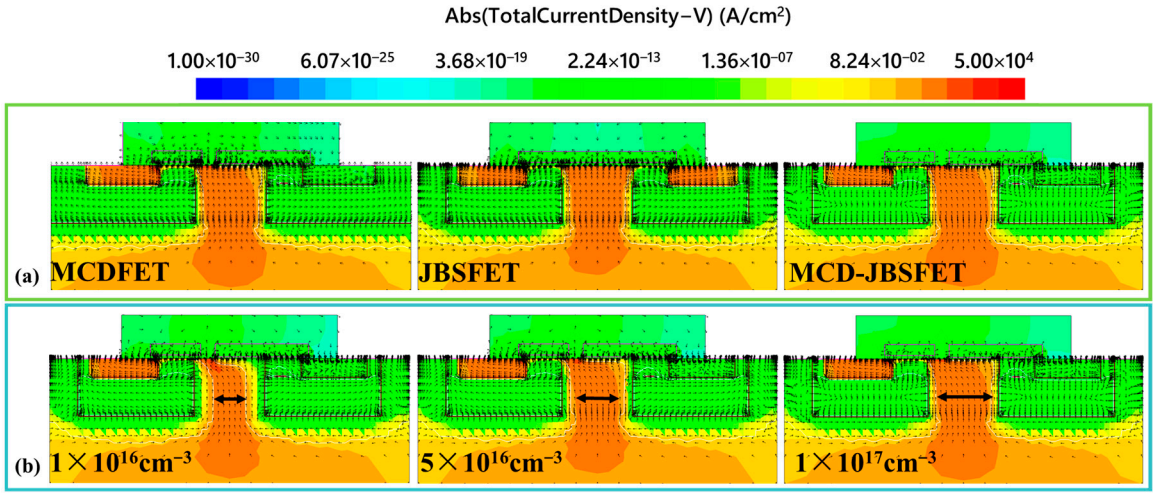


Figure 6. When I_{ds} = 100 A/cm^2, the forward conduction current distributions of (**a**) MCDFET, JBSFET, and MCD-JBSFET, and (**b**) MCD-JBSFET with CSL doping concentrations of 1×10^{16} cm^{-3}, 5×10^{16} cm^{-3}, and 1×10^{17} cm^{-3}, respectively.

3.2. Reverse Conduction Characteristics

The *I-V* curves of reverse conduction characteristics in the three types of devices at *V*gs= −5 V are illustrated in Figure 7. The reverse turn-on voltage (VR) of MCDFET increases with rising t_{co} due to the enlarging potential difference between the P-base region and channel region under the dummy gate [14,15], whose extracted values are 1.17 V, 1.63 V, 1.89 V, 2.10 V, and 2.24 V for t_{co} = 10, 20, 30, 40, and 50 nm, respectively. However, the values of V_R for MCD-JBSFET with various t_{co} remain nearly constant at 0.94 V, which is similar to that of the JBSFET, showing independence from t_{co}, as depicted in Figure 8. This is because electron current flows through the JBS rather than the MCD due to the lower Schottky barrier height between the metal and SiC material.

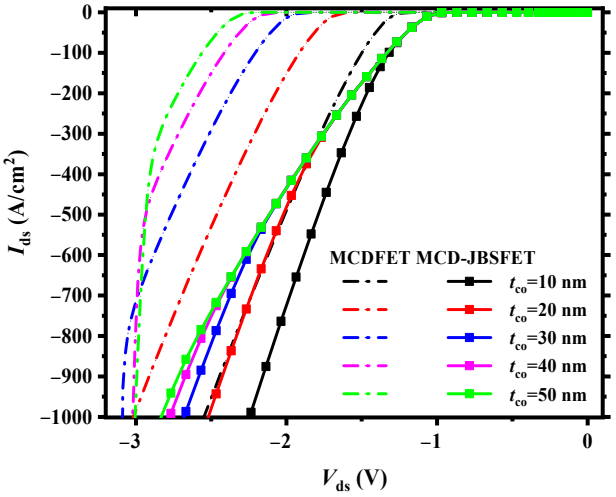


Figure 7. The reverse conduction characteristic curves for MCDFETs and MCD-JBSFETs with different t_{co}.

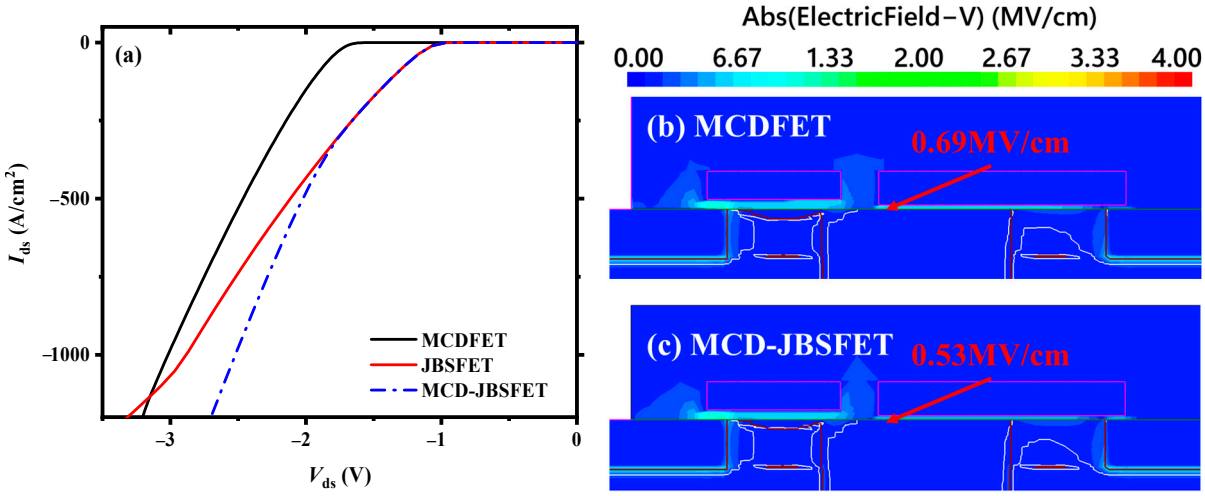


Figure 8. Under t_{co} = 20 nm condition, (**a**) the reverse conduction characteristic curves of three types of devices, and the E_{m_ox} distributions of (**b**) MCDFET and (**c**) MCD-JBSFET.

Owing to the thinner oxide layer in the MCD structure compared to t_{ox}, reliability concerns related to dummy gate oxide must be considered. As mentioned in Section 3.1, the overthin oxide layers, such as 10 nm, lead to unsafe E_{m_ox} values. Therefore, t_{co} was finally selected to be 20 nm in this paper to achieve a good compromise between reverse characteristics and oxide reliability [12,31]. Under this condition, the E_{m_ox} values for MCDFET and MCD-JBSFET measured at V_{ds}= −3 V, which is a typically reverse conduction operational voltage suggested in Figure 8a, are 0.69 MV/cm and 0.53 MV/cm, respectively, representing an order of magnitude reduction compared to the one biased at V_{DS} = 1200 V. Furthermore, many commercially available SiC MOSFETs have employed oxide thicknesses of 30 nm or less to reduce driving losses and enhance switching speeds, indicating the maturity of the fabrication technologies. Hence, the reliability of the oxide layer in the MCD is deemed acceptable.

The reverse conduction characteristic curves of MCDFET, JBSFET and MCD-JBSFET are illustrated in Figure 8. The reverse conduction characteristic curves of JBSFET and MCD-JBSFET exhibited extremely similar behaviors until the V_{ds} reached −1.63 V. At this voltage, the MCD in MCD-JBSFET was activated, allowing current to flow through both MCD and JBS paths, instead of solely through the JBS path, as shown in Figure 9. This mixed-conduction mode determined that the proposed device produced the lowest reverse

on-state voltage (V_{ron}) compared with the other two, with values of 2.46 V, 2.12, and 1.98 V for MCDFET, JBSFET, and MCD-JBSFET extracted at I_{ds} = -500 A/cm^2, respectively.

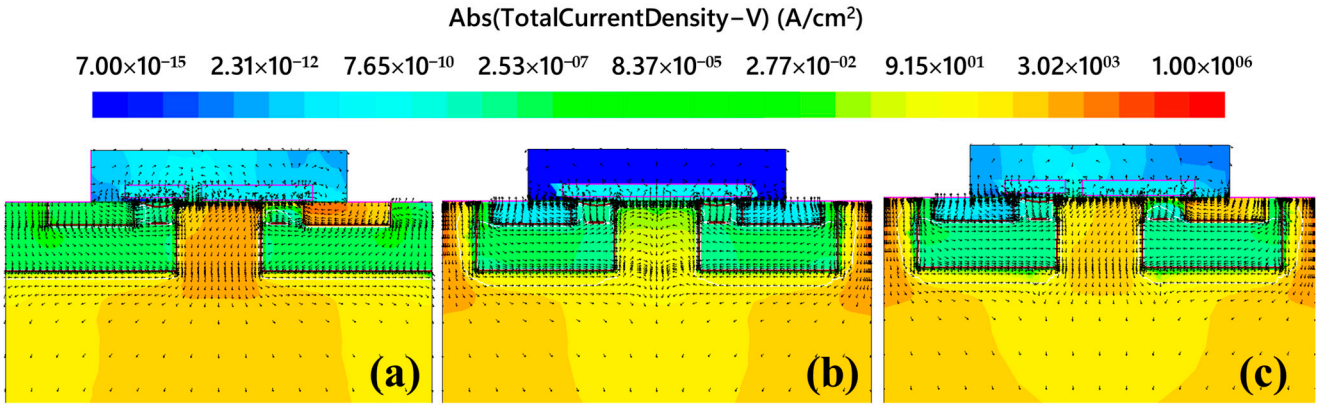


Figure 9. The distributions of reverse currents of (**a**) MCDFET, (**b**) JBSFET, and (**c**) MCD-JBSFET at $I_{ds} = -500$ A/cm^2.

In power SiC MOSFETs with identical active areas, the density of the true gate structure (e.g., the CUGP used here) determines the forward conduction capability, whereas the density of the dummy gate (e.g., the MCD in this paper) governs the reverse conduction capability. As depicted in Figure 8a, MCD-JBSFET showed superior reverse current conduction characteristics compared to the other two types, especially under high-current conditions. Hence, the proposed device could effectively decrease dummy gate density for the same reverse conduction currents, allowing more channels to be utilized as CUGP to flow forward current, thereby enhancing the power density. Furthermore, the t_{co} of MCDFET could not be fabricated too thin due to the constraint of E_{m_ox}, which limits the minimum V_R and restricts its reverse conduction characteristics. However, MCD-JBSFET employing the JBS mode effectively addresses these limitations. Therefore, all the features mentioned above highlight MCD-JBSFET as a viable solution to the points of difficulty of traditional MCDFET.

3.3. Surge Current Characteristic

Upon integration of JBS into MOSFET, the device can be operated in both forward and reverse conduction modes. Prolonged operation and high-current conditions, such as surge current conditions, can generate substantial heat accumulation, ultimately leading to lattice burnout or metal thermal failure, and thus threatening long-term reliability. To examine the surge current characteristics, three types of devices were subjected to a sinusoidal current source with a peak current of 500 A/cm^2 and a cycle duration of 10 ms, while a V_{gs} of -5 V was applied to ensure MOSFET channel cut-off. The surge current behavior of each device is illustrated in Figure 10. When the peak current value reached 500 A/cm^2, the maximum lattice temperatures were 577 K at 6.3 ms for MCDFET, 440 K at 6.1 ms for JBSFET, and 411 K at 6.7 ms for MCD-JBSFET, respectively. The MCD-JBSFET achieved the lowest lattice temperature, indicating the improvement of resistance to surge current. Figure 11 gives the maximum lattice temperature distributions across different devices. Due to the largest reverse conduction voltage drop and lower channel carrier mobility, the MCDFET exhibited hot spots concentrated in the MCD, resulting in the highest maximum lattice temperature among the three types of devices, while the JBSFET exhibited its peak temperature at the Schottky contact. This is because the JFET region beneath the JBS typically has lower doping concentration and narrower width to ensure blocking characteristics, leading to higher resistance and increasing thermal energy generation under identical current conditions ($Q = I^2Rt$ in simple terms). Nevertheless, the introduction of the MCD structure in JBSFET, e.g., MCD-JBSFET, redirected current to through both JBS and MCD, address-

ing issues caused by the MCD structure and avoiding bipolar degradation induced by triggering CUGP.

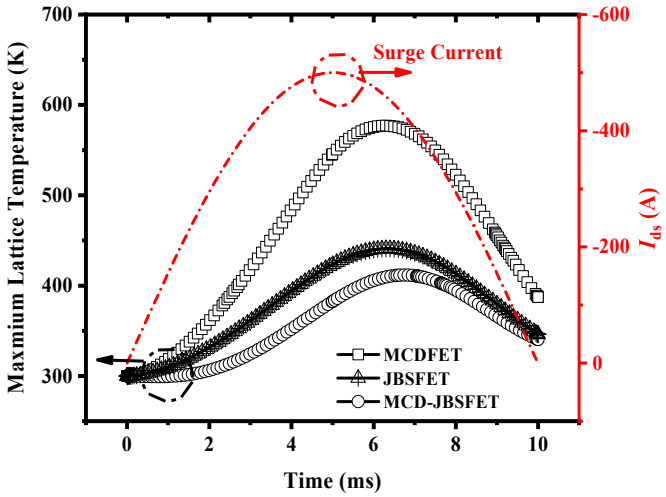


Figure 10. The maximum lattice temperature curves (marked with black dotted circle) of three types of devices with a peak surge current value of 500 A/cm^2 (red dotted line).

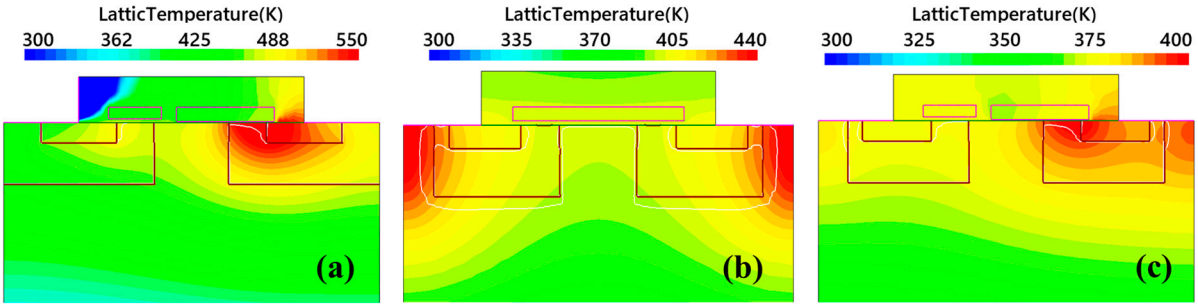


Figure 11. The distributions of maximum lattice temperature for (**a**) MCDFET, (**b**) JBSFET, (**c**) MCD-JBSFET at $I_{ds} = -500$ A/cm^2.

When the surge peak current raised from 500 A/cm^2 to 1000 A/cm^2, the maximum lattice temperature differences between three types of devices became more pronounced. The peak values of lattice temperature for MCDFET and JBSFET reached 1187 K and 1045 K, respectively, which exceeded the safe operating area of the metal, such as Al, which melted at 933 K, as shown in Figure 12a. For JBSFET, a new hot spot was observed at the channel region at $I_{ds} = -1000$ A/cm^2, as marked in Figure 12b. With the increase in the surge current, the JFET region under the JBS experienced elevated lattice temperature, resulting in the enhancement of the lattice vibration scattering, decreasing the mean free path, and incurring velocity saturation. When the surge current reached -800 A/cm^2, the current started to flow through the ohmic contact and channel into the drift region, as depicted in Figure 12c. In the mix-conduction mode of MCD-JBSFET, the peak value of lattice temperature consistently remained below 900 K, even when the current reached 1000 A/cm^2, indicating superior high-temperature robustness.

In the mix-conduction mode, it is essential to consider interface trap degradation caused by current flowing through MCD. No matter what structure SiC MOSFET has, interface trap degradation has been a long-standing issue. Under low-current conditions, current only flows under the dummy gate oxide in the reverse conduction conditions instead of the forward conduction conditions. Meanwhile, this current is significantly lower than that in the CUGP, resulting in relatively lower temperatures and thus inhibiting interface trap increase. Conversely, under high-current conditions, such as during surge current processes, further activation of the body diode allows current to flow through

the channel, elevating operational temperatures within both dummy oxide and true gate oxide regions. Additionally, the hot carrier injection effect caused by the strong electric field is another reason for interface degradation, which is mainly related to the maximum electric field near the SiC/SiO_2 interface. Under the reverse biased condition, the E_{m_ox} remains within the safe operating area of 4 MV/cm, as shown in Figure 3. While under the conducting mode, the E_{m_ox} is limited to only 0.54 MV/cm due to the relatively lower operational gate bias, as shown in Figure 8c, thereby mitigating hot carrier degradation. Collectively, these conditions suggest a similar total increase in interface traps for both dummy gate oxide and MOS-oxide.

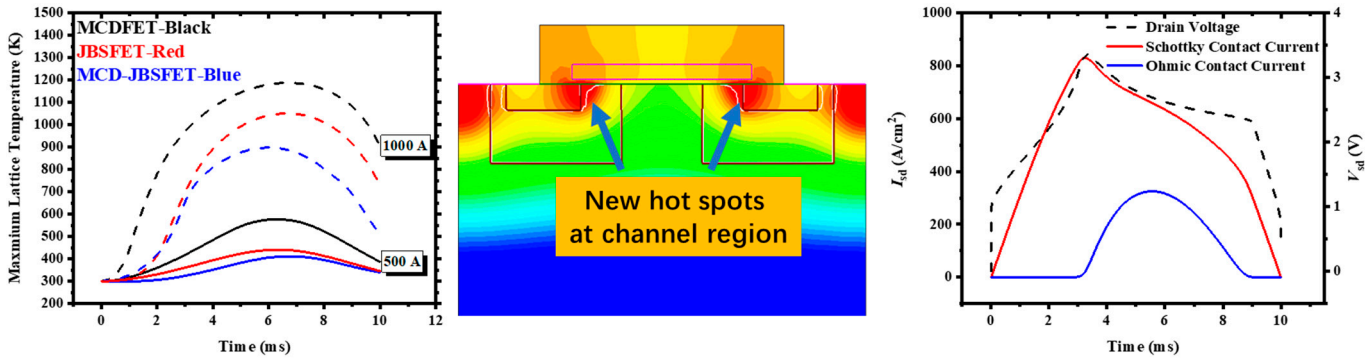


Figure 12. (**a**) The curves of the maximum lattice temperature of three types of devices with different peak values of surge currents, (**b**) the lattice temperature distribution of JBSFET at $I_{ds} = -1000$ A/cm^2, and (**c**) the curves of drain voltage, Schottky contact current and ohmic contact current during surge current progress with 1000 A/cm^2 peak value in JBSFET.

3.4. Capacitance, Gate Charge, and Switching Characteristics

The capacitance properties of three types of devices are illustrated in Figure 13. At V_{ds} = 800 V, the input capacitances (C_{iss}) were extracted at 8.3 nF/cm^2, 14.1 nF/cm^2, and 8.1 nF/cm^2, whereas the reverse capacitances (C_{rss}) were 5.9 pF/cm^2, 107.8 pF/cm^2, and 31.4 pF/cm^2 for MCDFET, JBSFET and MCD-JBSFET, respectively. Compared to JBSFET, introducing the MCD structure results in an obvious 65.5% reduction in C_{rss} by removing gate polysilicon above the JFET region. Additionally, the dummy gate reduced gate-to-source contact area, leading to a notable 42.5% decrease in C_{iss}.

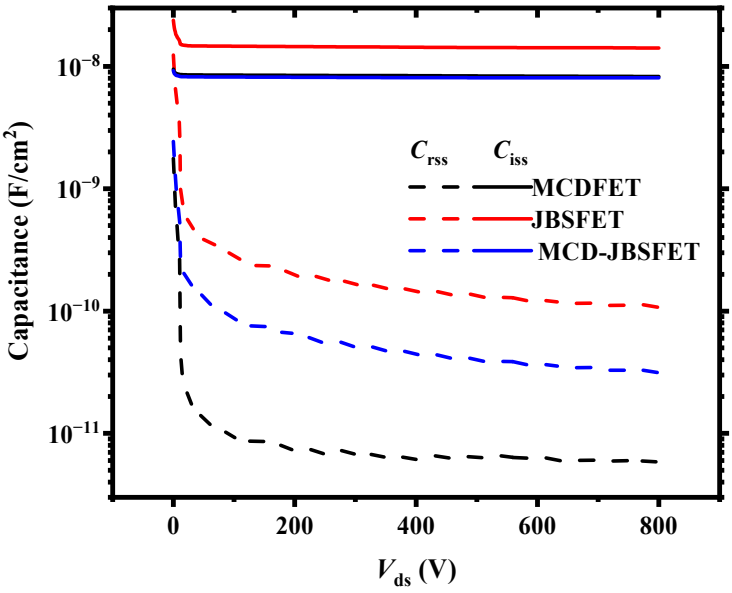


Figure 13. The curves of capacitance characteristic of three types of devices.

These capacitance reductions have a favorable impact on gate charge properties. Figure 14 gives the curves of gate charge (Q_g) characteristic of three types of devices with values of 176 nC/cm^2, 421 nC/cm^2, and 176 nC/cm^2 extracted at V_{gs} = 10 V for MCDFET, JBSFET, and MCD-JBSFET, respectively. The corresponding gate-to-drain charge (Q_{gd}) values are 18 nC/cm^2, 96 nC/cm^2, and 16 nC/cm^2 for the respective devices. Consequently, the figures of merit for $R_{on} \times Q_g$ and $R_{on} \times Q_{gd}$ were improved by a factor of 2.15 and 5.39 for JBSFET by introducing the MCD structure, respectively.

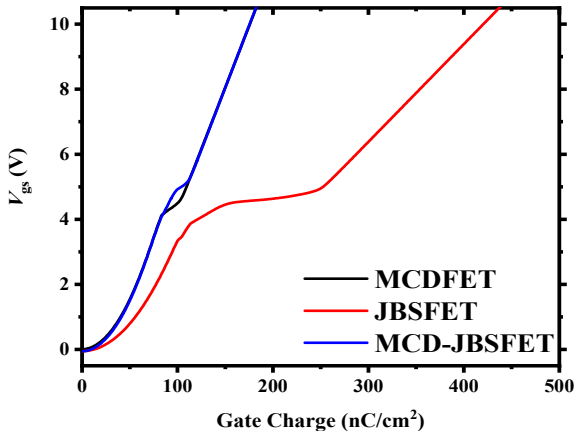


Figure 14. The curves of gate charge characteristic of three types of devices.

Figure 15a,b depict the switching characteristics for the devices with different structures and corresponding ideal turn-on switching waveforms. Simulations were conducted with an 800 V bus voltage and a gate pulse voltage ranging from 0 V to 15 V, as suggested by traditional 1200 V SiC MOSFET standards. It is evident that JBSFET exhibited the poorest switching performances, which could be attributed to the following reasons: (a) 0~t_1 period: the larger C_{iss} of JBSFET required more time to charge to reach threshold voltage; (b) t_1~t_2 period: JBSFET took the most time to achieve the highest saturate current compared with the other two due to its double channel current density; and (c) t_2~t_3 period: JBSFET has the largest C_{rss} and Q_{gd}, resulting in the lowest di/dt and an extended discharge time. These reasons are also suitable for the turn-off processes. Finally, the turn-on energy losses (E_{on}) calculated from Figure 16 were 1.43 mJ/cm^2, 5.61 mJ/cm^2, and 2.18 mJ/cm^2, whereas the turn-off energy losses (E_{off}) were 0.7 mJ/cm^2, 3.52 mJ/cm^2, and 1.49 mJ/cm^2 for MCDFET, JBSFET, and MCD-JBSFET, respectively. Adopting the MCD structure markedly improved the switching performance of the JBSFET, reducing total switching losses by 40.2% due to its improved capacitance and gate charge characteristics. Detailed electrical parameter values are illustrated in Table 2.

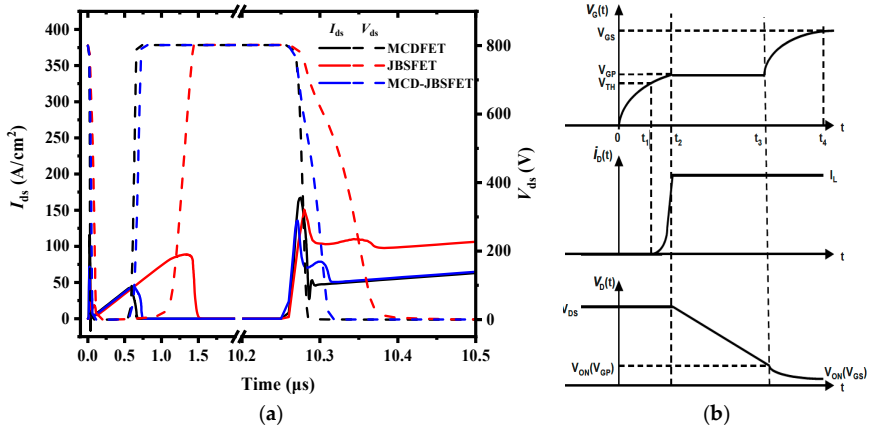


Figure 15. The (**a**) simulated switching characteristic curves of three types of devices at V_{ds} = 800 V and (**b**) ideal turn-on switching waveforms [32].

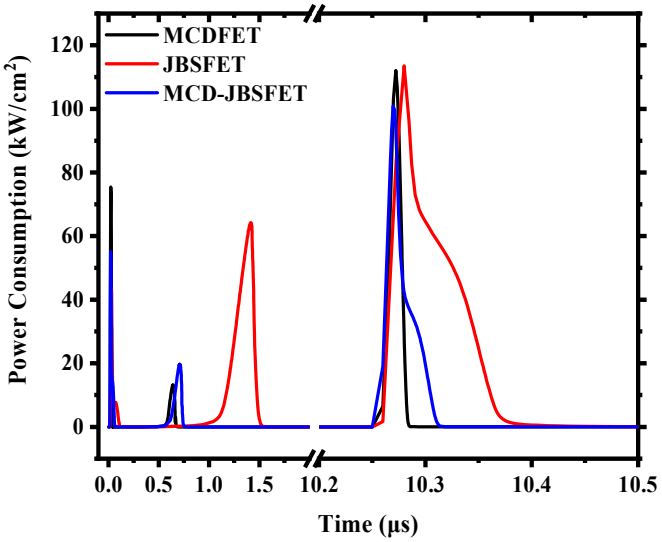


Figure 16. The switching losses of three types of devices during turn-on and turn-off processes.

Table 2. Detailed electrical parameters of three types of devices by simulation.

Parameters	MCD-JBSFET	MCDFET	JBSFET	Unit
BV	1451	1495	1434	V
R_{on}	1.03	1.07	0.98	mΩ·cm^2
Vth	3.7	3.7	3.5	V
V_R	0.84	1.63	0.94	V
V_{ron}	1.98	2.46	2.12	nF/cm^2
C_{iss}	8.1	8.3	14.1	pF/cm^2
C_{rss}	31.4	5.9	107.8	nC/cm^2
Q_g	176	176	421	nC/cm^2
Q_{gd}	16	18	96	mΩ·nC
$R_{on} \times Q_g$	191.84	188.32	412.58	mΩ·nC
$R_{on} \times Q_{gd}$	17.44	19.26	94.08	mJ/cm^2
E_{on}	2.18	1.43	5.61	mJ/cm^2
E_{off}	1.49	0.7	3.52	mJ/cm^2

4. Conclusions

In this paper, a SiC MOSFET integrated with both JBS and MCD structures on the same chip was proposed and simulated by TCAD. The MCD-JBSFET demonstrated superior performances under the reverse conduction conditions, such as the lowest V_R of 0.84 V and V_{ron} of 1.98 V extracted at $I_{ds} = -500$ A/cm^2. Therefore, the proposed structure could utilize a lower density of MCD to achieve similar reverse current conduction capability compared to MCDFET, enabling more channels to be employed for forward current conduction under the forward-biased conditions and thereby enhancing the power density. Furthermore, the MCD-JBSFET adopted the JBS-conduction mode under low reverse current conditions, effectively preventing the reliability challenges caused by high E_{m_ox} in dummy gate oxide. In addition, MCD-JBSFET also featured superior dynamic characteristics due to its split-gate structure and improved surge current reliability, such as the 42.5% and 65.5% reductions for C_{iss} and C_{rss}, as well as the enhancements in the figures of merit $R_{on} \times Q_g$ and $R_{on} \times Q_{gd}$ by factors of 2.15 and 5.39, respectively. The proposed device also exhibited a 15% decrease for the peak lattice temperature during surge current processes, attributed to mixed-conduction mode, and an optimization of 40.2% for the total switching losses due to split-gate structure. These improvements highlight the MCD-JBSFET as a promising solution to address the key limitations of both MCDFET and JBSFET, making it particularly suitable for high-frequency and high-current applications.

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