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Gate Oxide Reliability in Silicon Carbide Planar and Trench Metal-Oxide-Semiconductor Field-Effect Transistors Under Positive and Negative Electric Field Stress

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Abstract: This work investigates the gate oxide reliability of commercial 1.2 kV silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) with planar and trench gate structures. The performance of threshold voltage (V_{th}) and gate leakage current (I_{gss}) in SiC MOSFETs is evaluated under positive and negative gate voltage stress. The oxide lifetimes of SiC planar and trench MOSFETs at 150 °C are measured using constant voltage Time-Dependent Dielectric Breakdown (TDDB) testing. From the test results, it is found that electron trapping and hole trapping in SiO_2 caused by oxide electric field (E_{ox}) stress affect the V_{th} of SiC MOSFETs. The saturation and turnaround behavior of the V_{th} shift during positive and negative gate voltage stresses indicates that the influence of charge trapping in the gate oxide varies with stress time. The I_{gss} under positive and negative gate voltages depends on the tunneling barrier height for electrons and holes, respectively, which can be calculated using the Fowler–Nordheim (FN) tunneling mechanism. Moreover, the presence of near-interface traps (NITs) affects the barrier height for holes under negative gate voltages. The behavior of V_{th} shift and I_{gss} under high-temperature gate bias reflects the charge trapping occurring in different regions of the gate oxide. In addition, compared to SiC planar MOSFETs, SiC trench MOSFETs with thicker gate oxide tend to exhibit higher lifetimes in TDDB tests.

Keywords: threshold voltage; gate leakage current; gate oxide lifetime; charge trapping; planar and trench

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1. Introduction

Silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) have gained significant attention due to their potential to revolutionize various industries, especially in the field of electric vehicles. The intrinsic properties of SiC, such as its wide bandgap, high thermal conductivity, and excellent breakdown characteristics, make SiC MOSFETs particularly well suited for applications that require high efficiency, high power density, and reliable operation under extreme conditions. To further close the performance gap between SiC and traditional silicon devices, the performance of SiC MOSFETs has been gradually optimized through improvements in both process technology and structural design. Currently, commercial SiC planar and trench MOSFETs with gate oxide fabricated by thermally grown or deposited processes are available from various manufacturers [1,2]. The planar gate structure is a widely adopted MOSFET design in the market, recognized for its simplicity and mature manufacturing process. However, inherent limitations in channel mobility with planar MOSFETs have driven the development of trench gate structures, such as asymmetric and double trench structures [3,4]. SiC trench MOSFETs have high power

density and low on-resistance. Nonetheless, the reliability issues of SiC trench MOSFETs bring challenges to their widespread application [5–7]. Under high gate bias, the high electric field concentrate at the trench corner can degrade the oxide reliability. In addition, the planar and trench gate structures use different fabrication processes, leading to variations in interface states. Numerous experiments and studies have shown that the quality of the gate dielectric can be affected by the oxidation process [8–11]. It can be found that the density of interface states can be reduced by optimizing the oxidation process and implementing techniques such as passivation and interface nitridation. In summary, the different gate structures and gate oxide fabrication methods of SiC MOSFETs can significantly impact the reliability of gate oxide. SiC planar and asymmetric trench MOSFETs are two common types of commercial power devices. Reliability evaluation is essential to ensuring the lifetime and robustness of the SiC MOSFET in practical applications [8,9,12,13].

This study provides a comprehensive investigation into the reliability of gate oxide in SiC planar and asymmetric trench MOSFETs. The main parameters for evaluating gate oxide reliability include threshold voltage (V_{th}), gate leakage current (I_{gss}), and oxide lifetime. The high-temperature gate bias (HTGB) test is a common method employed to assess V_{th} stability [14–16]. The V_{th} shift can reflect the charge trapping of defects in SiO_2. There have been numerous publications on the testing and mechanism study of V_{th} stability in SiC MOSFETs [17–20]. Trapped electrons and holes can influence channel inversion, resulting in a positive and negative shift in the threshold voltage, respectively [21,22]. The gate oxide electric field (E_{ox}), stress time, temperature, and defect density in SiO_2 are important factors affecting the V_{th} shift. The variation in I_{gss} can demonstrate the effect of charge trapping on the barrier width for Fowler–Nordheim (FN) tunneling [23,24]. When continuous stress is applied to the gate oxide, electron trapping and hole trapping alter the actual electric field across the SiO_2. In addition, the oxide lifetime of SiC MOSFETs under typical operating conditions is commonly predicted using Time-Dependent Dielectric Breakdown (TDDB) testing and the E-model described by the thermochemical model [25]. Furthermore, considering that an increase in gate leakage current during TDDB testing can accelerate oxide breakdown, it is crucial to use accurate TDDB testing methods to reliably estimate gate oxide lifetimes [26]. Positive gate bias is applied to turn on the SiC MOSFET during operation, while negative gate bias is used to keep the MOSFET in the off state. Therefore, it is important to investigate the stability of the threshold voltage, the degradation of oxide lifetime, and the gate leakage current under both positive and negative gate bias conditions. While numerous previous studies have evaluated the gate reliability of commercial SiC MOSFETs, a thorough, side-by-side analysis of devices with planar and trench gate structures has been lacking. This research fills this gap by systematically comparing the reliability characteristics of these two common gate structures.

In this paper, the gate oxide reliability of SiC planar and asymmetric trench MOSFETs under a wide range of positive and negative E_{ox} stresses at 150 °C is investigated. The variation in the V_{th} shift with stress time is analyzed for both types of devices under E_{ox} stress. The processes of electron capture and hole capture in SiO_2 and the resulting impact on V_{th} are explained. Barrier height for tunneling and oxide thickness are calculated from the I_{gss} and oxide breakdown voltages of SiC planar and trench MOSFETs at 150 °C. Moreover, the variation in I_{gss} with stress time at different E_{ox} levels is discussed to determine the main factors affecting I_{gss} under positive and negative gate voltages. Furthermore, the gate oxide lifetime of SiC planar and trench MOSFETs is measured and compared under various gate biases using constant-voltage TDDB testing. Based on the test results and the E-model, the oxide lifetime of SiC MOSFETs under typical operating conditions is predicted. Additionally, the factors contributing to differences in oxide lifetime between the two types of devices are analyzed.

2. Experiment

Commercial 1.2 kV SiC MOSFETs with planar gate structure from Wolfspeed (Durham, NC, USA) and asymmetric-trench gate structure from Infineon (Neubiberg, Germany) are

selected for gate oxide reliability investigation. The cross-section schematics of SiC planar and trench MOSFETs are illustrated in Figure 1a,b. Table 1 provides specific details about the selected two types of devices, including package type, gate structure, on-resistance, and threshold voltage.

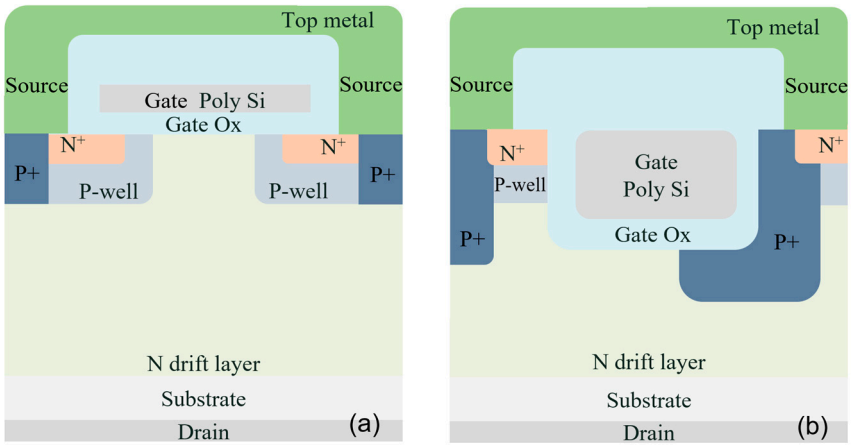


Figure 1. Schematic cross-section of (**a**) SiC planar MOSFET (C2M0280120D); (**b**) SiC asymmetric trench MOSFET (IMW120R220M1H).

Table 1. Device parameters of measured SiC MOSFETs.

Device Parameter	SiC Planar MOSFET	SiC Trench MOSFET
Package	TO247-3	TO247-3
Gate structure	Planar	Asymmetric trench
On-resistance (mΩ)	280	220
Threshold voltage at RT (V)	~6	~7

In this work, the gate leakage current, threshold voltage and oxide lifetime of SiC MOSFETs from two vendors are measured at 150 °C to investigate the stability of gate oxide under positive and negative gate voltage stresses. The V_{th} and I_{gss} are monitored using a Keysight B1506 power device analyzer from Keysight Technologies (Santa Rosa, CA, USA). For V_{th} testing, the gate and drain are connected, with the source being grounded. A constant current of 1 mA is applied to the gate and drain, and the voltage on the gate is measured as the threshold voltage. For I_{gss} testing, voltage is applied to the gate, while the source and drain are grounded. Figure 2 illustrates the test process and approach implemented by the B1506 automated measurement software (Easy Test Navigator). The testing procedure involves applying a constant gate bias stress to the SiC MOSFET for a total duration of 10 h. Throughout this period, the gate leakage current is continuously monitored and recorded to track any variations over time. In addition, V_{th} of SiC MOSFET is measured initially, prior to the application of stress, to establish a baseline. Subsequent V_{th} measurements are conducted at specific intervals during the 10 h stress period. This allows for the observation of any shifts in V_{th}, providing insight into changes in electrical characteristics of SiC MOSFETs under prolonged gate bias stress. In HTGB testing, a sample is selected for each test condition, ensuring that key performance parameters such as threshold voltage and on-resistance are consistent across samples. This approach minimizes the impact of device variation on the test results.

In addition, positive and negative TDDB measurements are performed on commercial SiC MOSFETs. Ten samples are selected and measured for each test condition. During the TDDB measurement, a constant voltage is applied to the gate oxide at high temperatures until the gate oxide breaks down. The drain and source are connected to the ground. The gate leakage current and failure time under constant-voltage stress are monitored using a 10-channel digital multimeter. Details of the specific test setup can be found in our

group's previous research [27]. In addition, based on the Weibull distribution of measured oxide lifetimes for 10 SiC MOSFETs, the time when 63% of the test population has failed is extracted as the oxide lifetime ($t_{63\%}$). To determine the oxide lifetime of SiC MOSFETs under operational conditions (~4 MV/cm), the E-model is used to fit the measured $t_{63\%}$ at different E_{ox} conditions.

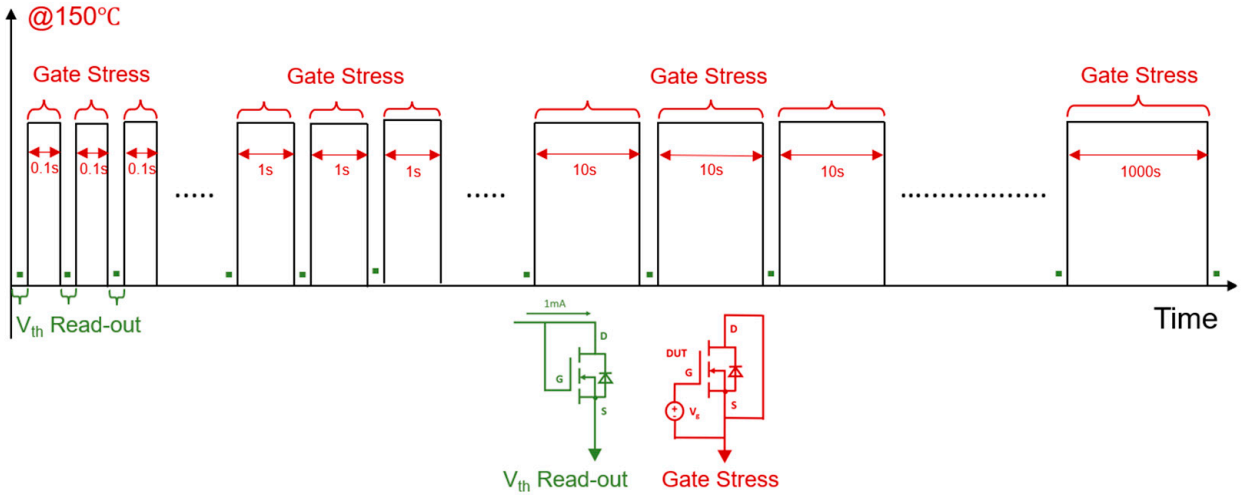


Figure 2. Test procedure for V_{th} and I_{gss} at 150 °C.

3. Results

3.1. I_{gss}-V_g Characteristic of Gate Oxide at 150 °C

The ramp-to-breakdown test at 150 °C under positive gate voltage is typically performed to estimate gate oxide thickness. As shown in Figure 3, I_{gss} tests under positive gate voltages are conducted on both SiC planar and trench MOSFETs. During the measurements, the drain and source of the packaged device are grounded and the gate voltage is gradually increased from 0 V until the gate oxide breaks down. As depicted in Figure 3a, the oxide breakdown voltage (V_{BR}) for SiC planar and trench MOSFETs at 150 °C is ~51 V and ~75 V, respectively. Assuming the critical gate oxide breakdown electric field is 11 MV/cm, the average oxide thickness (t_{ox}) for planar and trench devices is estimated to be ~46 nm and ~68 nm, respectively, using (1). Given the gate structure of trench devices, the oxide layer thickness varies between the sidewalls and the bottom of the trench [28]. The oxide thickness mentioned in this paper is the average thickness in the gate region, which is used to calculate the oxide electric field in subsequent sections, as shown in (2).

$$t_{ox} = \frac{V_{BR}}{11\ MV/cm} \quad (1)$$

$$E_{ox} = \frac{V_g}{t_{ox}} \quad (2)$$

From the I_{gss}-V_g test curves, it can be observed that the SiC planar and trench MOSFETs exhibit an exponential increase at V_g of around 27 V and 35 V, respectively. This behavior is attributed to electron injection through F-N tunneling [29]. From the F-N tunneling expression (3) [30], it is evident that the gate leakage current depends on the tunneling barrier height (Φ_B). The expressions for A and B are shown in (4) and (5). S is the area of the gate oxide. q is the electron charge. m_0 is the free electron mass. m_{ox} is the electron mass in the oxide. h is Planck's constant. Φ_B is the tunneling barrier height for electrons. According to (6), it is known that there is a linear relationship between $\ln\left(\frac{I_{gss}}{E_{ox}{}^2}\right)$ and $1/E_{ox}$. Figure 3b shows the $\frac{I_{gss}}{E_{ox}{}^2} - 1/E_{ox}$ plot obtained from the measured gate leakage current at 150 °C for SiC planar and trench MOSFETs. The Φ_B for electrons in SiC planar MOSFETs is calculated to be ~2.7 eV at 150 °C, which is close to the theoretical value [30]. Generally, near-interface

traps (NITs) can affect the measured effective electron barrier [31]. The Φ_B for electrons in SiC trench MOSFETs is slightly lower because the trench sidewall is the <1 1 $\bar{2}$ 0> crystal plane, which has fewer interface states, resulting in a reduced barrier height [2].

$$I_{gss} = ASE_{ox}{}^2 \exp\left(-\frac{B}{E_{ox}}\right) \tag{3}$$

$$A = \frac{q^3 m_0}{8\pi h m_{ox} \Phi_B} = \frac{1.54 \times 10^{-6}}{0.42 \times \Phi_B}\left(\frac{A}{V^2}\right) \tag{4}$$

$$B = \frac{8\pi\sqrt{2m_{ox}\Phi_B{}^3}}{3qh} = 4.42 \times 10^7 \Phi_B{}^{\frac{3}{2}}\left(\frac{V}{cm}\right) \tag{5}$$

$$\ln\left(\frac{I_{gss}}{E_{ox}{}^2}\right) = -\frac{B}{E_{ox}} + \ln(AS) \tag{6}$$

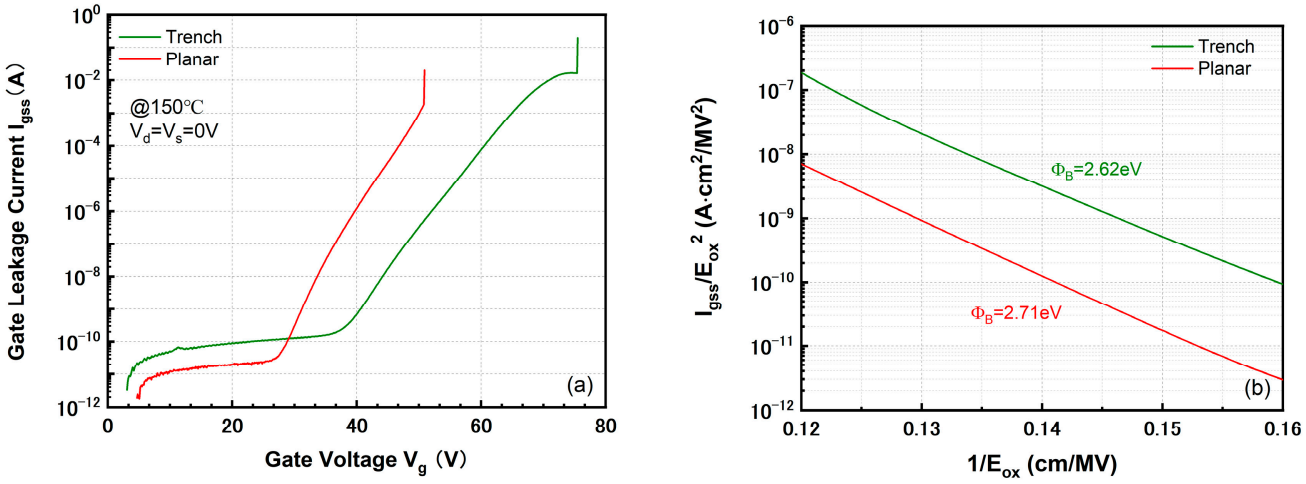


Figure 3. (**a**) Measured $I_{gss} - V_g$ characteristics; (**b**) $\frac{I_{gss}}{E_{ox}{}^2} - 1/E_{ox}$ plot at 150 °C obtained from measured I_{gss}.

Figure 4 shows the I_{gss} curves measured at negative gate voltages for SiC planar and trench MOSFETs. The negative gate voltage sweep is performed twice to avoid the influence of NITs with a net negative charge inside the SiO_2. For planar MOSFETs, the gate voltage is swept twice from 0 V to −35 V, while, for trench MOSFETs, it is swept twice from 0 V to −50 V. As shown in Figure 4a, the I_{gss} measured during the first negative gate sweep is higher than that of the second sweep. The increase in I_{gss} with gate voltage is related to hole injection through F-N tunneling from the SiC valence band. Therefore, it can be assumed that the hole barrier height is significantly affected by negatively charged NITs. The presence of NITs in SiC MOSFETs results in a higher gate leakage current under negative gate voltage. The hole injection generated by the first gate sweep can neutralize the negatively charged traps in the SiO_2. To restore the normal theoretical value of the tunneling barrier height for holes, the SiC MOSFET is first subjected to a negative gate sweep to mitigate the NIT effect, followed by a ramp-to-breakdown test, as shown in Figure 4b. It can be observed that the negative breakdown voltages of the gate oxide in SiC MOSFETs from two vendors are approximately equal to the positive breakdown voltages.

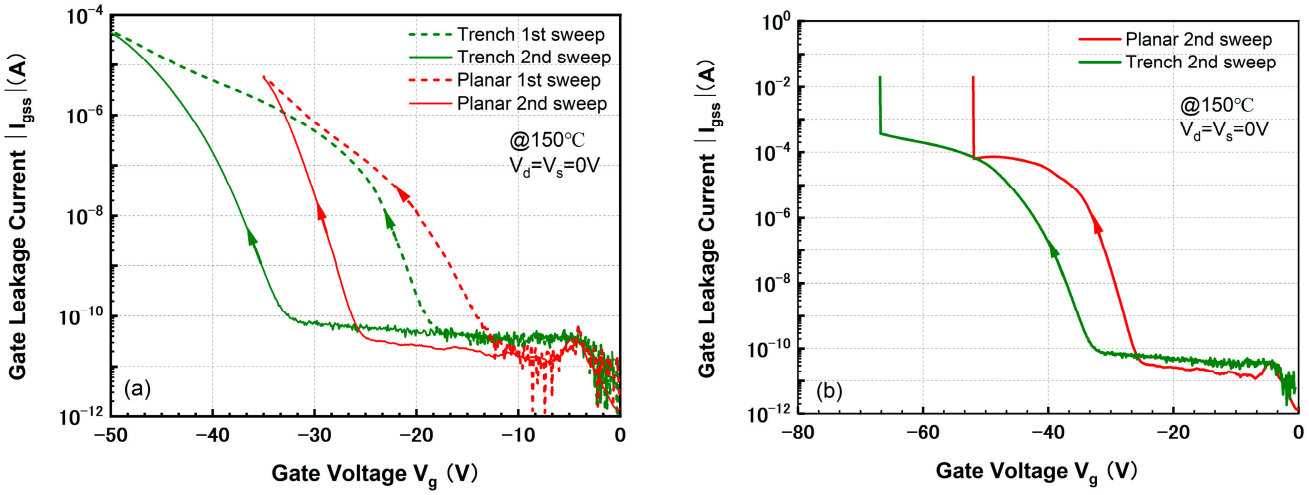


Figure 4. (**a**) Measured $|I_{gss}|-V_g$ characteristics obtained from two negative sweeps; (**b**) ramp-to-breakdown plots at 150 °C.

3.2. Influence of HTGB on Threshold Voltage

The V_{th} shift is a critical parameter indicating charge trapping in the gate oxide, particularly in the region near the SiC/SiO_2 interface. The V_{th} shift as a function of stress time under different positive gate oxide electric field stresses is recorded for SiC planar and trench MOSFETs, as shown in Figure 5. For planar MOSFETs, the selected E_{ox} stress range is from 4 MV/cm to 9.1 MV/cm, as depicted in Figure 5a. The V_{th} shift exhibits a negative value during the interval from 0.1 s to 1 s of stress time when E_{ox} is 9.1 MV/cm. This is attributed to the dominance of hole trapping in the SiO_2 caused by impact ionization, as shown in Figure 6b. Under a high electric field, electrons pass through the oxide layer. When they reach the anode, accelerated electrons with sufficient energy can cause impact ionization. The generated holes tunnel back into the oxide. Due to the much lower mobility of holes compared to electrons, holes are easily trapped by defects. With the increase in stress time, the V_{th} shift transitions from negative to positive values at a high E_{ox} of 9.1 MV/cm. This behavior occurs because, as injection time increases, hole capture in the gate oxide reaches saturation [32]. Meanwhile, trapped electrons in the oxide and the density of the acceptor-type interface states both increase [33]. When the stress time exceeds 1 s, V_{th} begins to shift positively, with the magnitude of the shift gradually increasing. This indicates that electron trapping surpasses hole trapping, as shown in Figure 6a, and its influence is becoming more significant [34,35]. The negative V_{th} shift is not observed at lower E_{ox} levels (<9 MV/cm). Instead, only a positive V_{th} shift due to electron trapping occurs, with the V_{th} shift increasing with the stress time at these lower E_{ox} levels. In addition, at high E_{ox} ($\geq$9 MV/cm), the V_{th} shift tends to saturate within the stress time range of 100 s to 1000 s. This saturation occurs because the pre-existing traps in the oxide layer become fully occupied by electrons [15]. After maintaining a saturated state for a period, V_{th} continues to increase rapidly, primarily due to newly generated oxide traps continually capturing electrons that tunnel into the SiO_2 via FN tunneling [36]. Figure 5b shows the variation in the V_{th} shift with stress time for SiC trench MOSFETs in the range of E_{ox} from 4 MV/cm to 9 MV/cm. When E_{ox} is 9 MV/cm, V_{th} exhibits a transition from a negative to a positive shift, which indicates that the primary charge trapping in SiO_2 transitions from holes to electrons. When E_{ox} is between 4 MV/cm and 8 MV/cm, the influence of electron trapping remains dominant.

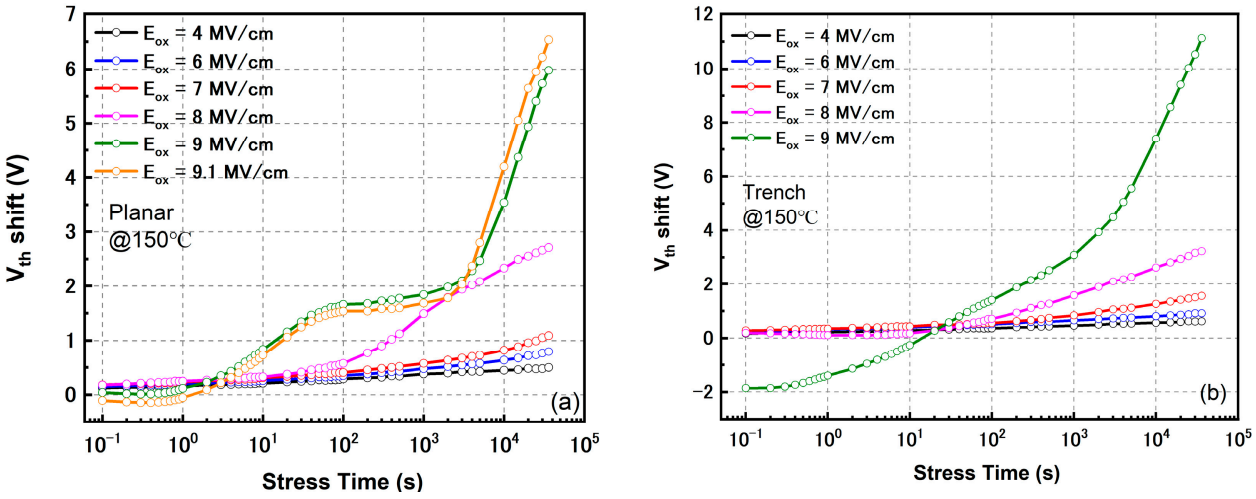


Figure 5. V_{th} shift at 150 °C under different positive gate bias stresses for (**a**) SiC planar MOSFETs; (**b**) SiC asymmetric trench MOSFETs.

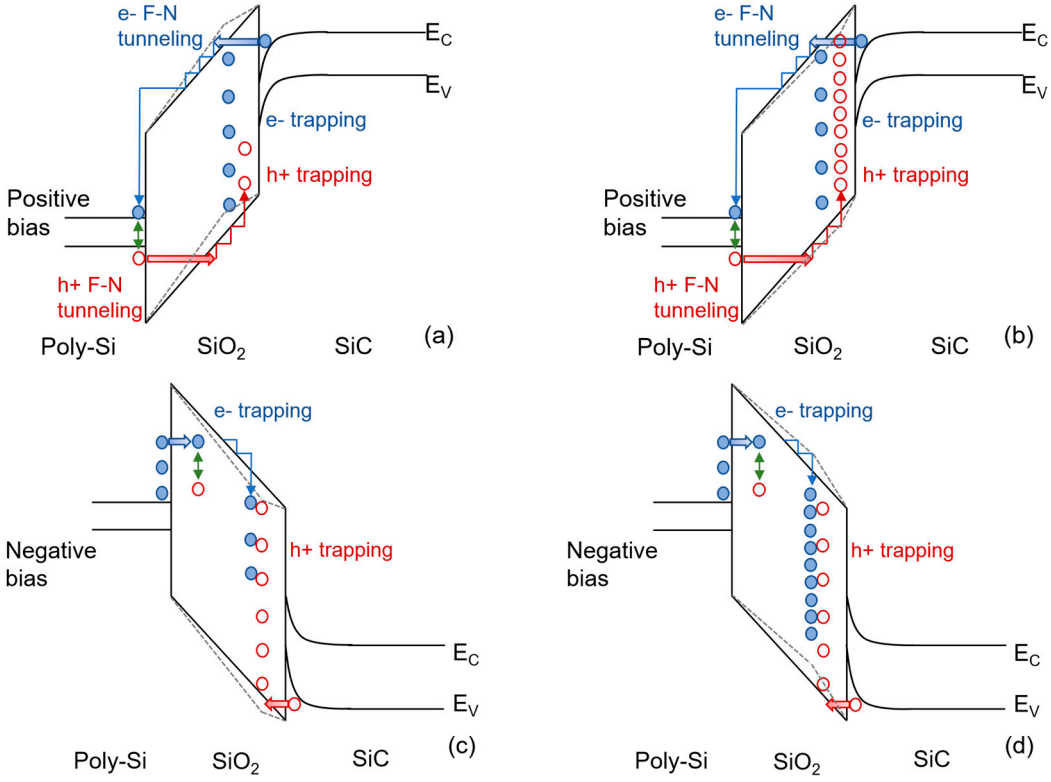


Figure 6. Schematics of band diagram under different gate biases. (**a**) Electron trapping dominant under positive gate bias; (**b**) hole trapping dominant under positive gate bias; (**c**) hole trapping dominant under negative gate bias; (**d**) electron trapping dominant under negative gate bias.

Figure 7 shows the V_{th} shift as a function of stress time for SiC planar and trench MOSFETs under negative gate bias stress. As shown in Figure 7a, the V_{th} shift in SiC planar MOSFETs is negative and gradually decreases with stress time. The negative V_{th} shift is caused by holes tunneling from the SiC valence band into the gate oxide, as illustrated in Figure 6c. Captured holes in SiO_2, which act as positive charges, enhance the inversion of the channel. In addition, it can be observed that the V_{th} value decreases rapidly until it approaches saturation when E_{ox} is less than −6.5 MV/cm. The saturation phenomenon of the V_{th} shift implies that the hole traps in the SiO_2 are almost completely occupied [37]. The

hole traps in SiC MOSFETs primarily include initial defects introduced during fabrication and new traps induced during stress. Figure 7b shows that, when E_{ox} is −9 MV/cm or −9.5 MV/cm, the V_{th} shift in SiC trench MOSFETs first decreases and then increases with stress time. This turnaround phenomenon is mainly due to the changing balance between electron trapping and hole trapping in SiO_2 under a negative gate voltage. Under negative bias conditions, electrons from the poly-Si gate tunnel into the gate oxide through FN tunneling. These electrons can gain sufficient energy to cause impact ionization, leading to the generation of additional electron traps [38]. As stress time increases, more electrons can tunnel into the oxide layer, where they become trapped, further contributing to the increase in the V_{th} shift. Moreover, the tunneling probability of electrons is enhanced with an increase in the negative gate bias voltage. As more electrons accumulate in the gate oxide, the V_{th} shift tends to increase, indicating that the effect of electron trapping is more pronounced under strong negative voltages, as shown in Figure 6d.

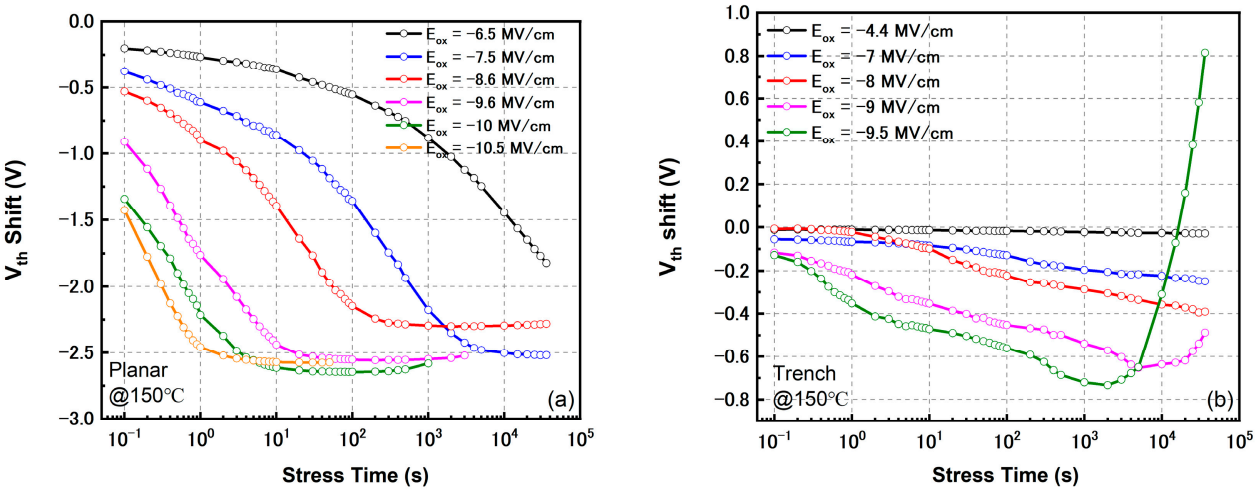


Figure 7. V_{th} shift at 150 °C under different negative gate bias stresses for (**a**) SiC planar MOSFETs; (**b**) SiC asymmetric trench MOSFETs.

Figure 8a,b show a V_{th} shift as a function of E_{ox} for planar and trench MOSFETs after 100 ms and 10 h of gate voltage stress, respectively. As shown in Figure 8a, when the stress time is 100 ms, the V_{th} shift in a SiC MOSFET initially increases and then decreases with the rise in positive E_{ox}. For SiC planar MOSFETs, the peak of V_{th} shift is at E_{ox} of 8 MV/cm. When E_{ox} exceeds 8 MV/cm, the positive shift of V_{th} is reduced due to the generation of hole trapping. The hole-trapping effect surpasses the electron-trapping effect at E_{ox} larger than 9 MV/cm, resulting in a negative V_{th} shift in SiC planar MOSFETs. For SiC trench MOSFETs, it is found that the maximum point of V_{th} shift is at E_{ox} of 7.5 MV/cm and that the negative V_{th} shift occurs after 8 MV/cm. The onset of a negative V_{th} shift in trench MOSFETs occurs at a lower E_{ox} compared to planar MOSFETs. This is because the gate oxide thickness in trench devices is unevenly distributed, with the oxide on the sidewalls being thinner. For SiC trench devices, the gate voltage is calculated based on the average oxide thickness. Given this calculation, the actual electric field in the oxide at the sidewall region should exceed the set E_{ox}. Under negative gate bias stress, the negative V_{th} shift in SiC planar and trench MOSFETs decreases as E_{ox} decreases, which is due to the gradual accumulation of hole trapping in the SiO_2. Compared to SiC planar MOSFETs, the absolute value of the V_{th} shift in SiC trench devices is lower. This indicates that negative bias has a greater impact on the negative threshold voltage shift in SiC planar MOSFETs. This may be due to the higher number of electron traps in SiC trench MOSFETs resulting in more electron trapping. However, further research is needed to confirm this. As illustrated in Figure 8b, after 10 h of positive gate stress, a significant accumulation of electrons occurs in the gate oxide of both SiC planar and trench devices, leading to a large positive V_{th} shift. Moreover, higher E_{ox} causes more electrons to accumulate in SiO_2 over the 10 h period,

leading to a greater V_{th} shift [39]. After 10 h of negative gate bias, it can be found that SiC trench MOSFETs can generate a large amount of electron trapping at E_{ox} = −9.5 MV/cm, leading to a positive V_{th} shift. Under other negative bias conditions, SiC trench MOSFETs only exhibit a negative V_{th} shift during the 10 h stress period because the electric field strength is insufficient for accumulating enough electron trapping. However, if the stress time is further extended, a positive threshold voltage shift is likely to be observed. For SiC planar MOSFETs, the impact of electron trapping is not very significant. Therefore, the negative V_{th} shift caused by hole trapping is substantial.

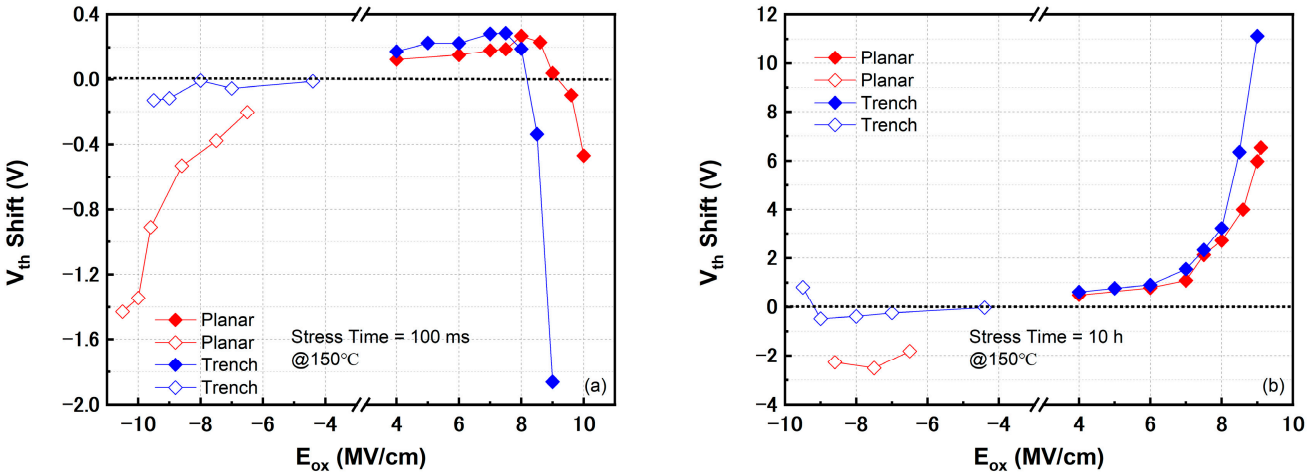


Figure 8. V_{th} shift as a function of E_{ox} at 150 °C with a stress time of (**a**) 100 ms; (**b**) 10 h.

3.3. Influence of HTGB on Gate Leakage Current

The gate leakage current is another significant parameter reflecting the performance of gate oxide. The magnitude of I_{gss} is influenced by the tunneling barrier width of gate oxide. Generally, charges trapped in SiO_2 can either widen or narrow the tunneling barrier, thereby affecting FN tunneling. Figure 9 illustrates the curves of I_{gss} with stress time for SiC MOSFETs under different positive gate bias stresses. From the perspective of the gate structure, when a positive voltage is applied to the gate of SiC planar MOSFETs, I_{gss} mainly consists of electrons from the N+ region, P-well region, and JFET region covered by poly-Si [40]. For SiC trench MOSFETs, I_{gss} with a positive gate bias is composed of electrons from regions on the gate sidewalls and bottom. As shown in Figure 9a, SiC planar MOSFETs exhibit a rising and then falling behavior at E_{ox} of 9.6 MV/cm, whereas the I_{gss} of the SiC trench MOSFET in Figure 9b demonstrates a continuous decrease at different gate biases. Based on previous studies, it is known that the rising behavior of I_{gss} is due to hole trapping in SiO_2 originating from impact ionization. When the captured charge in SiO_2 is dominated by holes, the FN tunneling current increases due to the reduced barrier width for tunneling, as shown in Figure 6b. While for SiC trench MOSFETs, no significant increase in leakage current is observed. Although the SiC trench device shows a negative shift of V_{th} by hole trapping in the time interval from 100 ms to 10 s at E_{ox} of 9.5 MV/cm, I_{gss} is not significantly affected by the hole trapping. V_{th} is mainly affected by charge trapping in the gate oxide located in the channel region on the sidewalls, while I_{gss} is composed of electrons originating from both the sidewall and bottom regions. The gate oxide in the bottom region is thicker; therefore, under the same gate voltage, although hole trapping dominates in the sidewall region, the lower E_{ox} in the bottom region of the SiO_2 mainly leads to significant electron trapping, which mitigates the effect of hole trapping. The electron trapping can increase the barrier width for tunneling, as illustrated in Figure 6a. Consequently, the I_{gss} of SiC trench MOSFETs gradually decreases under high E_{ox} with prolonged stress time.

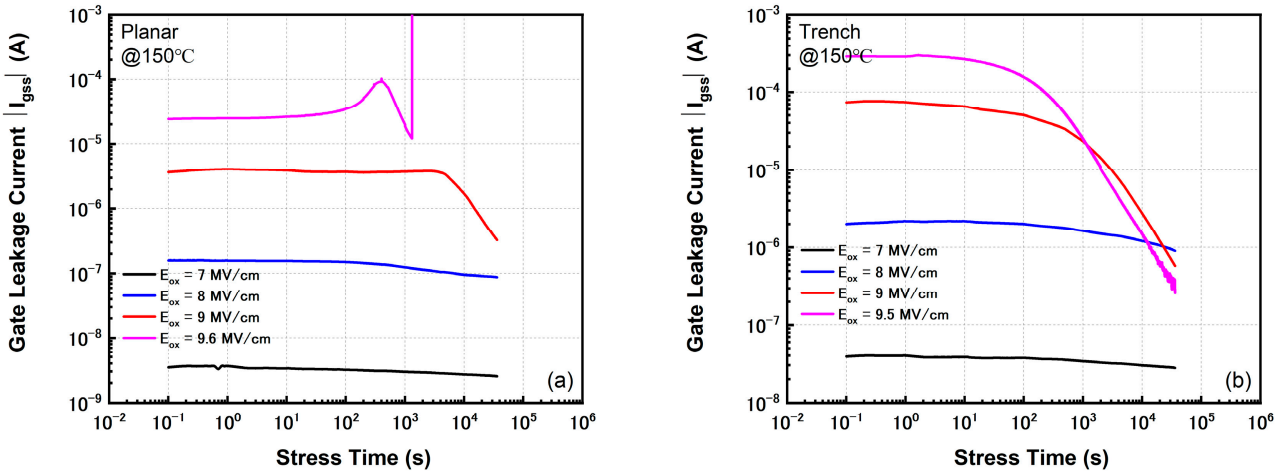


Figure 9. $|I_{gss}|$ as a function of stress time at 150 °C under different positive gate bias stresses for (**a**) SiC planar MOSFETs; (**b**) SiC asymmetric trench MOSFETs.

Figure 10 shows the time-dependent gate leakage current measurements with respect to the different negative gate voltage stresses. For both types of devices, the gate leakage current generated by hole FN tunneling decreases with increasing stress time. According to Figure 6c, the capture of the hole in SiO_2 causes an increase in barrier width for the hole, which reduces the hole FN tunneling current. Although the V_{th} shift in SiC trench MOSFETs reveals a rebound after 2000 s at E_{ox} of −9.5 MV/cm, this behavior is not observed in the I_{gss} measurements. This suggests that the impact of charge trapping in the gate oxide on I_{gss} and V_{th} is inconsistent. Due to the unique gate structure of trench MOSFETs, changes in V_{th} primarily reflect variations in charge within the gate oxide on the sidewalls of the channel region, whereas, for I_{gss}, changes in charge within the gate oxide at the bottom region are equally important.

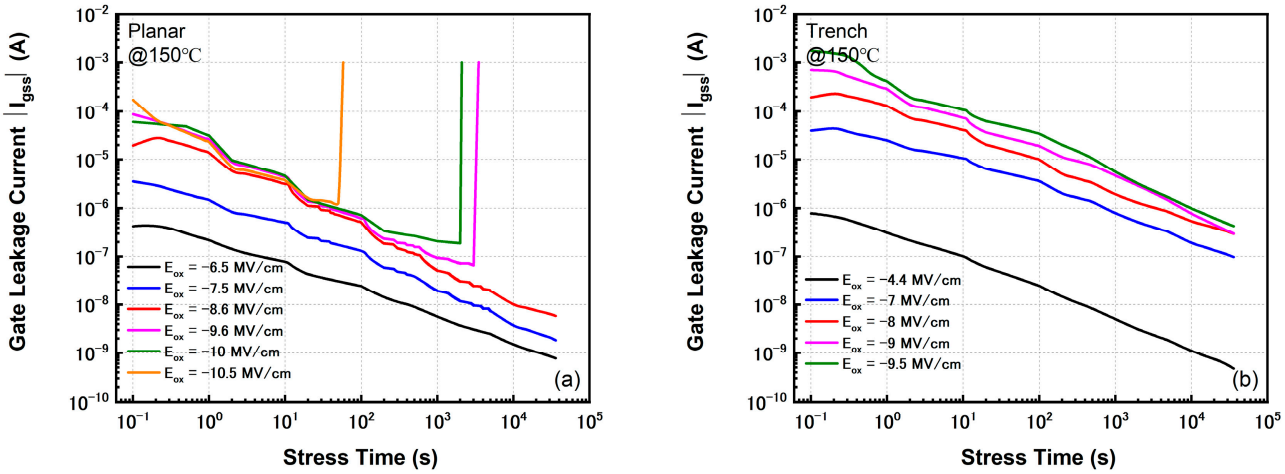


Figure 10. $|I_{gss}|$ as a function of stress time at 150 °C under different negative gate bias stresses for (**a**) SiC planar MOSFETs; (**b**) SiC asymmetric trench MOSFETs.

3.4. Constant-Voltage TDDB Test

The gate oxide lifetime of SiC planar and trench MOSFETs at 150 °C is assessed using the constant-voltage TDDB test. Figure 11a,b illustrate $t_{63\%}$ as a function of gate voltage and E_{ox}, respectively. For SiC planar MOSFETs, it can be observed that the E-model fitting of $t_{63\%}$ and E_{ox} produces two lines with different slopes under positive gate bias. The transition point where the slopes change is at E_{ox} of ~9.4 MV/cm. When the E_{ox} in the TDDB test ranges from 9.4 MV/cm to 9.9 MV/cm, the decay rate of $t_{63\%}$ accelerates as E_{ox}

increases. In the previous section, SiC planar MOSFETs show a significant rise in I_{gss} in the early stages of stress at E_{ox} of 9.6 MV/cm. It can be assumed that the increase in the FN tunneling current accelerates the degradation of gate oxide. In this case, the estimated oxide lifetime of SiC MOSFETs under operational conditions is overestimated. Therefore, the gate oxide stress that does not lead to significant hole trapping should be selected in the TDDB measurement to obtain accurate predictive values. For SiC trench MOSFETs, electron trapping continues to dominate the gate leakage current during TDDB tests, preventing any increase in I_{gss}. Compared to planar MOSFETs, trench MOSFETs accumulate more trapped electrons inside the gate oxide at high gate voltages, thereby suppressing the effect of hole trapping on I_{gss}. When the gate voltage in the TDDB test is negative, the oxide lifetime of the SiC planar MOSFET exhibits a linear relationship within the E_{ox} range of −8.5 MV/cm to −9.9 MV/cm. The same phenomenon can be observed in SiC trench MOSFETs. Table 2 shows the $t_{63\%}$ of SiC planar and trench MOSFETs obtained in the constant positive and negative gate voltage TDDB tests. Under the same gate voltage or E_{ox}, the oxide lifetime of SiC trench MOSFETs is higher than that of planar MOSFETs. This demonstrates the advantage conferred by the thick gate oxide layer fabricated through deposition [1]. In summary, SiC MOSFETs with a thicker oxide layer have a higher oxide lifetime.

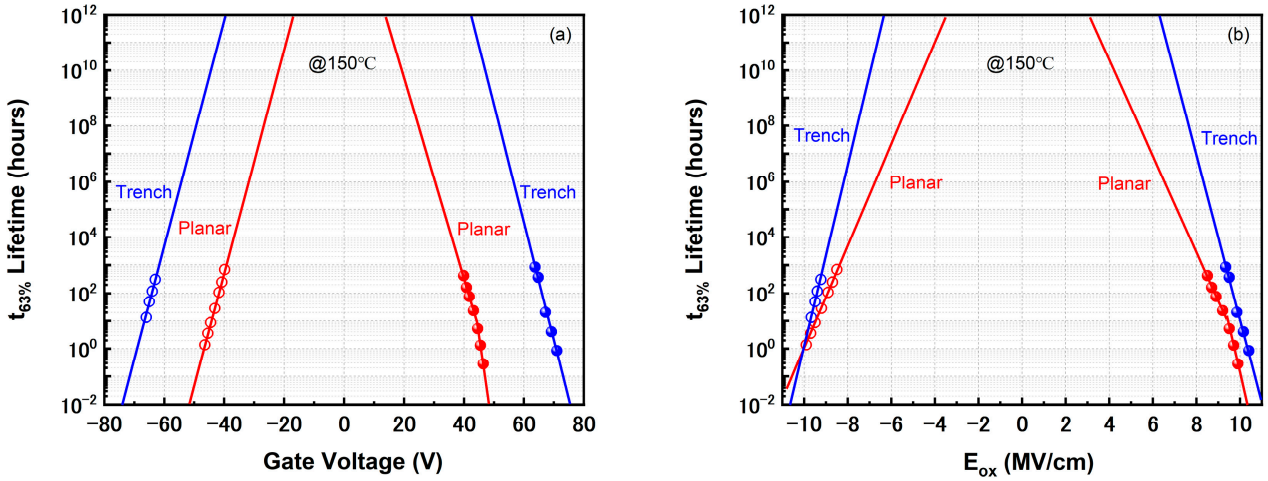


Figure 11. (**a**) $t_{63\%}$ vs. gate voltage at 150 °C; (**b**) $t_{63\%}$ vs. E_{ox} at 150 °C.

Table 2. Measured $t_{63\%}$ of SiC planar and asymmetric trench MOSFETs.

TDDB	SiC Planar MOSFETs			SiC Trench MOSFETs		
	V_g	E_{ox}	$t_{63\%}$	V_g	E_{ox}	$t_{63\%}$
Positive-TDDB	46.43 V	9.9 MV/cm	0.28 h	63.7 V	9.34 MV/cm	850 h
	45.49 V	9.7 MV/cm	1.31 h	64.8 V	9.5 MV/cm	369 h
	44.55 V	9.5 MV/cm	5.3 h	67.2V	9.85 MV/cm	20.31 h
	43.15 V	9.2 MV/cm	23.4 h	69.2 V	10.15 MV/cm	4.05 h
	41.74 V	8.9 MV/cm	75.2 h	71 V	10.4 MV/cm	0.85 h
	40.80 V	8.7 MV/cm	159.5 h	\	\	\
	39.87 V	8.5 MV/cm	419.5 h	\	\	\
Negative-TDDB	−46.43 V	−9.9 MV/cm	1.38 h	−63 V	−9.23 MV/cm	307.6 h
	−45.49 V	−9.7 MV/cm	3.6 h	−64 V	−9.4 MV/cm	117.5 h
	−44.55 V	−9.5 MV/cm	8.7 h	−65 V	−9.5 MV/cm	49.45 h
	−43.15 V	−9.2 MV/cm	28 h	−66 V	−9.67 MV/cm	13.3 h
	−41.74 V	−8.9 MV/cm	106.7 h	\	\	\
	−40.80 V	−8.7 MV/cm	248.4 h	\	\	\
	−39.87 V	−8.5 MV/cm	692 h	\	\	\

SiC MOSFETs exhibit differences in oxide lifetime when measured under positive and negative gate biases. For SiC planar MOSFETs, the oxide lifetime is generally longer under negative bias. Figure 12a shows the I_{gss} as a function of stress time measured by TDDB testing for SiC planar MOSFETs at E_{ox} of ±9.9 MV/cm. When E_{ox} is 9.9 MV/cm, the effect of hole trapping is dominant, which makes the I_{gss} show a clear upward trend in the early stage. When E_{ox} is −9.9 MV/cm, the effect of hole trapping causes I_{gss} to continuously decrease. The gate oxide is less prone to breakdown as I_{gss} continues to decrease. For SiC trench MOSFETs, the oxide lifetime measured under positive gate voltage tends to be slightly higher. As shown in Figure 12b, it can be observed that I_{gss} decreases at a faster rate with stress time under positive stress conditions. The decrease in I_{gss} under positive bias is primarily due to electron trapping, while the decrease under negative bias is caused by hole trapping. The rate of decrease is determined by the amount of charge trapped in SiO_2. From the test curves, the impact of electron trapping under a positive bias appears to be more pronounced. It can be considered that SiC trench MOSFETs have a higher density of electron traps in the gate oxide. In summary, charge trapping in the gate oxide significantly impacts the assessment of gate oxide lifetime in SiC MOSFETs. Considering that both electron and hole trapping can alter the effective electric field in the gate oxide, conducting gate oxide lifetime tests using a constant current is a more reliable and accurate TDDB testing method [41–44].

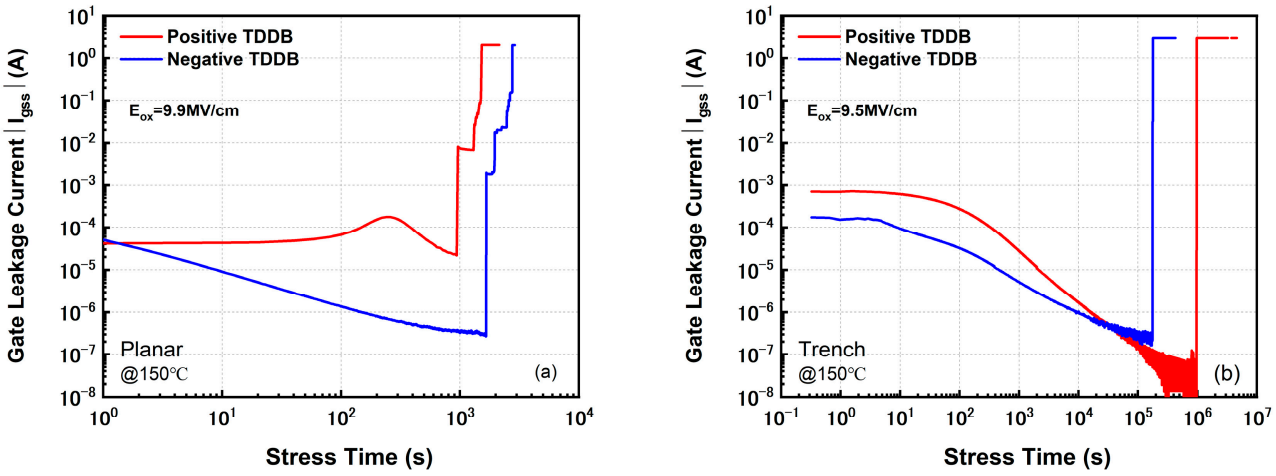


Figure 12. $|I_{gss}|$ vs. stress time at 150 °C in positive and negative TDDB tests for (**a**) SiC planar MOSFETs; (**b**) SiC asymmetric trench MOSFETs.

4. Conclusions

The influence of high-temperature gate bias stress on the gate oxide reliability of commercial 1.2 kV SiC planar and trench MOSFETs is investigated in this work. The threshold voltage of SiC MOSFETs is primarily influenced by electrons and holes trapped in gate oxide located in the channel region. The FN tunneling current composed of electrons or holes is influenced by the effective electric field and barrier height in SiO_2. For SiC trench MOSFETs, the variation in I_{gss} under constant gate voltage needs to consider the influence of charge trapping within oxide layers located at the sidewall and bottom of the gate. In SiC planar MOSFETs, significant hole trapping originating from impact ionization triggered by high positive voltage leads to a noticeable increase in I_{gss}, which in turn accelerates oxide lifetime degradation. Hole trapping in SiO_2 widens the tunneling barrier width for holes, causing I_{gss} in SiC MOSFETs to continuously decrease under negative gate voltage stress. TDDB test results reveal that SiC trench MOSFETs with a thicker oxide layer achieve a higher oxide lifetime compared to SiC planar MOSFETs. However, charge trapping in gate oxide under constant voltage stress can affect I_{gss} by altering the actual electric field within SiO_2 during TDDB measurement, leading to inaccurate predictions of oxide lifetimes. To

address this issue, constant current TDDB testing is recommended as a more accurate method for evaluating oxide lifetimes.

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