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Enhanced Readout Reliability in Phase Change Memory with a Dual-Sensing-Margin Offset-Compensated Sense Amplifier

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Abstract: Phase change memory (PCM) is considered one of the most promising candidates for next-generation non-volatile memory, owing to its scalability, durability, and cost-effectiveness. However, with the shrinking of device sizes and the reduction in supply voltages, achieving high-speed and reliable readouts in PCM has become increasingly challenging due to process variations. To address this, the dual-sensing-margin offset-compensated sense amplifier (DSOC-SA) is proposed. The DSOC-SA achieves the highest sensing margin, and the lowest read energy consumption compared to traditional sense amplifiers by utilizing a dual-sensing-margin structure, offset compensation, and strong positive feedback. Simulation results demonstrate that, compared to differential sense amplifier and offset-canceling current-sampling sense amplifier, DSOC-SA achieves a 5.6× and 1.6× improvement in sensing speed, respectively, while reducing power consumption by 87.1% and 51.2%.

Keywords: phase change memory (PCM); dual sensing margin; offset compensated

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1. Introduction

In recent years, rapid advancements in the Internet of Things (IoT), cloud computing, and artificial intelligence (AI) have driven extensive research into emerging non-volatile memory (NVM) technologies [1], including phase change memory (PCM), spin-transfer torque random access memory (STT-MRAM), and resistive switching random access memory (RRAM) [2–4]. These technologies address the performance and density gaps between dynamic random access memory (DRAM) and NAND, thanks to their nonvolatility [5], high speed [6], and high-density storage capacity [7]. Among these technologies, PCM stands out as a promising candidate for next-generation memory due to its excellent features, including its scalability [8], high endurance [9], and cost-effectiveness [10]. The storage mechanism of PCM is based on the reversible, thermally assisted phase transition between the crystalline state (SET) and the amorphous state (RESET) of chalcogenide phase change materials, such as $Ge_2Sb_2Te_5$ (GST) [11]. The amorphous phase, which is characterized by high resistance, typically represents "0", while the crystalline phase, with its lower resistance, represents "1". The resistance ratio between the SET and RESET states typically exceeds 10^2 [12], giving PCM superior sensing properties compared to other nonvolatile memories, such as MRAM, which has a resistance ratio of only 1.5 [5]. However, process variations in GST and programming errors, such as an insufficient SET programming time or RESET current, can significantly reduce the resistance difference between the SET and RESET states in the worst-case scenario [13]. As the power supply voltage (VDD) decreases and device sizes shrink, managing the fabrication process becomes increasingly challenging. This can lead to variations in the threshold voltage of PCM cells, driven by changes in oxide

thickness and the number of doped atoms in the transistor channel [14,15]. Such variations can make the performance of sense amplifiers (SAs) unpredictable, as both the sensing margin (SM) and sensing speed are highly sensitive to changes in process, voltage, and temperature (PVT). Furthermore, the dense integration of static PCM under low voltage conditions adds additional complexity. To enhance the competitiveness of PCM in layered storage systems, improving the sensing speed and reliability of the SA is therefore crucial.

Several advanced sense amplifier designs have been introduced in the literature to tackle this challenge. The approach in [16] exploits the difference between cell current and reference current to charge the bit line (BL) parasitic capacitance, comparing it to a fixed reference voltage. However, this method introduces a significant offset due to current mismatches. In [17], the differential SA structure improves sensing speed by employing fully symmetrical current mirrors and differential comparison techniques. However, this approach increases the number of current mirrors per sense amplifier, leading to higher area overhead. Additionally, the reference voltage for the differential comparator input does not track changes in the sensing node voltage, which impacts the sensing speed. To overcome these issues, [18] introduces single-reference parasitic matching, using varying reference currents that align with the read currents in the PCM array to improve sensing speed. However, the large reference array increases area overhead, particularly with longer bit lines, and may introduce additional transistor mismatches and offsets. In [19], a pseudo-differential structure is used to enhance the sensing margin, although the pre-charge time for the sensing voltage is heavily dependent on parasitic capacitance. [20] presents an offset-canceled current-sampling sense amplifier (OCCS-SA) that improves the sensing margin by employing a data-dependent reference generator, but it requires additional latch Sas and capacitors to manage offsets. Overall, achieving a balanced trade-off between sensing reliability, sensing speed, energy consumption, and area efficiency is a significant challenge.

In this paper, we propose a dual-sensing-margin offset-compensated sense amplifier (DSOC-SA) that achieves a large sensing margin and high sensing speed by utilizing offset cancelation technology and a dual-sensing-margin (DSM) structure. To demonstrate this, a 1024 × 32 PCM array was implemented, comprising 128 DSOC-Sas, 128 differential Sas, and 128 OCCS-Sas, all designed with identical mismatches in 40 nm CMOS technology. The experimental results show that the DSOC-SA achieves significant improvements in sensing speed, with improvements of 5.6× and 1.6×, respectively, while reducing read consumption by 87.1% and 51.2%, respectively, compared to the traditional differential SA and OCCS-SA. The remainder of this paper is organized as follows. Section 2 provides an overview of conventional sense amplifiers. The concept and operation of the DSOC-SA are introduced in Section 3. Section 4 presents the simulation results and compares the DSOC-SA with other sense amplifiers. Finally, Section 5 concludes the paper.

2. Conventional Sense Amplifier Architectures

Figure 1a illustrates the working principle of a traditional differential sense amplifier [17], which consists of two main stages: the equalization stage (P1) and the development stage (P2). In the P1 stage, when the voltage difference between the gate voltage of the clamping transistor (V_{clamp}) and the BL voltage (V_{BL}) exceeds the threshold voltage of the clamping transistor, the sense amplifier is activated, generating a large pre-charge current (I_{pre}) on the BL. This pre-charge current is composed of the current flowing through the target cell (I_{cell}) and the current flowing through the parasitic capacitance (I_{par}). Since the transistors M1–M3, M4–M6, M7–M8, and M9–M10 form current mirrors, the current through transistor M3 is equal to the current through transistor M1 (i.e., $I_{M3} = I_{M1} = I_{pre}$), and, similarly, $I_{M7} = I_{M8} = I_{ref}$, where I_{ref} is the current flowing through the reference cell. During the P1 stage, the current ($I_{pre} - I_{ref}$) charges node 1, while an equal current discharges node 2, resulting in $V_1 > V_2$. Once the circuit reaches a balanced state, the P2 stage begins. At this point, the parasitic current becomes negligible, and the actual read current from the target cell is compared with the reference current. If the target

cell is in the SET state, the SA output remains unchanged, maintaining $V_1 > V_2$. However, if $I_{cell} < I_{ref}$, node 1 is discharged by $I_{ref} - I_{cell}$, while node 2 is charged by the same current. In the early part of the P2 stage, parasitic current still dominates, causing slow changes in V_1 and V_2. As the parasitic current decreases and the phase-change cell current takes over, V_1 and V_2 change rapidly, and the SA output flips, making $V_1 < V_2$. This voltage flip contributes to the slow sensing in the differential SA scheme. To improve immunity to interference, the current mirrors in the differential SA must be better matched. When the difference between the phase-change cell current and the reference cell current is small, the width-to-length ratio of the current mirrors must be increased, which leads to an increased area. Consequently, improving the sensing window is limited. Additionally, the reference voltage input to the differential comparator cannot respond quickly to fluctuations in the sensing node voltage, which further limits the sensing speed of the SA.

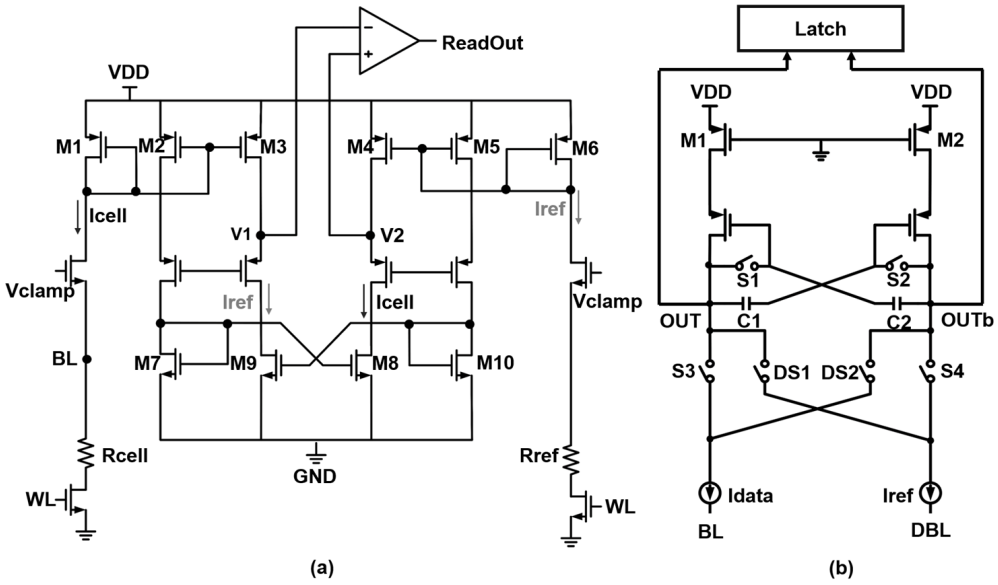


Figure 1. Circuit schematics: (**a**) differential SA; (**b**) OCCS-SA.

Figure 1b illustrates the circuit of the OCCS-SA [20], which is based on the CSB-SA [21]. By adding a pair of switches (DS1 and DS2), it creates a direct current path to the ground, generating strong positive feedback that improves both the sensing margin and sensing speed. The OCCS-SA operates in three stages: P1, P2, and the latch stage. In the P1 stage, transistors M1 and M2, connected to diodes, charge the BL and dummy BL, respectively. After this stage, the BL voltages of the target and reference cells are stored on the left electrode of capacitor C1 and the right electrode of capacitor C2. In the P2 stage, switches S1–S4 are off, and the grounding switches DS1 and DS2 are activated to amplify the signal sampled during P1. While the OCCS-SA provides strong positive feedback and a large SM, it comes with significant area overhead due to the separate latch and sensing sections, which require large capacitors.

3. Proposed DSOC-SA

In this part, we propose a dual-sensing-margin offset-compensated sense amplifier (DSOC-SA), with the circuit scheme and timing diagram shown in Figure 2. This design integrates both the latching and sensing functions of the SA, resulting in a more compact area compared to the OCCS-SA. The DSOC-SA operates in three stages: pre-charging (P1), voltage development (P2), and latching (P3). The scheme uses two identical transistors, M1 and M2, to perform current sampling and amplification. By ensuring the transistors are well-matched, current sampling is made independent of the threshold voltage (Vth), thereby mitigating performance degradation caused by offset.

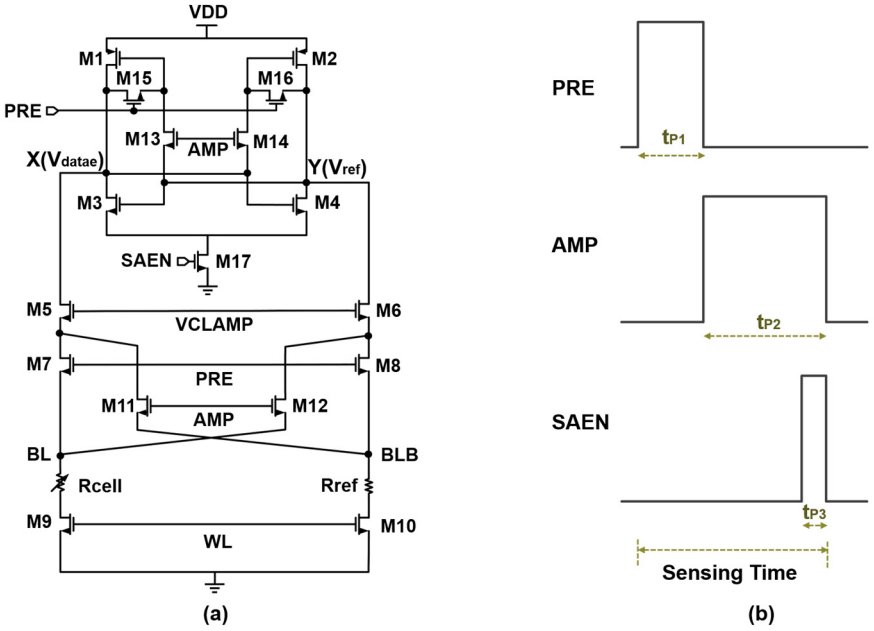


Figure 2. (**a**) Circuit schematic of proposed DSOC-SA. (**b**) Timing diagram.

Figure 3a illustrates the equivalent circuit of the DSOC-SA during the P1 stage. In this stage, switches S1, S2, S5, and S6 are activated, while switches S3, S4, S7, S8, and the enable transistor (M17) are deactivated. The PMOS transistors M1 and M2, connected to diodes, pre-charge the BL of the target cell and the reference cell, respectively. The voltage at node X reflects the resistance state of the target cell. Since the duration of this stage is primarily determined by the parasitic capacitance on the BL, its exact value can only be estimated. Therefore, adequate time must be provided for this stage to ensure that the voltage difference between nodes X and Y stabilizes. As depicted in Figure 3b, the second stage, known as the voltage development stage, commences with the rising edge of the AMP signal. In this stage, switches S1 and S2 are turned off, while switches S3 and S4 are turned on, providing strong positive feedback, rapidly amplifying the voltage difference between nodes X and Y. Meanwhile, switches S7 and S8 are on, further increasing the sensing margin.

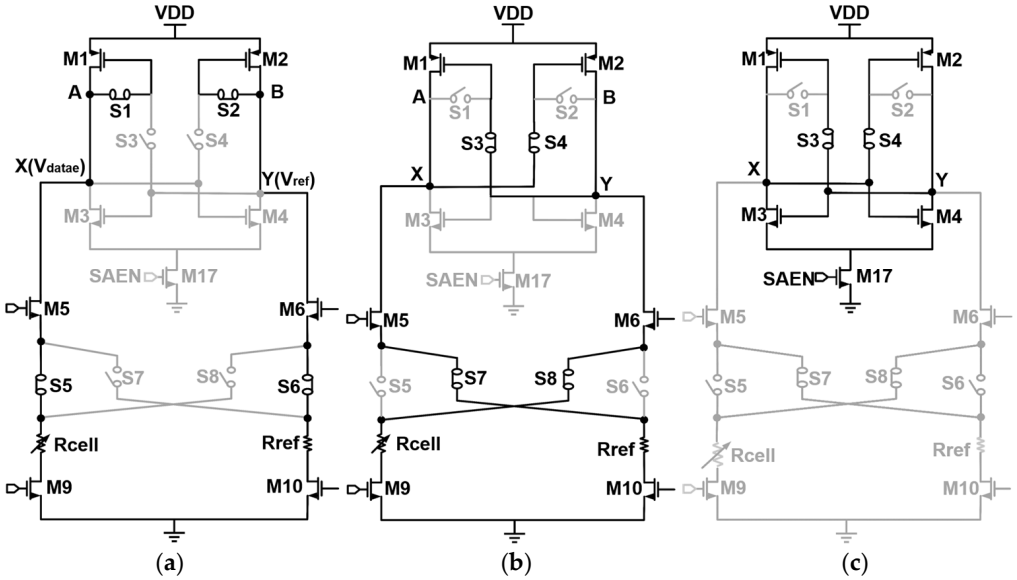


Figure 3. Operation of proposed DSOC-SA in different stages: (**a**) pre-charging stage; (**b**) voltage developing stage; (**c**) latching stage.

To illustrate how the DSOC-SA performs offset compensation, we assume that due to process variations, transistor M1 is enhanced while transistor M2 is weakened. In the P1 stage, the diode-connected PMOS transistors M1 and M2 pre-charge the BL for the target and reference cells, respectively. As a result, the voltages at nodes A and B are charged to VDD − $|V_{th1}|$ and VDD − $|V_{th2}|$, respectively. Although this charging is asymmetric, this offset between M1 and M2 is compensated in the subsequent stage. In the next stage, the voltages at nodes A and B are adjusted to VDD − $|V_{th2}|$ and VDD − $|V_{th1}|$, respectively. Figure 4 shows the transient response of the DSOC-SA in both the 0 and 1 states under mismatch conditions, demonstrating that strong positive feedback and offset compensation enable reliable data detection.

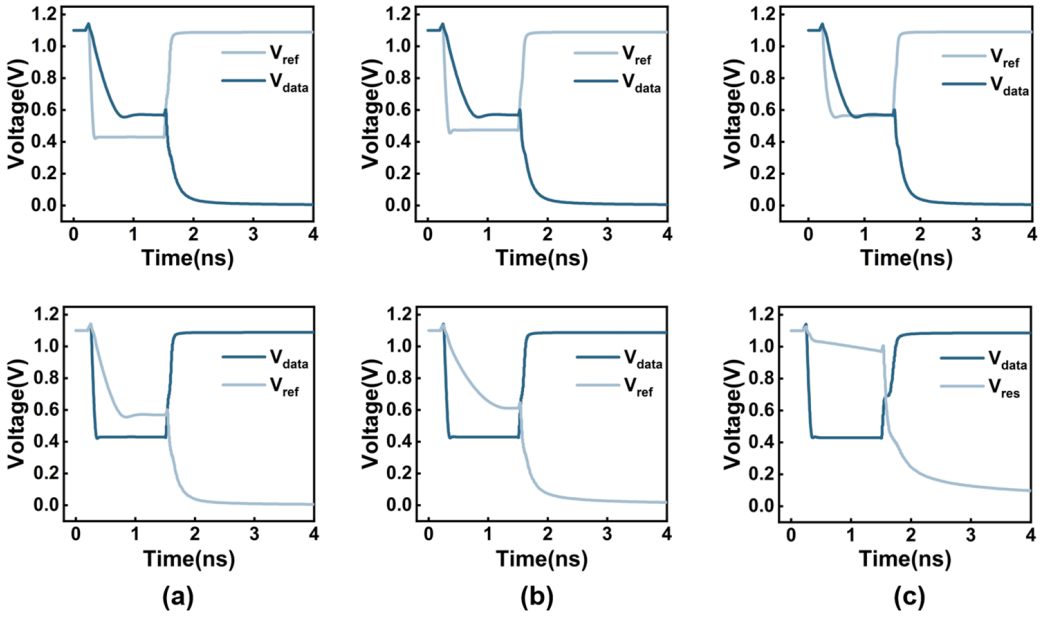


Figure 4. Simulated transient responses: (**a**) without mismatch; (**b**) 50 mV Vth mismatch between M1 and M2; (**c**) 200 mV Vth mismatch between M1 and M2.

Figure 5 illustrates how the DSM structure enhances read reliability. Given sufficient pre-charge time, by the end of the P1 stage, the current through transistor M1 (I_{M1}) becomes I_{cell}, while I_{M2} equals I_{ref}, resulting in a current difference of ΔI_{SA1} between nodes X and Y, where $\Delta I_{SA1} = I_{M1} - I_{M2}$. When the P2 stage begins, switches S7 and S8 are on, and the current through transistor M1 becomes $|I_{ref} - I_{cell}|$. Similarly, $I_{M2} = |I_{cell} - I_{ref}|$. This amplifies the current difference between nodes X and Y to $2 \times \Delta I_{SA1}$, effectively increasing the sensing margin. Moreover, the DSM structure can correct current sampling errors from the P1 stage. If the target cell is in the SET state ($I_{cell} > I_{ref}$), then during P1, $I_{M1} > I_{M2}$, leading to $V_{data} < V_{ref}$ in P1 and $V_{data} > V_{ref}$ in P2. If process variations cause transistor mismatches that lead to $I_{M1} < I_{M2}$, a sampling error occurs in P1, resulting in $V_{data} > V_{ref}$ by the end of P1. When switches S7 and S8 are on, I_{cell} discharges node Y. Due to strong positive feedback, V_{ref} continues to decrease toward the ground. As long as I_{cell} and I_{ref} are not reversed, the DSM structure can correct the current sampling error caused by transistor mismatches.

Figure 3c shows the latch stage. In the P3 stage, the DSOC-SA acts as a voltage-sensing amplifier, rapidly amplifying the voltage difference (ΔV) developed in P2 to produce digital signals (0 or 1), where $\Delta V = V_{data} - V_{ref}$. Although transistors M1–M4 may generate an offset voltage due to process variations during the transition from P2 to P3, this offset voltage is negligible compared to the ΔV achieved in P2. Therefore, unlike the OCCS-SA, the DSOC-SA can efficiently convert ΔV into a rail-to-rail output without requiring additional capacitors or a large latch circuit at the output.

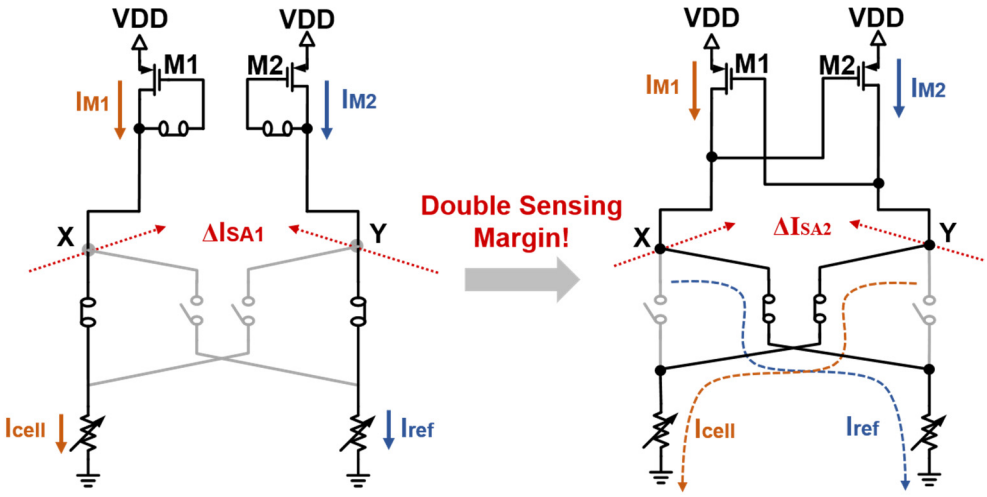


Figure 5. Explanation of the double sensing margin.

4. Simulations Results and Comparison

To assess the effectiveness of the proposed approach, the performance of DSOC-SA, differential SA, and OCCS-SA was compared using the Spectre simulator with standard 40 nm CMOS technology. The device parameters for PCM, as referenced from [22], are listed in Table 1. Figure 6 shows a typical programming curve for PCM. The initial state of PCM is generally amorphous (high-resistance). Applying a low-amplitude, long-duration current pulse, the GST material is heated to a temperature between its crystallization point and melting point, promoting nucleation and grain growth, which stabilizes it in a polycrystalline (low-resistance) state. To return the device to the amorphous state, a higher-intensity current pulse is applied, heating the GST material above its melting point. The pulse is then quickly removed, quenching the material rapidly to room temperature. This rapid supercooling causes the GST material to transition from crystalline to amorphous [23,24]. Based on this programming process, the critical nominal values for the SET resistance and RESET resistance are 50 K and 200 K, respectively, with variances of 10 K and 45 K. The supply voltage is fixed at 1.1 V, with each BL containing 1024 PCM cells to simulate the impact of parasitic capacitors on the BL.

Table 1. The list of design parameters.

Parameter	Value
VDD	1.1 V
R_{REF}	100 K
R_{SET} (μ)	50 K
R_{SET} (σ)	10 K
R_{RESET} (μ)	200 K
R_{RESET} (σ)	45 K

To evaluate the yield of a read operation, a Monte Carlo simulation is conducted to assess the read access pass yield ($RAPY_{CELL}$), defined as the sigma-level yield of a PCM cell where the read access is successful [25]. Since the ΔV variation in the sense amplifier and the offset voltage from process variations can be effectively modeled by a Gaussian distribution, $RAPY_{CELL}$ is represented as:

$$RAPY_{CELL0,1} = \frac{\mu_{\Delta V0,1} - \mu_{SA_OS}}{\sqrt{\sigma^2_{\Delta V0,1} + \sigma^2_{SA_OS}}} \quad (1)$$

$RAPY_{CELL0,1} = n\sigma$, indicating the probability of a successful read access, and is calculated by integrating the normal distribution from $-\infty$ to $+n\sigma$ [26]. Here, SA_OS represents the offset voltage of the sense amplifier, with $\mu_{\Delta V}(\mu_{SA_OS})$ and $\sigma\Delta V(\sigma_{SA_OS})$ denoting the mean and standard deviation of ΔV (SA_OS), respectively. Subscripts 0 and 1 indicate the RESET and SET states of PCM, respectively. In this brief, $RAPY_{CELL}$ is the minimum value between $RAPY_{CELL0}$ and $RAPY_{CELL1}$, with μ_{SA_OS} and σ_{SA_OS} set to 0 and 20 mV, respectively, and the target $RAPY_{CELL}$ set to 6σ. A total of 1000 Monte Carlo trials were conducted, setting a sensing time of 3.5 ns, where T_{P1} = 1.25 ns, T_{P2} = 2 ns, and T_{P3} = 0.25 ns. TP2 was set with a sufficient safety margin to ensure that even the weakest bit could be detected under worst-case operating conditions. Process variations in CMOS technology were included in the Monte Carlo simulations, with nominal threshold voltages for NMOS and PMOS set to 355 mV and −366 mV, respectively, each with a standard deviation of 10 mV. Since the resistivity of GST materials is inherently temperature-dependent, with GST resistance changes primarily driven by Joule heating [27], the reference cells in the memory array are constructed from the same material to track temperature-induced variations in the read current. The read throughput of devices in both the low-resistance and high-resistance states was measured at temperatures of −40 °C, 27 °C, and 85 °C. Table 2 presents the $RAPY_{CELL}$ values for the proposed DSOC-SA under these different temperature conditions. Notably, the worst $RAPY_{CELL}$ value in the RESET state at −40 °C was 6.04σ, still meeting the target $RAPY_{CELL}$ requirement. As previously mentioned, while the resistivity of chalcogenide materials decreases with rising temperature [28], the DSOC-SA can reliably sense data even when temperature-induced changes reduce the read-window, thanks to its DSM structure and strong positive feedback.

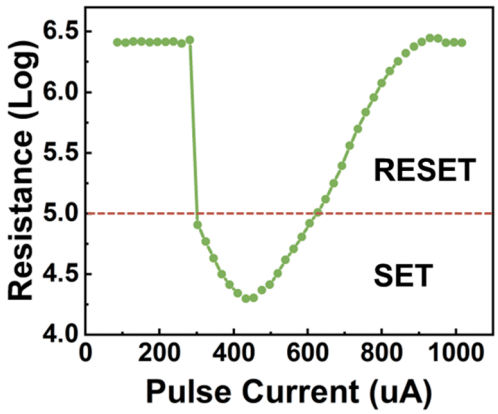


Figure 6. The typical programming curve of PCM.

Table 2. $RAPY_{CELL}$ at different temperatures with sensing time = 3.5 ns.

Temperature (°C)	State	μΔV (mV)	σΔV (mV)	$RAPY_{CELL}$ (σ)
−40	0	733.14	119.7	6.04
	1	606.9	60.7	9.5
27	0	739.3	66.7	10.62
	1	703.1	83.3	8.21
85	0	707.9	69.3	9.81
	1	682.4	42.6	14.5

Figure 7 shows the Monte Carlo simulation results for 4000 samples under the worst-case scenario (−40 °C), which corresponds to the lowest $RAPY_{CELL}$ value. This result highlights the importance of offset elimination in achieving the optimal $RAPY_{CELL}$, demonstrating that the DSOC-SA with offset compensation and a dual-sensing-margin structure can substantially enhance read reliability and sensing speed.

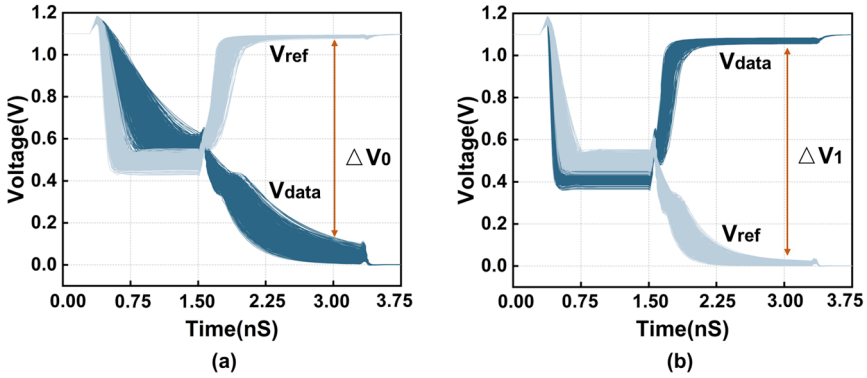


Figure 7. The Monte-Carlo simulation results of the proposed sensing scheme for the worst case: (**a**) State 0; (**b**) State 1.

Figure 8 presents a comparison of the ΔV distributions across different designs. To ensure a fair comparison, all sense amplifiers were simulated using transistors of the same size. Due to the mismatch in the current mirror structure of differential SA, an offset between the reference current source and the mirrored current source leads to a lower average ΔV compared to the other two structures. In contrast, the DSOC-SA, with its dual-sensing-margin structure, shows an average ΔV similar to that of the OCCS-SA. Additionally, the offset compensation in both DSOC-SA and OCCS-SA results in smaller ΔV variations than in the differential SA. Notably, for ΔV < 0.2 V, the differential SA shows a broader sample distribution, while DSOC-SA and OCCS-SA exhibit no sample distribution within this range. This indicates that differential SA is more likely to cause sensing errors when the voltage of SA_OS is larger, while DSOC-SA and OCCS-SA offer improved readout reliability.

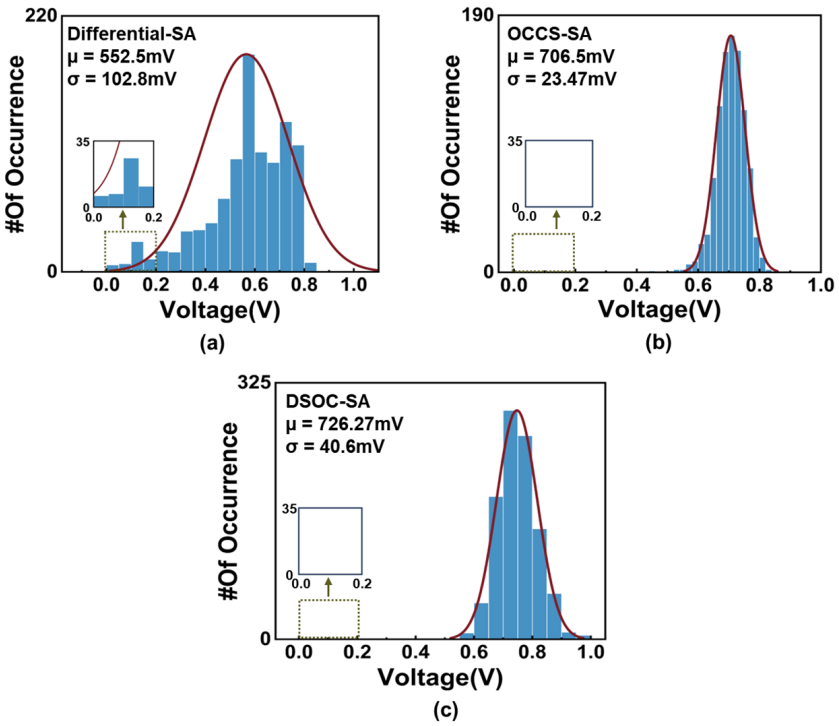


Figure 8. SM distribution: (**a**) differential SA; (**b**) OCCS-SA; (**c**) DSOC-SA.

Figure 9 compares the sensing delay of three sense amplifier designs. Sensing delay is defined as the time between the activation of the AMP signal and when the output voltage reaches either 0.9 VDD or 0.1 VDD. As the supply voltage decreases, the performance of

the sense amplifier deteriorates. Since the differential SA relies on the current difference between the target and reference cells to control the gate of the differential-input NMOS pair, it exhibits the highest sensing delay. In contrast, the proposed DSOC-SA shows the lowest sensing delay across a wide range of supply voltages, making it particularly well-suited for low-voltage applications.

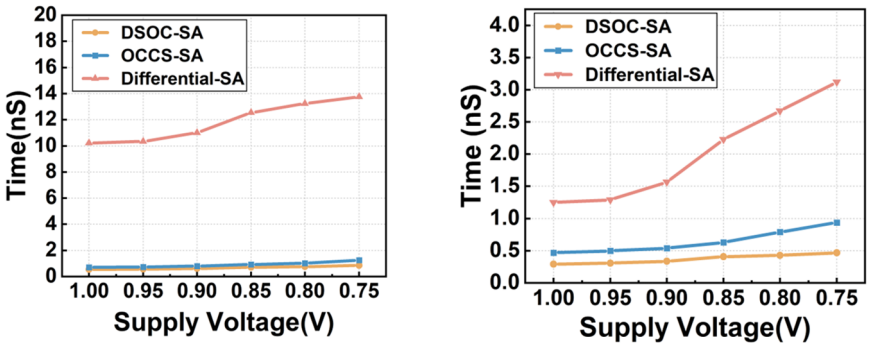


Figure 9. Variation in sensing delay with supply voltage between differential SA, OCCS-SA, and DSOC-SA: (**a**) Read 0; (**b**) Read 1.

Table 3 presents a performance comparison between DSOC-SA and traditional sense amplifiers. The DSOC-SA demonstrates the shortest sensing time and the lowest read energy. In contrast, differential SA relies on a long current mirror chain to meet the target $RAPY_{CELL}$, resulting in a longer sensing time and higher energy consumption per bit. Both DSOC-SA and OCCS-SA utilize a DSM structure, allowing them to quickly achieve the target $RAPY_{CELL}$. However, DSOC-SA stands out by integrating the sensing and latching circuits at the output, eliminating the need for additional capacitors or extra latching circuits, which significantly reduces area overhead. In terms of performance, DSOC-SA improves sensing speed by 5.6× and 1.6× and reduces power consumption by 87.1% and 51.2% compared to differential SA and OCCS-SA, respectively.

Table 3. Compensation between proposed DSOC-SA and OCCS-SA in 40 nm CMOS technology with identical transistor sizing.

	Differential SA [10]	**OCCS-SA [13]**	**This Work (DSOC-SA)**
VDD	1.1 V	1.1 V	1.1 V
Offset Cancelation	X	√	√
Area Consumption	Large	Large	Small
Sensing Time	19.6 ns	5.5 ns	3.5 ns
Average Read Energy/Bit	792 fJ	209 fJ	102 fJ

5. Conclusions

This paper introduces the dual-sensing-margin offset-compensated sense amplifier, a novel scheme aimed at achieving high-speed, reliable readout for phase change memory. By employing a DSM structure, offset compensation, strong positive feedback, and less transistors, DSOC-SA enhances read margin, and decreases area and read energy consumption compared to conventional SAs. Additionally, DSOC-SA demonstrates minimal sensing delay across a wide range of supply voltages, making it well-suited for low-voltage applications. Beyond PCM, DSOC-SA is also suitable for other resistive NVM devices.

Author Contributions: Conceptualization, Q.W. and X.L.; methodology, Q.W.; software, X.L., X.D. and C.X.; validation, Q.W. and C.X.; formal analysis, Q.W.; investigation, Q.W.; resources, X.L.; data curation, Q.W.; writing—original draft preparation, Q.W.; writing—review and editing, Q.W., C.X. and X.D.; visualization, X.L., X.D. and S.S.; supervision, X.L., Q.W., S.S. and Z.S.; project

administration, Z.S., S.S. and X.L.; funding acquisition, Z.S. and X.L. All authors have read and agreed to the published version of the manuscript.

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