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A Programmable Gate Driver Module-Based Multistage Voltage Regulation SiC MOSFET Switching Strategy

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Abstract: Silicon carbide (SiC) metal-oxide semiconductor field-effect transistors (MOSFETs), as a new material, have the advantages of low drain-source resistance, high thermal conductivity, low leakage current, and high switching frequency compared with silicon (Si)-based MOSFETs. Therefore, in many industrial applications, Si MOSFETs have been replaced by SiC MOSFETs. However, as the switching speed increases exponentially, some problems are amplified, the most serious of which is the overshoot of current and voltage. The increase in voltage and current slope caused by high switching speeds inevitably leads to overshoot, oscillations, and additional losses in the circuit. This paper focusses on the actual performance of the optimised switching strategy (OSS) in circuit testing and combines the existing simulation results to verify the practicability of OSS. In this paper, the optimised switching strategy is introduced first, and then, the LTspice model of SiC MOSFET is established in detail and verifies the feasibility of the OSS through half-bridge circuit simulation. Finally, the test platform is built using a programmable gate drive module (2ASC-12A1HP). Through a 400 V/30 A double-pulse test, the practicality of the OSS is verified. The experiments show that the OSS can greatly improve the switching performance of SiC MOSFETs.

Keywords: grid driver circuit control; silicon carbide MOSFET; double-pulse test circuit; voltage and current overshoot; LTspice

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1. Introduction

With the depletion of primary energy such as gas and oil, electric energy as a clean secondary energy has penetrated all aspects of people's production and life, and the development and progress of human society have been inseparable from electric energy. Nowadays, electronic technology is widely used in many different fields, such as industry, consumer, automobile, aerospace, etc. As people's requirements for size and cost become continue to rise, so do their requirements for efficiency and power [1].

After decades of development, traditional power semiconductor devices such as silicon (Si)-based devices such as the silicon-based insulated-gate bipolar transistor (Si IGBT) and the silicon oxide semiconductor field-effect tube (Si MOSFET) have matured, occupying a dominant position in the power semiconductor industry, featuring high manufacturing capacity and extremely low cost. However, due to the theoretical limitations of their materials, the development of silicon-based devices has almost reached its limits [2]. Therefore, new alternative materials are needed to meet the requirements of high-performance power systems, and SiC materials have many advantages in applications due to their inherent physical properties, such as wide band gap, high critical electric field, and high thermal conductivity [3–5]. Compared with silicon-based devices, SiC-based devices have many advantages in applications due to their physical properties, such as wide band gap, high critical electric field, and high thermal conductivity [2,6].

Among them, SiC MOSFETs exhibit switching loss that is more than one order of magnitude smaller than silicon IGBT due to its higher switching speed [7]. This allows

the SiC MOSFET to operate at higher switching frequencies, such as those above 100 kHz. Therefore, the volume of passive components such as inductors and capacitors in the circuit system can be greatly reduced, which highly improves the power density of the system. However, the high switching speed also brings new problems to practical applications.

Figure 1 shows the oscillations and overshoots of the drain-source voltage (V_{DS}) during the actual and ideal switching process. The turn-on and turn-off stages of the SiC MOSFET in the actual converter are accompanied by the current exchange between the device itself and the current diode. Due to the parasitic parameters in the circuit, there are overshoot and oscillation of drain-source current (I_{DS}) and gate-source voltage (V_{GS}) in the circuit during the switching process of the SiC MOSFET [8]. Because the parasitic parameters have great influence on the switching process, the increased switching speed is positively correlated with the severity of overshoot and oscillation [3,9].

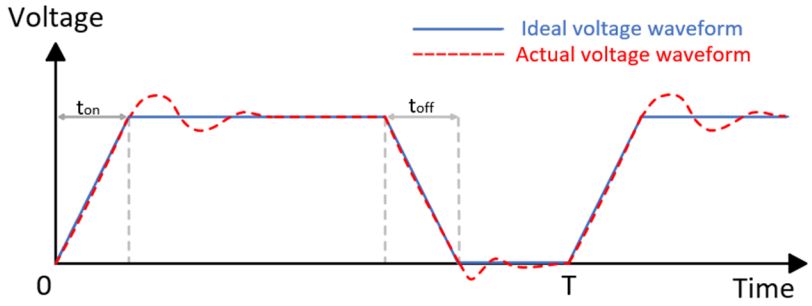


Figure 1. Drain-source voltage waveform during switching.

The higher switching speed mainly refers to the larger voltage change slope (dv/dt) and current change slope (di/dt). In this paper, dv/dt refers specifically to the drain-source voltage change slope (dV_{ds}/dt) of a SiC MOSFET and di/dt refers specifically to the drain-source current change slope (dI_{ds}/dt). A large di/dt will influence the parasitic inductance in the circuit, leading to voltage overshoot, which may harm the device [10]. At the same time, high dv/dt can also bring many problems, such as isolating power coupling through the drive loop, raising or lowering the drive voltage, and leading to misdirection problems. These problems due to high dv/dt induction require us to carry out certain inhibition or control of dv/dt of the SiC MOSFET [11]. Therefore, it is necessary to properly control the voltage and current slope of the SiC MOSFET using good gate driver methods [12].

In order to solve the problems caused by the high switching speed of SiC MOSFETs, many solutions have been proposed. In conventional methods, slowing down the switching speed can alleviate the over harmonic oscillation of the SiC MOSFET [13,14]. However, this solution means that the advantages of high-speed switching are lost [15–17]. Another common method is to add an RC buffer circuit. Although efficient buffer circuits have been proposed, the buffer circuit will increase the power loss of the entire circuit and affect the overall efficiency of the system [17]. Active gate drivers (AGDs) have been widely studied as a relatively new solution. The main advantage of AGDs is the reduction in oscillation and overshoot. However, it is also obvious that adding a device requires an additional power supply, which increases the power consumption of the circuit [18]. In [15], an active gate driver is proposed that can effectively suppress over harmonic oscillations and reduce power losses without affecting EMI (electromagnetic interference). The control strategy as in Article [15] involves reducing the current and voltage slope by changing the resistance of the gate driver circuit. However, the disadvantage is that the calculation process is complex and requires additional circuits [19–21]. In Article [22], a synchronous variable-amplitude driving method is proposed. While this method of controlling three variables is quite innovative, it still functions as an AGD and does not allow for the flexible control of each variable to achieve the optimal control effect.

Currently, programmable digital gate drivers (DGDs) are the newest technology in this field. Its advantages lie in its programmability, support for various semiconductor

devises, and ease of use [23]. The most outstanding point of DGDs is the ability to configure the gate driver voltage waveform turn-on and turn-off stages. This allows the designer to make changes to the gate voltage waveform through software without changing the hardware [24]. Article [25] demonstrates the modularity and extensibility of DGDs in applications. The correct gate voltage waveform configuration effectively alleviates the voltage overshoot.

Article [1] proposes an optimised switching strategy (OSS) based on variable voltage gate driver. This control method not only has the advantages of AGDs in waveform control but also allows for the easy operation of DGDs [12,15]. The principle of the optimised switching strategy is to change the slope of voltage and current during the turn-on and turn-off stages by changing the gate driver voltage. Specifically, after a certain delay period, the driver voltage is reduced and kept at a low level to directly control the di/dt and dv/dt [26–29]. The potential for the OSS is huge. Unlike other switching strategies, the OSS can make multiple adjustments to the waveforms of gate driver voltage. At the same time, the programmability of the gate driver voltage in software allows people to easily try different ways in experiments to find out the final answer to optimise SiC MOSFET device switching performance. Article [1] shows that the OSS has the ability to simultaneously control three variables: the delay time before the voltage drop, the drop time of the voltage, and the voltage drop. More variables mean better control performance, so the OSS can control more variables than AGDs and DGDs, achieving more accurate and better circuit control. Article [1] has verified the basic functions of the OSS through simulation. This paper mainly verifies the partial feasibility of the OSS through simulation and experimentation. While Article [1] offers a comprehensive explanation and simulation of the OSS, the simulation results alone do not sufficiently support its conclusion. This work integrates previous simulation results, constructs an experimental platform, and tests the device under the OSS to assure its practicality. Unfortunately, due to device limitations, the excellent performance of the OSS cannot be fully utilised [27].

The structure of this paper is mainly divided into four parts. The first part introduces the research background of OSS control of SiC MOSFET and expounds the necessity of OSS control of SiC MOSFETs. In the second part, the OSS control principle and double-pulse test detection principle of SiC MOSFETs are introduced. In the third part, LTspice simulation software (v17.1.6) is used to implement the proposed OSS, and the effectiveness of the OSS is preliminary verified. The fourth part is the experimental verification, which verifies the effectiveness and limitations of the OSS and verifies the feasibility and effectiveness of this control strategy in reducing the switching loss.

2. The Principles of the Optimised Switching Strategy and Double-Pulse Test

2.1. The Principles of the Optimised Switching Strategy

The OSS works by controlling the voltage drop delay time (t_d), voltage drop (V_{drop}), and voltage drop time (t_{vd}) to improve the SiC MOSFET switching performance [1]. The advantage of the OSS is that it has more control keys than AGDs and DGDs, which means that the switching performance of the semiconductor can be optimised. This section explains how the OSS works in detail.

One switching process of the SiC MOSFET can be divided into two steps: the turn-on stage and the turn-off stage. The SiC MOSFET model shown in Figure 2 includes junction capacitors (Cgd, Cds, and Cgs) and intrinsic parasitic inductors (Ls, Ld, and Lg) [15].

The turn-on stage is where the gate drive circuit emits a large amount of peak current to continuously charge the Cgd and Cgs capacitors. The turn-off stage is essentially the opposite of the order of the turn-on stage described above. The role of gate drive is to absorb a large amount of peak current, which can discharge the Cgd and Cgs capacitors as soon as possible. Due to the SiC MOSFET's low value of the threshold voltage (V_{TH}), it is usually necessary to use below-zero voltages as V_{MIN}, and the current filling capacity of the gate driver must also be much larger than the rated source current. Figure 3 shows the timing chart of the SiC MOSFET with the optimised switching strategy.

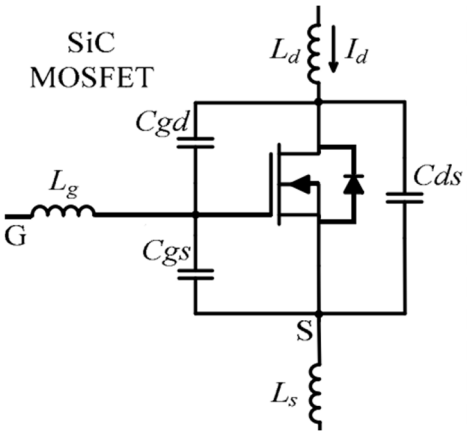


Figure 2. Schematic diagram of SiC MOSFET.

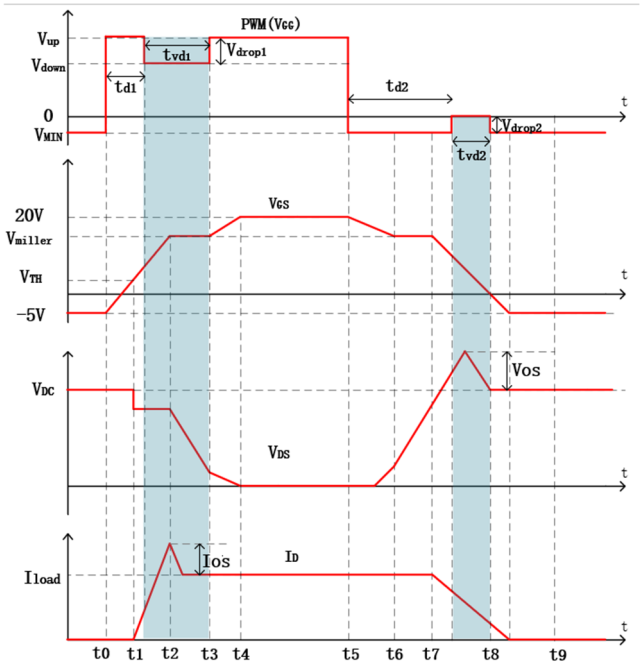


Figure 3. Timing chart of the SiC MOSFET with the OSS.

The Miller plateau is a phase during which a field-effect switching device such as a MOSFET or IGBT is turned on or off when the voltage is maintained at a relatively constant level. The induced voltage needs to cross the Miller platform to complete the switch conversion. Therefore, the Miller platform plays a very important role in the OSS.

The turn-on stage has four time periods:

1. t0→t1: The driver starts to output the forward drive voltage after receiving the open signal, at which time V_{GS} rises from V_{MIN} to V_{TH}. During this period, the I_D and V_{DS} remain basically unchanged because V_{GS} is still lower than V_{TH}, and most of the current in this phase is used to charge Cgs and Cgd.
2. t1→t2: V_{GS} rises from V_{TH} to the Miller platform (V_{miller}). During this period, I_D begins to gradually increase. V_{DS} is slightly reduced but still maintains a high voltage, because I_D is small and R_{DS} is large. At this time, the intrinsic diode of the SiC MOSFET is blocked.
3. t2→t3: V_{GS} is located at the Miller platform. For the SiC MOSFET, during this period, the full I_{load} flows to R_{DS}, and the diode is no longer in a blocked state, such that the drain voltage drops, and the on-resistance continues to decrease. Despite the full load current flowing through the MOSFET drain, R_{DS} remains high during this period.

4. t3→t4: V_{DS} continues to decline at V_{miller}, near the end of Miller's platform. Because when $V_{GS} > V_{MILLER}$, the SiC MOSFET is close to full conduction. The remaining gate current IG is distributed to Cgd and Cgs charging.

The turn-off process of a silicon carbide MOSFET consists of four time periods:

1. t5→t6: V_{GS} drops to V_{miller}. Drain current I_D remains unchanged. As V_{GS} decreases, the channel resistance increases, resulting in a slight increase in V_{DS}.
2. t6→t7: During this period, since V_{GS} remains almost constant, the size of the gate current is mainly determined by Cgd. Throughout the Miller platform, V_{DS} rises to the V_{DC} source voltage. I_D remains unchanged.
3. t7→t8: As V_{GS} continues to drop from the Miller platform voltage to V_{MIN}, I_D drops to near-zero amperes in this interval. V_{DS} is clamped to the drain voltage via the body diode inherent in the SiC MOSFET, which also means that the Cgd capacitor is fully charged.
4. t8→t9: I_D and V_{DS} remain unchanged. During the final shutdown interval, the internal input capacitor of the SiC MOSFET will not be fully discharged until V_{GS} drops below 0 V. For C_{iss} to discharge completely, V_{GS} must complete the device shutdown at a negative voltage.

In the turn-on stage, the OSS works by first applying a high V_{GS} to the gate at t0. I_{DS} starts to rise and V_{GS} drops to V_{drop} after the delay time t_{d1}. Then, after the delay time t_{vd1}, the gate obtains a high V_{GS} again. In the turn-off stage, V_{MIN} is kept applied to the gate. After the delay time t_{d2}, the SiC MOSFET starts connecting and V_{GS} rises to 0 V. After t_{vd2}, V_{DS} reaches the peak value, and V_{GS} goes back to V_{MIN}.

As can be seen from Figure 3, T_d, t_{vd}, and V_{drop} are the keys to the OSS control method. Therefore, the OSS can change the switching performance through the control of these three keys and achieve the best switching performance through a variety of combinations. However, this is difficult to perform because of the sheer volume of data. Therefore, it is more time-saving to derive these key values through formulas. These specific formulas have been shown in Article [1], so it will not be discussed in detail in this article. Similarly, due to the limitation of the length of this paper, this paper only explores the influence of different voltage drop delay times (t_d) on the switching performance of the SiC MOSFET module. Therefore, in the next chapter, we will test the optimal voltage drop delay time to verify that the OSS improves the switching performance of the SiC MOSFET.

2.2. The Principles of the Double-Pulse Test

Double-pulse testing (DPT) is a very advanced way of analysing the characteristics MOSFET and diode models. The principle of double-pulse test is to send two pulses to the gate of the SiC MOSFET, and through the control of these two signals, the characteristics of current and voltage can be observed. A DPT circuit is shown in Figure 4.

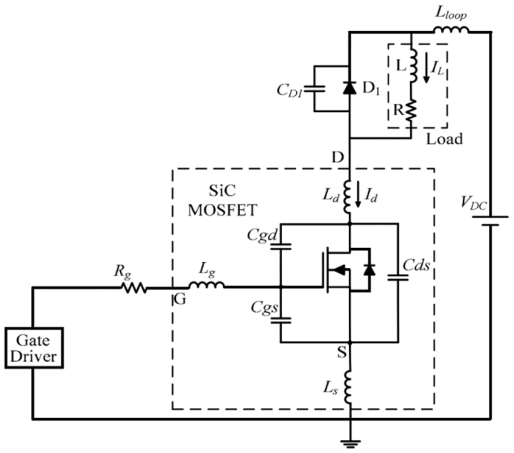


Figure 4. Circuit schematic of the SiC MOSFET under DPT.

In this circuit, the high-side MOSFET always turned off. The body diode of high-side MOSFET is used as a freewheel diode. Meanwhile, the low-side MOSFET works with a double pulse. When the low-side MOSFET turns on, current flows through the Ld and the low-side MOSFET. During this time, the current increases. Therefore, the switching current I_d can be adjusted by changing the gate drive voltage to achieve the purpose of controlling dv/dt and di/dt. In addition, when the low-side MOSFET turns off, the current in the inductor will go through the freewheel diode. In this way, the performance of the MOSFET during the turn-on and turn-off stages can be observed to determine whether the OSS is effective in suppressing overshoot and oscillation of current and voltage.

3. Simulation Verification of the Optimised Switching Strategy

To prove the performance of the OSS, this section will simulate the performance of the OSS with SiC MOSFETs. Infineon's 1.2 kV/250 A SiC MOSFET module (FF6MR12KM1P) is used in this paper. The specific data of the SiC MOSFET are shown in Table 1.

Table 1. Parameters of FF6MR12KM1P (TCJ = 25 °C).

Symbol	Parameter	Value	Unit
C_{iss}	Input capacitance	14.7	nF
V_{GS}	Gate-source voltage	−10/+20	V
C_{oss}	Output capacitance	0.88	nF
V_{TH}	Gate threshold voltage	4.5	V
C_{rss}	Reverse transfer capacitance	0.122	nF
V_{DS}	Drain-source voltage	1200	V
t_r	Rise time	32	ns
t_f	Fall time	45.2	ns
$R_{DS(on)}$	Drain-source on-state resistance	7.56	mΩ
$R_{G(int)}$	Internal gate resistance	1	Ω
I_D	Continuous drain current	250	A
Q_G	Total gate charge	0.496	μC

According to the formula in Article [1] and the data in Table 1, we calculate that the optimisation delay time t_{d1} is 28 ns and t_{d2} is 57 ns. t_{VD1} and t_{VD2} are simulated using the rise time (t_r) and fall time (t_f) in the device data table, respectively.

Simulation Verification and Results

In order to prove the superiority of the OSS in suppressing overshoot and oscillation, simulations are carried out, and the results are compared with the hard switching performance. The software LTspice is used to perform the simulation in the same way as in [1]. The difference is that different SiC MOSFETs are used in this paper. Figure 5 shows the simulation circuit in LTspice.

Because the simulation of the SiC MOSFET is carried out on LTspice, the double-pulse switching signal should be simulated first. The double-pulse switching waveform is shown in Figure 6.

A simulation experiment is very necessary; it can find the hazards and deficiency in the experiment in a timely manner and can be corrected without cost. Just like this study on the OSS, it can be verified on simulation software first and then verified experimentally after determining the superiority of the OSS.

Figure 7 shows the turn-on and turn-off waveforms of the SiC MOSFET under the OSS. The gate driver is −5 V/20 V and the voltage drop is 5 V.

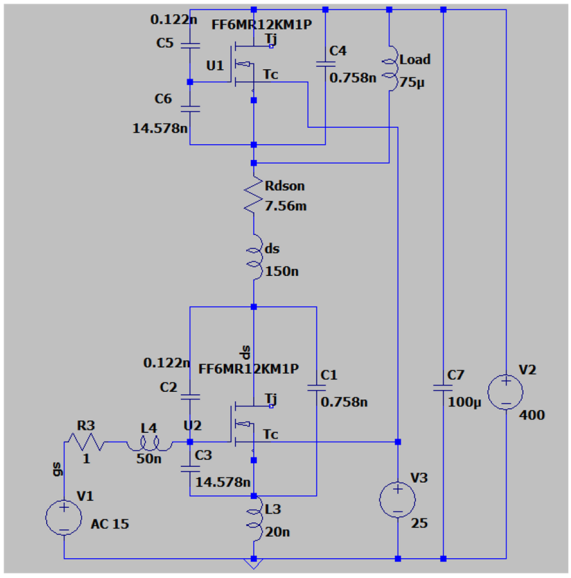


Figure 5. Simulation circuit in Ltspice.

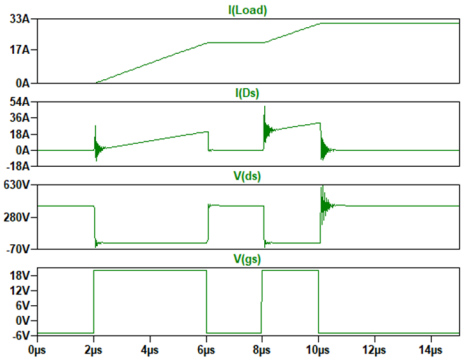


Figure 6. Double−pulse switching for SiC MOSFET.

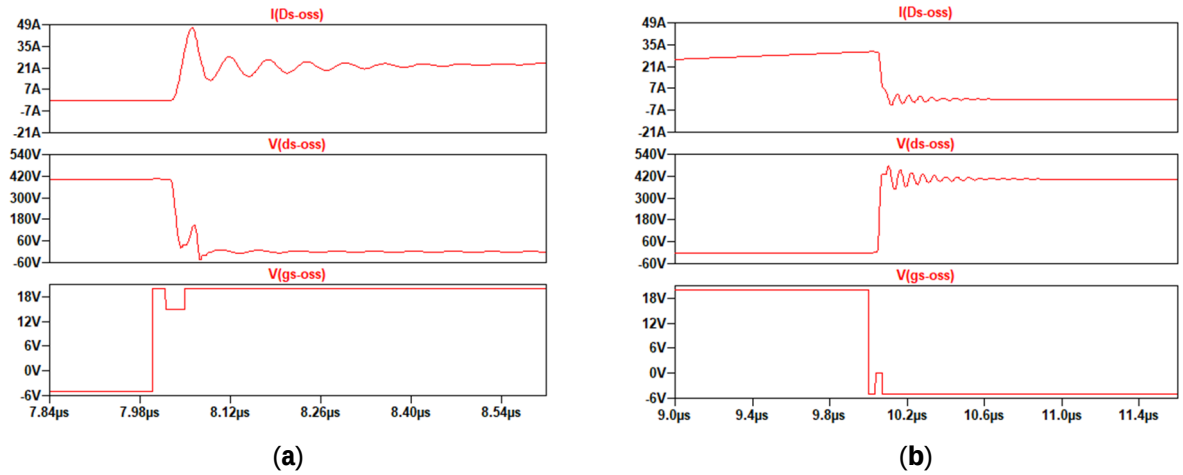


Figure 7. Waveforms of the SiC MOSFET under the OSS. (**a**) Turn−on stage; (**b**) turn−off stage.

As can be seen from Figure 7a, when the turn-on signal appears, a high V_{GS} (20 V) is applied to the gate. After the delay time t_{d1} (calculated as 28 ns), I_{DS} begins to rise and V_{GS} drops to 15 V. After the voltage drop time t_{vd1} (32 ns), the high V_{GS} (20 V) goes back to SiC MOSFET. Figure 7b shows that the device first discharges at −5 V during the shutdown phase. After the t_{d2} (calculated as 57 ns), V_{DS} begins to rise from 0 and V_{GS} rises to 0 V. After t_{vd2} (45 ns), V_{DS} reaches a peak value, and V_{GG} (−5 V) is charged again.

To show the performance of the OSS in suppressing overshoot and oscillation during SiC MOSFET switching, the simulation waveform of the OSS is compared with hard switching.

Figure 8a shows that both the peak value and oscillation of I_{DS} decrease significantly in the turn-on stage. Although V_{DS} has a larger bulge, which may increase the power losses, and unlike the turn-on stage, Figure 8b shows that the OSS successfully reduces oscillations and overshoots in the turn-off stage.

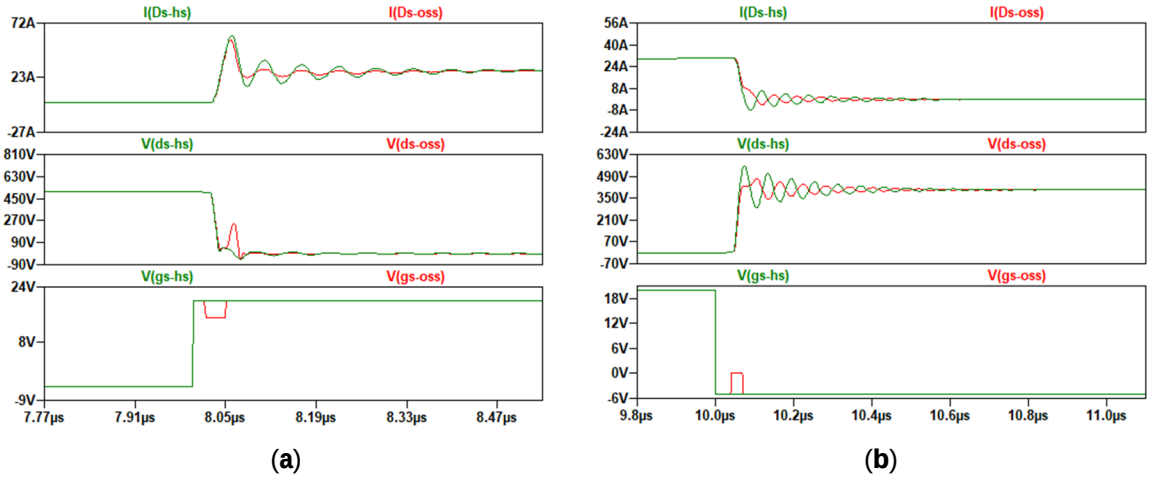


Figure 8. Switching performance comparison between the Hard Switching Strategy and the OSS. (**a**) Turn−on stage, (**b**) turn−off stage.

Combined with the turn-on stage and turn-off stage, it can be clearly seen that the OSS effectively reduces the overshoot and oscillation in the SiC MOSFET switching.

4. Experimental Verification of the Optimised Switching Strategy

In order to verify the feasibility of the OSS, experimental verification is carried out in this section. As shown in Figure 9, a double-pulse test circuit was constructed for the experiment. The DC bus voltage is 400 V, and the switching load current is 30 A.

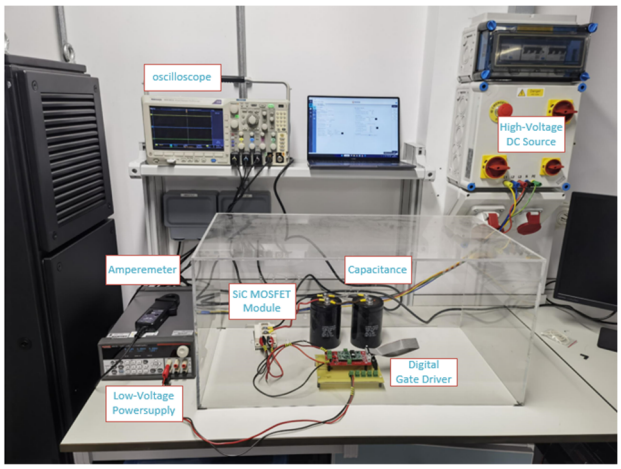


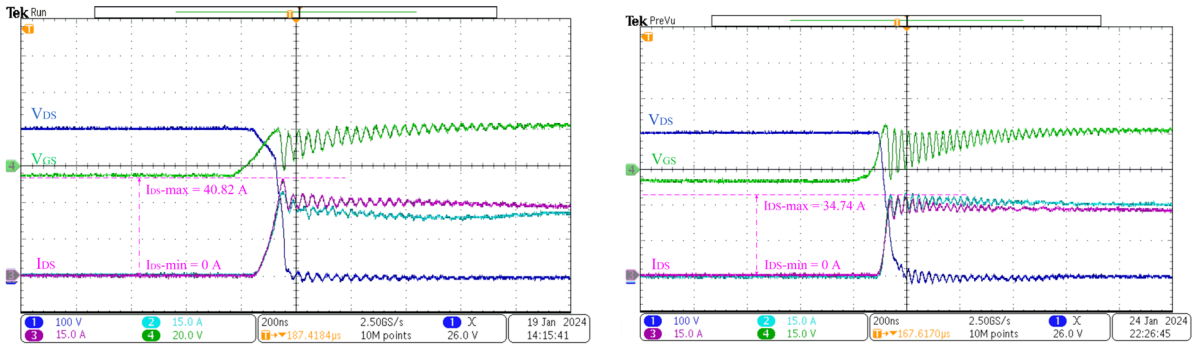
Figure 9. Photos of experimental equipment.

An Infineon 1.2 kV/250 A SiC MOSFET module (FF6MR12KM1P) is connected to an SP6CA1-1200V SP6LI Core Adapter Board. The SP6CA1 board carries a 2ASC-12A1HP SiC Driver Core, which forms a SiC MOSFET gate driver controller. Two capacitors are positioned in parallel between the DC-link and SiC MOSFET module; their role is to charge from the DC-link and then discharge to the SiC MOSFET to ensure the safety of experimental instruments and personnel. The power supply is responsible for supplying

power to the SP6CA1 and ensuring that the controller is operating at the rated voltage. The Tektronix MDO 3014 oscilloscope is used with the following probes: CP35 is used for I_{DS}, Tektronix TPP0250 for V_{GS}, and p5202A for VGS.

4.1. Turn-On Stage

Figure 10 shows a comparison of the SiC MOSFET between the OSS and HS during the turn-on stage.



(**a**) (**b**)

Figure 10. Turn-on switching performance comparison of SiC MOSFET. (**a**) HS. (**b**) OSS.

In Figure 10, the overshoot of I_D in the OSS is lower than that in HS. Meanwhile, the oscillation of V_{GS}, I_D, and V_{DS} in the OSS is smaller than that of HS.

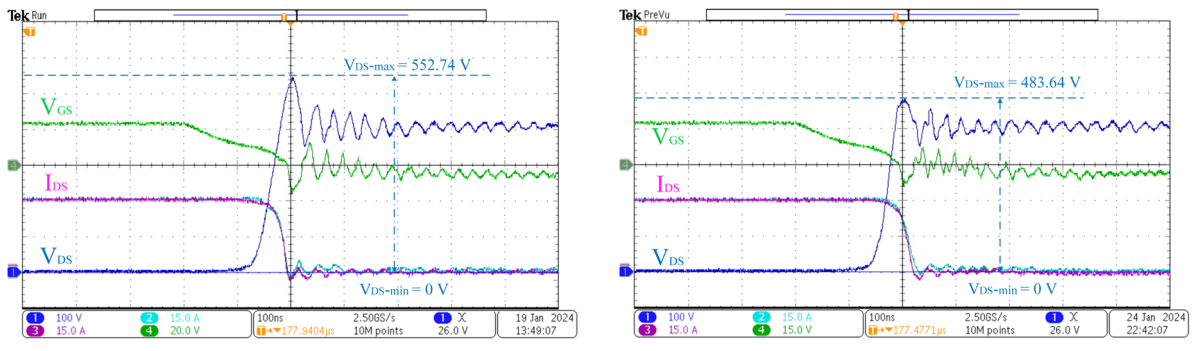
The SiC is shown in Table 2 and Figure 10. When the SiC MOSFETs are turned on, the use of the OSS can significantly reduce the peak and overshoot of the current. The peak current is reduced from 40.82 A in hard switching to 34.74 A in the OSS. It is a direct reduction of 6.08 A. As a result, the current overshot during the entire shutdown process is also reduced from 36.07% to 15.80%. It shows that the OSS can improve the switching performance of SiC MOSFET and reduce energy losses during the turn-on stage.

Table 2. The current peak value and overshoot during turn-on stage.

Unit	Rated Value	Peak Value	Overshoot (%)
I_{DS}(OSS)	30 A	34.74 A	15.80%
I_{DS}(HS)	30 A	40.82 A	36.07%

4.2. Turn-Off Stage

Figure 11 shows the waveforms of the SiC MOSFET during the turn-off stage.



(**a**) (**b**)

Figure 11. Turn-off performance comparison of SiC MOSFET. (**a**) HS. (**b**) OSS.

As regards Figure 11, it is worth mentioning that with the help of the OSS, the overshoot of V_{DS} has been significantly reduced compared with HS. The lower impulse of ids does not change much, because its waveform does not oscillate much in HS, so it cannot be compared to the OSS directly through the graph. The amplitude of oscillation of the voltage waveform is also slightly smaller. Interestingly, under the influence of the OSS, the waveforms of both V_{DS} and V_{GS} begin to become less rounded. In general, the effect of the OSS effectively reduces voltage oscillation and overshoot. Table 3 shows the specific data of overshoot during the shutdown process.

Table 3. The peak value and overshoot of the voltage during the turn-off stage.

Unit	Rated Value	Peak Value	Overshoot (%)
V_{DS}(OSS)	400 V	483.64 V	20.91%
V_{DS}(HS)	400 V	552.74 V	38.19%

As can be seen from Table 3 and Figure 11, when the SiC MOSFETs are turned off, the use of the OSS can significantly reduce the voltage peak and overshoot. The peak voltage data are reduced from 552.74 V in hard switching to 483.64 V in the OSS: a direct reduction of 69.1 V. As a result, the voltage overshoot during the entire shutdown process was reduced from 38.19% to 20.91%. The OSS can improve the performance of SiC MOSFET and reduce energy losses during the turn-off stage.

The experimental verification and analysis of the SiC MOSFET in the process have proved that the performance of the SiC MOSFET has been improved under the support of the OSS. The current overshoot and oscillation of the entire device are effectively suppressed in the turn-on stage, the peak current is reduced from 40.82 A to 34.74 A, and the current overshoot is reduced from 36.07% to 15.80%. Similarly, in the turn-off stage, the voltage overshoot and oscillation are also effectively suppressed, the peak voltage is reduced from 552.74 V to 483.64 V, and the voltage overshoot is reduced from 38.19% to 20.91%. Combining the two processes can be equivalent to a complete switching process, and using the OSS can effectively improve the switching performance of the SiC MOSFET.

5. Discussion and Conclusions

In this paper, the principle of overshoot and oscillation of current and voltage in the high-speed switching of SiC MOSFET are studied. The feasibility of an optimised switching strategy (OSS) is also verified. The simulation and experimental results show that the OSS can reduce current overshoot and voltage overshoot by optimising the voltage drop delay time for the turn-on and turn-off stages. In addition, the turn-on current overshoot is reduced by 14% and the turn-off voltage overshoot is reduced by 18.03% compared to the hard switch. This shows that the OSS implements a more comprehensive control strategy and demonstrates better switching performance. Therefore, the OSS proves its superior performance while being more flexible than traditional AGDs.

However, due to the limitations of laboratory equipment, their own level, research time, and other conditions, there are still some problems. First of all, the OSS is only verified in the aspect of controlling the voltage drop delay time and cannot fully reflect the superior performance of the OSS. Secondly, the feasibility and effectiveness of the dv/dt control strategy of the SiC MOSFET proposed in this paper have been verified only in the circuit with only one power MOSFET, and usually many circuits such as DAB, H-bridge, and other circuits have at least four power MOSFETs. The current circuit and control hardware support only one power MOSFET, which is still far from practical applications. Finally, the SiC MOSFETs used in this article are not very advanced. At present, some companies have developed newer and more advanced SiC MOSFETs. This new type of SiC MOSFETs also reduces power losses by using new structures. Although the performance improvement in the OSS for new SiC MOSFETs may be slightly reduced, it can be proven that the OSS can still improve the switching performance of all SiC MOSFETs and even all semiconductors.

The next step is to apply the OSS to more different types of semiconductor devices for feasibility testing and then optimise the OSS algorithm and control method based on the actual test results.

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