

Article

Three-Level Double LLC Resonant Converter with Ripple-Free Input Current for DC Microgrid Application

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Abstract: DC distribution systems have garnered interest in recent years due to their advantages over AC distribution systems, such as their high power conversion efficiency and lack of harmonic issues. An isolated DC-DC converter with low-input noise, high efficiency, and high-power density is required for DC microgrids within DC distribution systems. Although existing DC to DC converters have high efficiency and high power density, they still have input noise problems due to pulsating input currents. Thus, a large input filter should be inserted, which increases the cost and degrades the power density. In this study, a novel three-level double LLC resonant converter with zero-input-current ripple is presented for DC microgrid application with a high-voltage DC bus. The input-current ripple of the proposed converter theoretically decreases to zero without adding large input filters. Moreover, the voltage stress on each main switch is only half of the input voltage when using the modified three-level structure, which enables the use of low-voltage-rated power switches for high-voltage input applications. In addition, all the primary switches and secondary diodes are softly switched over a wide input voltage range. The experimental results of the prototype are presented to verify the performance of the proposed converter.

Keywords: zero-input-current ripple; three level; DC-DC conversion; low-voltage stress; LLC resonant; high efficiency; high-voltage input; DC distribution systems; DC microgrid



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1. Introduction

Recently, with the rapid growth of renewable energy systems and electric vehicles, research on DC distribution systems has been actively carried out due to their advantages over AC distribution systems, such as their high power conversion efficiency and lack of harmonic issues [1–6]. In addition, DC microgrids are considered to be the most viable solution for integrating renewable energy systems and energy storage systems, with DC loads such as electric vehicles and DC home appliances. Figure 1 shows a DC microgrid with DC distribution systems. To convert the high-voltage (HV) DC bus input to a low-voltage output for DC loads, an isolated DC-DC converter is required with the characteristics of low-input noise, high efficiency, and high power density. Half-bridge LLC resonant converters are popularly employed for DC loads in DC microgrids [7–11] because the main switches and rectifier diodes can be operated under zero-voltage switching (ZVS) and zero-current switching (ZCS) conditions over a wide input voltage range, respectively, which enables high efficiency to be achieved. For DC loads in DC microgrids with a higher DC bus voltage, three-level (TL) LLC resonant converters can be used. A fixed-frequency-controlled hybrid full-bridge (HFB) TL LLC resonant converter was introduced in [12]. All of the main switches were softly switched, and the voltage stress on each primary switch was half the input voltage. However, its efficiency was lower than that of variable-frequency-controlled LLC resonant converters. Another TL LLC resonant converter [13] was presented. Its output voltage regulation was achieved by pulse frequency modulation (PFM), which improved the efficiency of the TL LLC converter with fixed-frequency control [12]. However, to ensure that the voltage stress on each switch was maintained at half the input

voltage, dead-time zones were additionally required in their driving signals, which made the driving circuits more complex. In [14], a TL double LLC (DLLC) resonant converter was proposed, which improved the complexity of the driving circuit. Moreover, it has constant high efficiency and a soft-switching ability over a wide input voltage range. However, in terms of the input-current ripple, all circuit topologies mentioned above are buck-derived topologies with a discontinuous input current, causing di/dt noise on the input side. Thus, a large input filter should be inserted, which increases the cost and degrades power density.

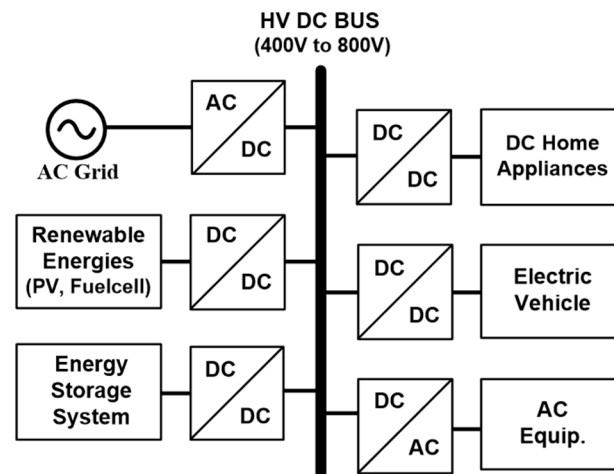


Figure 1. Configuration of DC microgrid within DC distribution systems.

To minimize the input-current ripple, firstly, current-fed converters with a continuous input current [15–18] can be considered, but because most of them are boost topologies, they are not suitable for applications with high inputs and low outputs, unlike those with step-down buck-derived topologies. As another solution, a half-bridge converter with input-current-ripple reduction (HBC-CRR) [19] was presented. Although it is a buck-derived topology, its input-current ripple is reduced substantially by using two split windings and a clamp capacitor. However, its primary switches and secondary diodes operate under hard-switching conditions, and its secondary diodes have high-voltage stress during small-duty operation, increasing power losses. In [20], a novel high-efficiency LLC resonant converter was proposed, which improved the drawbacks of hard-switching operation and high-voltage stress on the secondary diodes in [19]. However, for higher-voltage input applications, all the primary switches suffer from high-voltage stress, resulting in high cost and poor efficiency.

In this paper, a novel high-efficiency TL double LLC resonant converter with zero input-current ripple and low-voltage stress is presented for high-voltage input applications. The input noise components, due to input current pulsation, are significantly reduced without the addition of bulky input filters. Moreover, the voltage across each primary switch is clamped to half the input voltage, which allows the use of low-voltage-rated power switches for high-voltage input applications. In addition, all primary switches and secondary diodes operate with ZVS turn-on and ZCS turn-off over a wide input voltage range, which enables high efficiency to be achieved.

2. Proposed TL Double LLC Resonant DC-DC Converter

2.1. Circuit Description

The circuit diagram of the proposed resonant converter is shown in Figure 2. It is a three-level double LLC resonant tank converter based on a structure that combines two LLC resonant converters in series with clamp capacitors. (S_1, S_3) and (S_2, S_4) are treated as two switch pairs. The gate signals for each switch pair, which are 180° out of phase, are driven at a constant duty cycle of 0.5, with pulse frequency modulation (PFM) control. Thus, in a series-interleaved double LLC resonant structure, the input-current ripple with

a phase difference of 180° is canceled out and theoretically becomes zero regardless of the input voltage and load variations. Moreover, because it is a three-level topology with double LLC resonant tanks, the voltage across each primary switch is maintained at half the input voltage, and all primary switches and secondary diodes operate in ZVS turn-on and ZCS turn-off, respectively, over a wide input voltage range, reducing the switching loss. In addition, there are almost no voltage spikes across the primary switches after they are turned off, since the inductance energy of the resonant inductors and transformer magnetizing inductances is absorbed by the clamp capacitors. As a result, no snubber is required, and switching losses are improved.

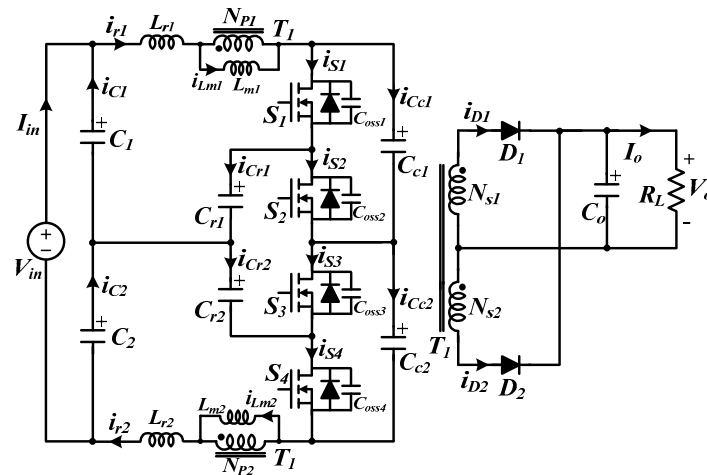


Figure 2. Circuit diagram of proposed resonant converter.

To simplify the analysis, several assumptions are made:

- The output capacitor C_o is large enough that the output voltage V_o and output current I_o can be considered constant during a switching period T_s .
- The capacitances of the clamp capacitors C_{c1} and C_{c2} are sufficiently large; therefore, the voltage of the clamp capacitors can be assumed to be constant. They are equal to C_c .
- The input capacitors C_1 and C_2 are equal to C .
- The resonant capacitors C_{r1} and C_{r2} are equal to C_r .
- The resonant inductors L_{r1} and L_{r2} are equal to L_r .
- The parasitic output capacitances of the four primary switches are equal to C_{oss} and treated as constant values during the dead-time period.
- The main transformer has windings: $N_{p1} = N_{p2} = N_p$; a turn ratio: $n = N_p/N_s$; and a magnetizing inductance: $L_{m1} = L_{m2} = L_m$.

2.2. Operation Principle

Figures 3 and 4 show the key waveforms and operation modes of the proposed resonant converter, respectively. The resonant inductances (L_{r1} and L_{r2}), transformer magnetizing inductances (L_{m1} and L_{m2}), resonant capacitors (C_{r1} and C_{r2}), and switch output capacitors (C_{oss}) are assumed to be identical to each other. Since double LLC resonant tanks are connected in parallel, when one switch operates, the two LLC resonant tanks are involved in the operation at the same time. The clamp capacitors (C_{c1} and C_{c2}) are charged with the same voltage, as $V_{in}/2$, and act as another voltage source. Prior to t_0 , all secondary diodes are in their off-state, and the output is separated from the primary side. L_r and L_m resonate with C_r , and i_{Lr1} and i_{Lr2} are equal to $i_{Lm1} = -I_{m1}$ and $i_{Lm2} = I_{m2}$, respectively, where I_{m1} and I_{m2} are the peak currents of the magnetizing inductance.

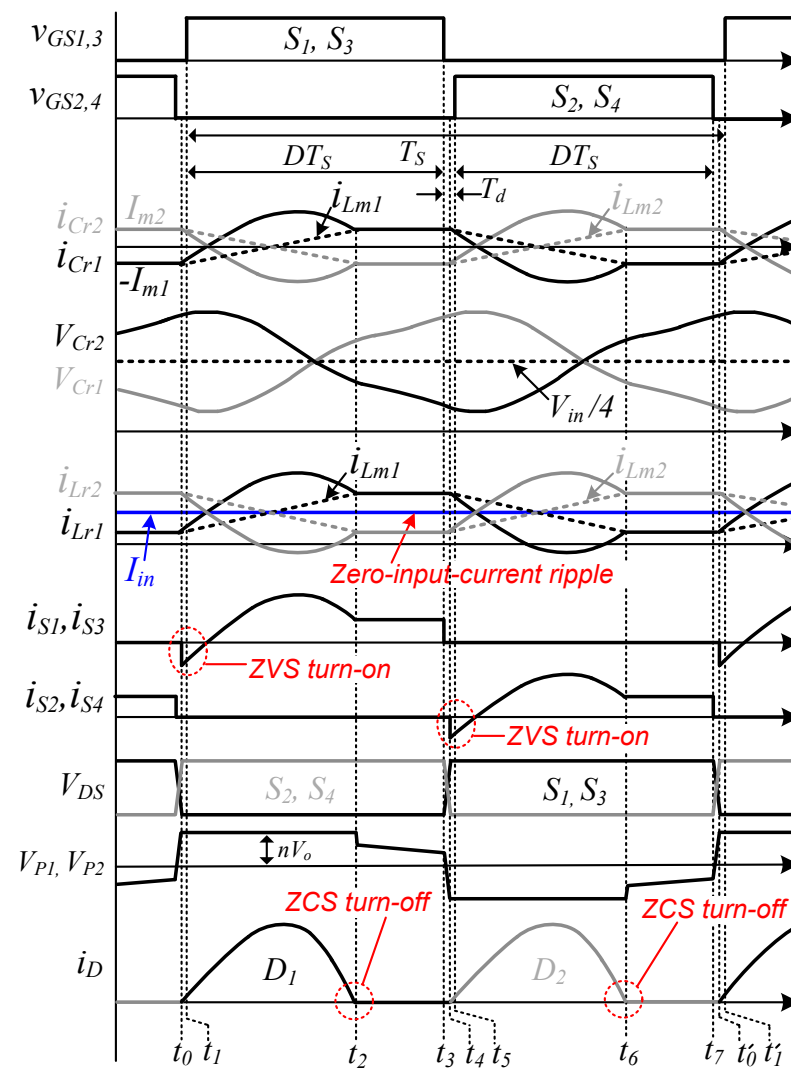


Figure 3. Key waveforms of the proposed resonant converter.

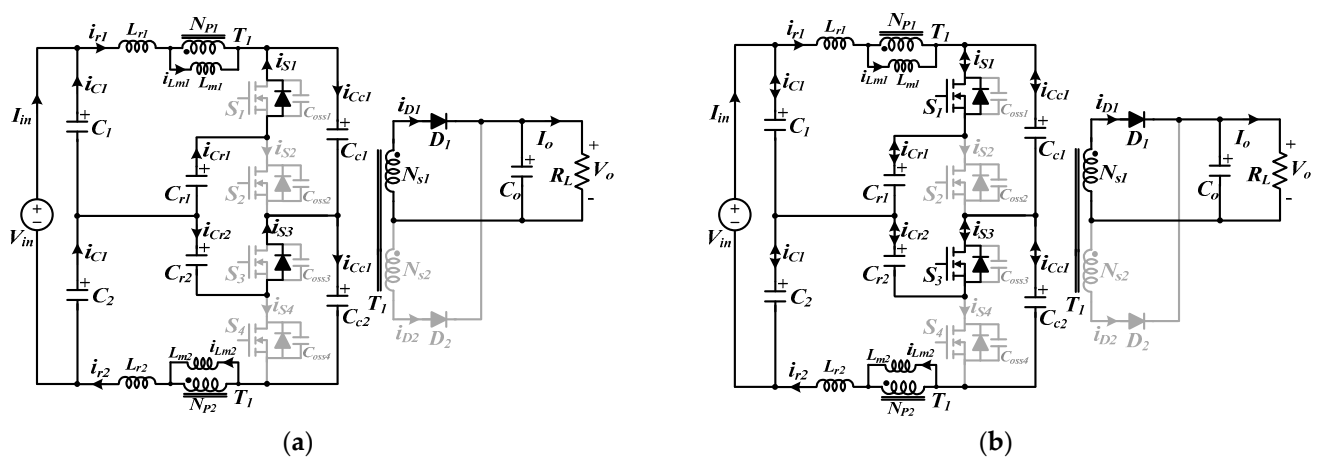


Figure 4. Cont.

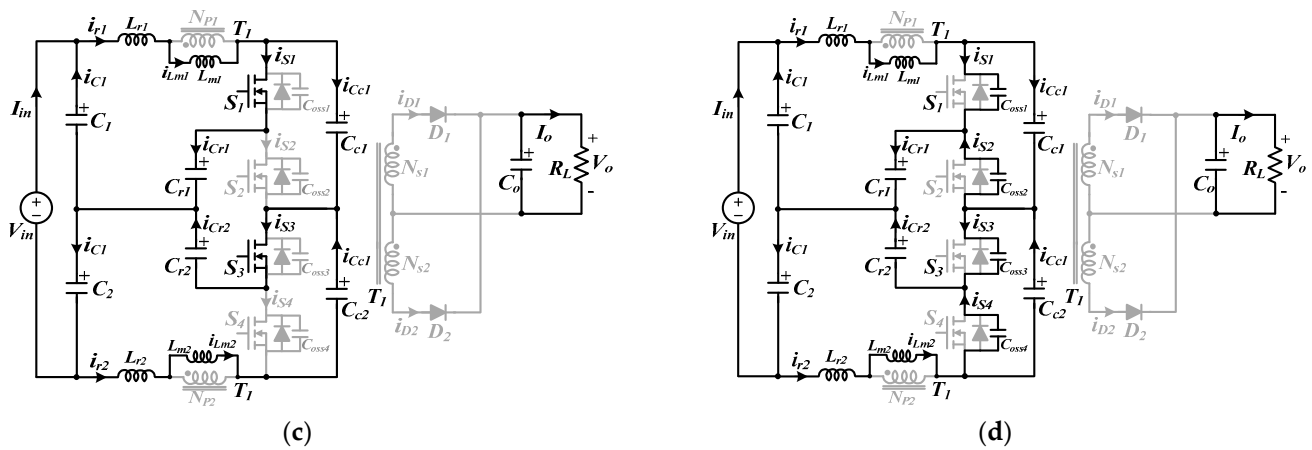


Figure 4. Operation modes of the proposed converter in half cycle. (a) Mode 1, (b) Mode 2, (c) Mode 3, and (d) Mode 4.

(1) Mode 1 $[t_0, t_1]$: Mode 1 begins when the C_{oss} of S_1/S_3 and S_2/S_4 is completely discharged and charged, respectively, and the body diodes of S_1 and S_3 start to conduct at t_0 . D_1 begins conducting. The primary voltages of the transformers V_{P1} and V_{P2} are clamped by the reflected voltage nV_o . The $i_{Lm1}(t)$ and $i_{Lm2}(t)$ are linearly increased and decreased by nV_o , respectively. A difference of half the input voltage $V_{in}/2$ and the reflected voltage nV_o is applied to each resonant tank, and L_r and C_r begin to resonate. At this stage, input power is transferred to the output. The currents in the resonant inductor and the magnetizing inductance of the transformer can be written as follows:

$$\begin{aligned} i_{Lr1}(t) &= I_{in} + i_{Cr1}(t) \\ &= I_{in} - I_{m1} \cos \omega_{r1}(t - t_0) + \left(\frac{1}{2} V_{in} - nV_o - V_{Cr1}(t_0) \right) / Z_{r1} \sin \omega_{r1}(t - t_0) \end{aligned} \quad (1)$$

$$\begin{aligned} i_{Lr2}(t) &= I_{in} - i_{Cr2}(t) \\ &= I_{in} + I_{m2} \cos \omega_{r1}(t - t_0) + (nV_o + V_{Cr2}(t_0)) / Z_{r1} \sin \omega_{r1}(t - t_0) \end{aligned} \quad (2)$$

$$i_{Lm1}(t) = -I_{m1} + nV_o / L_{m1}(t - t_0) \quad (3)$$

$$i_{Lm2}(t) = I_{m2} - nV_o / L_{m2}(t - t_0) \quad (4)$$

$$V_{C1} = V_{C2} = V_{Cc1} = V_{Cc2} = V_{in}/2 \quad (5)$$

where V_{in} is the input DC voltage, and the angular frequency ω_{r1} and characteristic impedance Z_{r1} are given by

$$\omega_{r1} = 2\pi f_{r1} = \frac{1}{\sqrt{L_r C_r}}, \quad Z_{r1} = \sqrt{\frac{L_r}{C_r}} \quad (6)$$

(2) Mode 2 $[t_1, t_2]$: At time t_1 , S_1 and S_3 are turned on under the ZVS conditions. In this mode, the equations of the voltages and currents are the same as those of Mode 1.

(3) Mode 3 $[t_2, t_3]$: Because the resonance formed with C_{r1}/L_{r1} and C_{r2}/L_{r2} ends at time t_2 , D_1 is turned off under the ZCS condition, which eliminates its reverse-recovery problems. L_{m1} and L_{m2} participate in the resonances. All secondary diodes are turned off, and the output side is disconnected from the primary side. In this mode, C_o only supplies power to the load. This mode can be achieved by eliminating the reflected voltage nV_o . The currents of the resonant inductor and transformer magnetizing inductance can be expressed as

$$\begin{aligned} i_{Lr1}(t) &= i_{Lm1}(t) = I_{in} + i_{Cr1}(t) \\ &= I_{in} + i_{Cr1}(t_2) \cos \omega_{r2}(t - t_2) + \left(\frac{1}{2} V_{in} - V_{Cr1}(t_2) \right) / Z_{r2} \sin \omega_{r2}(t - t_2) \end{aligned} \quad (7)$$

$$\begin{aligned} i_{Lr2}(t) &= i_{Lm2}(t) = I_{in} - i_{Cr2}(t) \\ &= I_{in} - i_{Lr2}(t_2) \cos \omega_{r2}(t - t_2) + V_{Cr2}(t_2) / Z_{r2} \sin \omega_{r2}(t - t_2) \end{aligned} \quad (8)$$

where

$$\omega_{r2} = \frac{1}{\sqrt{(L_r + L_m)C_r}}, \quad z_{r2} = \sqrt{\frac{(L_r + L_m)}{C_r}} \quad (9)$$

(4) Mode 4 [t_3, t_4]: S_1 and S_3 are turned off and the converter enters a dead-time period at time t_3 . During this time, the C_{oss} of S_2 and S_4 is discharged, and the voltage across switches S_2 and S_4 is linearly decreased to half the input voltage. The C_{oss} of S_1 and S_3 is charged, and the voltage across S_1 and S_3 is linearly increased from zero.

3. Steady-State Analysis

3.1. DC Voltage Gain

The fundamental harmonic approximation (FHA) method [7,9,10] has been used to analyze the voltage gain of the proposed resonant converter. The equivalent circuits for the proposed converter are derived as shown in Figure 5. Considering double LLC resonant tanks in parallel, the AC equivalent load resistance R_{ac} , the input voltage $V_{i,1}$, and the output voltage $V_{o,1}$ within the fundamental components of the resonant tanks can be obtained as follows:

$$R_{ac} = \frac{16n^2 R_L}{\pi^2} \quad (10)$$

$$V_{i,1}(t) = \frac{V_{in}}{\pi} \sin 2\pi f_s t \quad (11)$$

$$V_{o,1}(t) = \frac{4nV_o}{\pi} \sin 2\pi f_s t \quad (12)$$

The DC voltage gain M of the proposed double LLC tank converter can be expressed as

$$\begin{aligned} M &= \frac{V_{o,1}(t)}{V_{i,1}(t)} = \frac{nV_o}{V_{in}/4} = \frac{Z_p}{Z_s + Z_p} \\ &= \frac{1}{\sqrt{\left(1 + \frac{1}{2L_n} \left(1 - \frac{1}{f_n^2}\right)\right)^2 + Q^2 \left(f_n - \frac{1}{f_n}\right)^2}} \end{aligned} \quad (13)$$

where the inductor ratio L_n , quality factor Q , and normalized switching frequency f_n can be expressed as

$$L_n = \frac{L_m}{L_r}, \quad Q = \frac{1}{R_{ac}} \sqrt{\frac{L_r}{C_r}}, \quad f_n = \frac{f_s}{f_r} \quad (14)$$

where f_s is the switching frequency and $f_r = 1/2\pi\sqrt{L_r C_r}$ is the resonant frequency.

The curves of the DC voltage gain against the normalized frequency (f_n) at different Q values and with $L_n = 3.5$ are shown in Figure 6, which is based on the experimental parameters. To ensure the ZVS operation of the proposed converter, it must be operated in the negative slope region of the voltage gain curves. The proposed converter has unity gain when the switching frequency is equal to the resonant frequency. The voltage gain increases when the switching frequency is lower than the resonant frequency. As can be seen from the graph, when the input voltage decreases from 400 V to 300 V, the switching frequency is lowered from 195 kHz ($f_n = 1$) to 110 kHz ($f_n = 0.57$) to achieve a voltage gain of 1.28. As a result, the output voltage is maintained at a constant voltage (48 V) without being lowered.

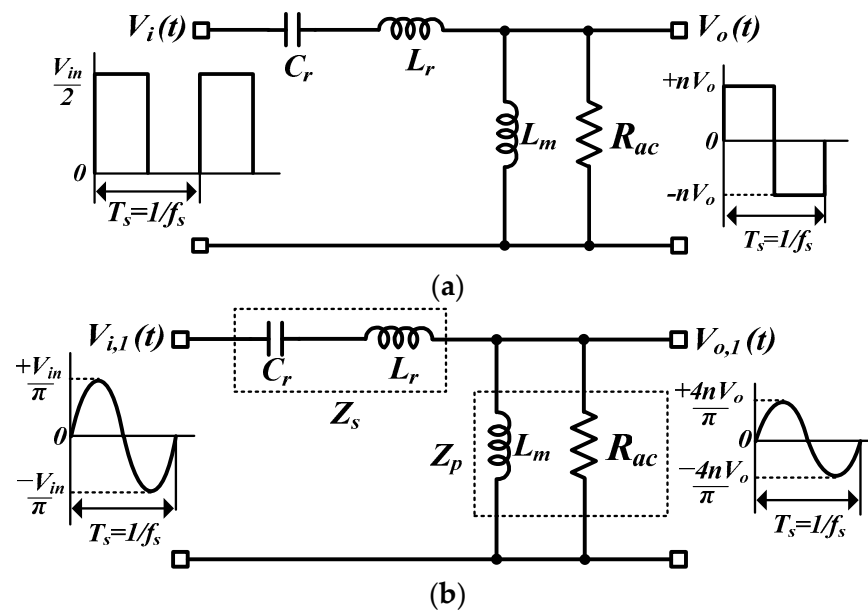


Figure 5. Equivalent circuits of the proposed resonant converter. (a) AC equivalent circuit, (b) simplified equivalent circuit for FHA.

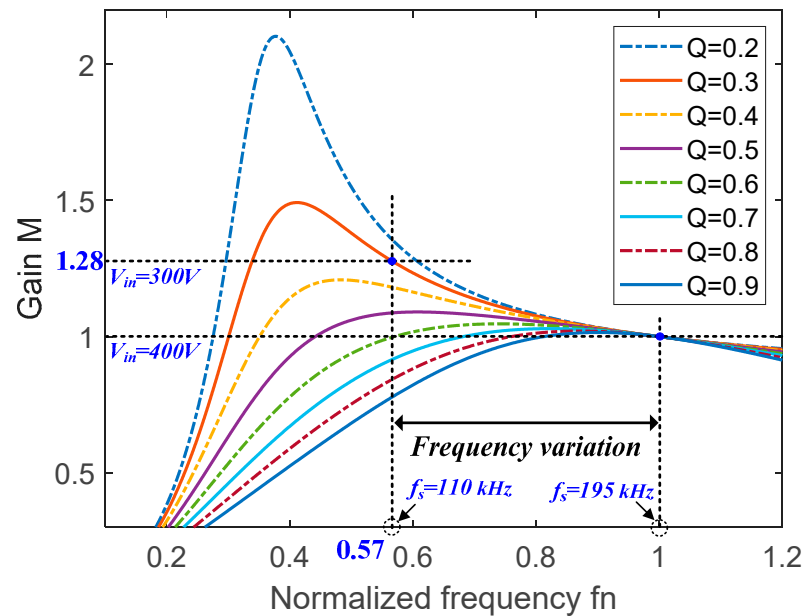


Figure 6. The normalized DC voltage gain curves at different Q values with $L_n = 3.5$.

3.2. Input-Current Ripple

Figure 7 illustrates that the input-current ripple is caused by the difference between i_{Lr1} and i_{Lr2} when the L and C values of the resonance tanks are mismatched. In the proposed converter, if the waveforms of the resonant inductor currents i_{Lr1} and i_{Lr2} are the same, the input-current ripple theoretically becomes zero. To analyze the input-current ripple caused by the mismatched resonant elements, it is assumed that the two magnetizing inductances are equal, and the resonant capacitors and inductors are as follows:

$$C_{r1} = C_r, C_{r2} = (1 + a)C_r, L_{r1} = L_r, L_{r2} = (1 + b)L_r \quad (15)$$

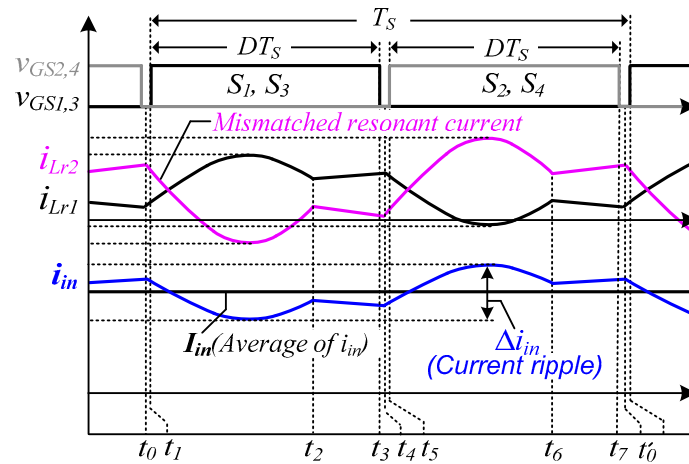


Figure 7. Input-current ripple caused by the tolerances of the resonant elements.

The resonant inductor currents can be obtained as follows:

$$i_{Lr1}(t) = I_{in} + d_1 \sin(\omega_{r1}(t - t_0)) + d_2 \cos(\omega_{r1}(t - t_0)) \quad (16)$$

$$i_{Lr2}(t) = I_{in} - d_3 \sin(e\omega_{r1}(t - t_0)) - d_4 \cos(e\omega_{r1}(t - t_0)) \quad (17)$$

where

$$\begin{aligned} d_1 &= i_{Cr1}(t_0), \quad d_2 = \frac{V_{in}/2 - nV_o - V_{Cr1}(t_0)}{Z_{r1}} \\ d_3 &= i_{Cr2}(t_0), \quad d_4 = \frac{-(nV_o + V_{Cr2}(t_0))}{Z_{r1} \sqrt{\frac{(1+b)}{(1+a)}}} \\ e &= \frac{1}{\sqrt{(1+a)(1+b)}} \end{aligned} \quad (18)$$

From (16) and (17), the input-current ripple Δi_{in} can be obtained as follows:

$$\begin{aligned} \Delta i_{in} &= [i_{Lr1}(t) + i_{Lr2}(t)]/2 - I_{in} \\ &= [d_1 \sin(\omega_{r1}(t - t_0)) + d_2 \cos(\omega_{r1}(t - t_0)) \\ &\quad - d_3 \sin(e\omega_{r1}(t - t_0)) - d_4 \cos(e\omega_{r1}(t - t_0))] \end{aligned} \quad (19)$$

From (19), it can be observed that if the tolerances a and b of C_r and L_r are within the $\pm 2\%$, $\pm 5\%$, and $\pm 10\%$ range, respectively, the input-current ripple occurs within approximately 10%, 20%, and 35%, respectively.

3.3. Comparison of Converter Circuit Topologies

A comparison of the proposed topology with other different topologies has been performed mainly in terms of the input-current ripple. The comparative results are presented in Table 1. The series resonant LC-DAB converter [21], using simple fixed-frequency modulation (FFM), can operate with ZVS and ZCS in a wide operating range, but it requires additional switches on its secondary side. In addition, TL LLC resonant converters [12–14] have the advantages of a soft-switching operation over a wide input voltage range and low-voltage stress on their switches. However, all circuit topologies mentioned above are buck-derived topologies with discontinuous input currents, which causes di/dt noise on the input side. On the other hand, although the proposed topology and HBC-CRR [19] are buck-derived converters, they have a continuous input current with low current ripple. However, the primary switches and secondary diodes in [19] operate under hard-switching conditions. In addition, for higher-voltage input applications, all the primary switches suffer from high-voltage stress. In contrast, the proposed converter improves the drawbacks of the hard-switching operation and high-voltage stress on the switches in [19].

Table 1. Comparison of the proposed topology with other topologies.

Parameters	HBC-CRR [19]	LC-DAB [21]	HFB-TL-LLC [12]	TL-LLC [13]	TL-DLLC [14]	Proposed Topology
Continuous input current	Yes	No	No	No	No	Yes
Input-current ripple	Low	High	High	High	High	Very low
Input voltage range (V)	360–400	80	200–400	500–700	400–600	300–400
Output voltage (V)	12	50–160	360	54	48	48
Output power (W)	240	1500	1440	540	480	240
Modulation method	PWM	FFM	PS-PWM	PFM	PFM	PFM
Soft-switching capability	No	Yes	Yes	Yes	Yes	Yes
Number of switches	2	8	6	4	4	4

PS: phase shift; DAB: dual active converter; PWM: pulse-width modulation; FFM: fixed-frequency modulation.

4. Design Considerations

This section illustrates an example of the design of the proposed resonant converter, and particularly the design of the double LLC resonant tanks, which is based on the design specifications listed in Table 2.

Table 2. Design specifications.

Items	Values
Input voltage range (V_{in})	300 V–400 V
Output voltage (V_o)	48 V
Output power (P_o)	240 W
Resonant frequency (f_r)	195 kHz
Switching frequency range	110 kHz–195 kHz

4.1. Transformer Turn Ratio

The proposed converter has unity gain at the maximum input voltage $V_{in(max)}$, and its switching frequency is equal to the resonant frequency in the unity gain. The turn ratio of the transformer n can be obtained using Equation (13):

$$n = \frac{M_{V_{in(max)}} V_{in(max)}}{4V_o} = 2.08 \quad (20)$$

Thus, the transformer turn ratio n is approximately 2. Considering the magnetic core characteristics and turn ratio of the transformer, the number of turns in the primary and secondary windings of the transformer is selected to be 12 and 6, respectively.

4.2. Quality Factor

To simplify the design of the double LLC resonant tanks, L_n is selected to be 3.5. The available Q values are then limited to 0.53 to meet the condition of $\sqrt{L_n} Q \leq 1$. As shown in Figure 6, the DC voltage gain M at $L_n = 3.5$ can be plotted based on these results. The DC voltage gain of the resonant tanks required to regulate the output voltage at the minimum input voltage $V_{in(min)}$ and $n = 2$ is 1.28 according to (13). However, to prevent the converter from entering non-ZVS operation at $V_{in(min)}$ and in the full-load condition, the required maximum gain of the resonant tanks should be sufficiently larger than 1.28. To achieve sufficient gain, the Q value of the resonant tank needs to be smaller, but a smaller Q value leads to higher current stress. Therefore, considering the sufficient gain and appropriate current stress of the resonant tanks, Q is selected to be 0.3.

4.3. Resonant Capacitor

The AC equivalent load R_{ac} in the full-load condition is calculated as follows:

$$R_{ac} = \frac{16n^2 R_L}{\pi^2} \approx 62.25 \, \Omega \quad (21)$$

According to (14) and (21), the resonant capacitance can be obtained as

$$C_r = \frac{1}{2\pi R_{ac} Q f_r} \approx 44 \, \text{nF} \quad (22)$$

The maximum voltage of the resonant capacitor is given by

$$V_{Cr(max)} = I_{Cr(pk)} \times X_{Cr} = \frac{I_{Cr(pk)}}{2\pi f_s C_r} \quad (23)$$

where $I_{Cr(pk)}$ denotes the peak current of the resonant capacitor and f_s denotes the switching frequency.

4.4. Resonant Inductor

From (14) and (22), the resonant inductance is obtained as

$$L_r = (R_{ac} Q)^2 C_r \approx 15 \, \mu\text{H} \quad (24)$$

4.5. ZVS Conditions for Switches

The magnetizing inductance of the transformer L_m is 52.5 μH , which can be calculated from $L_m = L_n \cdot L_r$. The maximum magnetizing inductance for the ZVS can be calculated as

$$L_m \leq \frac{\pi \sqrt{L_r C_r} T_d}{4C_{oss}} \times \frac{nV_o}{V_{in}/2} = \frac{T_r T_d}{8 C_{oss}} \quad (25)$$

From (25), the maximum L_m for ZVS operation is about 260 μH . Considering that the magnetizing inductance is 52.5 μH , this is a reasonable value for the given input voltage range. Therefore, the main switches can be operated under ZVS conditions over a wide input voltage range.

5. Simulation and Experimental Results

To verify the performance of the proposed converter, the 240 W prototype shown in Figure 8 has been built and tested. The PFM control of the proposed converter was implemented using a TI TMS320F28069M Digital MCU. The simulation and experimental parameters are listed in Table 3. The input voltage range and the output voltage were 300–400 V and 48 V, respectively. FQPF16N25 (250 V) MOSFETs with Si8261 gate drivers were used as the main switches. Figures 9–11 show the experimental waveforms of the switches and diodes at input voltages of 300 V and 400 V, respectively. The switches and diodes operate with ZVS turn-on and ZCS turn-off, respectively, so no snubber is needed and the switching loss is improved. Moreover, as shown in Figure 10, the maximum switch voltage stress is about 200 V with no voltage spikes, which is half of the input voltage (400 V). This result indicates that the low-voltage-rated switches, 250 V and 500 V MOSFETs, can be used for 400 V and 800 V input applications, respectively. Figure 12a shows the experimental waveforms of the resonant tanks at $V_{in} = 300$ V. The resonant tanks operate well, which is in good agreement with our theoretical analysis. Figure 12b shows that when the values of L_r and C_r are mismatched with tolerances of about 5%, an input-current ripple of about 20% occurs without a pulsating shape, which is almost the same as the values analyzed in Section 3.2. Additionally, spike noises are observed in the input current, which occur due to current changes accompanying the turn-on and turn-off of main switches in current paths with parasitic inductances, especially during

dead time. To reduce spike noise, parasitic inductances must be reduced. The dynamic response of the output voltage to load changes at the input voltages of 300 to 400 V is shown in Figure 13. The corresponding output voltage is well-regulated and stable in the dynamic load condition over a wide input voltage range when the load is changed stepwise from 20% to 100%. Figure 14 illustrates the simulated clamp-capacitor voltage imbalance with an input voltage. The two clamp capacitors are equally charged to half the input voltage if there is no voltage imbalance. The clamp-capacitor voltage imbalance mainly occurs when the resonant currents of the double LLC resonant tanks are imbalanced due to the tolerance of the L_r and C_r values of the resonant tanks, particularly at the minimum input voltage. When L_r and C_r values are mismatched with tolerances of $\pm 10\%$ and $\pm 20\%$, the maximum imbalance of the clamp-capacitor voltage occurs at about 6.6% and 13.3% at the minimum input voltage of 300 V, respectively. However, as the input voltage increases, the capacitor voltage imbalance decreases. The measured efficiency under different load conditions, with an input voltage of 300–400 V, is shown in Figure 15. A maximum efficiency of 94.63% is measured at a 400 V input and under full load conditions. As the input voltage decreases, the efficiency decreases, mainly because the circulating current increases.

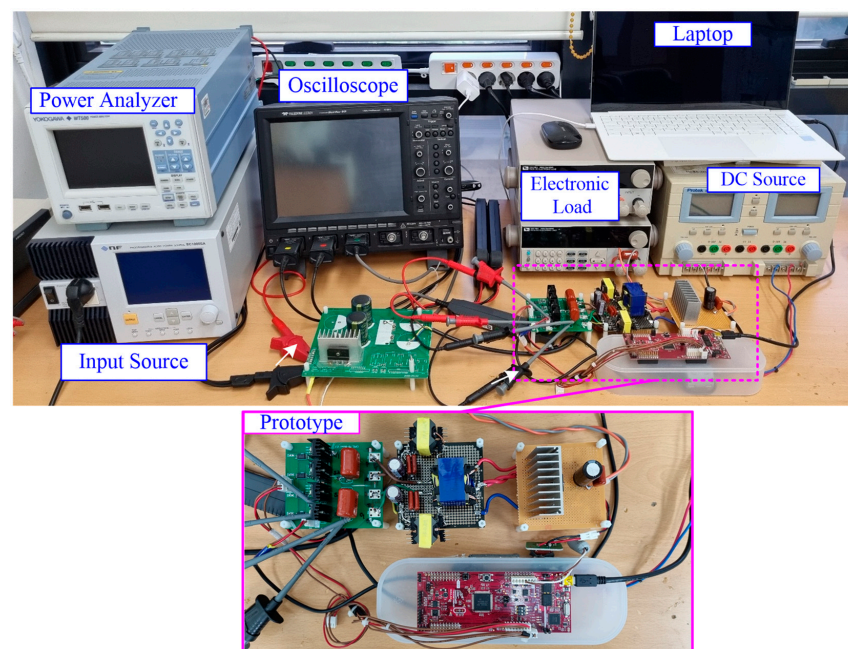


Figure 8. Photograph of the experimental setup.

Table 3. Experimental parameters.

Parameter	Specification
Primary switches S_1 – S_4	FQPF16N25 (250 V, 9.5 A, 0.23 Ω)
Modulation method	PFM
Duty ratio range	0.5 (fixed)
Switching frequency	110–195 kHz
Resonant frequency	195 kHz
Transformer ($N_{p1}:N_{p2}:N_{s1}:N_{s2}$)	PQ3535 (12:12:6:6)
Magnetizing inductances L_{m1} , L_{m2}	52.5 μ H
Leakage inductors L_{r1} , L_{r2}	15 μ H
Input capacitors C_1 , C_2	22 μ F
Resonant capacitors C_{r1} , C_{r2}	44 nF
Clamp capacitor C_{C1} , C_{C2}	4.7 μ F
Output capacitor C_o	1000 μ F
Secondary diodes D_1 , D_2	30CPQ150 (150 V 30 A: 15 A $\times$ 2)

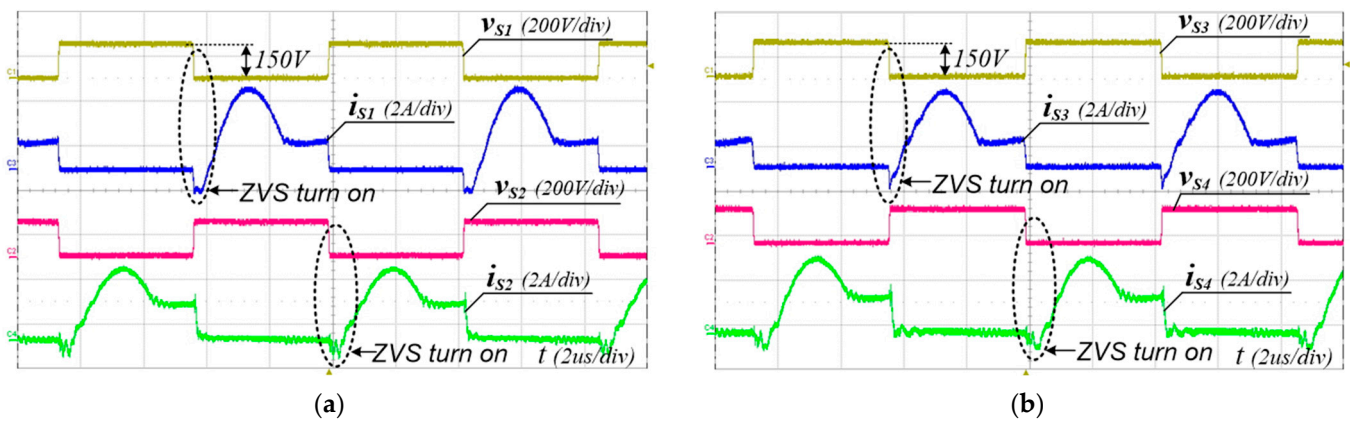


Figure 9. Experimental voltage and current waveforms of switches at $V_{in} = 300$ V and $I_o = 5$ A (full load). (a) S_1 and S_2 , (b) S_3 and S_4 .

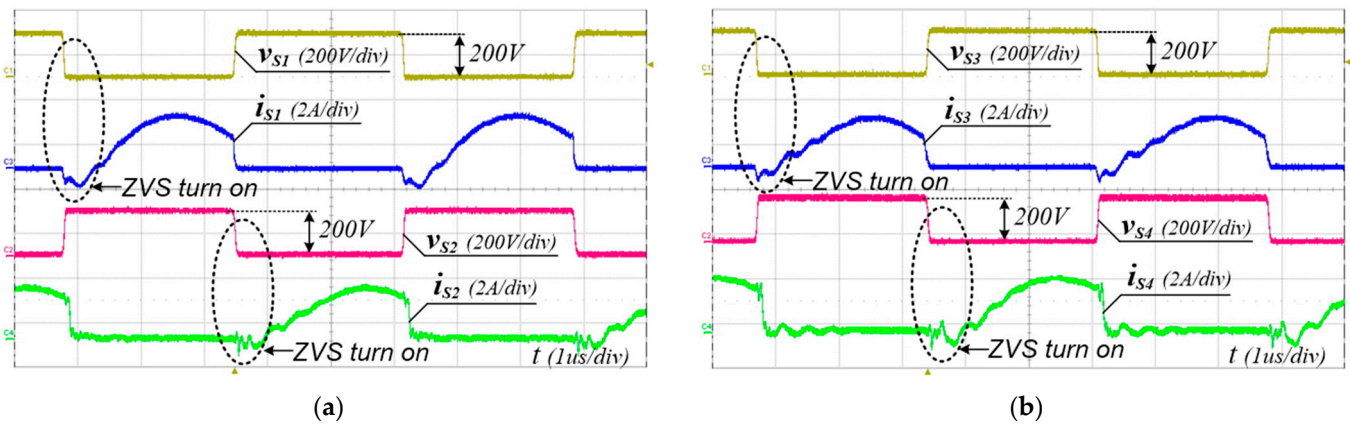


Figure 10. Experimental voltage and current waveforms of switches at $V_{in} = 400$ V and $I_o = 5$ A (full load). (a) S_1 and S_2 , (b) S_3 and S_4 .

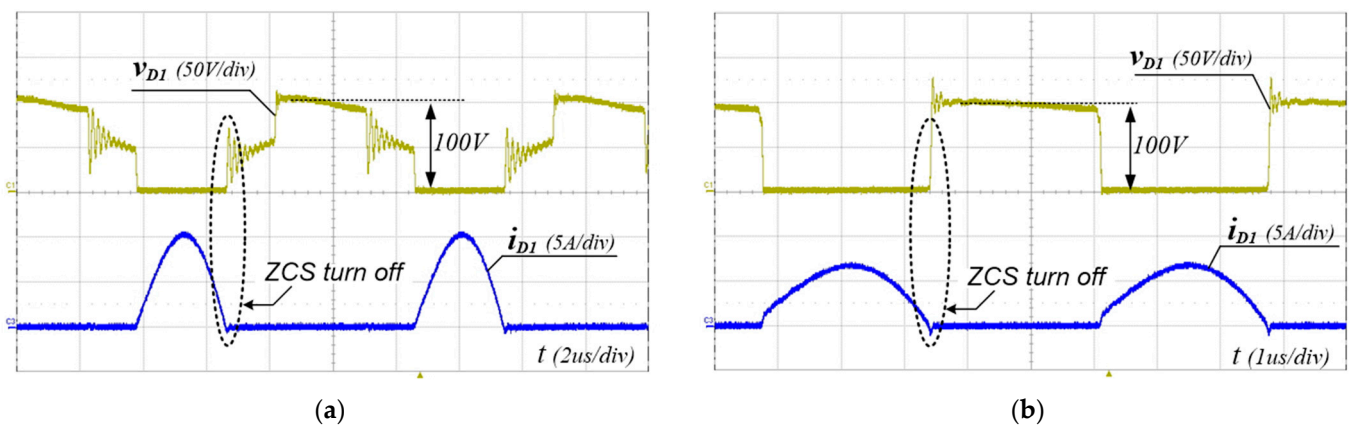


Figure 11. Experimental voltage and current waveforms of Diode D_1 at $I_o = 5$ A (full load). (a) $V_{in} = 300$ V, (b) $V_{in} = 400$ V.

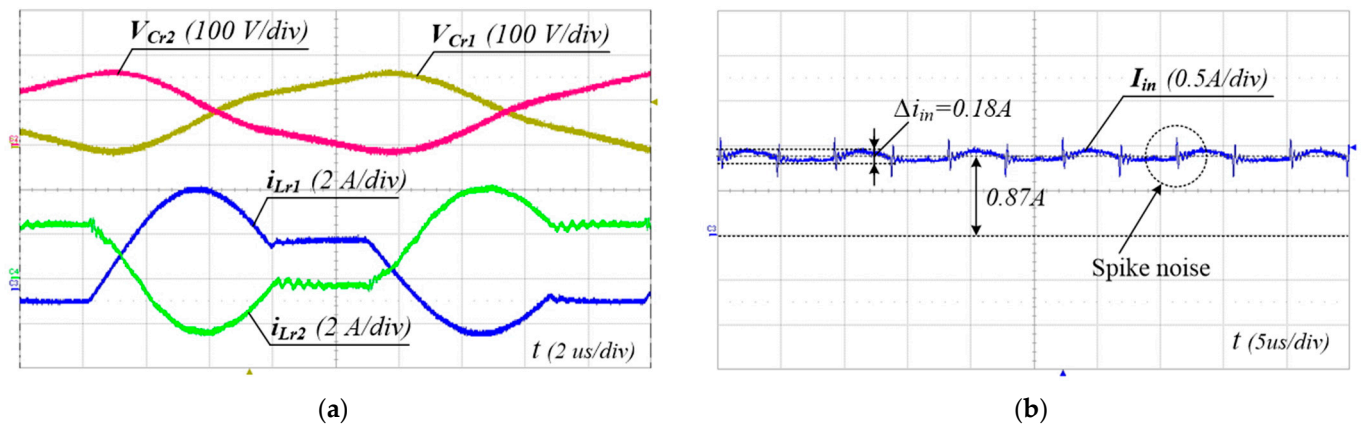


Figure 12. Experimental waveforms at $V_{in} = 300$ V and $I_o = 5$ A (full load). (a) Current and voltage of the resonant tanks, (b) input-current ripple.

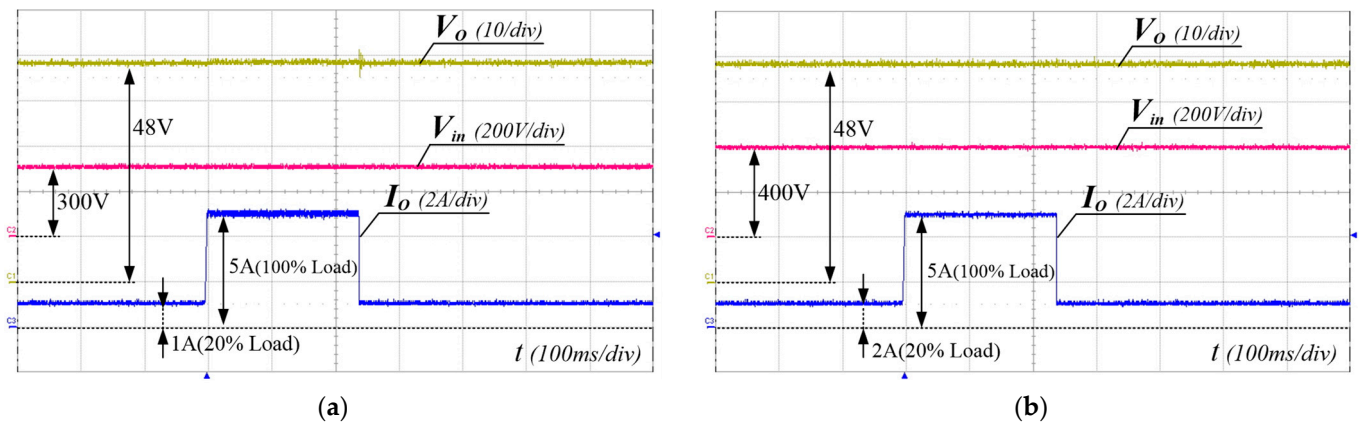


Figure 13. The dynamic response of the output voltage with respect to load changes. (a) $V_{in} = 300$ V, (b) $V_{in} = 400$ V.

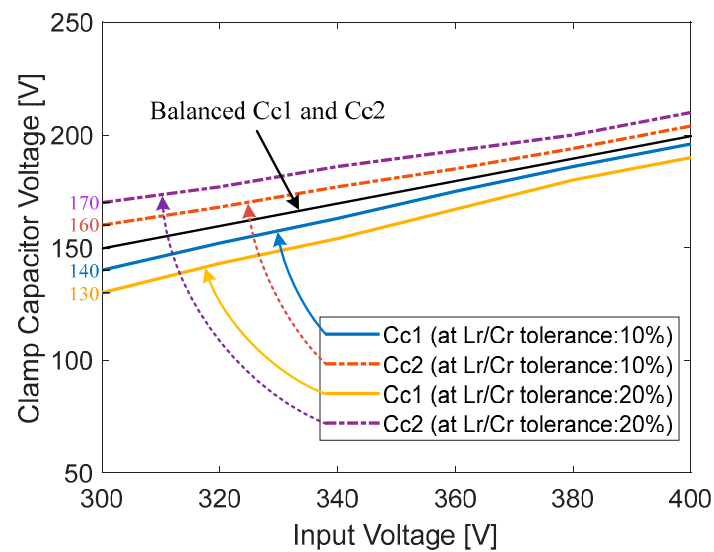


Figure 14. Simulated clamp-capacitor voltage imbalance with input voltage.

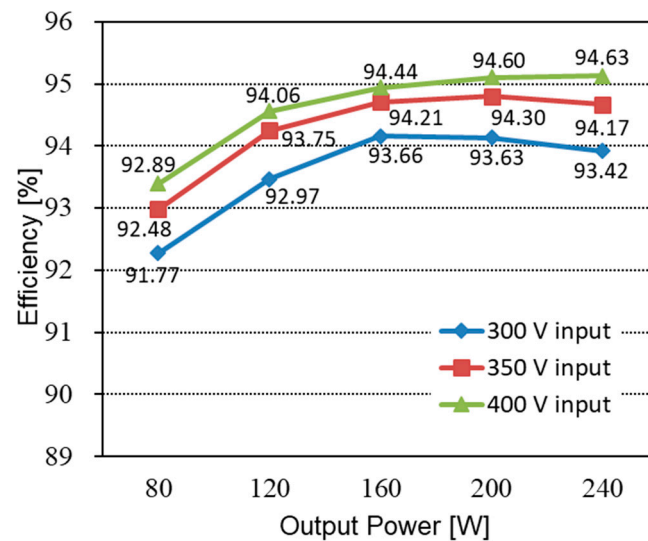


Figure 15. Measured efficiency curves of the proposed converter according to the output power.

6. Conclusions

A novel high-efficiency three-level double LLC resonant DC-DC converter with a ripple-free input current and low-voltage switch stress has been presented. The input noise components, which are due to the pulsating input current, can be significantly reduced without the addition of large input filters. Moreover, the voltage stress on the primary switches is only half the input voltage, which allows the proposed converter to use commercially available low-voltage-rated power switches for higher-voltage input applications. All the primary switches and secondary diodes are softly switched over a wide input voltage range, reducing switching loss. The advantages of the proposed converter mentioned above have been verified by the experimental results of a prototype converter with a 300–400 V input, 48 V/5 A output, and 195 kHz resonant frequency. The maximum efficiency of the proposed converter is about 94.63% under full load conditions at a 400 V input. As a result, since the proposed converter has the advantages of reduced input noise, low-voltage switch stress, and high efficiency, it is suitable for applications in DC-DC converters used in a DC microgrid with high-voltage DC bus.

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