

## Article

# A 60 GHz Power Amplifier with Neutralization Capacitors and Compensation Inductors

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**Abstract:** In this paper, we present a high power-added efficiency (PAE) and high gain per stage 60 GHz power amplifier (PA). The proposed PA consists of a two-stage common-source amplifier that incorporates neutralization capacitors and compensation inductors to enhance both gain and efficiency. The gain characteristics are analyzed, demonstrating that the proposed design improves both gain and efficiency. Implemented in 65 nm CMOS technology, the PA achieves a saturated output power of 13.4 dBm at 60 GHz, with a maximum PAE of 26.7% from a 1 V supply. The output 1 dB compression point is 10.5 dBm, with a PAE of 16%. The PA occupies a core chip area of 0.094 mm<sup>2</sup>.

**Keywords:** 60 GHz; CMOS; gain; millimeter wave; neutralization capacitor; power-added efficiency; power amplifier; transformer

## 1. Introduction

Recently, the unlicensed 60 GHz band has gained attention for its ability to transmit tens of gigabits per second of data due to its wide bandwidth [1–3]. In this frequency band, low-power, high-efficiency designs are critical for handheld device applications. Additionally, multiple-input multiple-output (MIMO) and phased array techniques have been introduced to enhance data rates and extend communication distances. However, these techniques require multiple transmitters and receivers, leading to increased power consumption, which makes their use in handheld devices challenging. In particular, power amplifiers (PAs) consume substantial DC power while offering limited efficiency.

As a key component, PAs with high power-added efficiency (PAE) and output power exceeding 13 dBm are essential for reducing battery consumption and extending the operating time of handheld devices. Thus, designing highly efficient PAs is a primary challenge for next-generation millimeter-wave (mm-wave) wireless systems. PA efficiency represents a significant bottleneck, especially in transmitter arrays. Over the past decade, significant progress has been made in developing high-power, high-efficiency PAs for mm-wave bands [4–14]. CMOS processes are widely used in mm-wave PA design due to their low cost and ability to integrate with digital baseband circuitry. Transformer-based common-source amplifiers are popular for their compact size and simple power matching and combining capabilities [7–14]. Most of the published CMOS PAs focused on achieving high output power by employing cascode topologies [8,9], power combining architectures [10–12], and linearity enhancement techniques [13]. Power combining techniques enable higher output power and gain [10–12], but this technique suffers from large chip areas and limited PAE. For instance, a PA with a two-way, four-stage common-source [10] achieved a saturated output power (PSAT) of 16 dBm, but with a PAE of only 17%. A 32-way, four-stage common-source PA [11] showed a gain of 21.9 dB and a PSAT of 24.1 dBm but required a large chip area and a huge power consumption. The linearized PA [13] achieved a PSAT of 15 dBm with a PAE of 26%, and an output 1 dB compression point (OP1dB) of 14 dBm with a PAE of



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21%. However, this PA exhibited a limited gain of 14 dB due to the linearization technique. A variable gain PA [14] provides a variable gain of 23.5 dB, but requires multiple stages, limiting its PAE to 21.5%.

In this study, a high-efficiency 60 GHz PA was implemented for handheld devices such as smart phones, gaming consoles, augmented reality, and virtual reality devices. The proposed circuit uses a two-stage common-source amplifier with compensation inductors and neutralization capacitors to achieve high PAE and high gain per stage. As a result, the PA successfully achieved a power gain of 18.3 dB, an OP1dB of 10.5 dBm, and a peak PAE (PAE<sub>peak</sub>) of 26.7% at 60 GHz. The measurement results indicate that the proposed PA is suitable for low-power mm-wave handheld devices.

## 2. Design Methodology

### 2.1. Active Device

The output power and efficiency of the PAs highly depend on active devices and parasitic components, as PAs typically utilize large transistors to achieve high output power. This issue becomes more pronounced in the mm-wave band, where operating frequencies approach the cut-off frequency and maximum oscillation frequency, leading to reductions in power gain and output power. Additionally, the parasitic capacitance of active devices further limits bandwidth, power gain, output power, and PAE. PAE can be expressed as

$$\text{PAE} = \frac{P_{\text{OUT}} - P_{\text{IN}}}{P_{\text{DC}}}, \quad (1)$$

where  $P_{\text{OUT}}$ ,  $P_{\text{IN}}$ , and  $P_{\text{DC}}$  are the output power, input power, and power dissipation of the PA. PAE is a metric for rating the efficiency of the PA. To mitigate these challenges, careful design of transistor size and interconnections is essential.

To optimize the transistor size for the PA, we compared the performance of the power stage based on different device configurations. Table 1 presents the load-pull simulation results comparing transistors with one  $4 \mu\text{m} \times 25$  fingers, two  $2 \mu\text{m} \times 25$  fingers, and four  $1 \mu\text{m} \times 25$  fingers in a differential common-source amplifier with neutralization capacitors [7]. All configurations maintain a total transistor width of  $100 \mu\text{m}$  to achieve an output power above 13 dBm. The simulation results indicate that the configuration with two  $2 \mu\text{m} \times 25$  fingers delivers superior PSAT and PAE<sub>peak</sub>. As a result, we selected two  $2 \mu\text{m} \times 25$  fingers for the power cell in the power stage of this design.

**Table 1.** Performance comparison of load-pull simulation results at 60 GHz.

| Topology                      | $4 \mu\text{m} \times 25$ Fingers | $2 \times 2 \mu\text{m} \times 25$ Fingers | $4 \times 1 \mu\text{m} \times 25$ Fingers |
|-------------------------------|-----------------------------------|--------------------------------------------|--------------------------------------------|
| PSAT (dBm)                    | 15.2                              | 15.9                                       | 15.5                                       |
| PAE <sub>peak</sub> (%)       | 33.8                              | 37.5                                       | 36.5                                       |
| Power Gain (dB)               | 11.1                              | 12.0                                       | 12.2                                       |
| $Z_{\text{opt}}$ ( $\Omega$ ) | $21.1 + j15.3$                    | $16.3 + j16.5$                             | $17.4 + j21.0$                             |

Figure 1a illustrates the proposed layout of the unit transistor cell for the drive and power stages. The unit cell employs transistors with a width of  $2 \mu\text{m}$  and 25 fingers, occupying an area of  $15 \times 9 \mu\text{m}^2$ . To optimize the layout, the source is connected using multiple metal layers (M4–M7) and linked to a double-sided ground plane (M1–M2). The M1 and gate poly are connected on both sides and routed to M8. Additionally, gate–source and gate–drain overlap is minimized to reduce parasitic capacitance. Figure 1b shows the layout of the two  $2 \mu\text{m} \times 25$  fingers devices, which occupy an area of  $28 \times 9 \mu\text{m}^2$ . The unit transistors are placed adjacent to each other, with the sources directly connected to minimize interconnection resistance. The gate and drain are routed through thick metal layers M8 and M9, respectively. In electromagnetic (EM) simulations, interconnection losses resulted in power gain degradations of 0.2 dB and 0.3 dB for the single  $2 \mu\text{m} \times 25$  fingers and two  $2 \mu\text{m} \times 25$  fingers transistors, respectively.

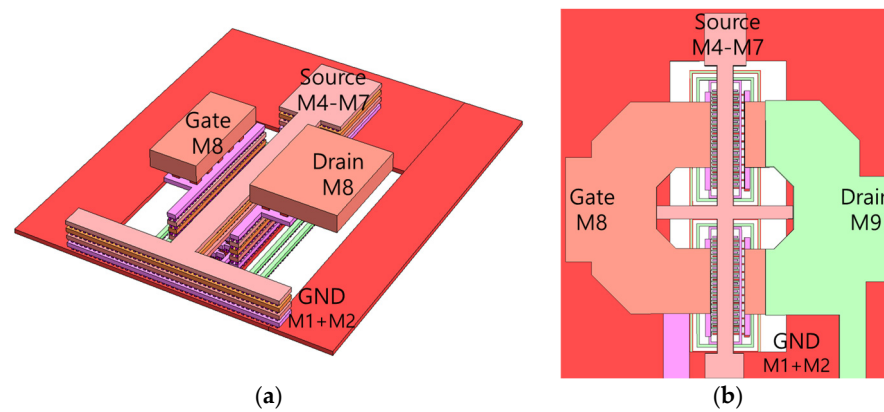


**Figure 1.** Transistor layout of (a)  $2\ \mu\text{m} \times 25$  fingers and (b)  $2 \times 2\ \mu\text{m} \times 25$  fingers.

## 2.2. Neutralization Capacitors

In addition to optimizing transistor configuration and layout, neutralization capacitors [7] are employed to enhance gain and stability. Figure 2 shows the schematic and layout of the differential amplifier with neutralization capacitors for the power stage. The gate-to-drain parasitic capacitance,  $C_{gd}$ , creates a feedback path that degrades power gain, reverse isolation, and stability. The neutralization capacitors,  $C_N$ , address these issues by neutralizing  $C_{gd}$ , effectively eliminating the feedback path.

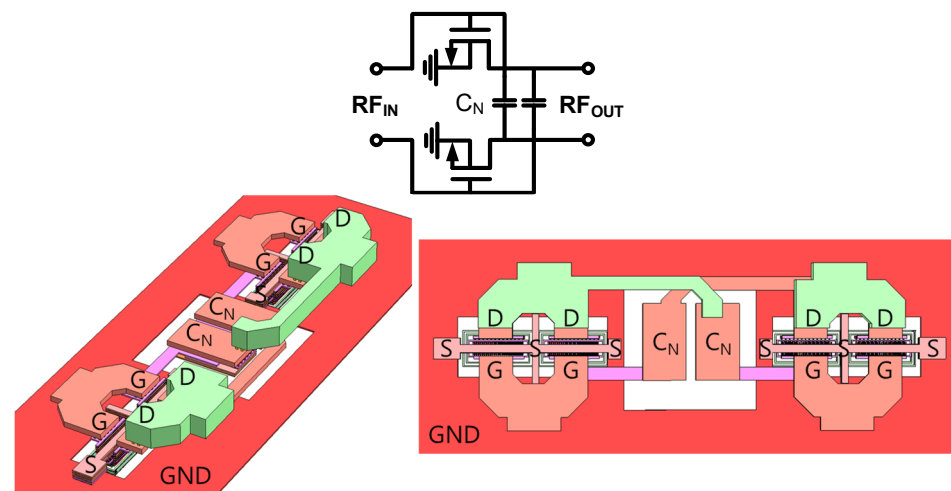


**Figure 2.** Schematic and layout of differential amplifier with neutralization capacitors, where G, D, and S are gate, drain, and source, respectively.

The custom-designed metal–oxide–metal (MOM) capacitor [15] was used for  $C_N$ , rather than the standard foundry-provided MOM capacitor. The custom MOM capacitor utilizes a multi-stack metal plate design for a smaller chip area, shorter interconnections, and sufficient vias to reduce parasitic resistance. Moreover, the custom MOM capacitor exhibited a minimal process variation of less than  $\pm 2\%$ , compared to  $\pm 11\%$  for the foundry-provided MOM capacitor, as shown in simulations.

Figure 3 illustrates the simulated maximum available gain (MAG) and stability factor of the differential common-source amplifier with the neutralization capacitor  $C_N$ . The amplifier remains stable with up to  $\pm 20\%$  variation in  $C_N$ . A capacitance of 27 fF was selected for  $C_N$ , slightly smaller than the required value for maximum stability, to account for additional parasitic capacitance. With the neutralization technique, the power stage achieves a MAG of 13.1 dB, an improvement of 3.0 dB compared to the design without neutralization. The neutralization capacitor is also applied to the driver stage to further enhance stability and gain.

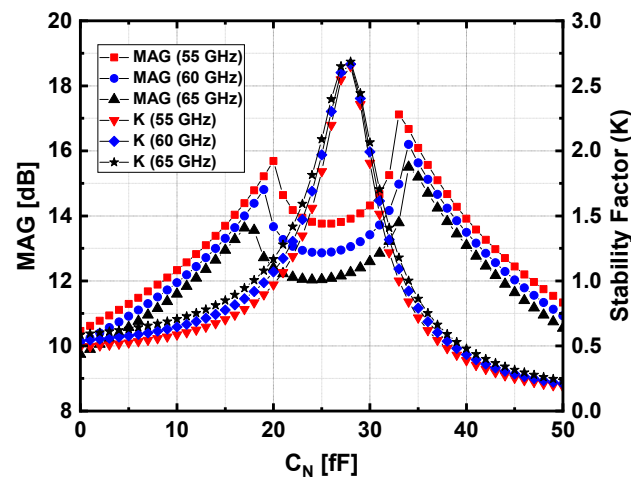


**Figure 3.** Simulated MAG and stability factor of the differential common-source amplifier with neutralization capacitor  $C_N$ .

### 2.3. Proposed PA Design with Transformers and Compensation Inductors

A simplified schematic of the proposed 60 GHz PA and the layout of the transformers are shown in Figure 4. The PA consists of a two-stage differential common-source amplifier with transformers,  $TF_1$ – $TF_3$ , a matching network with compensation inductors, and neutralization capacitors,  $C_{N1}$  and  $C_{N2}$ . The transistor size of the power stage is two times larger than that of the driver stage. The power stage has two  $2\ \mu\text{m} \times 25$  fingers devices, whereas the driver stage has a single  $2\ \mu\text{m} \times 25$  fingers device. In the power stage, two  $2\ \mu\text{m} \times 25$  fingers devices provide a better gain, PAE, and PSAT than a single  $4\ \mu\text{m} \times 25$  fingers device. The neutralization capacitors  $C_{N1}$  and  $C_{N2}$  are chosen to be 13.5 fF and 27 fF, respectively, for better power gain, isolation, and stability.

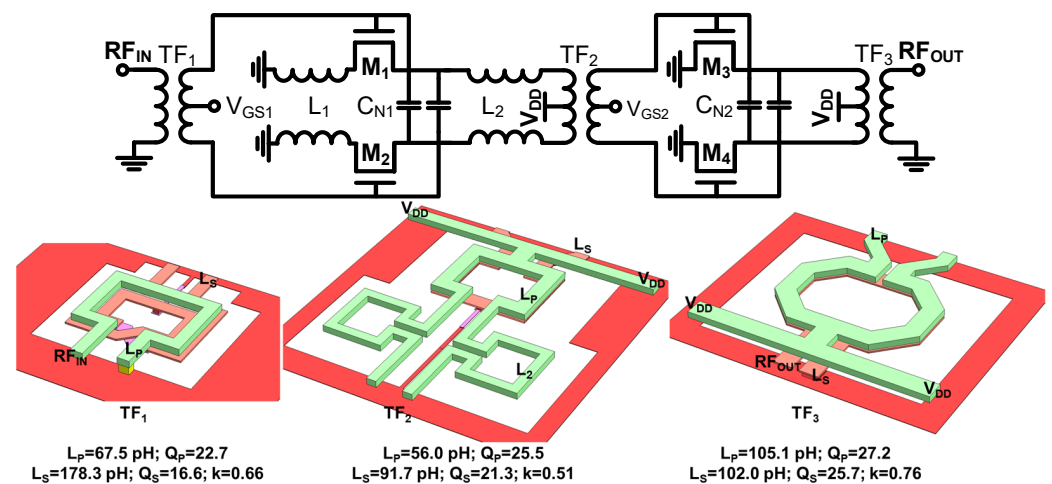


**Figure 4.** Schematic of proposed PA and layout of transformers.

The first stage of the PA is implemented using a differential common-source amplifier with neutralization capacitors and inductive source degeneration. Inductor  $L_1$  is connected to the source terminals of the transistors  $M_1$  and  $M_2$ , creating a series–series negative feedback loop. This feedback improves OP1dB and stability while slightly reducing power gain. The inductive source degeneration technique at the power stage also enhances the linearity, but the gain reduction at the second stage requires a higher linearity at the first stage.  $L_1$  is set to 24 pH to balance the improvement in OP1dB and stability with the reduction in gain. In the simulation, a 0.5 dB improvement in OP1dB is achieved, with a 1.5 dB reduction in gain, while the stability factor increases from 10 to 15 at 60 GHz.

A highly efficient matching network is crucial for enhancing gain, PAE, and PSAT. Transformer-based matching networks, paired with compensation inductors, are used to achieve high efficiency and a compact design. The transformers are implemented using two vertically coupled top metal layers. The input transformer balun  $TF_1$  has a turn ratio of 1:2 for impedance transformation. The output transformer  $TF_3$  is designed with a high coupling factor of 0.76, as the insertion loss of the transformer is proportional to the square of the coupling factor [16]. The inter-stage matching network uses compensation inductors  $L_2$  and a transformer,  $TF_2$ , with a lower coupling coefficient and a 1:1 turn ratio. A coupling coefficient of 0.51 was selected for  $TF_2$  considering the matching loss and bandwidth. A lower coupling coefficient results in wider bandwidth but increases matching loss [4]. The compensation inductor  $L_2$  helps optimize the matching loss. As shown in Figure 5, the simulated inter-stage matching loss is 1.9 dB at 60 GHz. The inter-stage matching network, which combines the moderately coupled transformer  $TF_2$  with the compensation inductor  $L_2$ , delivers high efficiency and gain by compensating the impedance mismatch between the driver-stage output and the power-stage input. Consequently, the matching loss of the inter-stage matching network with  $TF_2$  and  $L_2$  is 3.4 dB smaller than that with the transformer without a compensation inductor in the simulation.

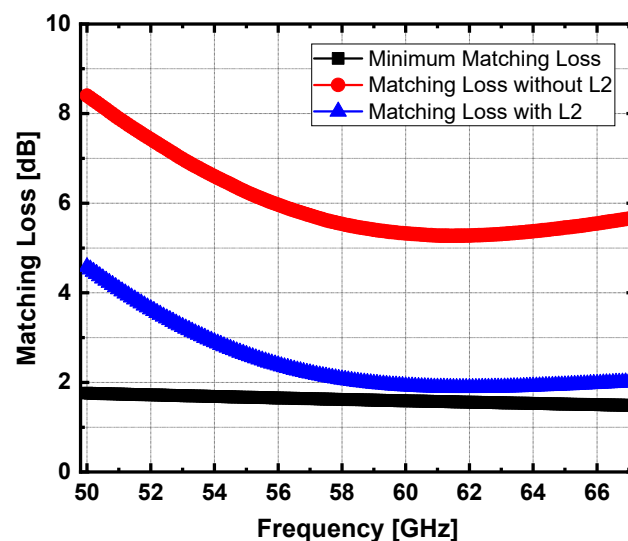


Figure 5. Simulated inter-stage matching losses.

A ground plane with a mesh pattern using the two bottom metal layers is used. The neutralization capacitors, inductors, interconnections, and transformers are all simulated using the HFSS 3-D EM simulator developed by Ansys, Canonsburg, PA, USA. The transistors, M1–M4, have a gate length of 60 nm. With the neutralization capacitors and compensation inductors, the proposed PA achieved a simulated gain of 17.6 dB, a simulated PSAT of 14 dBm, and a simulated  $PAE_{peak}$  of 26.5% at 60 GHz.

### 3. Results

The proposed PA circuit was implemented in a standard 65 nm CMOS technology. Figure 6 depicts a chip photograph of the proposed PA. The PA chip occupies an area of  $0.58 \times 0.46 \text{ mm}^2$  including the bond pads and  $0.094 \text{ mm}^2$  excluding the pads. The PA dissipates a power of 58 mW from a 1 V supply voltage. Figure 7 illustrates measurement setups for the S-parameter and power handling capability. The S-parameter was measured with an E8361A vector network analyzer manufactured by Keysight, Santa Rosa, CA, USA and the results were calibrated using the Picoprobe SOLT (short–open–load–thru) GSG-67A calibration substrate. The large-signal measurements were performed with a signal generator, frequency multiplier, power sensor, and high-precision power meter. The

measured losses of the probe tips, adapters, and coaxial cables were de-embedded from the raw measurement data.

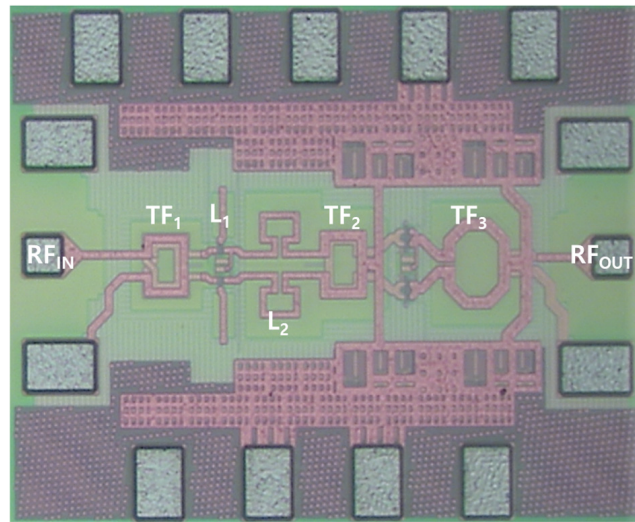


Figure 6. Microphotograph of proposed PA.

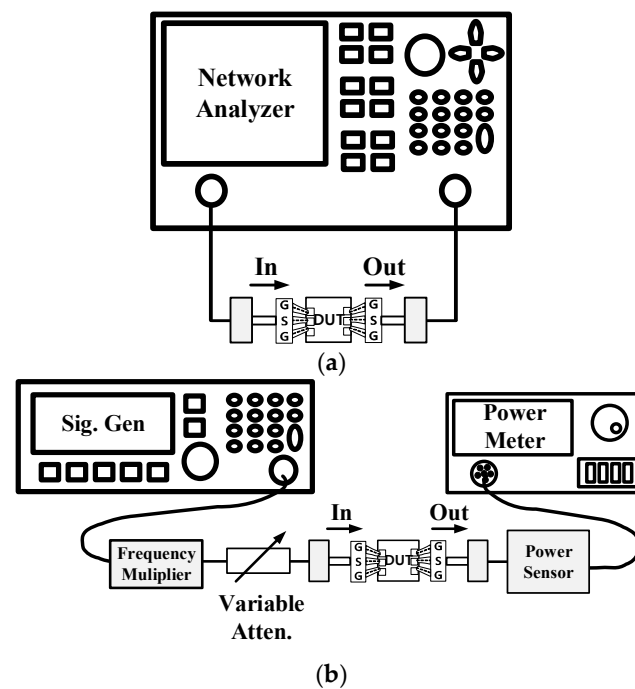


Figure 7. Measurement setups for (a) S-parameter and (b) large-signal measurements.

Figure 8 shows the simulated and measured power gains of the 60 GHz PA. The measured gain of the proposed PA is 18.3 dB at 60 GHz. The measured peak gain is 18.7 dB at 58.3 GHz and the measured 3 dB bandwidth is 10.1 GHz (54.4–64.5 GHz). The difference between the simulated and measured data is probably due to the inaccuracy of the transistor model at 60 GHz, especially the drain-to-gate capacitance. Figure 9 depicts the simulated and measured input and output return losses of the proposed PA. The measured input and output return losses are larger than 8.4 dB and 6.0 dB, respectively, for 55.2–66 GHz. Figure 10 illustrates the simulated and measured reverse isolation of the proposed PA. The reverse isolation is smaller than  $-39$  dB in the 60 GHz band.

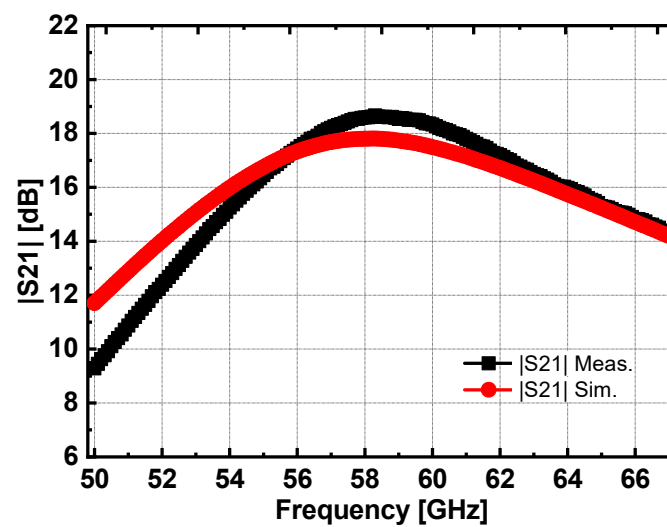


Figure 8. Simulated and measured power gains of the proposed PA.

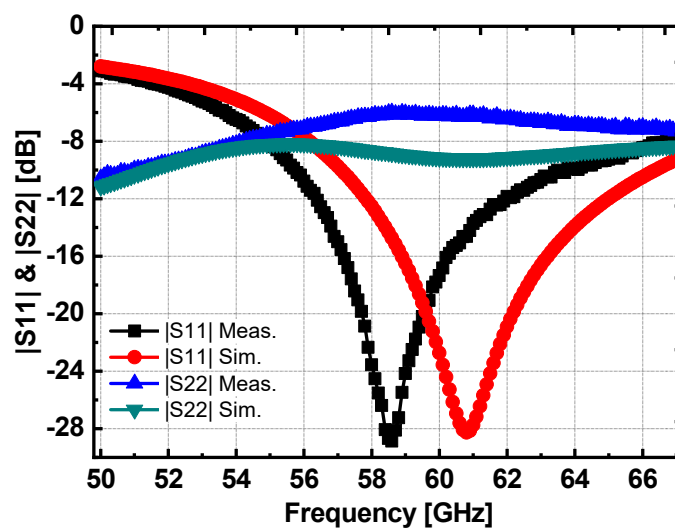


Figure 9. Simulated and measured input and output return losses of the proposed PA.

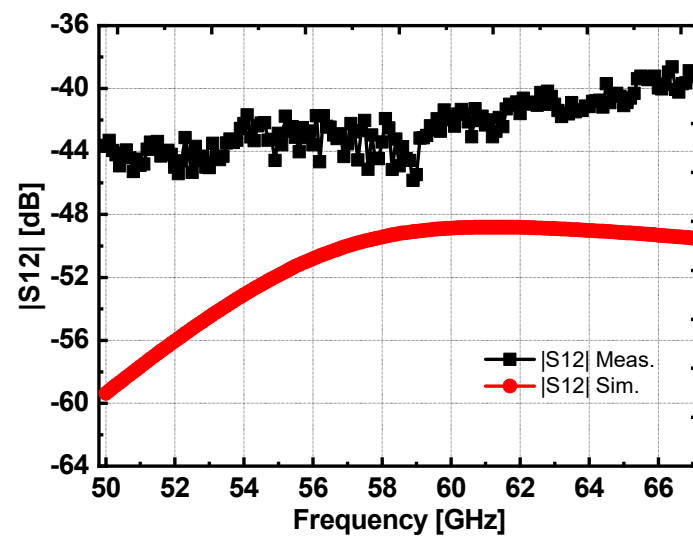


Figure 10. Simulated and measured reverse isolation of the proposed PA.

Figure 11 shows the measured power gain, output power, and PAE. OP1dB and PSAT are 10.5 dBm and 13.4 dBm at 60 GHz, respectively. The maximum PAE is 26.7%. The measured PSAT is limited due to the limited input power of the signal generator and frequency multiplier. The neutralization capacitors and compensation inductors enhance the gain and PAE, which are suitable for low-power mm-wave handheld devices.

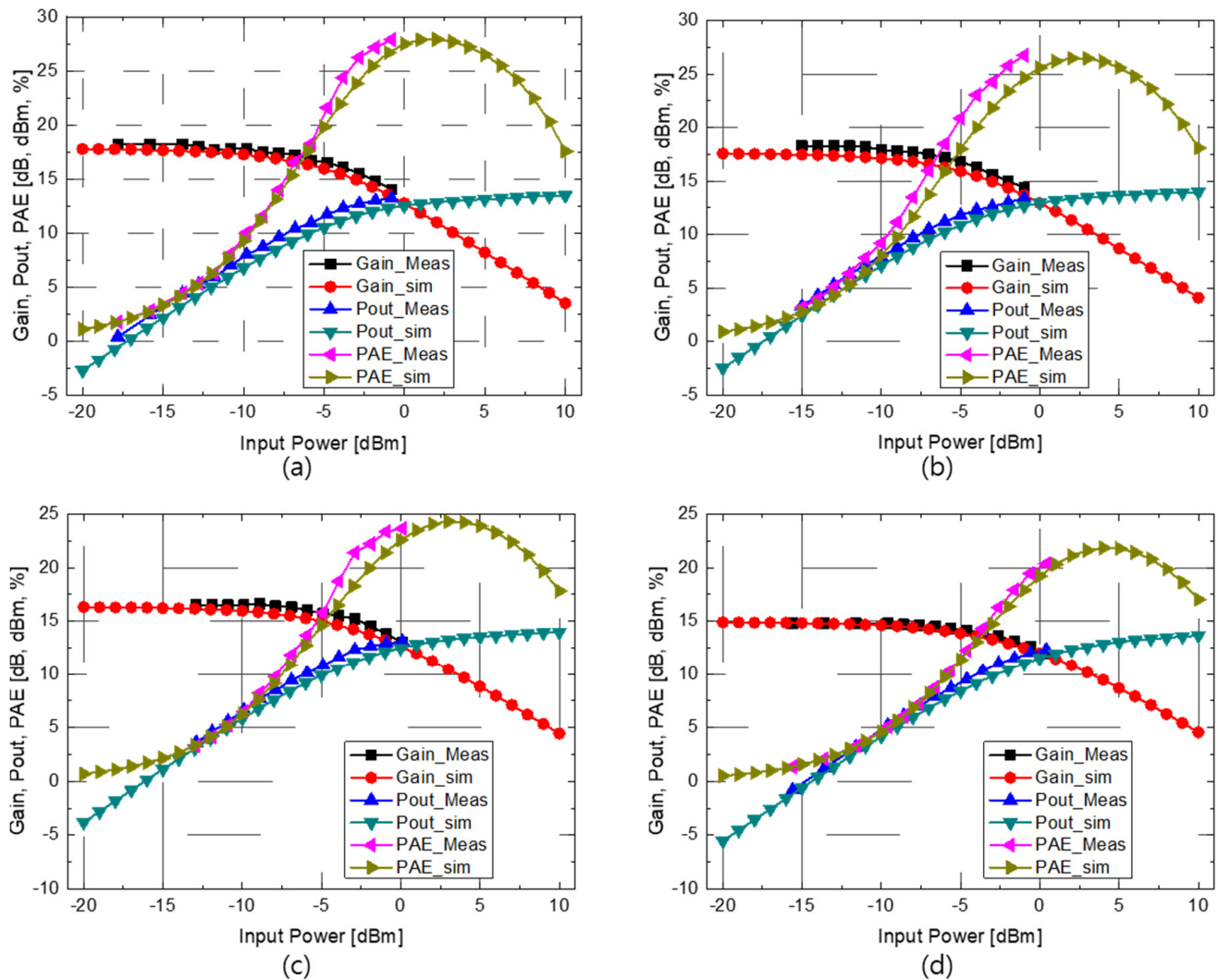


**Figure 11.** Simulated and measured power performances of the proposed PA at (a) 57 GHz, (b) 60 GHz, (c) 63 GHz, and (d) 66 GHz.

#### 4. Discussion

Table 2 compares the performance of the state-of-the-art 60 GHz CMOS PAs. The proposed PA demonstrates high gain per stage and a high peak power-added efficiency (PAE). The PA in [8] achieves a high PAE, but it is implemented using 22 nm CMOS technology, which offers a significantly higher cut-off frequency and maximum oscillation frequency. The PA in [11] attains high output power, due to the use of larger transistors; however, this results in a substantial DC power consumption of 942 mW. The proposed PA utilized the neutralization capacitors and compensation inductors and enhanced the gain and PAE, which are suitable for low-power mm-wave handheld devices.

**Table 2.** Performance comparisons of the state-of-the-art 60 GHz CMOS PA.

|                         | This Work        | [8]                   | [9]                      | [10]             | [11]              | [12]             | [13]             | [14]             |
|-------------------------|------------------|-----------------------|--------------------------|------------------|-------------------|------------------|------------------|------------------|
| Process                 | 65 nm CMOS       | 22 nm CMOS            | 65 nm CMOS               | 65 nm CMOS       | 65 nm CMOS        | 16 nm CMOS       | 40 nm CMOS       | 55 nm CMOS       |
| Topology                | 1-way 2-stage CS | 1-way 2-stage cascode | 1-way 4-stage CS cascode | 2-way 4-stage CS | 32-way 4-stage CS | 4-way 2-stage CS | 1-way 4-stage CS | 1-way 4-stage CS |
| Frequency (GHz)         | 60               | 62                    | 60                       | 60               | 60                | 65               | 60               | 60               |
| V <sub>DD</sub> (V)     | 1.0              | 2                     | 1.2                      | 1.2              | 1.2               | 0.95             | 2                | 1.2              |
| Gain (dB)               | 18.3             | 23.3                  | 25.4                     | 25               | 21.9              | 18 *             | 14               | 22.5             |
| Gain/stage (dB)         | 9.2              | 11.7                  | 6.4                      | 6.3              | 5.4               | 9.0              | 7.0              | 5.6              |
| PSAT (dBm)              | 13.4             | 13.6                  | 12.2                     | 16               | 25.1              | 17.9             | 15               | 14.4             |
| P1dB (dBm)              | 10.5             | 12.1                  | 11.3                     | 11.3             | 21.7              | 13.5             | 14               | 13               |
| PAE <sub>peak</sub> (%) | 26.7             | 28.3                  | 8.9                      | 17               | 21                | 26.5             | 26               | 21.5             |
| PAE <sub>1dB</sub> (%)  | 16               | 26 *                  | 6.5 *                    | 7 *              | 7 *               | 15               | 21 *             | 17.7             |
| P <sub>DC</sub> (mW)    | 58               | 33                    | 186                      | 185              | 942 *             | -                | 110              | 67.2             |
| Area (mm <sup>2</sup> ) | 0.094            | 0.065                 | 0.36                     | 0.20             | 1.17              | 0.107            | 0.2              | 0.15             |

\* Graphically estimated.

## 5. Conclusions

A 60 GHz PA circuit was implemented and designed using a standard 65 nm CMOS technology. The PA with neutralization capacitors and compensation inductors provides a gain of 18.3 dB with a maximum PAE of 26.7% at 60 GHz from a 1 V supply voltage. Furthermore, the PSAT is 13.4 dBm. The measurement results indicate that the proposed PA is suitable for application to low-power mm-wave handheld devices.

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