

Article

A Methodology for the Design of a Compliant Electrocardiograph: A Case Study

Luis Alberto Gordillo-Roblero ¹, Jorge Alberto Soto-Cajiga ^{1,*}, Carlos Romo-Fuentes ²,
Luis Felipe Martínez-Soto ^{1,3} and Noé Amir Rodríguez-Olivares ¹

- ¹ National Laboratory for Research on Medical Technologies (LANITEM), Center for Engineering and Industrial Development (CIDESI), Pie de la Cuesta 702, Des. San Pablo, Queretaro 76125, Mexico; luis.gordillo@cidesi.edu.mx (L.A.G.-R.); lmartinez@cidesi.edu.mx (L.F.M.-S.); noe.rodriguez@cidesi.edu.mx (N.A.R.-O.)
- ² EMC Test Lab (LEMC), Advanced-Technology Unit (UAT), Engineering Faculty, National Autonomous University of Mexico (FI-UNAM), Fray Antonio de Monroy e Híjar 260, Villas del Mesón, Juriquilla, Queretaro 76226, Mexico; carlosrf@unam.mx
- ³ Electrical Testing and Electromagnetic Compatibility Laboratory (LPECE), Center for Engineering and Industrial Development (CIDESI), Pie de la Cuesta 702, Des. San Pablo, Queretaro 76125, Mexico
- * Correspondence: jsoto@cidesi.edu.mx; Tel.: +52-442-144-0912

Abstract: This document presents the methodology for designing an electrocardiograph capable of acquiring IEC 60601-2-25-compliant signals. The objective of developing this methodology is to address a signal incompatibility problem that has existed in academia for years, specifically in physiological processing research. This problem is related to the signal's sampling rate and/or noise levels, and it becomes evident when one signal processing method is intended to work with another, either as a subsequent or simultaneous process. Even though matching algorithms can be implemented to remedy this incompatibility problem, the ultimate solution is the standardization of signals, which depends exclusively on the standardization of hardware. The signal incompatibility problem is urgent to solve because it makes the integration and scalability of different academic works difficult, preventing academia from reaching the stage of development that commercial equipment displays in automatic interpretation procedures. The design methodology presented in this document addresses the stated problem by creating an open-source hardware device capable of acquiring compliant signals, with careful consideration given to Signal Integrity and EMC concepts—a methodology that can be extended to other physiological acquisition systems. The expedited availability of the device's design documentation and fabrication files is also an advantage of this work.

Keywords: ECG; electrocardiograph; EMC; open-source hardware; physiological signals; signal acquisition; signal integrity; signal processing



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1. Introduction

In general, the definition of “design” is complex. Design involves art, but it is also a scientific process. For electronics engineers, design involves selecting and arranging components in such a way as to best accomplish a particular purpose. This includes optimizing resources, analyzing trade-offs, and making the product attractive, safe, compliant, and functional.

Electronics play an important role in industries where life-supporting systems are used, such as aeronautics and healthcare, to name two. These industries are subject to a broad spectrum of stringent regulations (as should be expected), and some of these regulations apply specifically to the performance of electronic circuitry; from components quality, through manufacturing processes, design standards, and finally, regulations to validate functional performance. The need to comply with these regulations demands human resources with a solid background in electronics engineering, but most importantly, with a

solid understanding of electromagnetic theory, since the concepts of Signal Integrity (SI) and Electromagnetic Compatibility (EMC) are closely related to this theoretical foundation, and both are equally important to the design and development of mixed-signal boards, as is the case with modern physiological signal acquisition systems, like an electrocardiograph.

For some academics, electronics design does not contribute to science. The common misconception of thinking about electronics at a hobbyist level (Arduino, Raspberry Pi, and other off-the-shelf solutions for research) is probably the reason behind this widespread belief. Coincidentally, in the ECG signal processing field, some of these same academics name the lack of quality signals as an obstacle to conducting their research. The inconvenience of this attitude within academic communities is that it discourages the development of specialized hardware needed to solve valid scientific problems that academia has been lagging for years. For example, in academia, specifically in the ECG signal processing field, despite decades of research, no clinically ready solutions have been created. In other words, no algorithms in academia that are ready to use in hospitals, like those developed by Philips or General Electric, currently exist. One of the reasons behind this problem is the lack of compliant and standardized signals that can facilitate the integration and scalability of diverse works, signals which in the end depend on hardware. On the other hand, as electronics engineers in the research field, our duty is to find a way to make science serve society, disregarding the common trend of limiting scientific research to the development of “computational models”, which often are no more than an assembly of previously published techniques. Academia should not forget that problem-solving is the main reason for science to exist.

Indeed, when designing for Electromagnetic Compatibility, it is not practical to mathematically analyze a circuit board due to the complexity of the mathematical equations that describe the simplest interference problem that can occur over a single trace segment (Section 1.5 of ref. [1], p. 37), such as electric coupling or magnetic coupling. In fact, when designing a board for Signal Integrity and EMC requirements, more mathematically complex phenomena are happening at the same time, i.e., signal reflection, signal returns, shielding, controlled impedances, or electromagnetic radiation. For a circuit designer, it is of practical use to understand the way the different physical parameters are interrelated in order to optimize circuit design. One should not forget that the primary objective of designing a board is to serve a purpose and validate its functional performance through compliance with applicable norms and standards. In our case study, we are creating a “physical model” that can receive biopotential signals as input and deliver a compliant digital signal as output, with the intention of solving a scientific problem in the ECG signal processing field.

The design methodology presented in this document can be used for designing most physiological signal acquisition systems, such as the electromyograph, electroencephalograph, respiration, or others. However, the nature of physiological signals demands special architectures for each one of them. In fact, the scientific problems that can be cited for each area of signal processing research are similar. For example, even though low efficiency in clinical applications is a common trend in all areas of signal processing research [2–7], there are not yet papers reporting low efficiency in the automatic interpretation of physiological signals as a general problem. For all these reasons, the format used in this design methodology is to describe a general design procedure and then apply it to our case study, an electrocardiograph. In this way, the design methodology can be extended to other systems’ designs.

Physiological signal acquisition systems share one thing in common: they acquire tiny biopotentials on the order of 1 mV and transfer them for processing via high-speed digital communications. They are considered mixed-signal boards, and they are not easy-to-do circuits. Even projects with enough funding and vast community support, like OpenECG [8,9], failed to grow and disappeared. OpenECG had the objective of reaching interoperability in electrocardiography by fostering standards and offering manufacturers feedback on their implementations. By offering feedback to manufacturers, it is evident that one of

the reasons for the disappearance of this project was indeed the unwillingness to develop the specialized hardware required themselves; otherwise, they would not have had to persuade manufacturers. On top of that, we could add the unwillingness of manufacturers to cooperate. Other projects, like PhysioNet [10] (<https://physionet.org>, accessed on 23 October 2024), due to their lack of interest in open-hardware development, are indeed the cause of the incompatibility problems currently found in academia. Fortunately, projects like the Kenshin Project (<https://kenshin-ai.org>, accessed on 23 October 2024), focused on bringing academic results to society, are already published. This document is part of this latter project.

2. Problem Definition

Signal acquisition systems for medical applications are complex devices that require specialized hardware and advanced software capabilities to be effectively used in clinical practice. In electrocardiography, commercial electrocardiographs are the most advanced devices, offering the best-known performance in both hardware and signal processing capabilities; however, multiple articles report low efficiency in their automatic interpretation capabilities [2,11,12]. This may sound like a good opportunity for academic research. Unfortunately, because commercial equipment is proprietary and its signal processing algorithms are not disclosed, academia has no means to directly contribute to improving the last cited efficiency reports. In fact, in academia, nothing at the same stage of development as commercial equipment yet exists, neither in hardware nor in clinical signal processing capabilities.

In the academic environment, especially in the field of physiological signal processing, the lack of open and compliant hardware architectures has limited academia from achieving results that can be effectively transferred to society. Firstly, because the hardware serves as the medium of transfer, and secondly, because developing applications to be used in clinical practice requires the integration and scalability of multiple application-specific algorithms. To carry out the latter, undoubtedly, the standardization of data, methods, and systems is a must [13,14]. Additionally, a goal-oriented communication tool, like the one suggested in ref. [15], for coordinating and promoting collaboration is also required.

Currently, the lack of open signal acquisition systems forces researchers to use signals from different public databases. These signals are generally acquired with different equipment and therefore present different signal characteristics (such as sampling rate and noise level) [16,17], causing a signal incompatibility problem that prevents the scalability and integration of algorithms that could lead to the development of applications that can be evaluated in clinical practice. The incompatibility problem is evident when one signal processing method is intended to work with another, either as a subsequent or simultaneous process. From personal experience, the incompatibility problem occurred when we attempted to use the output of a denoising algorithm [18] as the input for a subsequent waveform recognition process [19].

Most of the world's signal processing research is currently conducted using the resources provided by PhysioNet [10]. This was our case, and working with this databank is where the signal incompatibility problem was found. For example, the signals chosen for our denoising process were taken from the PTB diagnostics database [16]. These signals were sampled at 1 kHz, have not been annotated by cardiologists, and have acceptable system noise levels. For the waveform recognition process, we chose the QT database [17] because these signals are annotated by cardiologists, which is a requirement if the intention of an algorithm is the extraction of physiological parameters. However, the QT database is sampled at 250 Hz, and its noise level is significantly higher than that of the PTB database.

As one may now notice, using the output of the denoising algorithm (not annotated) as the input for the waveform recognition process (annotated) was not viable because of the different sampling rates and the different system noise levels. Thereby, we had only three options to proceed: (1) force the signal characteristics to match, (2) force the algorithm's control parameters to operate under this unnecessary condition, or (3) solve the

problem from the root and create an open electrocardiograph that would allow us to integrate a new standardized signal databank, in which problems like this could be eliminated. We chose the latter option because we believed it would have the greatest impact.

It is important to notice that, generally, the just-mentioned signal incompatibility problem appears in all types of physiological signals where the integration and scalability of algorithms are required to reach clinical levels of usability. This is currently a common problem whose solution is the availability, standardization, and compliance of hardware—a solution that cannot yet be found in academic resources.

In academia, the development of many acquisition systems for ECG signals has been published. Unfortunately, due to the widespread belief that circuit design is not a matter of science within some academic communities, none of the published works have enough design quality to be compliant and useful in clinical applications, like automatic interpretation procedures. Three of the best-published hardware architectures are [20–22], and none of them have the intention of developing diagnostic-grade equipment. In ref. [20], the authors developed the architecture for a Holter device with a sampling rate of 250 Hz, which, according to the IEC 60601-2-25 [23], is not useful for diagnostic applications since at least a minimum sampling rate of 500 Hz is required. Also, in this work, a system noise evaluation was not performed; therefore, it is not possible to conclude if the signals are further compliant in this aspect. In ref. [21], a basic single-channel circuit made with an instrumentation amplifier and an Arduino Uno board is presented. No Signal Integrity considerations were taken, nor was a signal quality evaluation performed, since the objective of the authors was to generate an animation for educational purposes. In ref. [22], even when some IEC compliance parameters were evaluated, the device still needs improvements to be useful in automatic interpretation procedures.

Table 1 summarizes, through a checklist, the characteristics required for an electrocardiograph to be useful in automatic interpretation procedures in an academic research environment. One of the special characteristics of this work is the availability of its design documentation through the project webpage, as this allows any research team to fabricate their own Kenshin electrocardiograph with minimal effort, assembling it themselves or by hiring an electronics assembly house. This availability can help to spread this device within the academic community, and this dissemination is what can ultimately contribute to ECG signal standardization. The design documentation is particularly useful because it eases fabrication, avoiding redundant work in electronics design and also lowering production costs.

Table 1. Characteristics that an electrocardiograph should comply with to be useful in academic signal processing research.

Designer/Manufacturer	Open-Source Hardware	Design Documentation Availability	Compliant Signals	12-Leads
Segura-Juarez et al. [20]	✓	×	×	×
Ojeda-Misses et al. [21]	✓	×	×	×
Moumtadi Fatima et al. [22]	✓	×	×	×
GE—MAC VU360 [24]	×	×	✓	✓
Philips—PageWriter TC70 [25]	×	×	✓	✓
Gordillo-Roblero et al. (this proposal)	✓	✓	✓	✓

According to IEC 60601-1-2-25 [23], sections 201.12.4.106.1 and 201.12.4.107.3, an ECG signal should comply with the following parameters:

- The skew between channels shall not be larger than 100 μ s.
- Signals shall be sampled with at least 500 samples/s per channel during data acquisition.
- Amplitude quantization shall be $\leq 5 \mu$ V/LSB.
- The noise level shall not exceed 30 μ V peak-to-valley.

Compliance with these signal parameters was used to validate the performance of our design methodology. Additionally, other essential performance requirements specified in Section 201.4.3.101 of [23], such as defibrillation protection, electrical safety, filters,

electrostatic discharge, conducted disturbances, and electrosurgery interference protection, should be considered during the design of an IEC-compliant electrocardiograph.

3. Methodology

Acquisition systems for physiological signals in the medical field share one similarity: they acquire biopotentials in the range of microvolts and deliver a digital signal via high-speed communications for further processing. However, due to their nature, each type of physiological signal has different hardware requirements and different compliance requirements. Nevertheless, they still can be classified as mixed-signal boards, therefore having the same electronics design considerations. It is worth mentioning that this is not a study whose objective is to collect data for analysis; therefore, a research design (as a structured plan) may not be outlined. Instead, this document describes a design methodology whose objective is to detail (through a case study) the process of creating a solution—an electrocardiograph that can contribute to solving the problem of ECG signal standardization. This solution will later be validated through applicable IEC parameters.

In academia, the main objective of any work is to solve a scientific problem. Once the scientific problem is defined (the signal incompatibility problem described in Section 2) the design of the electrocardiograph can begin. This device should be a fully compliant, diagnostic-grade device because we want to use it for automatic interpretation procedures in clinical practice. Keeping the scientific problem that we need to solve in mind is of utmost importance, as is having a personal awareness of what we are doing, why we are doing it, and how we plan to do it. The first will help us to visualize the product we want to build, and the latter will provide us with the motivation required. As soon as we can imagine the finished product, the first immediate step is to find out the standards and norms that apply to our device and, from here, to define a list of technical requirements: mechanical, electrical, and for data processing. Later, we must acknowledge whether we have the necessary skills and tools to successfully perform the task.

Nowadays, electronics design is not as easy as interconnecting components on a printed circuit board (PCB). Due to the rise of clock frequencies and the lowering of digital levels, many digital engineers now need to think as if they were analog designers working with radio signals, which is the right thing to do. In addition, modern electronics are subject to a series of legal EMC (Electromagnetic Compatibility) requirements that must be fulfilled in order to put any product on the market. European regulations subject virtually all electronic devices to these laws, and even though American regulations have a few exceptions, maintaining good design practices in all cases is desirable. For medical devices, the FCC (Federal Communications Commission) does not have any mandatory EMC standards (Section 1.5.6 of ref. [1]), but the IEC-60601-1-2 [26] (International Electrotechnical Commission) has effectively become the worldwide de facto standard, making an IEC approval certificate a must for marketing an electrocardiograph. Local standards and local sanitary regulations also need to be considered.

Aside from the EMC legal requirements, the fact that physiological signals are commonly 1 mV in amplitude highlights another important consideration during the design process, namely Signal Integrity. EMC and Signal Integrity are closely related topics; the difference is that Signal Integrity becomes an unofficial, self-validated test. This means that an electrocardiograph can obtain an EMC certificate by keeping radiation low. However, if it delivers polluted signals, it renders the electrocardiograph unusable.

EMC and Signal Integrity (SI) requirements are usually met by implementing proper design techniques. The study of electromagnetic theory plays an important role in this because it not only helps in analyzing information found on Internet forums, and in separating facts from inaccuracies, but more importantly, because we, as designers, are required to understand the reasons behind some well-proven rules of thumb. This is noteworthy because mathematically analyzing circuit radiation during the design process is impractical (Section 1.5.6 of ref. [1]), and Electromagnetic Interference (EMI) simulation is only practical in specific cases. Circuit designers need to be aware of radiation or susceptibility dangers.

Placing components and routes in certain configurations can unintentionally cause a circuit to act like an antenna, making it inadvertently receive or produce unwanted levels of radiation.

Each printed circuit board has special considerations that depend on the nature of its application. For example, these considerations may vary if high-speed communications like USB (Universal Serial Bus) are required, if RF (Radio Frequency) communications are needed, if a motor control circuit is being designed, or if a circuit for acquiring biopotentials is being designed. Different considerations should be taken into account for each combination of cases, and sticking to the IPC standards for manufacturing and PCB design is recommended. In this case study, we are dealing with a mixed-signal board. This board takes highly sensitive analog signals as inputs and provides high-speed digital communications as output.

Now that we have at least mentioned the basic design concepts, it is important to understand that electronics design is not a linear process. A “general-to-specific approach” first requires imagining an original, finished product. As we go deeper into details, new design knowledge gets used as feedback to improve the original design, and we continue repeating these iterations until we are satisfied and ready to manufacture. This does not mean we have to manufacture many devices before being ready for mass production; feedback should ideally be provided during the design process.

In general, electronics design is a process that demands high levels of knowledge. It requires a solid background in electronics and electromagnetic theory. It requires knowledge of the norms, standards, and regulations, and it even requires some techniques and additional knowledge that can sometimes only be acquired through experience. The more knowledge we have, the better designers we can be. The design methodology for our case study is shown in Figure 1, and it can be described as follows.

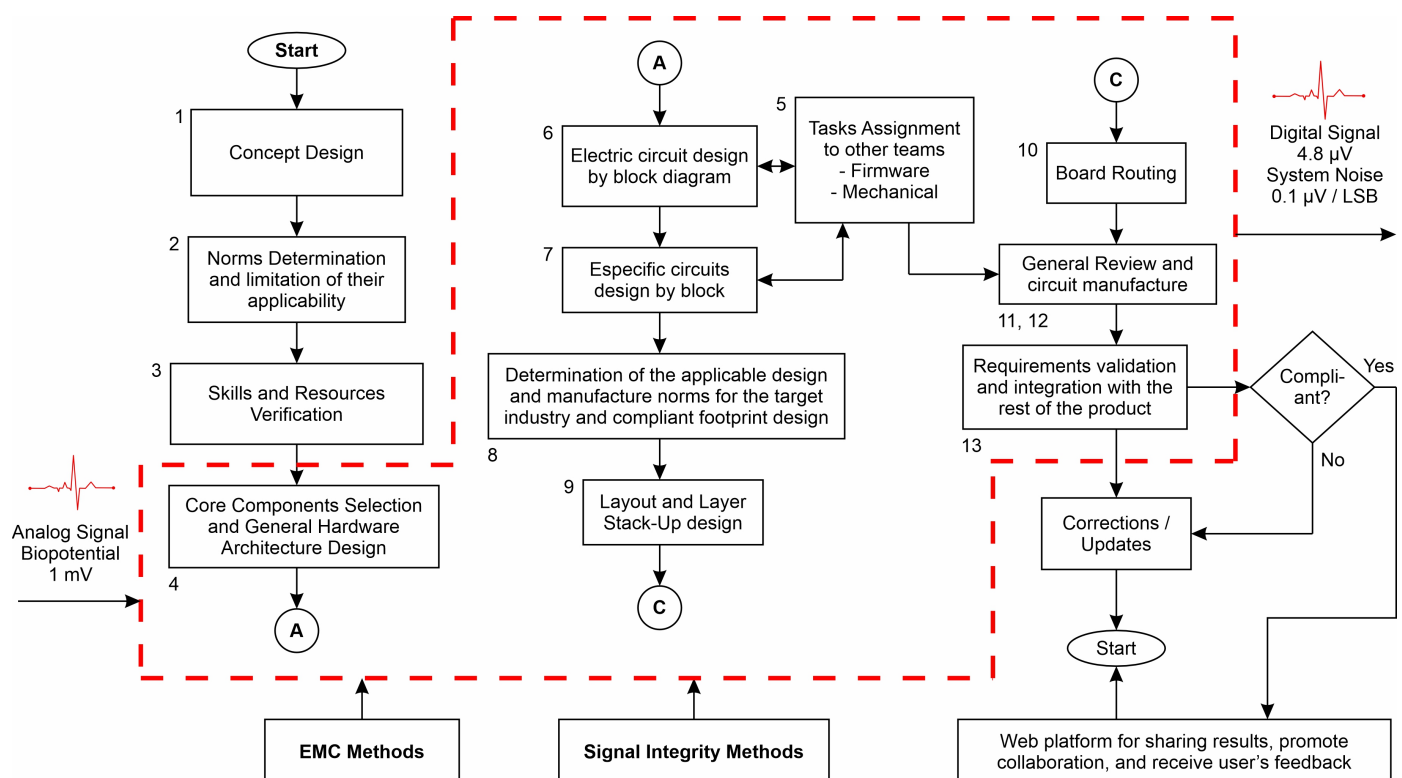


Figure 1. Design Methodology Block Diagram—Signal Integrity and EMC are concepts that are considered throughout the entire design process, from schematic design to PCB design. Each block number in the figure is explained in the list item of the same number.

1. Clearly define a preliminary version of the finished product. This will allow us to define an initial set of technical specifications, which can be mechanical, electrical, or for data processing. This preliminary version will allow us to discover which norms and standards may apply to our new product.

For our study case:

We want to design an electrocardiograph that is a simple, low-cost device with USB connectivity and provides the best signal quality. This device is meant to acquire signals that will be used to create a new signals databank in an academic environment, i.e., for research purposes. The preliminary version of our finished device is shown in Figure 2.

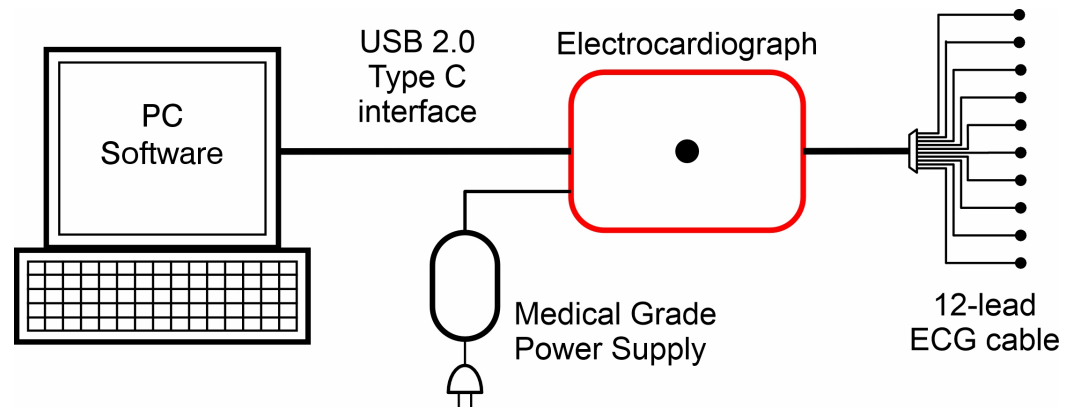


Figure 2. Design concept for the Kenshin device.

2. Now that we have defined what we want to achieve in general terms, we can determine the applicable norms, standards, and legal regulations that apply. The enormous task of reading and understanding these carefully is crucial, since no product can reach the market without being compliant. The new device design must be in accordance with all applicable requirements before proceeding; otherwise, product development will be an obvious waste of time and resources. At this stage, it is important to define and consider the Technology Readiness Level (TRL) [27] desired in the current design iteration, as this assessment may help to save resources.

For our study case:

We are developing a clinical-grade electrocardiograph with USB connectivity. Our goal is to introduce it into clinical practice, although it will initially be used exclusively in academic research environments. Academic labs are expected to collect the data for conducting the necessary research, paving the way for the device's eventual readiness for public use. Acknowledging this scenario, we can set the TRL to level 4, for now.

The applicable norms for a commercial electrocardiograph are the IEC 60601-1 [28], IEC 60601-2-25 [23], IEC 60601-1-2 [26], ANSI/AAMI EC11 [29], and ANSI/AAMI EC53 [30]. Fortunately, all of them are summarized in the IEC series. Additionally, to qualify for the USB-IF logo, we are required to comply with the USB Type-C Functional Test Specification and the USB 2.0 Electrical Test Specification. However, as we are planning to reach a TRL-4, our focus is now on designing the circuitry to comply with the following norm requirements that apply to signal quality only:

- Acquisition of IEC 60601-2-25-compliant signals; this is no more than 30 μV of system noise, at least 5 μV of amplitude resolution, at least 500 samples/s, and a skew between channels of less than 100 μs .
- Proper functioning of USB communications.
- Compliance with USB power requirements.
- To have defibrillator protection and Electrosurgical Interference Suppression (ESIS) circuits.

At this stage of development, we can save some resources by disregarding certain norm requirements and still achieve a fully functional device. For example, at this TRL-

4 level, we do not have to invest in the development of a fully compliant enclosure or medical-grade power cords as stated in ref. [28], nor do we need an embedded printer or display. Although this electrocardiograph will initially be used in academic research environments, it is important to design the electronic circuitry in accordance with IEC requirements to facilitate its eventual transition into clinical practice.

Before proceeding with the hardware design, it is important to be aware that electrocardiographs are complex machines that require specialized hardware, dozens of algorithms for basic functionality, and even more for automatic interpretation capabilities. Based on the problem definition previously stated, the main objective of developing this new product is to provide the academic community with an open hardware device for integrating a new standardized databank. Therefore, we limit the current design iteration to acquiring signals and ensuring these signals are compliant. For now, we are not planning to integrate algorithms for basic clinical use or automatic interpretation functionality; therefore, standards applied to medical software were not considered.

3. Now that the technical requirements needed to develop a commercial-grade device are known, and the limitations for the current design iteration are identified, we have to determine if we have the necessary skills to develop our target device. If not, we need to acquire these skills, integrate new members into the team, or simply stop the new product development. Proceeding without the required skills is definitely not recommended because they are necessary for identifying potential mistakes and evaluating results. Equally important is to check the availability of the required manufacturing technology and financial resources.

For our study case:

The most critical areas of knowledge for our design are Signal Integrity and design techniques for EMC compatibility, aside from all the applicable norms, of course. Without knowing EMC or SI design techniques, it is better not to continue. These books [1,31] provide the PCB design techniques needed to design a device that will pass the EMC regulations tests of IEC 60601-1-2 and the signal quality requirements of IEC 60601-2-25. It is important to read the norms carefully, highlighting all that might apply to our device, not only for this current iteration (TRL-4) but for the commercial version as well. All of this knowledge should be fresh in our minds during the design process.

4. Next comes selecting the core electronic components, accessories, materials, and basic mechanical requirements. These are the cornerstones on which we are going to start building the circuit, beginning with designing a general hardware architecture.

For our study case:

For data processing and communications, we selected the affordable PIC32MZ2048EF M064 [32] microcontroller from Microchip Technologies, Inc. (Chandler, AZ, USA). This microcontroller has an integrated USB 2.0 High-Speed peripheral, including the PHY layer for High-Speed. It is easy to program, the IDE (Integrated Development Environment) is provided free of charge, an evaluation board is available for its PIC family, and there are non-BGA packages available, which facilitates rework. Finally, its programmer (the PICKit™ series) is low-cost.

For signal acquisition, we considered three different options: a set of instrumentation amplifiers, and two Analog-Front-End (AFE) solutions, one from Analog Devices, Inc. (Wilmington, MA, USA) [33] and the other from Texas Instruments, Inc. (Dallas, TX, USA) [34]. We chose the ADAS1000 [33] from Analog Devices because of its configuration flexibility and because its datasheet explicitly states compliance with a wider range of standards, specifically IEC 60601-2-25 and AAMI EC38 [35], which deal specifically with diagnostic devices and ambulatory applications, respectively.

For the enclosure, despite the IEC specification for Ingress Protection (IP) and other requirements, we decided to work with 3D-printed materials, since, for now, we still want to keep the electrocardiograph within academic communities. For power management, linear regulators specifically designed for analog applications are leading the list. We

chose the ECG cable to be a standard DB-15 because it is used by a wider spectrum of manufacturers. Our electrocardiograph will also include a set of reusable electrodes for pediatric and adult use. The general hardware architecture designed for the selected core components is shown in Figure 3.

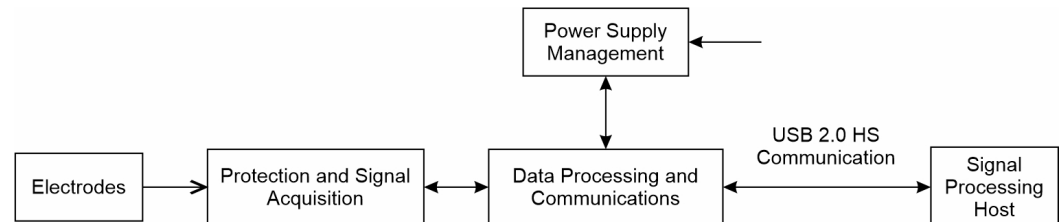


Figure 3. General hardware architecture.

5. With the cornerstones defined, we can now outline a set of guidelines so that the different involved teams can begin to work. For example, we can now approximate the size of the board so that the mechanical team can work on the enclosure styling. From the datasheets of the selected components, we can determine the exact communications and data processing structures required, so that the firmware engineers can start developing something concrete with the help of a development board (if available). Since the PCB is a mechanical component too, continuous communication between the mechanical engineer and the PCB designer will be required. Often, an experienced electronics design engineer can propose an accurate board size so that the mechanical team can work simultaneously. The same applies to firmware; an experienced electrical designer can suggest guidelines so that the firmware team does not get delayed. In general, continuous communication in all stages of the design process is required between the different design teams.

For our study case:

Designing a diagnostic-grade, 12-lead electrocardiograph requires two ADAS1000 integrated circuits. The ADAS1000 datasheet makes it clear that using two of them in a master/slave configuration means we will require three SPI interfaces for data acquisition, plus one USB 2.0 High-Speed peripheral for communications. Also, from the ADAS1000 datasheet, we can define the data frame structures required for the SPI interfaces, which provides the firmware team with enough information to start developing a functional program. Aside from this, now that we know the IC package sizes, the amount of auxiliary circuits, and other mechanical requirements (like battery compartments, indicators, or audible alarm locations), we can define a mechanical layout and a PCB size. With this information defined, the mechanical team can start styling the enclosure to make it attractive.

6. With the firmware and mechanical requirements defined and the core components selected, we can start working on what is really the subject of this article: electronics design. We start by drawing a block diagram of the required circuitry and then go into the specifics of each block.

For our study case:

Once the core components are defined and different tasks have been assigned, we can start drawing a block diagram of the circuitry needed from the general hardware architecture (Figure 3). This new block diagram, shown in Figure 4, will eventually become the circuit schematic from which the PCB will be built.

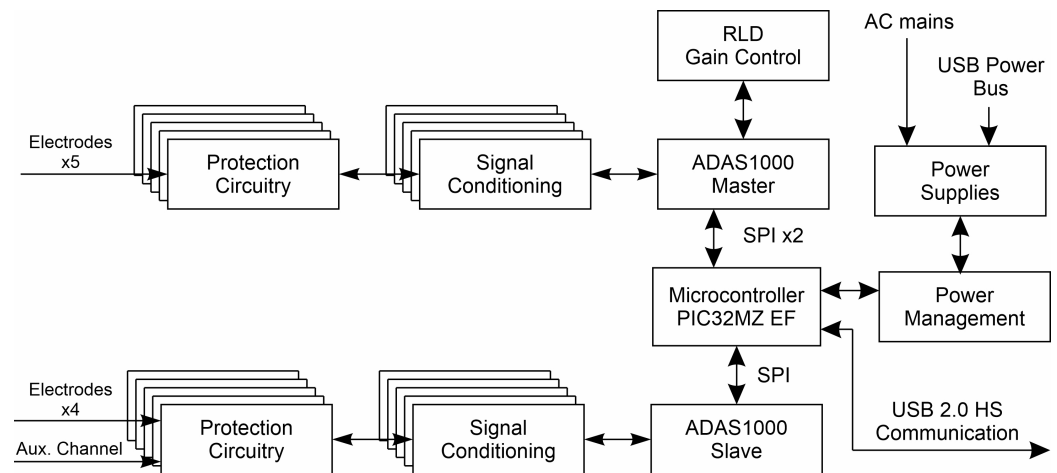


Figure 4. Circuit block diagram.

7. Now, we focus on a single block at a time. Based on the regulations previously identified, we will design the actual electrical circuit for each block. Our job as designers is to choose the highest quality components possible for the device, trading between performance, price, and availability.

For our study case:

The following subsections, 7a to 7j, detail the circuits designed for each block of Figure 4.

- (a) Board power supplies—This board can be powered from two different sources. One is an external Class II medical-grade power supply (CON2), for compliance with IEC 60601-1 regarding Means of Patient Protection. The other power supply comes from the USB port, needed to comply with the USB Type-C requirement that any device should be able to be enumerated by the host even when no external supply is present. This second power supply uses the USB connector (CON5), which is part of the USB circuit. These two power supply entries are shown in Figure 5. Please take into consideration that the complete schematic diagram and the Bill of Materials (BOM) detailing all part numbers can be downloaded from https://kenshin-ai.org/e_ht-01/ (accessed on 23 October 2024) for a clearer reference.
- (b) Power management—From the USB 2.0 Type-C specification, we know that once a device is connected to a USB host, the device can only draw a maximum of 100 mA until it gets enumerated. Once enumerated, the host can deliver up to 500 mA to the device. Moreover, for any USB device, the maximum capacitance allowed for direct-connect is 10 μ F. Based on these requirements, we need to set control circuitry for charging the bulk capacitors needed on the board.

For a mixed-signal circuit like this electrocardiograph, it is of utmost importance to supply the analog circuitry with the cleanest source possible. For this reason, for the ADAS1000 ICs, we chose linear regulators specially designed for RF and analog applications. The ADAS1000s (the master and the slave), as they are mixed-signal ICs, require two regulators: one to supply their digital circuitry side and the other to supply their analog circuitry side. For both sides, we chose regulators from the same series, offering the same performance but with different voltage output levels (U10 and U1; see Figure 6). For the microcontroller, we chose a linear regulator with a higher current capacity (U2). Pi filters for EMI rejection were considered for all three linear regulators.

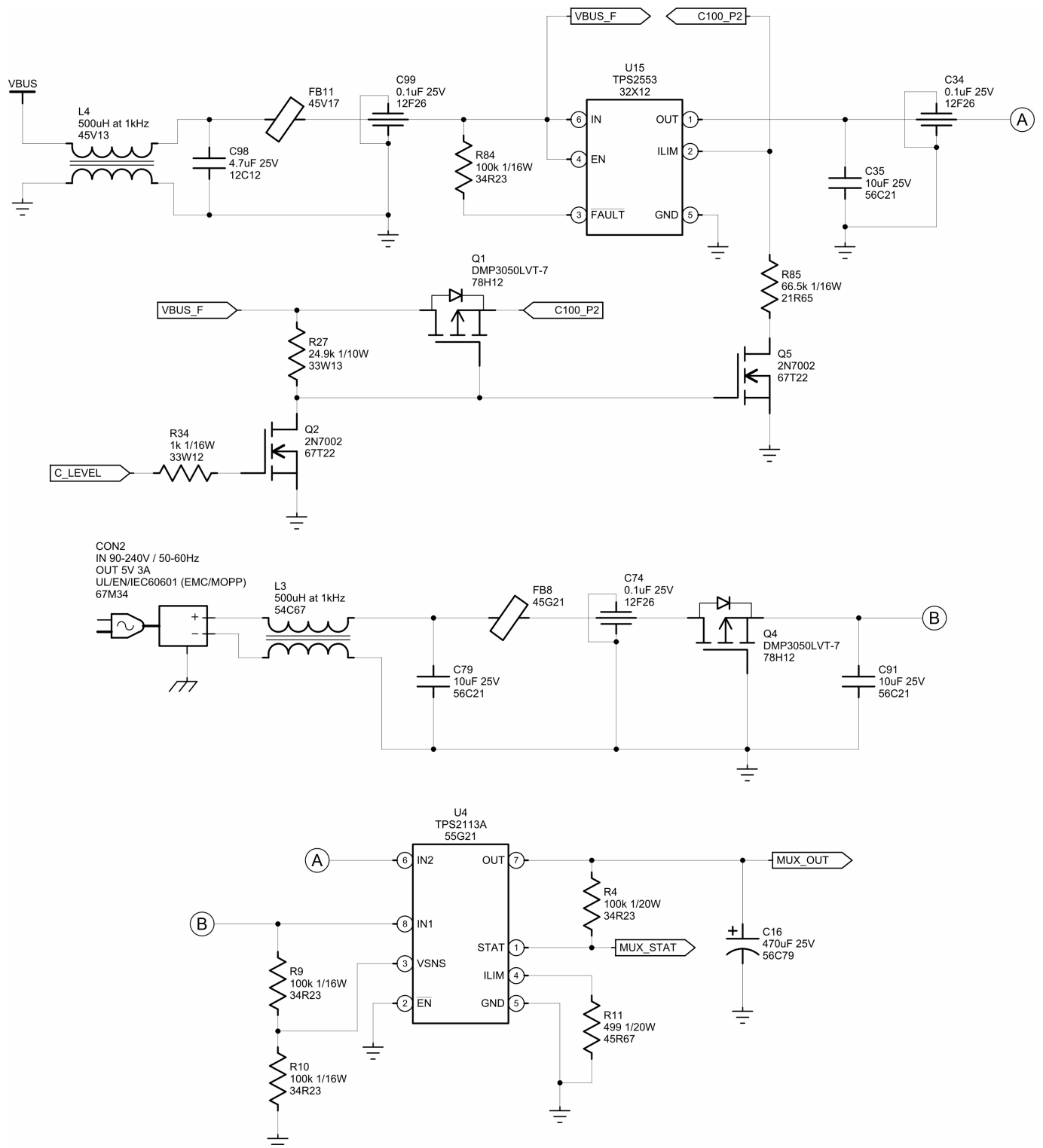


Figure 5. Power supply entry circuit.

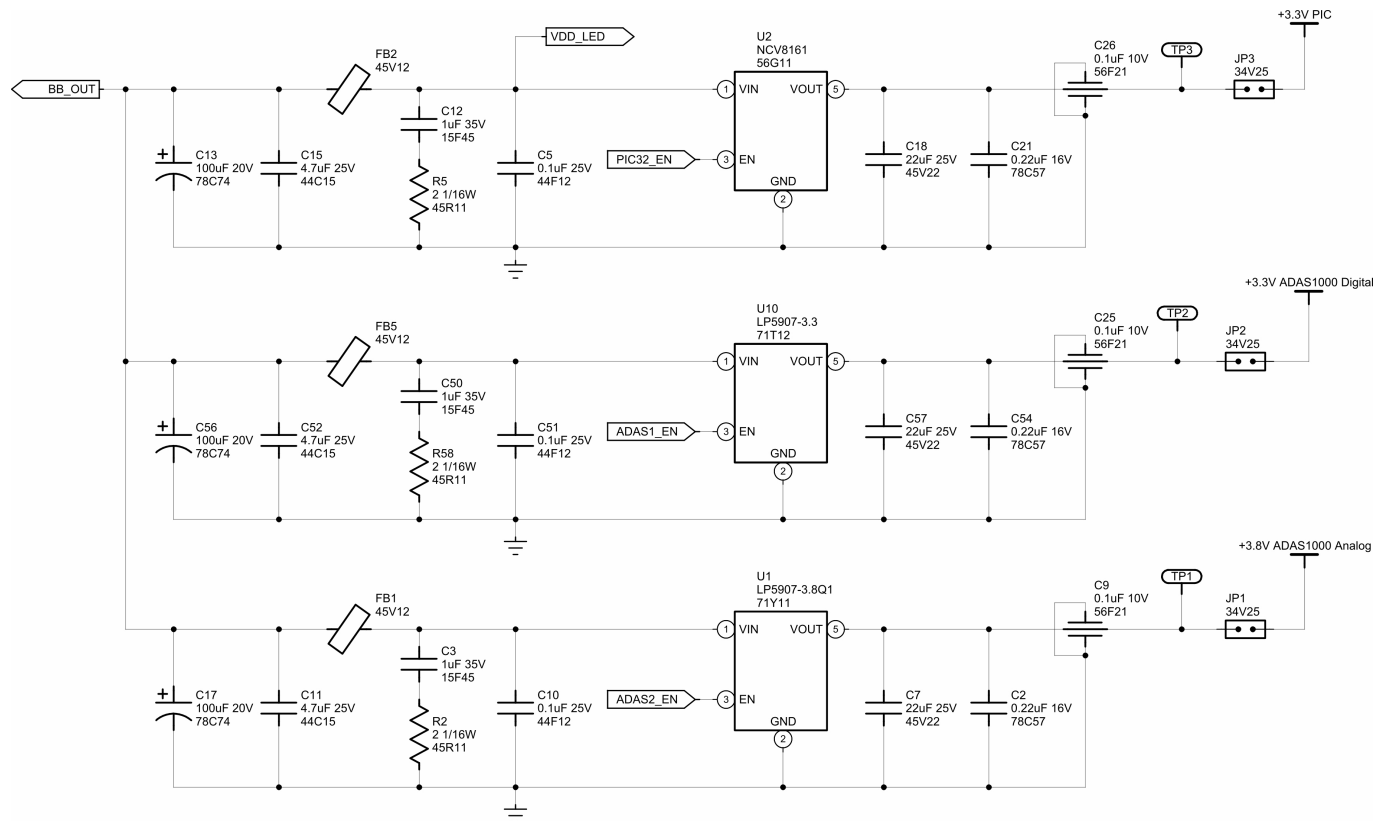


Figure 6. Board's linear regulators.

Figures 5–7 illustrate a part of the board's power management circuit, from the power entry connectors to the power multiplexer (U4) that automatically selects the power source. These circuits start with their respective power supply connectors (CON2 and CON5), and each power chain immediately goes through a choke coil (L4 and L3) and then through pi filters to improve EMI rejection.

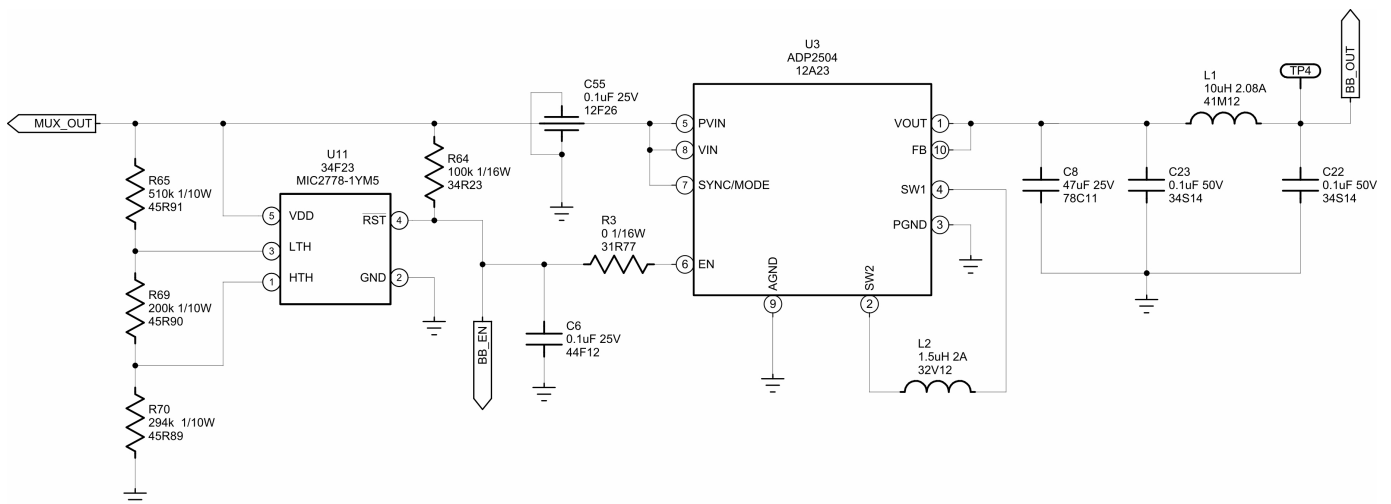


Figure 7. Buck-boost DC-to-DC converter.

The power coming from CON5 (VBUS) goes through a current limiter (U15) that keeps the current below 100 mA. This current limiter is configurable. According to its datasheet, the ILIM pin has to be tied to VDD to operate below 100 mA, and placing a resistor of approximately 66.5 k from ILIM to the ground changes the current limit to remain below 500 mA. We used a set of low RDSon MOSFETs to control this configuration. The gate of Q2

is connected to a microcontroller output pin that is configured as open-drain. The reason for making it open-drain is to ensure the current limiter operates below 100 mA when the system is powered up. The microcontroller program can later decide which current limit to use. It is important to recall that USB devices are “plug and play”, meaning that the enumeration process can occur at any time. For the power chain coming from the barrel connector (CON2), there is only a P-MOSFET for polarity protection (Q4), and a small bulk ceramic capacitor (C91) is placed before reaching the power multiplexer. The output multiplexer (U4) is configured to automatically give priority to the external power source.

At the multiplexer (U4) output, we placed an electrolytic bulk capacitor (C16) intended to service the whole board. This capacitor gets charged through the power multiplexer’s built-in current limiter (1 A), so its inrush current is controlled.

The power chain continues in Figure 7. For the C16 capacitor, we added a voltage monitor (U11) whose function is to deliver a digital high output on its $\overline{RST}$ pin when the voltage in C16 reaches 4.5 V. This signal is used to control the enable pin in the next step of the chain, a buck-boost converter (U3). The purpose of this buck-boost converter is to improve the PSRR (Power Supply Rejection Ratio) for the linear regulators; it feeds the regulators a constant 5V output, regardless of voltage fluctuations coming from the USB port or the external power supply.

The buck-boost converter has a programmed ramping power-up feature that helps limit the inrush current for charging the C13, C56, and C17 capacitors; these capacitors are shown in Figure 6. To pass EMC regulations, the capacitors’ inrush current must be limited. If inrush current is not controlled, it can reach excessive levels, causing power rail instability, circuit radiation, and shortening the capacitor lifespan.

The linear regulators shown in Figure 6 (U2, U10, U1) are in parallel, and they have their own voltage monitor (U9, please refer to the complete schematic). The purpose of this voltage monitor is to power up the microcontroller until the C13, C56, and C17 capacitors reach 4.5 V. Then, once the microcontroller program starts execution and the USB device is enumerated, the host computer software, or the microcontroller itself, can control the enable pins of the two ADAS1000 regulators.

- (c) Microcontroller programmer interface—The interface used to program the microcontroller is the ICSP (in-circuit serial programming), which is proprietary to Microchip. We improved the circuit diagram that Microchip provides in its commercial documentation in order to enhance EMC. For example, we know that to provoke a Master Reset in the microcontroller, we need to drive pin 9 in U6 (Figure 8) low. Normally, pin 9 is pulled up through a single resistor and driven low by the programmer or a microswitch. For EMC, we need to limit the charge/discharge current in C93; therefore, we used two resistors, R87 and R89. The circuit charges the capacitor through R87, limiting circuit radiation. The resistor, in series with R87 and R89, reduces the quiescent current for the /MCLR pin. We did not merge R87 and R89 in order to reduce the charging time of C93 while maintaining a low quiescent current and providing EMI immunity through C93.

If provoking a microcontroller reset by pushing the microswitch, C93 will start to discharge through another resistor, R83, which is in series with the microswitch. R83 is a low-value resistor, but it helps limit the discharging current while providing an acceptable digital low level for the MCLR pin. ESD protection was also added with the help of the TPD3E001 (U13), which is a set of low-capacitance TVSs designed for high-speed data applications. This ESD protection is the same model as the one used for the USB bus (U8, Figure 8), thereby minimizing the number of different components and keeping the cost of the board assembly low.

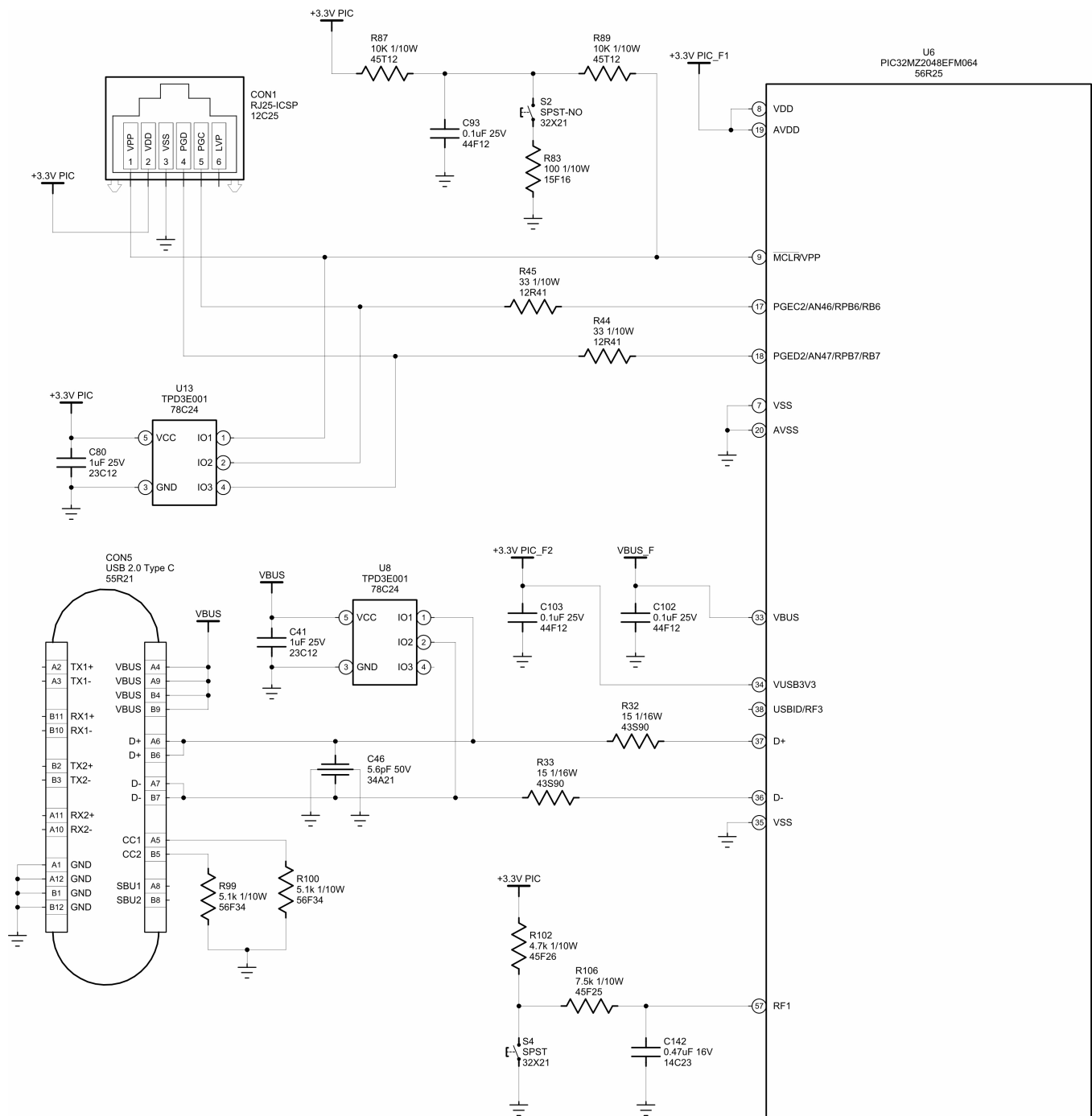


Figure 8. Programmer circuit, USB peripheral, and user switch.

- (d) **USB peripheral**—Electrically, the Universal Serial Bus (USB) is not so complex; it is just a couple of wires that operate in differential mode with controlled impedance. The circuit implemented in this electrocardiograph is shown in Figure 8. A filter for EMI is required, and it was implemented effectively using an X2Y capacitor (C46). Additionally, a pair of termination resistors were placed in case of signal reflection problems (R32 and R33).

For ESD protection, the TPD3E001 (U8) from Texas Instruments was used; this is an integrated circuit specifically designed for USB applications. The complex part of implementing USB communications is controlling the differential pair impedance on the PCB; this is part of the layout and layer stack-up planning. Therefore, in designing this

part of the circuit, all the considerations provided by Texas Instruments in their application note [36] were taken, and they will be explained in list item number 3.

- (e) User push buttons—The board has two user push buttons for general use; they are identical. One of them (S4) is shown in Figure 8. These circuits were designed for EMC as well. The resistors in these circuits were configured to control the charge/discharge currents of the bouncing capacitor (C142). The resistors prevent high currents from radiating out of the circuit, and the capacitor provides enhanced immunity to the microcontroller input pin.
- (f) User LEDs—There is a series of 10 LEDs on the board (R111–R118, R105, and R108), allowing it to display a 32-bit data word if eight LEDs are used to display an 8-bit byte, and the remaining two to indicate four different shifts. These LEDs can be used for any purpose required by the programmer. While designing this part of the circuit, special care was taken to avoid overloading the microcontroller's sink/source drivers. According to the microcontroller datasheet [32], the PIC32MZ family has different current drivers for different groups of pins. Their capacities run from 15 mA to 25 mA. As we are using pins from different drivers, we chose LED resistors that ensure, in the case of having the 10 LEDs in the on-state, the maximum current drawn is 21.5 mA. Please refer to the complete schematic diagram to see port distribution and circuits (https://kenshin-ai.org/e_ht-01/, accessed on 23 October 2024).
- (g) Defibrillator protection—This circuit was designed using a special solution from Maxim Integrated [37]. This integrated circuit has four specialty TVSs that cause minimal distortion to the ECG signal since they have very low capacitance (3pF). It has a quick response time (2 ns) and can withstand more than 100,000 defibrillator pulse discharges without failure. The schematic diagram for this circuit is shown in Figure 9. This specialty TVS diode (U12) differs from a standard ESD application in that, for ESD cases, the electrostatic energy can be driven and dissipated by the TVS itself. This is not the case for the MAX30034, which requires an auxiliary resistor (R74) to dissipate the high energy coming from the defibrillator. According to the application note [38], this resistor should be able to dissipate more than 20 W; therefore, we used a 25 W resistor to have a safety margin. A second resistor (R12) with pulse-withstanding capabilities should be placed in series to minimize the remaining energy that can reach the analog circuitry. In Figure 9, a single circuit is illustrated, but all electrodes should have this protection.

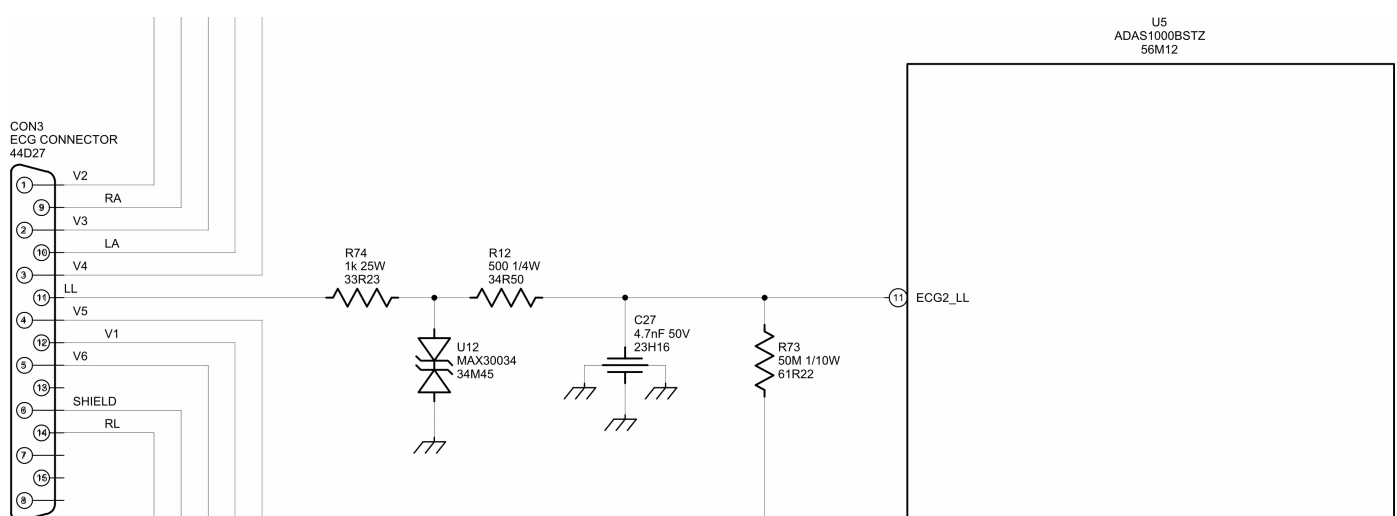


Figure 9. ECG channel protection circuitry (only one channel shown).

- (h) ESIS Filter—In Figure 9, an RC low-pass filter is formed by a single X2Y capacitor (C27) and the same resistors used for the defibrillator protections (R74 and R12). This low-pass filter was designed to have a cut-off frequency of 22.197 kHz, which is

high enough to avoid interference with the ECG signal's bandwidth and yet provide rejection to the electrosurgical interference, which is in the 100 kHz–5 MHz band. The energy sourced by electrosurgery equipment is also dissipated by the defibrillator protection circuitry.

- (i) **Analog Acquisition Circuitry**—The ADAS1000 integrated circuit (IC) is the analog core of this electrocardiograph. This IC greatly simplifies acquiring ECG signals. At the board level, the device routing is reduced to directly tie the ECG cable wires to the ADAS1000. All the necessary processing, such as lead formation and analog-to-digital conversion, is performed on-chip. Even auxiliary circuitry for filters, pacemaker detection algorithms, digital lead formation, and respiration signal acquisition are available on-chip.

To configure a 12-lead electrocardiograph, two ADAS1000 ICs are required; they should be synced in a master/slave configuration (see U5 and U7 on pages 2 and 3 of the complete schematic diagram). Syncing these devices (gang mode operation, according to their datasheet) only requires four wires; these signals are all generated by the master and passed to the slave. The first wire is used to pass a clock signal. The second wire is used to pass a conversion sync trigger to ensure both ICs start converting at the exact same time. The third wire is used to pass the common-mode analog signal to the slave, and the fourth is used to pass different test tones to facilitate calibration.

- (j) **SPI Interfaces**—All data acquired and/or processed by the two ADAS1000 ICs on the board is made available to the microcontroller through SPI interfaces; three SPI interfaces are required. Two are configured as slaves, and they are used to retrieve ECG data from both the master and the slave, one for each. The third SPI interface is configured as a master interface and is located on the master ADAS1000; this interface has a fixed sampling rate of 128 kHz and is used specifically for pacemaker detection. During the design process, the SPI interfaces were routed to be independent, i.e., we are not using the daisy-chain configuration common in this kind of interface. This allows data to be transmitted to the microcontroller faster while keeping the SPI clock low. This is achieved since data transmission practically occurs in parallel with the help of each peripheral's hardware. Termination resistors were considered for the three SPI interfaces, and test points were also provided.

The full schematic document can be downloaded from the project webpage (https://kenshin-ai.org/e_ht-01/, accessed on 23 October 2024).

8. Once the full schematic diagram has been drawn and all part numbers are fully defined (electrical design completed), we proceed to draw all the necessary footprints for the PCB. Taking the IPC standards for the target industry into consideration, as well as Design For Manufacturability (DFM), is highly recommended.

For our study case:

For footprint design, the following standards apply: IPC-7352 [39], IPC-7351B [40], IPC J-STD-001 [41], and IEC 61188-7 [42]. Fortunately, the design process can be simplified by the use of compliant tools like Footprint Expert [43] from PCBLibraries, Inc. For medical equipment, IPC also has the IPC-6012EM [44], which is an addendum that contains qualifications and performance specifications for rigid printed boards in the medical segment of the electronics industry.

9. Now, we have all the necessary footprints. Before proceeding to routing, we need to define a board layout. This is of utmost importance because success in passing the EMC tests described in IEC 60601-1-2 completely depends on this planning. The board layout also determines the quality of our signals, i.e., Signal Integrity. Correctly planning a layout requires proper knowledge about signal returns, grounding, shielding, transmission lines, etc. Fortunately, many books have been written on these topics; our best recommendations are *Signal Integrity* [31] by Eric Bogatin and *Electromagnetic Compatibility Engineering* [1] by Henry Ott. If Signal Integrity and EMC

are not taken into account from the beginning, there is little hope a design will work the first time [31].

For our study case:

The analysis for planning a good layout starts by determining the type of circuitry we have to route. For our electrocardiograph, we have low-level analog signals and high-speed digital communications; this is a mixed-signal circuit in which the low level of the analog signals makes them especially susceptible to digital noise and radiation. To avoid pollution of the analog signals, we need to confine the digital circuits and the digital high-speed communications to a limited area of the board. To achieve this, we need to make sure that all digital returns are within their corresponding areas.

For the power supply rails, we need to make sure we are not creating common impedance paths. If switching-mode power supplies are used, we need to enclose switching devices within the power supply area since they are very noisy digital circuits, especially if inductors are being used. Finally, for the analog circuitry, we have to ensure a clean ground and make sure that the ground level is maintained constant throughout the board. To achieve this, physical sections are created on the ground plane and then connected together through carefully placed bridges on the same ground plane. The intention is to prevent return currents from crossing sections while maintaining the ground level constant on the board. Digital clocks are usually buried between ground planes, and trace impedances are also plane-dependent. With these design rules in mind, we can start defining a board layout and, immediately after, the layer stack-up. If high currents are expected, we need to check the IPC recommendations for trace widths. The layout used in our case study is shown in Figure 10.

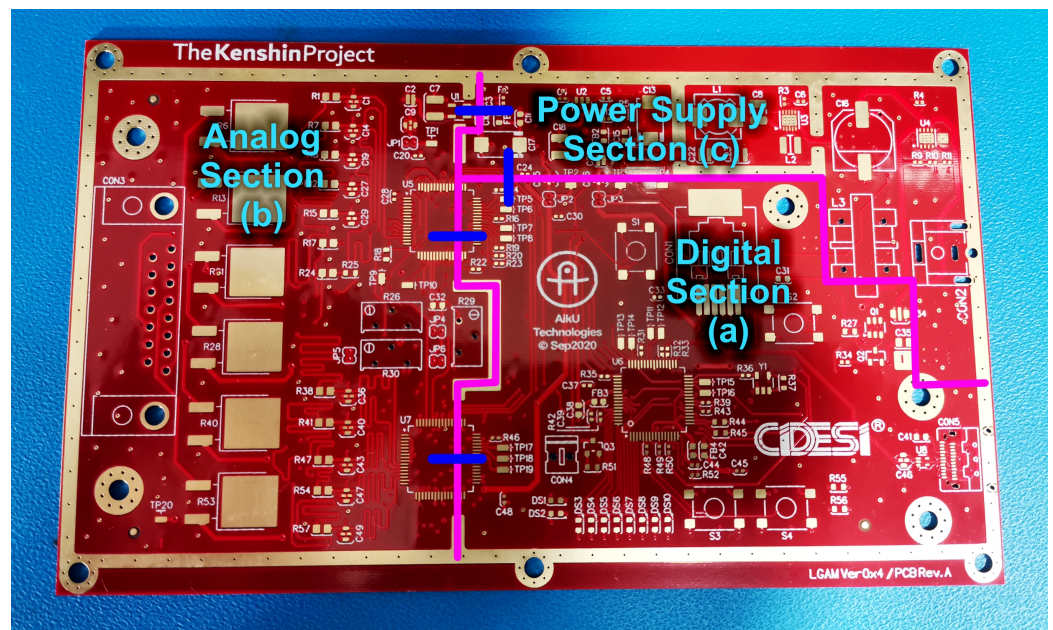


Figure 10. Board layout. In purple, the lines delimiting sections. In blue, the position of the ground bridges.

For the layer stack-up, we should analyze the kinds of signals that we have in the circuit and refer to any available application notes to see if there are special requirements. If application notes are not available, or no special requirements exist, we should use our criteria to route the signals as best as possible. For example, from a Texas Instruments application note [36,45], we know that the USB bus has to be routed with a controlled impedance of 90 ohms, in a differential-pair microstrip configuration. To meet this requirement, it is recommended to vary the trace width because, usually, a set of prefixed laminated structures is provided by PCB manufacturers at standard cost. Custom laminated structures

are available at a higher cost, but using the most cost-effective option is preferred. The multilayer laminated structure we use for our electrocardiograph is illustrated in Figure 11. The artwork assignment corresponds to the files that can be downloaded from the project webpage [46].

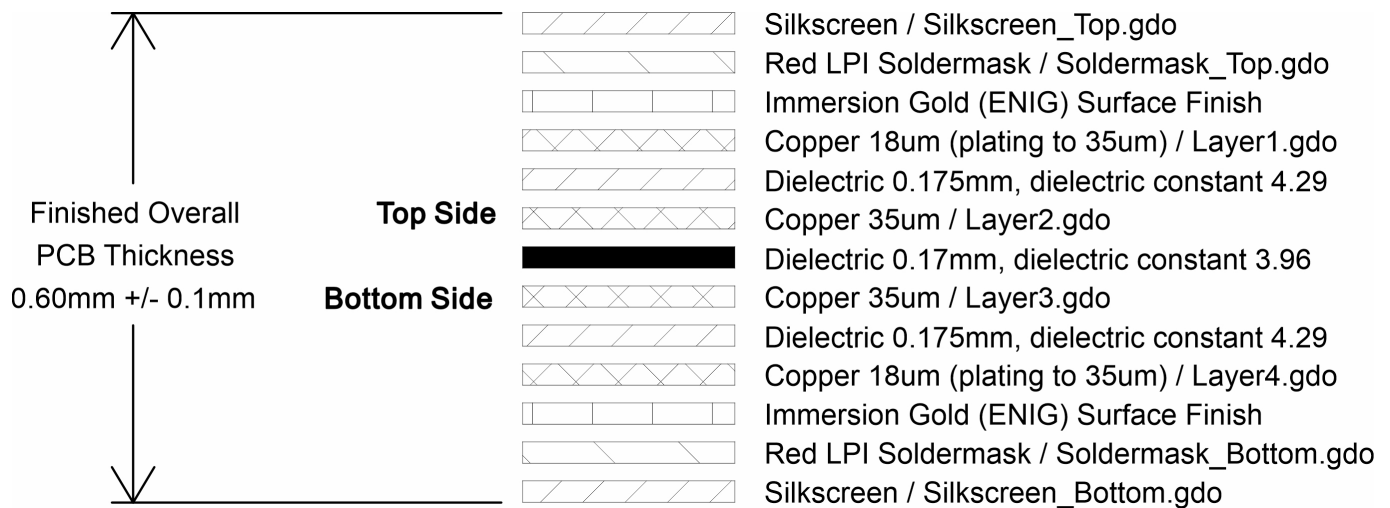


Figure 11. Four-layer laminated structure/artwork assignment for the Kenshin device.

We chose a 4-layer structure because, according to our experience and the topics explained in previous sections, this is enough for our design needs. As Mr. Henry W. Ott stated, a design team with considerable EMC expertise can create an acceptable design of a 4-layer PCB, whereas a less-experienced team would be better off designing a 6-layer PCB ([1], p. 635). After defining the laminated structure, the first immediate step is to designate a layer to be the general ground of the circuit; we chose layer 2. The ground sections and bridges are located in this layer.

To meet our EMC needs, we used different layer stack-ups in the various sections of the board. For the digital section, we used the layer stack-up illustrated in Figure 12a. This configuration is necessary to bury digital signals and clock signals between ground planes, preventing these signals from radiating outside of the board. For the analog section, the layer stack-up configuration is different. It is illustrated in Figure 12b. The purpose of this configuration is to provide a solid ground reference, tightly coupled to the signals coming from the ECG cable. We tried to prevent the ECG signals from changing layers because each via can create undesirable parasitic effects. For the power supply section, we used the configuration illustrated in Figure 12c. We defined two ground layers (2 and 3) and basically used layer 4 for the traces that cannot be easily routed from the components placed on layer 1, and vice versa.

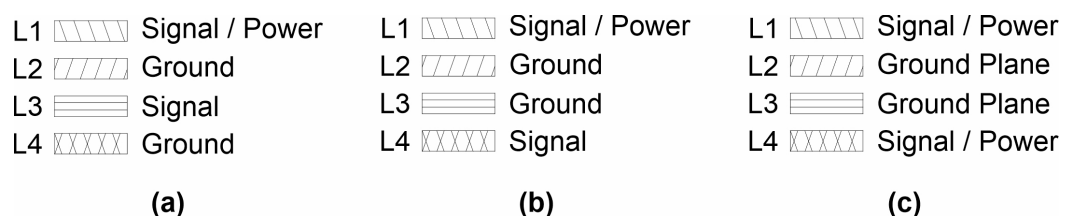


Figure 12. The different section layer stack-ups used in the Kenshin device: (a) Digital section. (b) Analog section. (c) Power supply section.

As part of the layout, an external ground plane placed under the circuit board was considered. The purpose of this plane is to provide shielding against electrical fields since we are not using a metallic enclosure. This external ground plane, illustrated in Figure 13, is a simple PCB with a HASL (Hot Air Solder Leveling) finish.

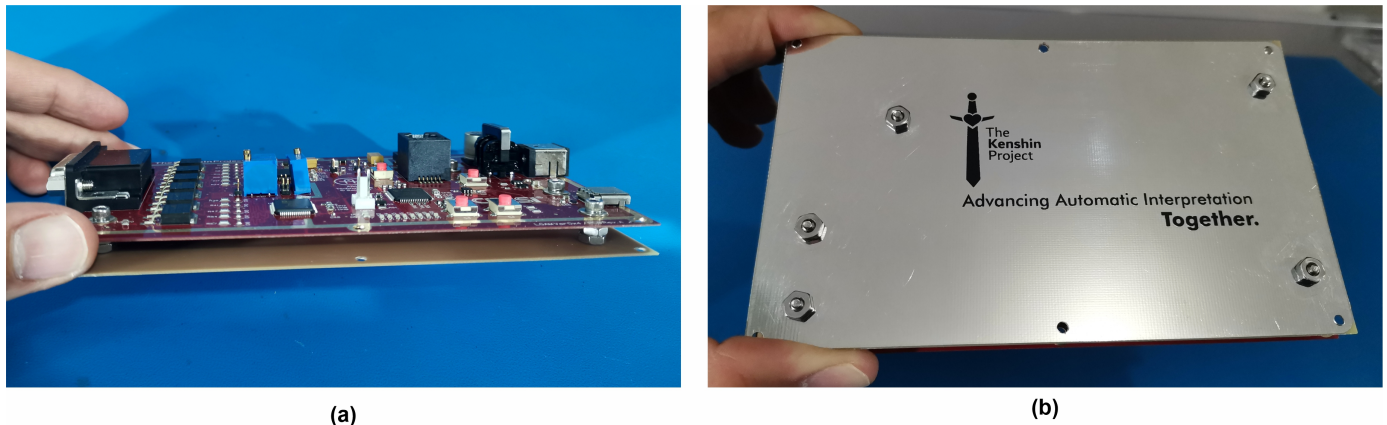


Figure 13. Shielding plane: (a) Front view. (b) Bottom view.

10. Once the layout is planned and the different layer stack-ups are defined for each section of the board, the next step is to route all the circuit connections according to EMC and SI considerations. For instance, if we need controlled impedance transmission lines, as is the case for the USB differential pair, now is the time to find a transmission line calculator [47] and at least understand the purpose of this requirement, as well as the electromagnetic theory behind this calculator. The same method applies to all digital traces where matching impedances is necessary in order to avoid signal reflections, such as SPI. Other EMC and SI considerations that are worth investigating further are crosstalk, length-matching for improving the Common-Mode Rejection Ratio (CMRR), techniques to reduce radiation and improve immunity, common impedance, decoupling and its capacitor placing techniques, etc.

For our study case:

Generally, the minimum trace width, clearance, and drill size we can use in our circuit depend on the PCB manufacturer and the price we are willing to pay. In our case, in which we have a controlled impedance differential pair in microstripline configuration (USB), the laminated structure of our PCB should already be chosen because the trace width and the space between the traces will depend on the height between the traces and the ground plane. For our electrocardiograph, in order to achieve a 90 ohm impedance, we had to use a trace width of 0.19 mm, spaced 0.16 mm from each other. This geometry depends on the characteristics of the laminated structure chosen and the nature of the differential protocol [48]. All the design parameters and the calculation results are illustrated in Figure 14.

In the full schematic document, it can be seen that termination resistors were placed in all SPI traces. This was performed to match impedances and help mitigate signal reflections. In general, all the mentioned topics should be studied by the designer in order to perform a good routing process. To avoid making this document more extensive, we invite the reader to download the design documentation where the PCB fabrication file (Gerber files), named according to Figure 11, is available. Some IPC standards are defined for the current capacity of traces. This board does not have high current requirements; therefore, avoiding common impedances is enough to prevent EMC problems.

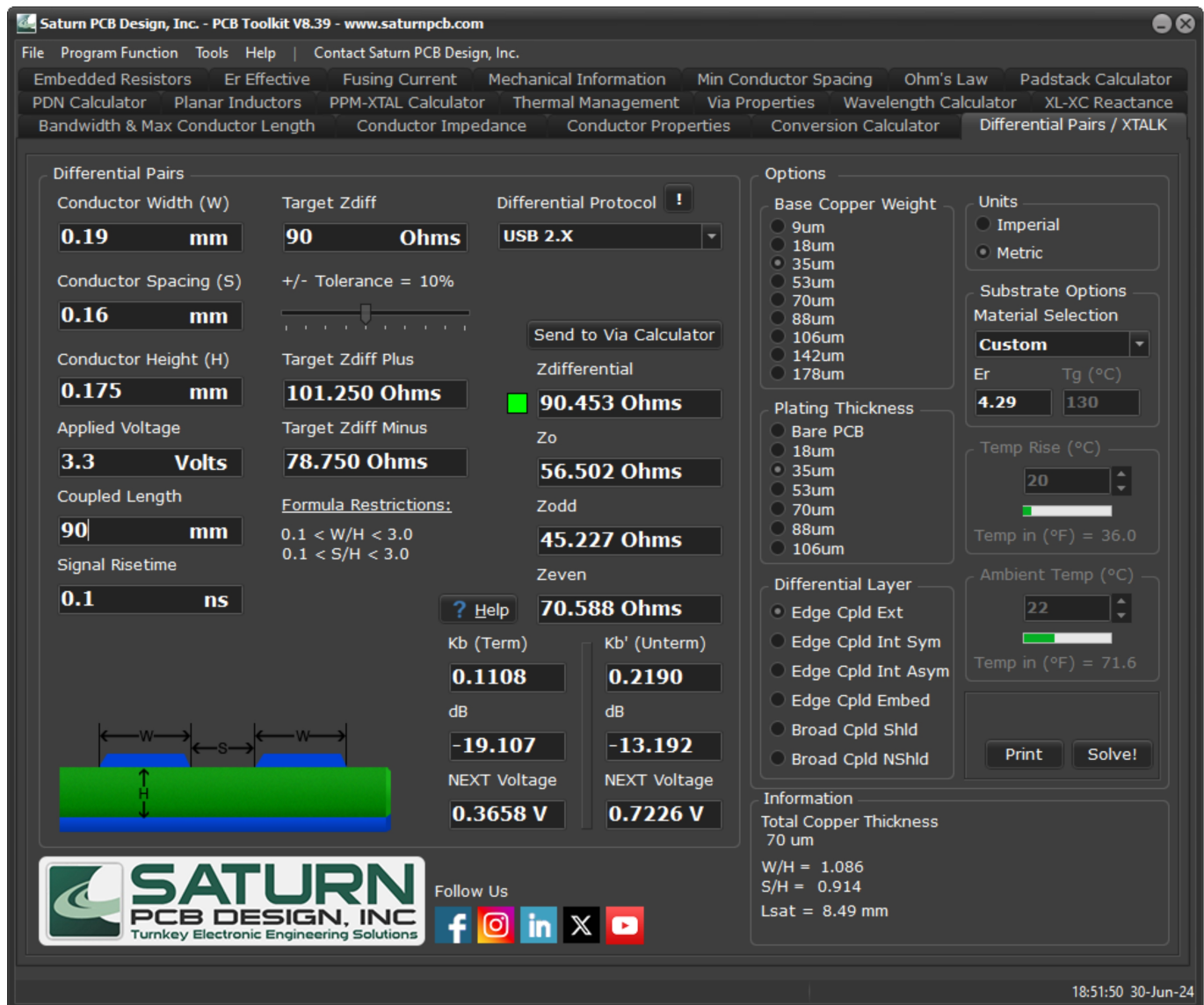


Figure 14. USB differential pair geometry calculation using software from SATURN PCB Design, Inc. [47].

11. Once the routing process is finished, an intensive review should be done. From the schematic design to the finished PCB, we need to check all the schematic symbols and their physical pin numbers in search of crossed relationships. We need to review the layout and the routing strategies used, and, if possible, we should schedule a review meeting with the other circuit designers, as well as the firmware and mechanical teams.

For our study case:

Designing an electrocardiograph is a complex task. In this circuit, we have 351 components and nearly one thousand connections; therefore, it is important to double-check every detail.

12. When revisions are complete, it is time to manufacture the prototype. It is a good design practice to generate all the necessary engineering drawings for our PCB before manufacturing.

For our study case:

The most common drawings for a printed circuit board are the fabrication drawing, the configuration drawing, and the assembly drawing. The fabrication drawing details the laminated structure of the board and all the necessary drill sizes. The configuration

drawing is used by the mechanical team to design the enclosure and is the reference for other mechanical requirements. Finally, the assembly drawing is used to assemble and debug the circuit. All the engineering drawings for our case study can be downloaded from the project webpage (<https://kenshin-ai.org>, accessed on 23 October 2024).

13. Validate the circuit and integrate it with the rest of the product.

For our study case:

Once our prototype is assembled, it is time to power it up. As stated before, designing an electrocardiograph is a complex task, and validating the circuit does not simply mean that everything in the schematic diagram matches what is manufactured on the circuit board. Validating the circuit means evaluating the functional performance through circuit functionality, EMC compliance, and signal quality.

It can sometimes be hard to make a circuit work the first time; therefore, when planning the device's development, budget and time should be allocated accordingly. Validating small parts of the circuit independently is sometimes desired. It is possible to work on the whole board while setting provisions to validate parts of the circuit independently as well. In both cases, saving resources is the intention. In our case, we tried to validate the circuit as a whole, and we had to fabricate the PCB twice due to small mechanical problems, such as footprint mismatches. Fortunately, the device was fully functional after the first assembly.

4. Results

The completed circuit board is shown in Figure 15.

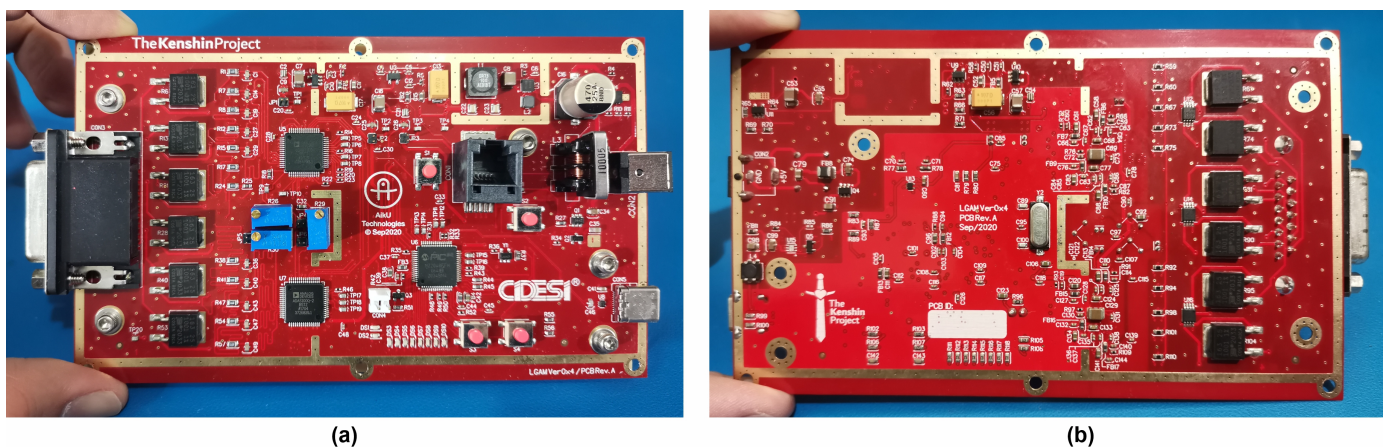


Figure 15. The Kenshin PCB: (a) Top side (b) Bottom side.

The circuit's general validation was conducted using test tones generated by the master ADAS1000 itself. In Figure 16, a square-wave test tone is presented. The LA electrode corresponds to the first electrode (in logic-processing order) of the master device, and the V3 electrode corresponds to the first logical electrode of the slave device. Being able to acquire these test tones means that most parts of the circuitry are operating properly. The SPI interfaces are functional, the USB communications are functional, both ADAS1000s (master and slave) are synced and working well, the power supplies are satisfactory, and the microcontroller program (firmware) is functional as well. This is a good beginning, but aside from evaluating whether the circuitry is functional, we also need to evaluate the signals' parameters mentioned in Section 2 in order to comply with the IEC 60601-2-25 standard [23] related to signal quality.

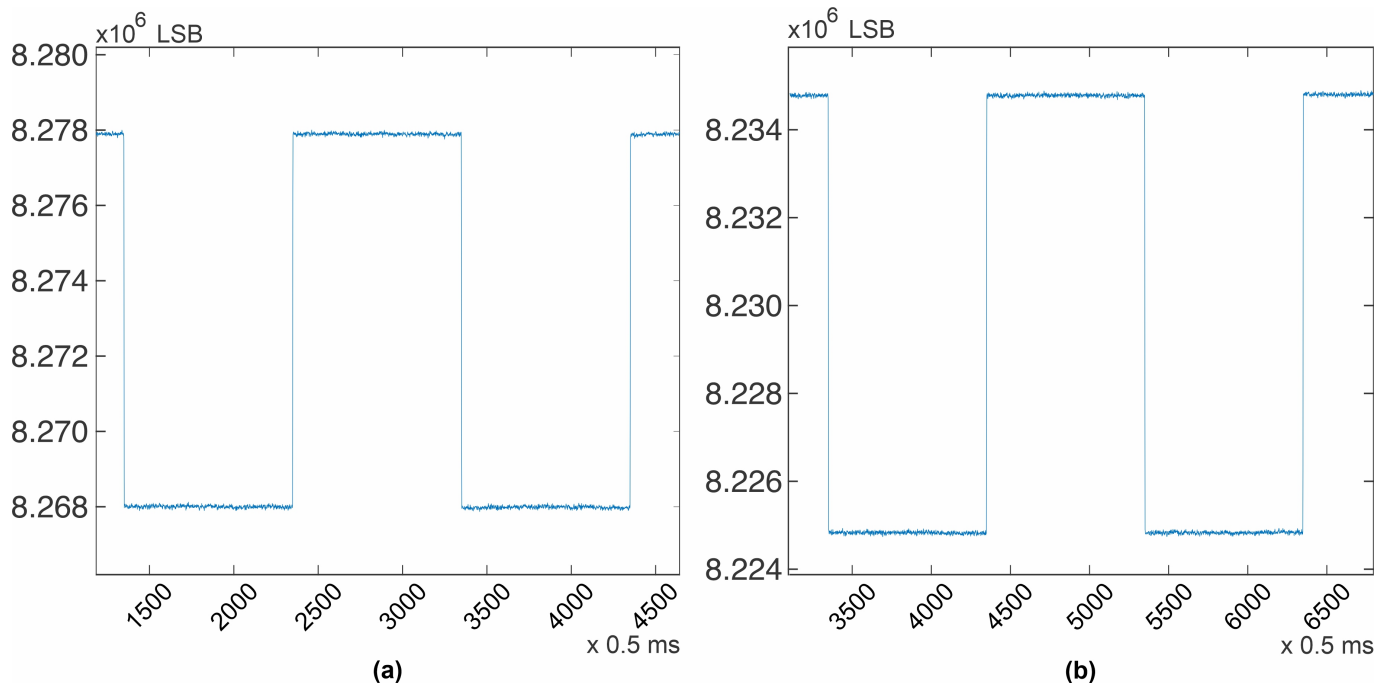


Figure 16. Test tone: 1 mV square wave, sampling rate 2 kHz; (a) LA electrode and (b) V3 electrode.

Indeed, the sampling rate of our electrocardiograph is greater than 500 samples/s. For measuring the system noise, which is the second parameter to evaluate, there are only two references available. The first reference is a patient simulator device, which, according to its manufacturer, can deliver a clean ECG signal of 1 mV peak-to-peak (p-p). The second reference is a test tone generator built into the ADAS1000 for calibration purposes, the same test tone shown in Figure 16. This test tone is also 1 mV p-p.

Using the patient simulator to estimate system noise is not viable because there is no way to differentiate the noise produced by the patient simulator from the noise generated by our electrocardiograph. Calculating system noise by superimposing a clean signal over an acquired signal (thus determining SNR—Signal-to-Noise Ratio) is not recommended because unknown offsets could be caused by the experimenter.

Therefore, the reference we considered the best for measuring the system noise was the square-wave 1 Hz test tone shown in Figure 16. We know from the datasheet that this signal is 1 mV in amplitude with a tolerance of $\pm 10\%$. However, we cannot physically measure the system's noise amplitude on this square-wave signal, even when there is a pin to make this signal available outside of the ADAS1000, because the measuring instrument would introduce unknown noise as well, due to the instrument circuitry and the cable probes. Considering all of this, we developed the following method:

1. We calculated the average level of the square wave at its high level and its low level (note that these are essentially DC levels, similar to an ECG baseline segment, and same as the test tone suggested in IEC 60601-2-25 for evaluating system noise). These average values are illustrated in Figure 17a.
2. The distance between the two average values (low level and high level) should be 1 mV, according to the ADAS1000 datasheet.
3. By dividing 1 mV by the number of LSBs (least-significant bits) between the two average values, which is 9.909029183×10^3 , we obtained the ADC resolution of $0.100918059 \mu\text{V}$. This is our system's resolution, which is below the limit of $5 \mu\text{V}$ set by the IEC 60601-2-25; therefore, our signal meets the requirement. The ADC readings and the number of LSBs are completely dependent on the format and resolution of the analog-to-digital converter being used. The ADAS1000, sampling at 2 kHz, uses a 19-bit resolution ADC, left-justified in a 24-bit data word [33]. All figures in this document display a decimal conversion.

4. For measuring system noise, we calculated an average of all the peaks at one level of the square wave (low or high should be the same). This is illustrated by the blue line in Figure 17b. We did the same for all the valleys, as illustrated by the red line in Figure 17b. As the objective is to measure the system noise level in μV , as required by the IEC standard, no frequency components were discriminated. All peaks and valleys contributed equally to their corresponding average value.
5. Calculating the LSBs between the red line and the blue line and multiplying this number by the system resolution calculated in Step 3 resulted in system noise of $5.17 \mu\text{V}$, which is indeed below $30 \mu\text{V}$; therefore, our signal complies with this requirement as well.

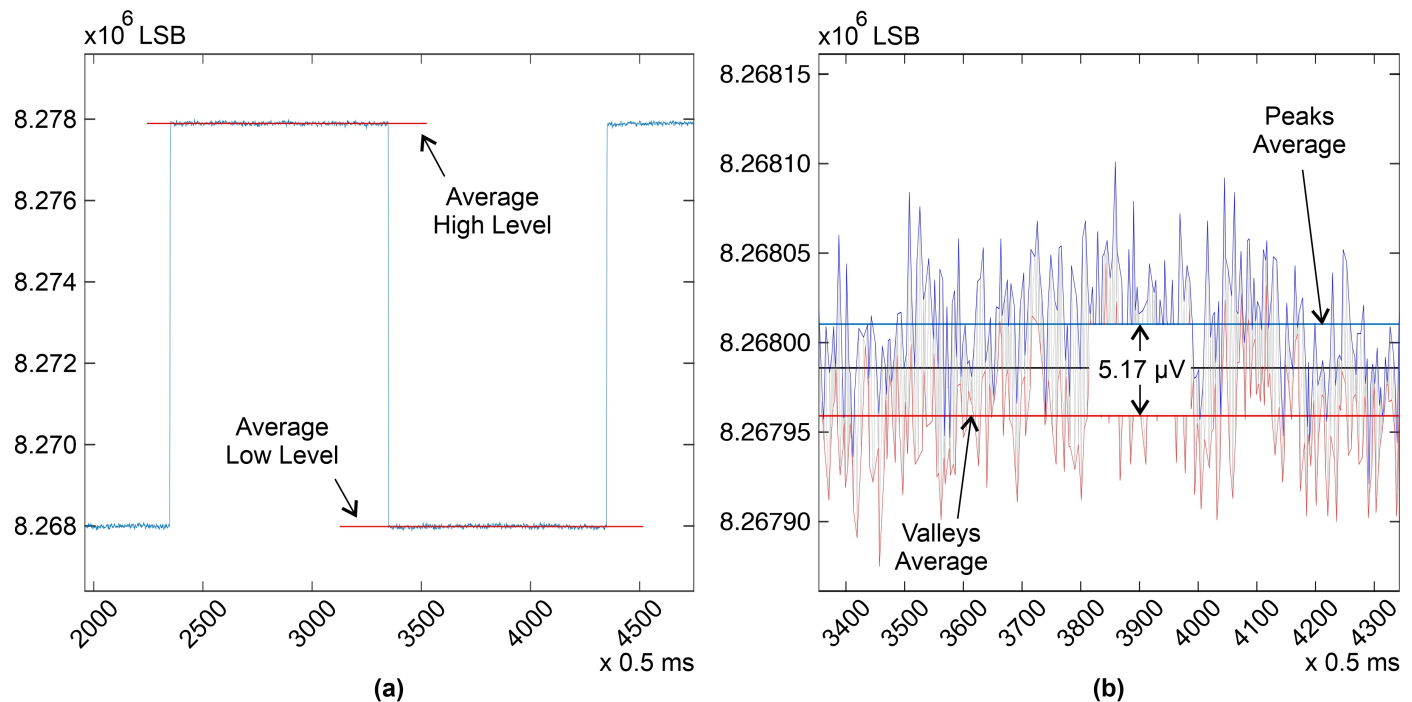


Figure 17. Illustration of the methodology for calculating the system's noise: (a) Illustration of the averages calculated in high and low levels for calculating system resolution; (b) Blue indicates the peaks of the system's noise and their average value. Red indicates the valleys of the system's noise and their average value. Black indicates the average value of peaks and valleys together.

The method illustrated in Figure 17 accounts for the noise generated only by the electrocardiograph. This noise level demonstrates that the PCB layout and the power supplies are well-designed and fully functional.

Finally, to validate the skew between channels, a new 1 Hz square-wave test tone was acquired at 16 kHz. At this sampling rate, the time (horizontal) resolution is $62.5 \mu\text{s}$. Figure 18 shows the same test tone acquired with two different channels: Figure 18a was acquired with the RA electrode, which is processed by the master ADAS1000 integrated circuit, and Figure 18b corresponds to the V3 electrode, which was processed by the slave device. A mark was placed on each signal to evaluate its horizontal position. As can be observed, these positions are identical in both signals (13,607), which means the skew between these two channels is practically $0.0 \mu\text{s}$, which is indeed below $100 \mu\text{s}$ as specified in IEC 60601-2-25 Section 201.12.4.107.3 [23].

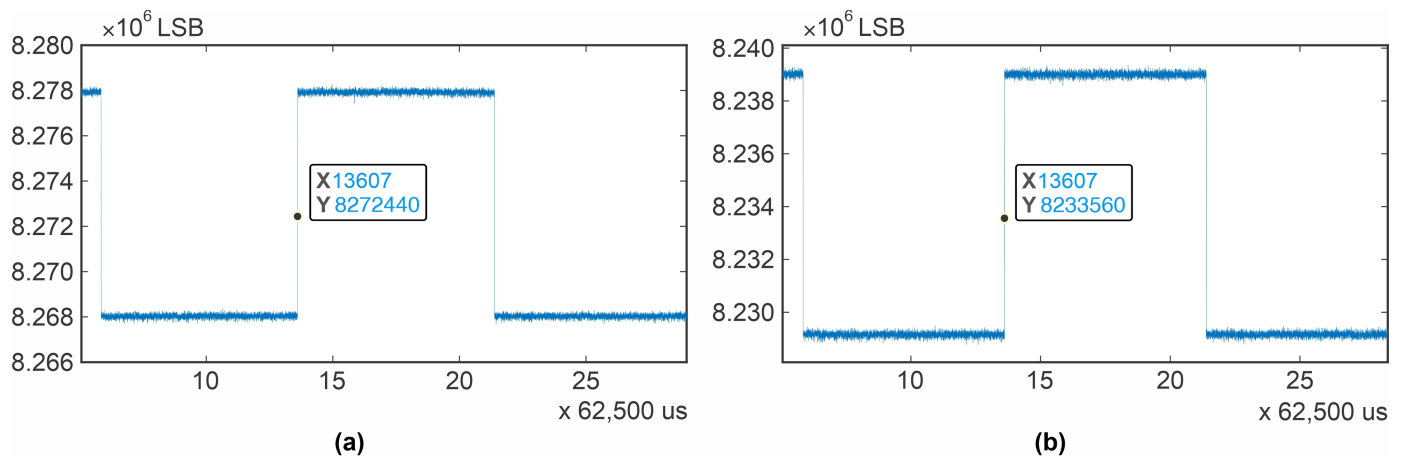


Figure 18. Test tone: 1 mV p-p square wave, 1 Hz, sampling rate 16 kHz. (a) RA electrode and (b) V3 electrode.

In order to test the electrocardiograph with ECG signals, we used the patient simulator model PS420 from FLUKE (Everett, Washington). The cable set designed for our electrocardiograph has a DB-15 connector and no resistors in-cable for defibrillator protection. These protection resistors were designed to be on-board to control their tolerances firsthand, thereby not relying on the cable manufacturer.

For acquiring ECG signals, both ADAS1000s were configured to operate in electrode mode, since no signal processing is performed by the ADAS1000s in this mode. In electrode mode, the differential amplifiers for lead formation are fed with the WCT (Wilson Center Terminal) on their inverting input, and the corresponding ECG electrode on their non-inverting input. All the available filters within the ADAS1000 were disabled; the acquired signals are shown in Figures 19 and 20. In Figure 19, we can observe that electrodes LA, LL, and RA are slightly noisier than the rest of the electrodes. This was confirmed to be a patient simulator issue. Using the system resolution previously calculated in Figure 17, in Figures 19 and 20, we calculated noise levels in specific segments of the signals (peak-to-valley) and observed that in all channels the system noise remained below 30 μ V.

Table 2 summarizes the parameters for signal quality compared with the values measured in the Kenshin device.

Table 2. IEC 60601-2-25 parameters that apply to signal quality in diagnostic applications.

Parameter	IEC 60601-2-25 Specification	Value Measured in the Kenshin Device	Meet the Requirement
System noise Level	Shall not be greater than 30 μ V at the baseline.	5.17 μ V, measured in a square wave, 1 Hz, 1 mV	✓
Amplitude quantization	Less than 5 μ V/LSB	0.100918059 μ V/LSB	✓
Skew-between channels	No larger than 100 μ s	Practically 0.0 μ s	✓
Sampling rate	At least 500 samples/s	2 kHz at best noise performance mode. Additionally, 16 kHz and 128 kHz sampling rates are available	✓

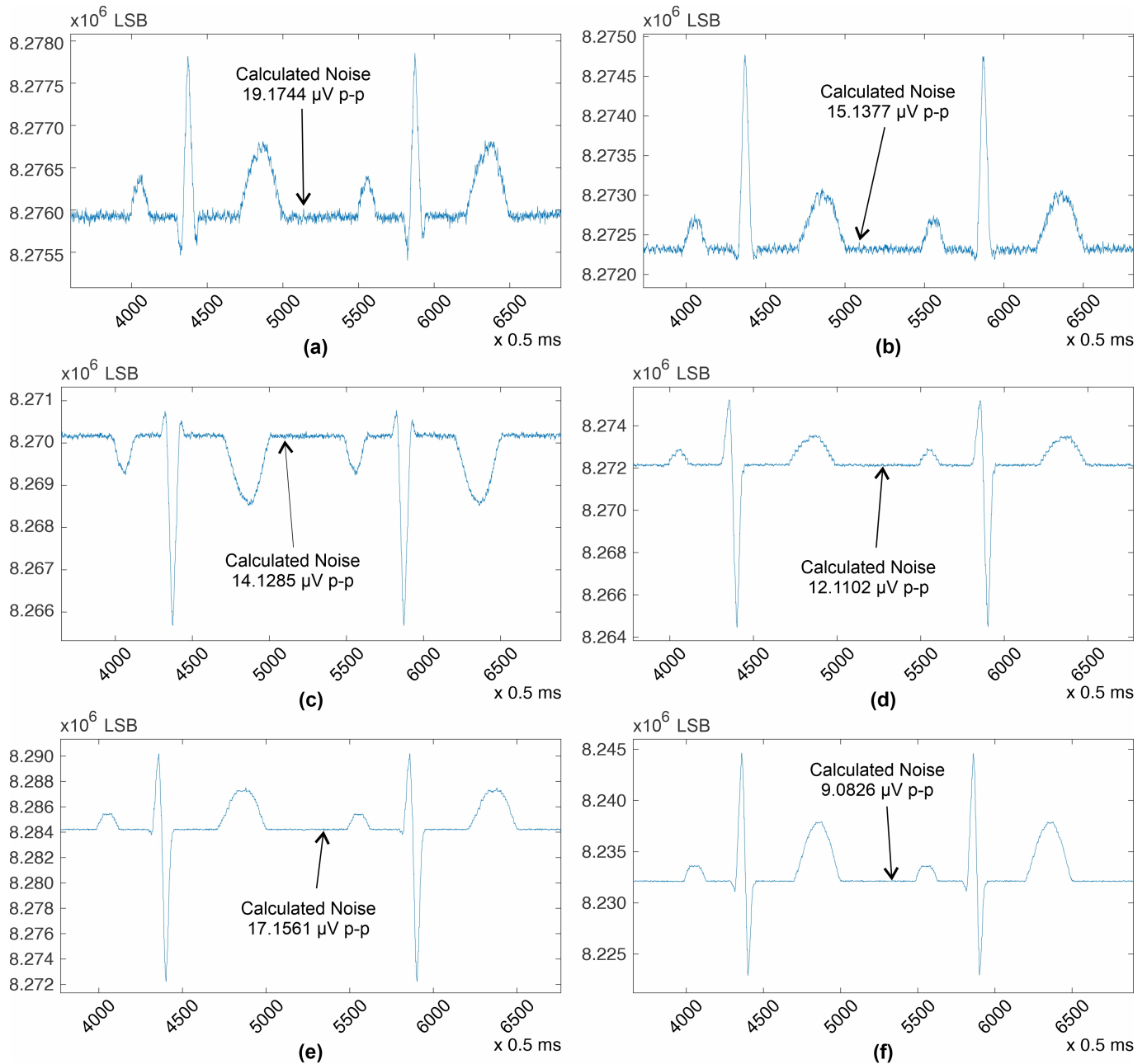


Figure 19. ECG signals from the FLUKE PS420 patient simulator: (a) LA electrode, (b) LL electrode, (c) RA electrode, (d) V1 electrode, (e) V2 electrode, and (f) V3 electrode.

To further validate the design methodology presented in this document, a series of EMC tests were performed in our case study. The evaluation was conducted according to the test plan of the LPECE (Electrical Testing and Electromagnetic Compatibility Laboratory, owned by CIDESI) and in collaboration with the EMC Test Lab (owned by the UAT-FI-UNAM). The starting point is the standard IEC 60601-1, which defines the general requirements for the basic and essential performance of Medical Electrical Equipment. Section 17 refers to the collateral standard IEC 60601-1-2 for checking compliance with Electromagnetic Compatibility. For medical power supplies, Section 4.10 of IEC 60601-1 also refers to IEC 60601-1-2 in defining the requirements for voltage dips, short interruptions, and voltage variations on the supply mains. Additionally, Section 7.1.1 of IEC 60601-1-2 specifies the mandated standard for evaluating conducted and radiated emissions, CISPR 11. A list of the performed precompliance tests, along with their status, is shown in Table 3.

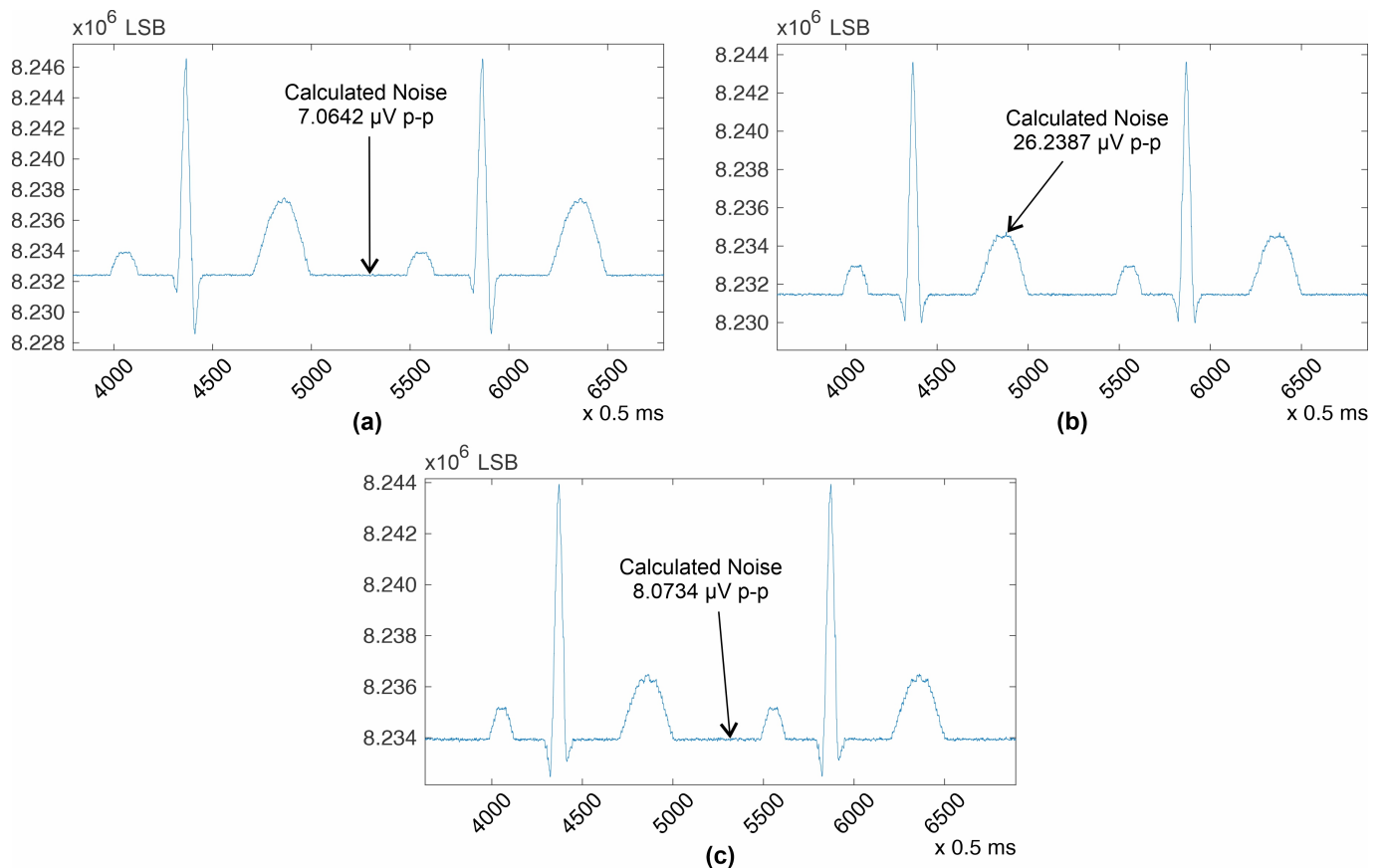


Figure 20. ECG signals from the FLUKE PS420 patient simulator: (a) V4 electrode, (b) V5 electrode, and (c) V6 electrode.

All tests shown in Table 3 were properly evaluated according to the norm and using the appropriate instruments, except the CISPR 11 for radiated emissions. The norm defines the test levels for the 30–230 MHz band exclusively for quasi-peak detectors, which is a piece of equipment that we still do not have available. However, the EMC Test Lab (LEMC), in its semi-anechoic chamber, has an average detector that can be used to estimate the needed quasi-peak values. According to the literature (p. 145 of ref. [49]), the average detector values should be below the quasi-peak detector values. Therefore, taking the CISPR standards into consideration, it is suggested to add 10–13 dB (μ V/m) to the average value for obtaining a quasi-peak estimation. After the addition, and comparing the resulting signal with the test levels, we observed that the Kenshin device still has a large margin for compliance. Curiously, in ref. [50], the authors specify that using a quasi-peak detector to cover a narrow band of 30–1,000 MHz could take up to five hours. Not to mention that the device under test still needs to be rotated, and the detector antenna needs to be rotated to both horizontal and vertical positions as well. Therefore, the authors in ref. [50] suggest using other, faster methods for evaluating radiation emissions for precompliance tests, such as the one we carried out using the average detector.

All the official test reports are included in the design documentation, which is available for download from https://kenshin-ai.org/e_ht-01/ (accessed on 23 October 2024).

Table 3. Precompliance electromagnetic compatibility tests performed on the Kenshin electrocardiograph.

Test Method	Type	Phenomenon	Test Levels	Status
IEC 61000-4-2	Immunity	Electrostatic Discharge	± 8 kV contact; ± 2 kV, ± 4 kV, ± 8 kV, ± 15 kV air	Passed
IEC 61000-4-3	Immunity	Radiated RF EM Fields	Professional healthcare facility environment; 3 V/m; 80 MHz–2.7 GHz; 80% AM at 1 kHz	Passed
IEC 61000-4-8	Immunity	Rated Power Frequency Magnetic Fields	Professional healthcare facility environment; 30 A/m; 50 or 60 Hz	Passed
IEC 61000-4-4	Immunity	Electrical fast transients/burst	Professional healthcare facility environment; ± 2 kV; 100 kHz repetition frequency	Passed
IEC 61000-4-5	Immunity	Surges Line-to-Line	Professional healthcare facility environment; ± 0.5 kV, ± 1 kV, ± 2 kV	Passed
IEC 61000-4-6	Immunity	Conducted disturbances induced by RF fields	Professional healthcare facility environment; 3 V, 0.15 MHz–80 MHz; 6 V in ISM bands between 0.15 MHz and 80 MHz; 80% AM at 1 kHz	Passed
IEC 61000-4-11	Immunity	Voltage dips	0% U_T ; 0.5 cycle at 0°, 45°, 90°, 135°, 180°, 225°, 270° and 315°; 0% U_T ; 1 cycle and 70% U_T ; 25/30 cycles, single phase at 0°	Passed
IEC 61000-4-11	Immunity	Voltage interruptions	0% U_T ; 250/300 cycle	Passed
CISPR 11	Conducted Emission	Conducted Disturbances	Measured in Test Site (AC mains power port); Class A; Group 1; ≤ 20 kVA; Quasi-peak: 0.15 to 0.50 MHz, 79 dB (μ V/m), 0.50 to 5 MHz, 73 dB (μ V/m), 5 to 30 MHz, 73 dB (μ V/m)	Passed
CISPR 11	Radiated Emission	Electromagnetic Radiation Disturbances	Semi-Anechoic Chamber; Class A; Group 1; 3 m measuring distance; ≤ 20 kVA; Quasi-peak: 30 to 230 MHz, 50 dB (μ V/m); 230 to 1000 MHz, 57 dB (μ V/m). Average: 1 to 3 GHz, 56 dB (μ V/m)	Passed

5. Limitations and Further Works

This device is intended to be at TRL 4, which means that it should be sufficient to validate the technology in a laboratory environment. Electrocardiographs are complex machines, not only due to all the hardware certifications required but also because of the software needed to make them fully functional. Since a vast amount of work is yet to be carried out, it is important to note that the present work is limited to the development of a functional device for acquiring IEC 60601-2-25-compliant signals. Even though the firmware is almost fully developed, computer programs for signal management still need to be developed. For further reference, a list of the most urgent tasks can be found on the project webpage under the “Scientific Research” menu (<https://kenshin-ai.org>, accessed on 23 October 2024).

In the long term, this project aims to create a commercial-grade electrocardiograph within a fully open-access environment. Thousands of papers have been published over the course of many years on ECG signal processing, yet a single, integrated algorithm for automatic interpretation at the clinical practice level in academia still does not exist. We recognize that achieving this advanced level of development is not a job for a single institution but for the collective academic community around the world. In fact, not even giant companies with their own research centers [51,52] have been able to reach the required levels of efficiency for reliable use in clinical practice.

The applications for the analog core of this electrocardiograph, the ADAS1000, can be expanded to different applications, such as ambulatory care or monitoring. For example, the ADAS1000 can be used to develop a Holter device or a training assistant. We expect to keep working on the development of new devices in the near future in order to ensure that we do not limit the applicability of the Kenshin Project. In order to ensure this project’s continuity, the hardware proposed in this document has been made open-source, expecting the academic community to back up the design data published.

6. Conclusions

This document describes the process of designing a compliant physiological signal acquisition system, applied to a case study, namely an electrocardiograph. The design approach progresses from the general to the specific, and its motivation comes from the intention to solve a scientific problem: the need to integrate a new standardized signal databank to facilitate signal processing research in the academic environment. Specifically, the standardization of signals aids in the integration and scalability of different algorithms. Although the electrocardiograph cannot integrate the new standardized databanks by itself, standardization of signals completely depends on the standardization of the hardware, which is what the device developed with the presented methodology achieves.

The design methodology in this document was first presented in a general way and then applied to a case study with the intention of extending it to the development and standardization of other physiological acquisition systems. This approach is justified because the electronic design considerations are expected to be the same, and because the problem of low efficiency in automatic interpretation in clinical practice, which has been reported for practically all kinds of physiological signals, arises from the same cause as the original motivation for this work: the signal incompatibility problem caused by different sampling rates or varying noise levels.

Related to hardware development, the design methodology presented in this document is different from other publications in various aspects. For example, in this design methodology, topics like Electromagnetic Compatibility (EMC) and Signal Integrity (SI) have been integrated throughout the entire design process, as they should be, since EMC and SI cannot be easily added once the design is finished. In modern electronics, especially in mixed-signal boards, EMC and SI are the main building blocks of every design. Another important contribution of this article is that the device produced with this design methodology is a diagnostic-grade device that complies with the IEC 60601-2-25 requirements for signal quality and has also passed nine different precompliance tests for Electromagnetic Compatibility, rather than just being a device for educational purposes developed without formal knowledge in electronics design and applicable norms, and with no intention of developing a diagnostic-grade device.

Finally, in order to help with hardware standardization, the resulting device documentation and fabrication files were made available to the academic community through the Kenshin Project webpage (https://kenshin-ai.org/e_ht-01/, accessed 23 October 2024), which is an open platform specializing, for now, in leveraging efficiency in the automatic interpretation of ECG signals. The newly created electrocardiograph is an open-source hardware tool that currently does not exist in academia, either in terms of expedited availability or design quality. One might think that using a single commercial model would solve the problem, but making academia rely on a commercial partner is not a good idea, as academia would lose freedom. That is what another project did (OpenECG), and this approach has now been proven not to work. The ideal approach would be to have academia lead research from electronics design to signal processing research, thereby inherently ruling the market.

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Informed Consent Statement: Informed consent was obtained from all subjects involved in this study.

Data Availability Statement: The design documentation of the electrocardiograph presented here, which includes signals, Matlab workspaces, schematic documents, fabrication files, Bill of Materials, and official test reports, is available at the project webpage (<https://kenshin-ai.org>, accessed on 23 October 2024).

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Abbreviations

The following abbreviations are used in this manuscript:

BGA	Ball Grid Array
AAMI	Association for the Advancement of Medical Instrumentation
ANSI	American National Standards Institute
CIDESI	Center for Engineering and Industrial Development
CISPR	Comité International Spécial des Perturbations Radioélectriques
ECG	Electrocardiogram
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESIS	Electrosurgical Interference Supression
FI	Faculty of Engineering
HASL	Hot Air Solder Leveling
IDE	Integrated Development Enviroment
IEC	International Electrotechnical Commission
IPC	Institute of Printed Circuits
LANITEM	National Laboratory for Research on Medical Technologies
LPECE	Electrical Testing and Electromagnetic Compatibility Laboratory
PCB	Printed Circuit Board
RF	Radio Frequency
SI	Signal Integrity
SPI	Serial Peripheral Interface
TRL	Technology Readiness Level
UAT	High-Technology Unit
UNAM	National Autonomous University of Mexico
USB	Universal Serial Bus

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