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Design of Voltage–Current Reference Source in CMOS Technology

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Abstract: A design methodology for a resistorless low-power two-in-one voltage and current reference source working in subthreshold and moderate regions is described. The presented novel universal reference voltage–current source was implemented in ten different designs for seven different CMOS technologies. Six versions of these designs were silicon-proven using four different CMOS technologies. The example of implementation in 130 nm technology provides a reference current of 5 µA and reference voltage of 800 mV at supply voltages ranging from 0.9 V to 2.0 V with a total current consumption of 15 µA. The proposed circuit occupies a 1200 μm^2 chip area and achieves 280 and 118 ppm/°C for all process corners and temperature variation from −40 °C to 125 °C. The power supply rejection ratio of output I_{REF} without any filtering capacitor at 100 Hz and 10 MHz is 128 dB and 100 dB, respectively. The equivalent output current noise in the bandwidth from 1 Hz to 10 MHz reaches 9.1 nA_{RMS}.

Keywords: bandgap; voltage reference; current reference; integrated circuits; subthreshold

1. Introduction

Reference voltage and current sources are necessary for many analog, mixed-signal, RF and digital integrated circuits. They are used to provide stable voltage and current bias for many SoC (System on Chip) building blocks, such as amplifiers, DAC and ADC, LDO, PLL and memories. The reason why the voltage and current reference block is so important is that it can provide stable reference voltage and/or current; i.e., it is insensitive to variations in the temperature, process and supply voltage. This circuit should be autonomous because it is needed at SoC start-up, when the voltage supply is switched on, and should be based on intrinsic physical properties, or on reproducible technology parameters. The wide usage of battery-operated wireless communication systems and portable electronic devices drives the continuous evolution of integrated circuits, aiming at lower power consumption and reduced supply voltage. In CMOS technology, both requirements are generally satisfied by shrinking MOSFET dimensions. Therefore, new circuit architectures can be necessary to satisfy circuit specifications.

This paper describes a design methodology for a resistorless low-power voltage–current reference source working in subthreshold and moderate regions. The proposed methodology was verified using ten different source designs for seven different CMOS technologies. Six versions of these designs were silicon-proven using four different CMOS technologies. The novel voltage–current reference source presented here consists of MOSFETs only. It is designed for low supply voltages, with a small temperature coefficient, low sensitivity to process variations and small area occupation on the chip. The presented examples of implemented reference source designs prove the transferability of such architecture between different technologies and nodes.

The paper is organized in the following way: Section 2 presents the known solutions of voltage and current reference circuits. The design and operating principles of the proposed

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voltage–current reference source are described in Section 3, which is focused on the method of the systematic design of the proposed voltage–current reference circuit. Section 4 gives details of the innovative circuit implementation with simulation and measurement results. Finally, conclusions are drawn in Section 5.

2. Known Reference Source Circuits

Most of the commonly used voltage and current reference sources use the architecture that has been called bandgap, described by Robert Widlar [1] and applied to the LM113 integrated circuit [2]. These first integrated reference voltage sources, using bipolar transistors, provided a reference voltage of 1.25 V, as temperature compensation usually occurs at this value. However, two main problems arise when scaling CMOS technologies: the presence of real bipolar transistors is not advisable, as this requires more processing steps and the production of more masks for the photolithography process, and the fact that the design of bandgap reference voltage circuits becomes difficult when the supply voltage decreases to 1.25 V, as this is an insufficient supply level to ensure correct operation.

In order to reduce the manufacturing cost of voltage or reference current sources in SoCs, their design should include only standard components available in a given CMOS process. A common solution to make this possible is to use parasitic bipolar transistors with vertical orientation that are always present in all CMOS technologies [3,4]. There are architectures based on bipolar transistors that allow the reference voltage to be reduced at supplies below 1 V. This is obtained using the resistance subdivision method as introduced in [5] and then extended by extra compensation circuitry in [6] and with improved PSRR [7]. The subsequent paper [8] improves the start-up of that architecture.

Other types of reference sources, implemented in a standard CMOS technology, are based on a weighted difference between the gate-source voltages of two MOSFETs [9]. However, design solutions of this type typically use one or more resistors that largely increase the area of the circuit [10].

In many architectures of all-MOS voltage or current references, the operating principle is based on the thermal properties of CMOS transistors biased in the weak inversion region [11]. However, unlike the bandgap reference circuits that are insensitive to process corners, the problem of reference sources based on MOSFETs in the subthreshold region is the process corner spread of threshold voltages. That may result in significant reference voltage and current variation up to 30%. To overcome this problem, another subthreshold voltage reference circuit resisting process corner variation was presented in [12] using MOSFETs with two different threshold voltages. With this technique, the variation can be reduced to $\pm 0.7\%$ in the worst process corner. The challenge is that the circuit includes several big resistors, which increases the silicon area. The next interesting solutions for low-power applications were proposed in [13,14], but the influence of process corners was not analyzed appropriately.

In summary, the existing publications are not focused enough on the analysis of process corner variations or the influence of device matching. Usually, the analytical derivations and simulation results are presented only for the typical process corner.

3. Novel Voltage–Current Reference Source Design and Principle of Operation

The schematic of the proposed two-in-one voltage and current reference source circuit built with MOSFET devices only is shown in Figure 1. This circuit is based on the development described in [15]. The principle of operation is presented in Figure 2.

The three-color families of characteristics shown in Figure 2 visualize the process corner spread of I_{DS} current vs. temperature. The typical corner is labeled as *TT*. The *FF* and *SS* corners correspond to "fast" (highest I_{DSAT}, lowest V_{TH}) and "slow" (lowest I_{DSAT}, highest V_{TH}) MOSFETs, respectively. The current mirrors M_1–M_2 and M_3–M_4 form a closed loop gain greater than unity operating as a proportional to absolute temperature (PTAT) voltage source [11], which is shown in Figure 3. The equations derived from work [11] cannot be used because the presented circuit can work in both weak and moderate inversion.

That is why the formula describing the ΔV_{GS} voltage was derived directly from the EKV continuous MOSFET model, valid for all regions of operation [16].

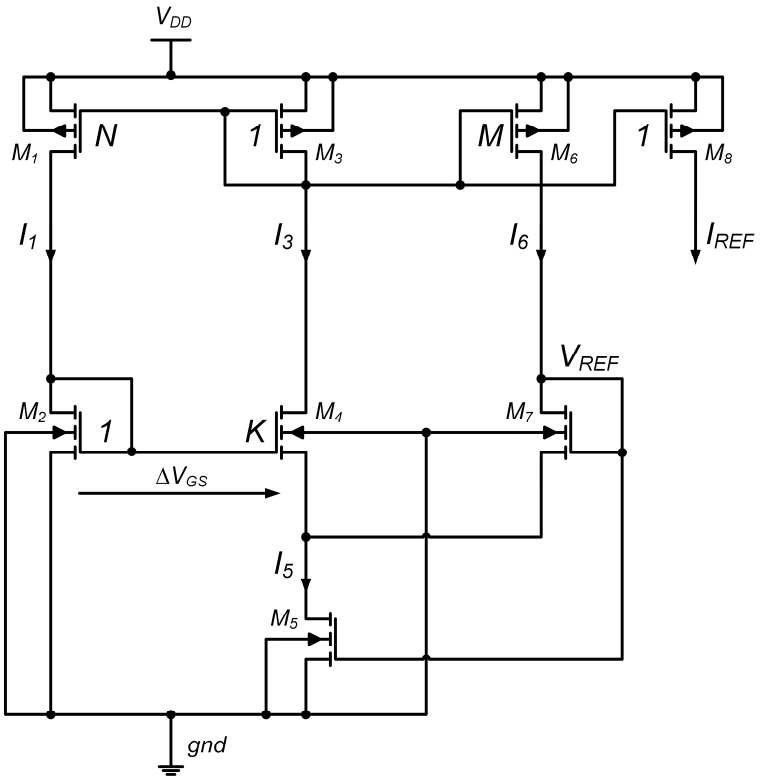


Figure 1. Proposed voltage and current reference source (start-up circuit not included).

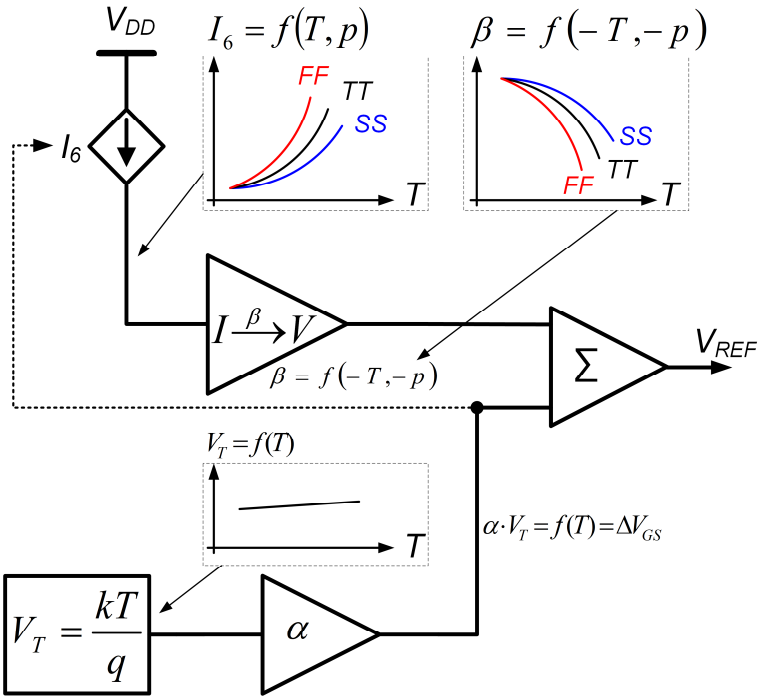


Figure 2. Resistorless CMOS voltage reference source—principle of operation.

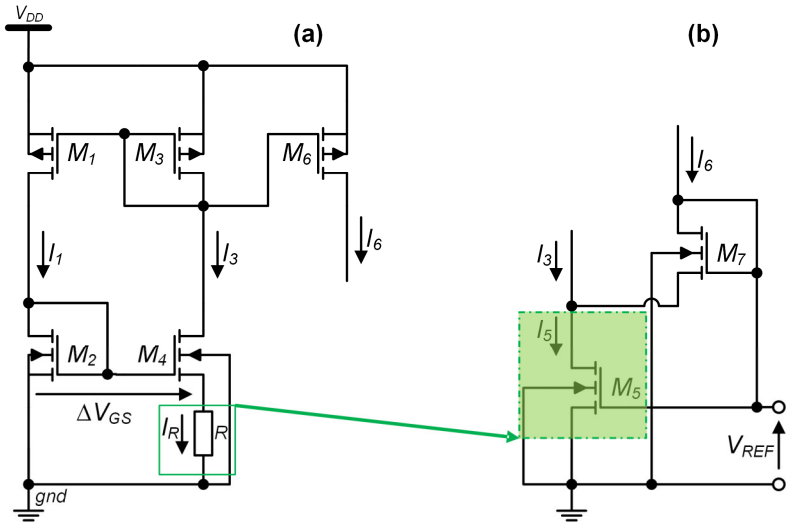


Figure 3. (**a**) Schematic of ΔV_{GS} PTAT source and I_6 bias current. (**b**) PVT compensation circuit.

The equation for MOSFET drain current can be expressed as follows:

$$I_D = 2n\beta {V_T}^2 \left[ln^2 \left(1 + e^{\frac{V_G - V_{TO} - nV_S}{2nV_T}} \right) - ln^2 \left(1 + e^{\frac{V_G - V_{TO} - nV_D}{2nV_T}} \right) \right], \quad (1)$$

where n is the subthreshold slope factor whose value depends on the process, $\beta = \mu C_{ox} W/L$, where μ is the electron or hole mobility in the channel, C_{ox} is the thin gate oxide capacitance per unit area, and W and L are the channel width and length, respectively. $V_T = kT/q$ is the thermal voltage, $V_G/V_S/V_D$ are gate/source/drain to substrate voltages, respectively, and V_{TO} is the threshold voltage. The reverse current is several orders of magnitude smaller than the forward current and can therefore be ignored in further calculations. The following dependencies for the drain currents of transistors M_2 and M_4 are then obtained:

$$I_1 = I_{D2} = 2n\beta_2 {V_T}^2 ln^2 \left(1 + e^{\frac{V_G - V_{TO}}{2nV_T}} \right), \; I_3 = I_{D4} = 2n\beta_4 {V_T}^2 ln^2 \left(1 + e^{\frac{V_G - V_{TO} - \Delta V_{GS}}{2nV_T}} \right). \quad (2)$$

Solving the system of equations for ΔV_{GS}, assuming that $I_1 = NI_3$, $\beta_4 = K\beta_2$, one obtains

$$\Delta V_{GS} = 2V_T ln \left(\frac{e^{\sqrt{S \cdot IC}} - 1}{e^{\sqrt{IC}} - 1} \right), \quad (3)$$

where S is the loop gain: $S = N \cdot K$, where N, K are MOSFET size ratios: $N = \frac{S_{M1}}{S_{M3}}$, $K = \frac{S_{M4}}{S_{M2}}$, $S_{MN} = \frac{W_N}{L_N}$. IC is MOSFET inversion coefficient: $IC = \frac{I_{D4}}{2n\beta_4 {V_T}^2}$.

If the inversion coefficient IC is close to zero (transistors $M_{2,4}$ are in weak inversion), the expression under the natural logarithm in Formula (3) can be approximated by the square root of S (4), as shown in Figure 4.

$$\lim_{IC \to 0} \left(\frac{e^{\sqrt{S \cdot IC}} - 1}{e^{\sqrt{IC}} - 1} \right) = \sqrt{S}. \quad (4)$$

When the IC inversion coefficient is close to unity (transistors $M_{2,4}$ are in moderate inversion), this relationship over a small range of loop gains (sufficient for practical applications) can be approximated by the linear function $f(S)=S$ (Figure 4). After the above approximations are applied, the formula for ΔV_{GS} is given by

$$\Delta V_{GS} = V_T lnS \text{ for } IC << 1, \quad (5)$$

$$\Delta V_{GS} = 2V_T lnS \text{ for } IC \cong 1. \quad (6)$$

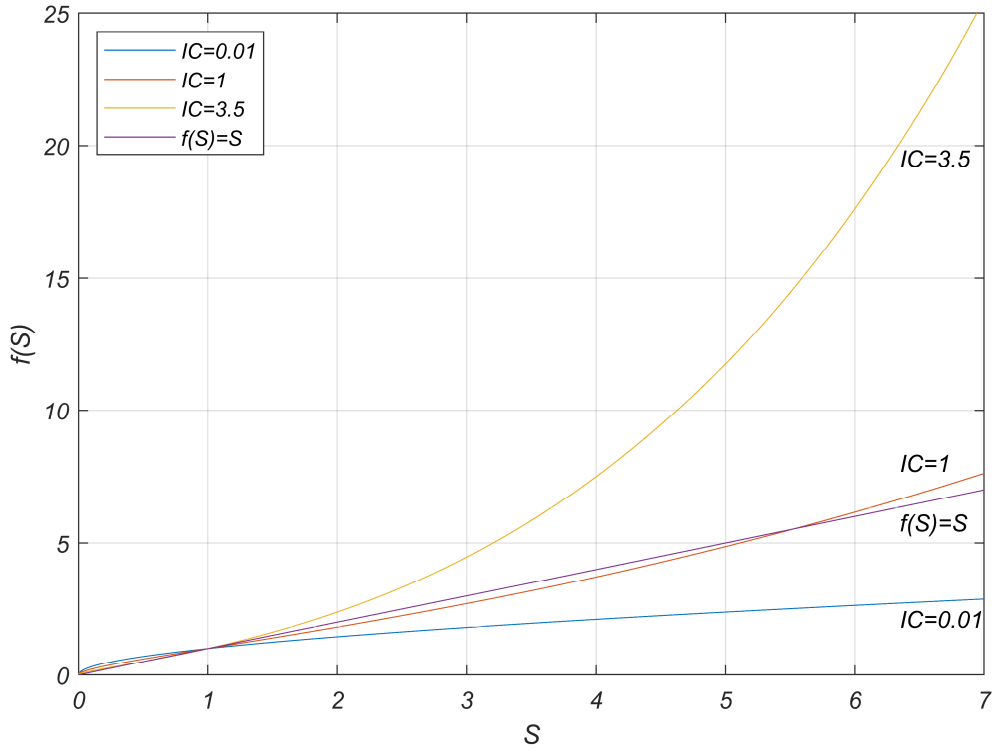


Figure 4. Expression $f(S) = \left(\frac{e^{\sqrt{S \cdot IC}}-1}{e^{\sqrt{IC}}-1}\right)$ as a function of the loop gain parameter S at different values of the channel inversion coefficient IC.

Equation (5) is a well-known solution from [11], while (6) is the authors' new solution for transistors M_2 and M_4 working in moderate inversion.

In the presented reference source, the resistor R (Figure 3a) is replaced by n-MOSFET M_5 (Figure 3b) working in the linear region of weak or moderate inversion. This MOSFET is biased by the stable output reference voltage V_{REF} to make sure that r_{ds} of M_5 varies only with process and temperature, not with supply voltage. This behavior modifies the generated currents I_5 and I_3. This is shown by the current characteristics $I_6 = f(T,p)$ in Figure 2. Then, current I_3 is multiplied M times by the current mirror M_6 and biases transistor M_7 operating in saturation. It converts the current I_6 into a voltage V_{REF} by coefficient β (Figure 2). The conversion coefficient β varies with process and temperature in the opposite way to I_6. The PVT compensation circuit can be described by Equation (7):

$$V_{REF} \cong \frac{2 + A_M + \sqrt{{A_M}^2 + 2A_M}}{2} \cdot \Delta V_{GS} + V_{TH7}\ , \quad (7)$$

$$A_M = \left(\frac{2}{M^{-1}+1}\right) A\ , \quad (8)$$

$$A = \frac{\beta_5}{\beta_7} = \frac{S_5}{S_7}\ , \quad (9)$$

By substituting (3) in (7), the expression describing the output reference voltage V_{REF} is given by

$$V_{REF} \cong \left(2 + A_M + \sqrt{{A_M}^2 + 2A_M}\right) \cdot V_T ln\left(\frac{e^{\sqrt{S \cdot IC}} - 1}{e^{\sqrt{IC}} - 1}\right) + V_{TH7}. \quad (10)$$

After the approximation (5 and 6) is applied, the simplified solution is shown below:

$$V_{REF} \cong \frac{\left(2 + A_M + \sqrt{{A_M}^2 + 2A_M}\right)}{2} \cdot V_T lnS + V_{TH7} \qquad \text{for weak inversion} \tag{11}$$

$$V_{REF} \cong \left(2 + A_M + \sqrt{{A_M}^2 + 2A_M}\right) \cdot V_T lnS + V_{TH7} \qquad \text{for moderate inversion} \tag{12}$$

The reference voltage can be made temperature-independent by applying transistor sizing so that the thermal voltage multiplier (with a positive temperature coefficient) compensates for the temperature variation of the threshold voltage of transistor M_7 (with a negative temperature coefficient). By differentiating the Equation (12) over temperature, one obtains

$$\frac{\partial V_{REF}}{\partial T} = k \cdot \frac{\partial V_T(T)}{\partial T} + \frac{\partial V_{TH7}(T)}{\partial T}\ , \tag{13}$$

$$k = \left(2 + A_M + \sqrt{{A_M}^2 + 2A_M}\right) \cdot ln\left(\frac{e^{\sqrt{S \cdot IC}} - 1}{e^{\sqrt{IC}} - 1}\right)\ . \tag{14}$$

To include higher-order temperature compensation effects in the analytical model, one would have to assume that the *k* factor depends on the temperature, as *IC(T) = f(T)* ≠ *const.*, which can be described by the formula

$$IC(T) = \frac{I_{D4}(T_0) \cdot \left[1 + tc_1 \cdot (T - T_0) + tc_2 \cdot (T - T_0)^2\right]}{2V_T^2 \cdot \frac{W}{L} \cdot KP_4(T_0) \cdot \left(\frac{T}{T_O}\right)^{0.5}}\ , \tag{15}$$

where T_0, tc_1 and tc_2 are room temperature (300 °K) and temperature coefficients of the first (K^{-1}) and second order (K^{-2}), respectively. By differentiating (13) over temperature and neglecting higher-order effects from (15), one obtains

$$k = -\frac{\left(\frac{\partial V_{TH7}(T)}{\partial T}\right)}{0.086\frac{mV}{^\circ K}}\ . \tag{16}$$

As indicated by (15), the temperature coefficient varies with the process parameters that change with temperature. Such dependencies create second-order effects (visible during the simulation of the final circuit) that have been omitted for simplicity.

The second functionality of the presented circuit is the current reference source. By adding an additional transistor M_8 to the schematic, it is possible to form an output current mirror (Figure 1). To do that, it is necessary to choose different dimensions for transistors M_2, M_4, M_5, M_7 and to select the appropriate loop coefficients *N* and *K* and multiplier *M* for current mirror M_6. Using (10) and assuming $I_{REF} = I_6$, the expression for the reference output current I_{REF} is given by

$$I_{REF} = \frac{\frac{\left(1+A_M+\sqrt{{A_M}^2+2A_M}\right)\beta_5 {\Delta V_{GS}}^2}{2} + \beta_5 \Delta V_{GS}(V_{TH7} - V_{TH5})}{M+1}\ . \tag{17}$$

By differentiating (17) over the temperature, one obtains

$$\begin{aligned} \frac{\partial I_{REF}}{\partial T} &= m \cdot V_T \beta_5 \left(\frac{\partial V_{TH7}(T)}{\partial T} - \frac{\partial V_{TH5}(T)}{\partial T}\right) + m \cdot V_T (V_{TH7} - V_{TH5}) \frac{\partial \beta_5(T)}{\partial T} \\ &+ l \cdot m^2 {V_T}^2 \frac{\partial \beta_5(T)}{\partial T} + m \cdot \beta_5 (V_{TH7} - V_{TH5}) \frac{\partial V_T(T)}{\partial T} + 2l \cdot m^2 V_T \beta_5 \frac{\partial V_T(T)}{\partial T}\ , \end{aligned} \tag{18}$$

where

$$l = \frac{\left(1 + A_M + \sqrt{{A_M}^2 + 2A_M}\right)}{2}\ , \tag{19}$$

$$m = ln\left(\frac{e^{\sqrt{S \cdot IC}} - 1}{e^{\sqrt{IC}} - 1}\right). \quad (20)$$

Assuming that both M_5 and M_7 transistors are the same type, $\frac{\partial V_{TH7}(T)}{\partial T} \cong \frac{\partial V_{TH5}(T)}{\partial T}$, a condition on the temperature stability of the new current reference source is obtained:

$$l \cdot m = \frac{19.34(V_{TH5} - V_{TH7})\left(300\frac{\partial \beta_5(T)}{\partial T} + \beta_5\right)}{150\frac{\partial \beta_5(T)}{\partial T} + \beta_5} \quad (21)$$

The presented architecture is based on MOSFET characteristics in the weak (subthreshold) and moderate inversion regions to make use of the PTAT voltage source made by the M_1–M_4 subcircuit, which gives such behavior in those regions. There is no major difference in terms of PVT stability between weak and moderate, and rigid separation between both regions does not exist. The used supply voltage level and current values in bias branches will determine the regions of MOSFET operation. The visible trade-off between those two regions of MOSFET operation is power consumption vs. I_{REF} and V_{REF} random spread during device fabrication. It is related to higher mismatch effects in the deep subthreshold region. It is possible to mitigate that by increasing the width and length of the M_2, M_4 pair mainly, as well as the M_5, M_7 pair. The increasing area of current mirrors has a positive influence for output variation improvement at the expense of PSRR decreasing.

The analysis and theoretical calculations for the presented reference voltage–current source were performed in Matlab and wxMaxima software for solving symbolic equations. Verification and implementation were performed using Cadence Virtuoso with the Spectre SPICE simulator. All layouts were drawn with the Virtuoso Layout Editor and verified and RC-extracted using Cadence's QRC and PEX Calibre from Siemens.

4. Example Implementation of a Novel Voltage–Current Reference Source

The presented reference voltage–current source was implemented in ten different designs for seven different CMOS technologies: ATMEL 0.5 µm, IBM 180 nm RF, IBM 180 nm HV, SMIC 180 nm, LFoundry 150 nm, UMC 130 nm and UMC 90 nm. The prototype circuit was manufactured in six versions using four technologies: UMC 90 nm, UMC 130 nm, LFoundry 150 nm and SMIC 180 nm. One of them is presented in detail below.

4.1. Schematic, Layout and Simulation Results of the New Voltage–Current Source

The example implementation of the proposed circuit shown in Figure 5 was designed in UMC CMOS 130 nm technology. The dimensions of the transistors used are indicated in Table 1 together with their drain currents.

In addition to the generic schematic of the proposed voltage–current reference source the cascode stage was added, formed by M_{10} native n-MOS with nearly zero threshold voltage, to improve the efficiency of the current mirror. Since the reference source has two stable states corresponding to the voltage given by (10) and to zero voltage, a capacitor-less start-up circuit formed by transistors $M_{11,12}$ is used to ensure that the former stable state is achieved. The final layout of the designed reference source is shown in Figure 6. The silicon dimensions are 25 µm × 48 µm.

Table 1. Dimensions of transistors used in the proposed circuit together with their drain currents for typical process corner (process = TT, T = 27 °C; V_{DD} = 1.2 V).

Device	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_{10}	M_{11}	M_{12}	M_{13}
W_{tot} [µm]	2 × 40	2 × 9	2 × 40	28 × 9	1.42	2 × 40	1.42	2	10	72	2 × 40
L [µm]	1	0.5	1	0.5	0.88	1	2 × 0.88	10	0.12	0.12	1
I_{DS} [µA]	5.0	5.0	5.0	5.0	10.0	5.0	5.0	5.0	0	0	5.0

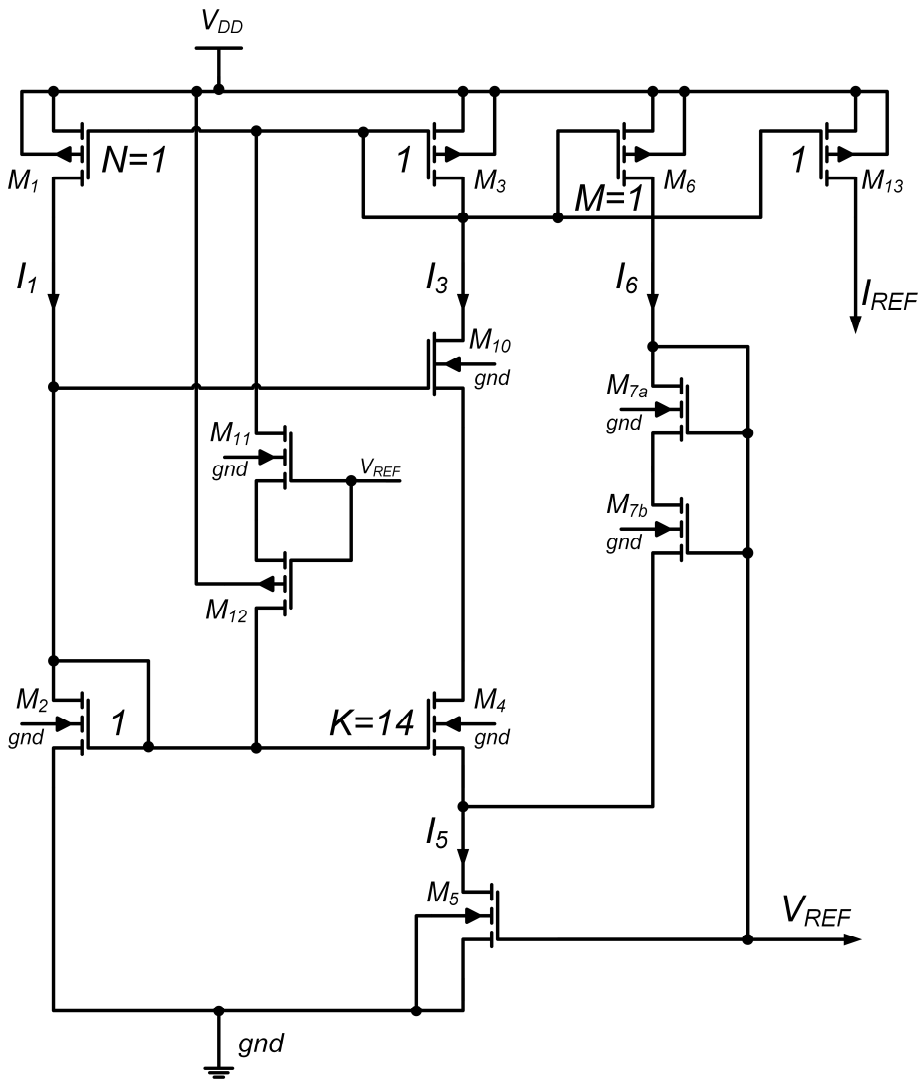


Figure 5. Schematic of the proposed voltage–current reference source implemented in UMC 130 nm technology together with start-up circuit $M_{11–12}$.

The key features of the designed circuit (obtained from post-layout simulations) are listed in Table 2. The reference output voltage and current at 27 °C and temperature coefficients are summarized for each process corner in Table 3.

Table 2. Summary of the post-layout simulation results at typical process corner, T = 27 °C, V_{DD} = 1.2 V.

Parameter	Unit	Value
Technology feature size	um	130
Supply current (output I_{REF} not included)	µA	15.0
Supply voltage range	V	0.9–2.0
Temperature range	°C	−40–125
Reference output current (I_{REF})	µA	5.00
Temperature coefficient (TC_I) of I_{REF}	ppm/°C	280
Line sensitivity of I_{REF} (in V_{DD} range)	%	±4.0
Process corners sensitivity of I_{REF}	%	±7.4

Table 2. *Cont.*

Parameter	Unit	Value
I_{REF} MC 3σ × 1000 runs Process only	µA	M = 4.99; σ = 0.06
I_{REF} MC 3σ × 1000 runs Mismatch only	µA	M = 5.01; σ = 0.26
I_{REF} MC 3σ × 1000 runs Process and Mismatch	µA	M = 5.00; σ = 0.27
Noise density @ 100 Hz @ 100 kHz 1 Hz–10 MHz	 pA/√Hz pA/√Hz nARMS	 81 4.8 9.1
PSRR @ 100 Hz @ 10 MHz @ 1 GHz	 dB dB dB	 128 100 66
Reference output voltage (V_{REF})	mV	800
Temperature coefficient (TC_V) of V_{REF}	ppm/°C	118
Line sensitivity of V_{REF} (in V_{DD} range)	%	±0.9
Process corners sensitivity of V_{REF}	%	±5.2
V_{REF} MC 3σ × 1000 runs Process only	mV	M = 800; σ = 11
V_{REF} MC 3σ × 1000 runs Mismatch only	mV	M = 800; σ = 9
V_{REF} MC 3σ × 1000 runs Process and Mismatch	mV	M = 800; σ = 14
Noise density @ 100 Hz @ 100 kHz 1 Hz–10 MHz	 µV/√Hz µV/√Hz µVRMS	 3.9 0.23 293
PSRR @ 100 Hz @ 10 MHz @ 1 GHz	 dB dB dB	 40 10 3.5
Settling time	µs	4.7
Chip area	μm^2	1200

Table 3. Summary of reference voltages, currents and temperature coefficients.

Process Corner	I_{REF} [µA]	TC_I [ppm/°C]	V_{REF} [mV]	TC_V [ppm/°C]	I_{DD} [µA]
SS	4.59	509	841	186	19.1
SF	4.67	888	816	340	19.5
TT	5.00	280	800	118	20.8
FS	5.25	545	782	72.8	21.9
FF	5.33	390	758	54.5	22.2

Figures 7–12 show the results of post-layout simulations of the implemented reference voltage and current source circuit. The TC performance at temperatures ranging from −40 °C to 125 °C at V_{DD} = 1.2 V is demonstrated in Figure 7.

The circuit has been verified for large supply voltage variations (Figure 8). The results indicate that the circuit generates stable reference voltage and current with the supply as low as 0.9 V for any process corner. The bottom value of supply voltage is imposed by the transistors in the current generator circuit. The p-MOS M_1, M_3, M_6 and M_{13} must operate

in saturation. Additionally, to maintain stable output reference voltage, transistor M_7 must work in saturation. The lowest value of the supply voltage might be reduced by removing cascode M_{10}.

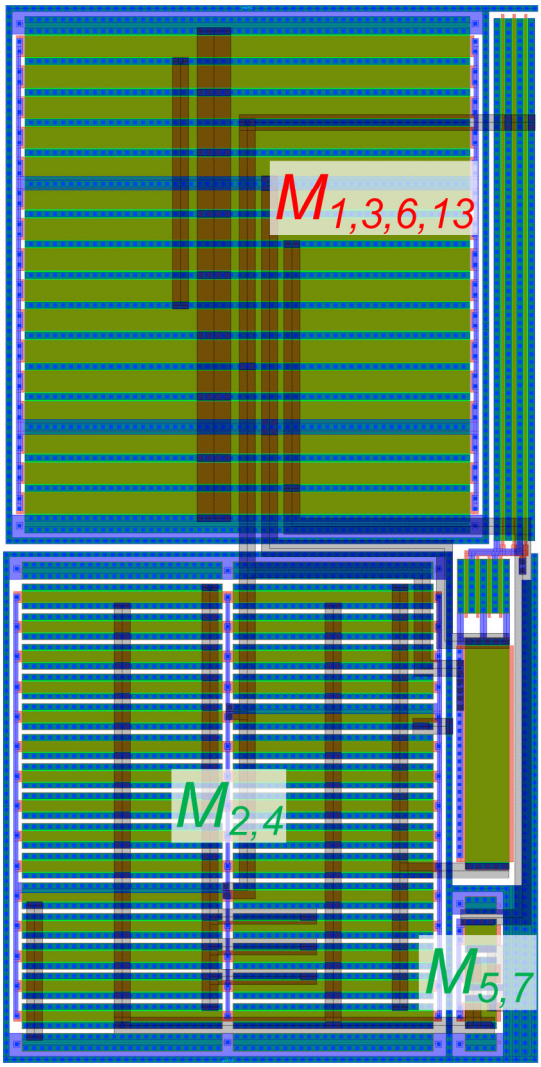


Figure 6. Layout of the designed voltage–current reference source implemented in UMC 130 nm technology.

The settling time for the circuit at start-up is shown in Figure 9 during transient simulation.

Monte Carlo (MC) simulations were performed to determine the process and transistor mismatch effects on the output reference voltage and current. The MC analysis proved that the presented current reference source should be very reproducible with the process fluctuation, which is shown in Figure 10a. On the other hand, the variations in device matching have a significant impact on output reference voltage and current level and repeatability from chip to chip (Figure 10b,e). Figure 10c,f show the MC analysis with device matching and process parameter fluctuation simultaneously.

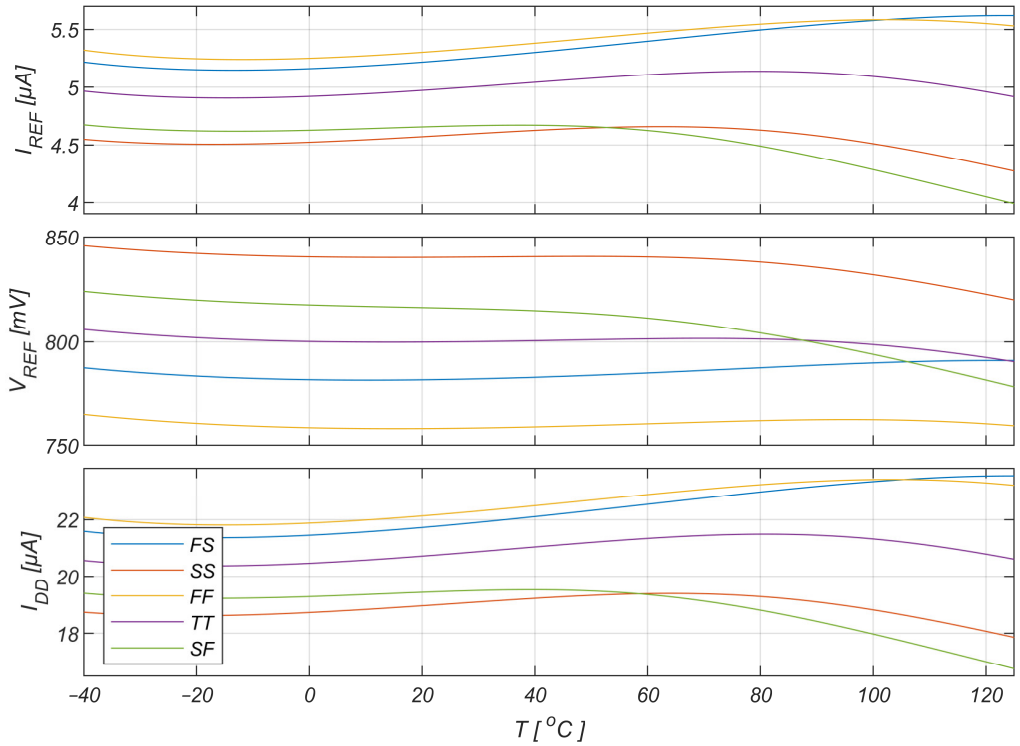


Figure 7. The reference output current and voltage versus temperature for different process corners at supply voltage 1.2 V.

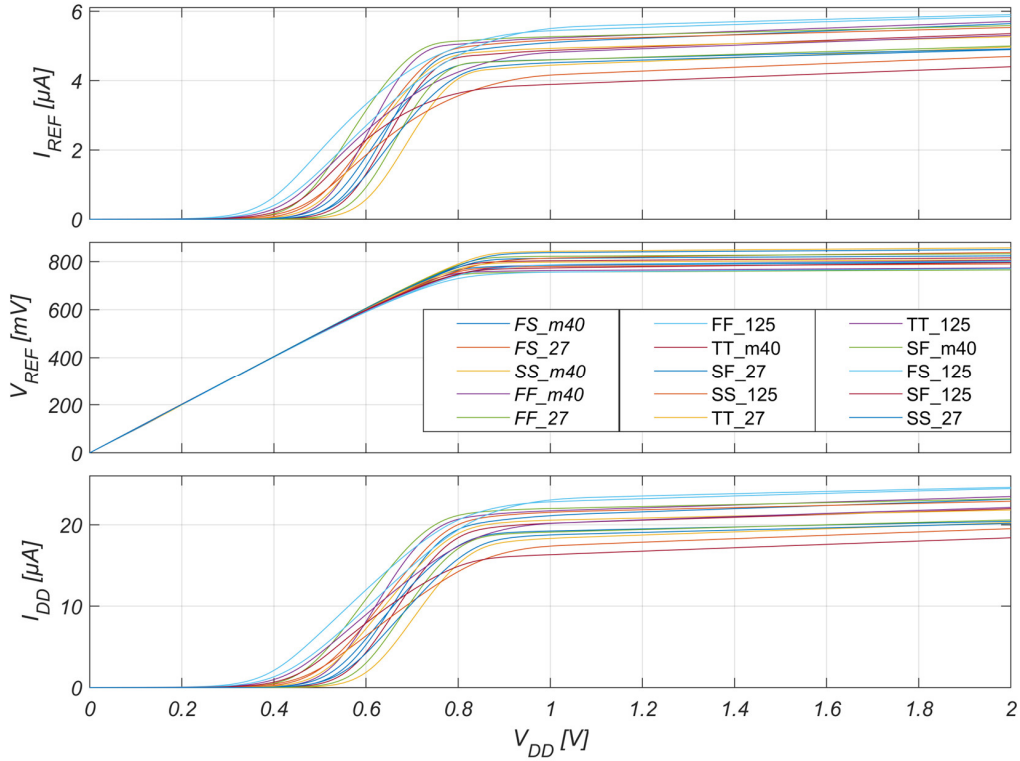


Figure 8. The output reference voltage and current as a function of supply voltage for all process corners and edge temperatures.

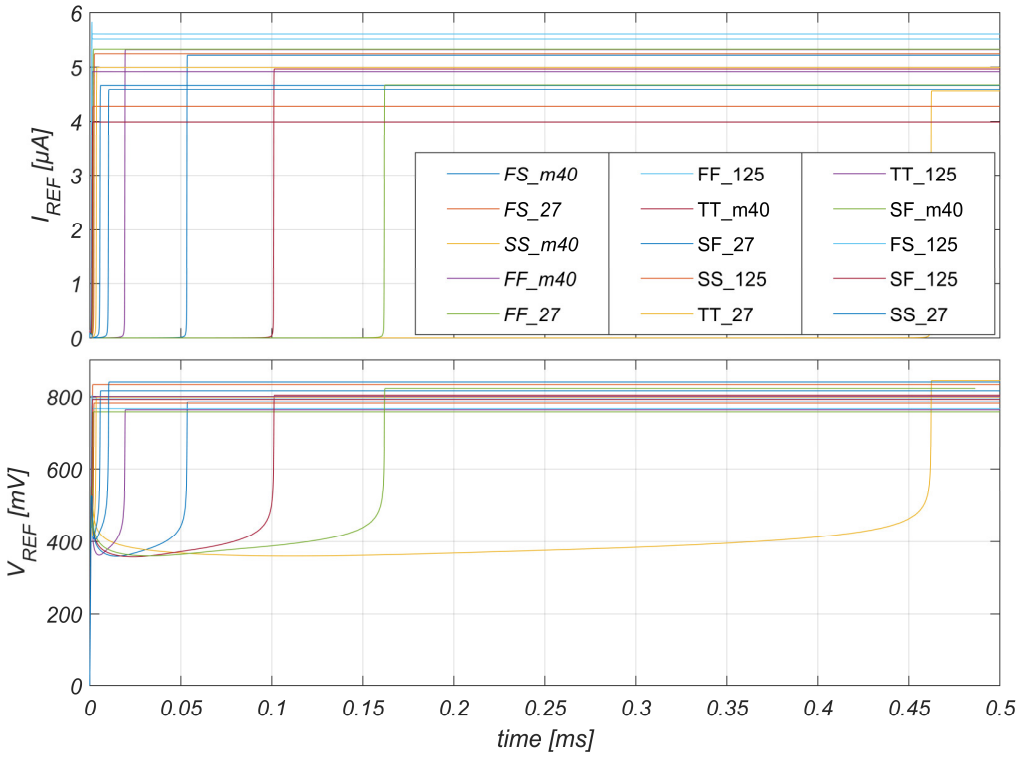


Figure 9. Transient response of the voltage and current source at start-up for all process corners and edge temperatures at supply voltage 1.2 V.

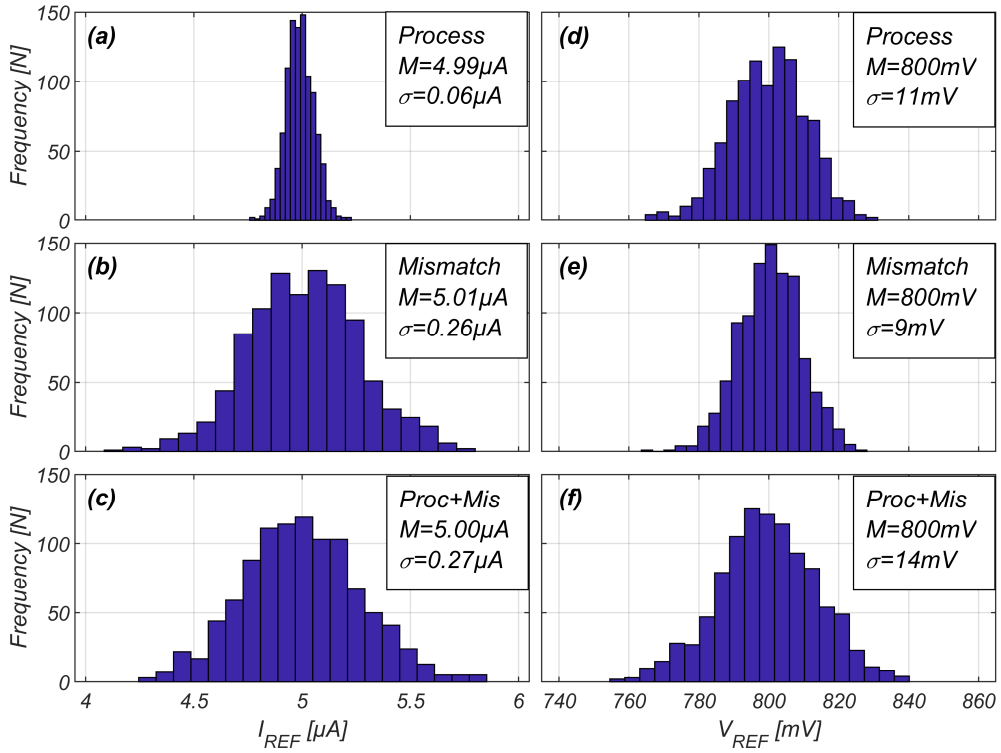


Figure 10. The results of the Monte Carlo simulations of I_{REF} and V_{REF} at 27 °C for 1000 runs at supply voltage 1.2 V. (**a**,**d**) Variation in the process parameters only. (**b**,**e**) Variation in device matching only. (**c**,**f**) Variation in device matching and process parameters simultaneously.

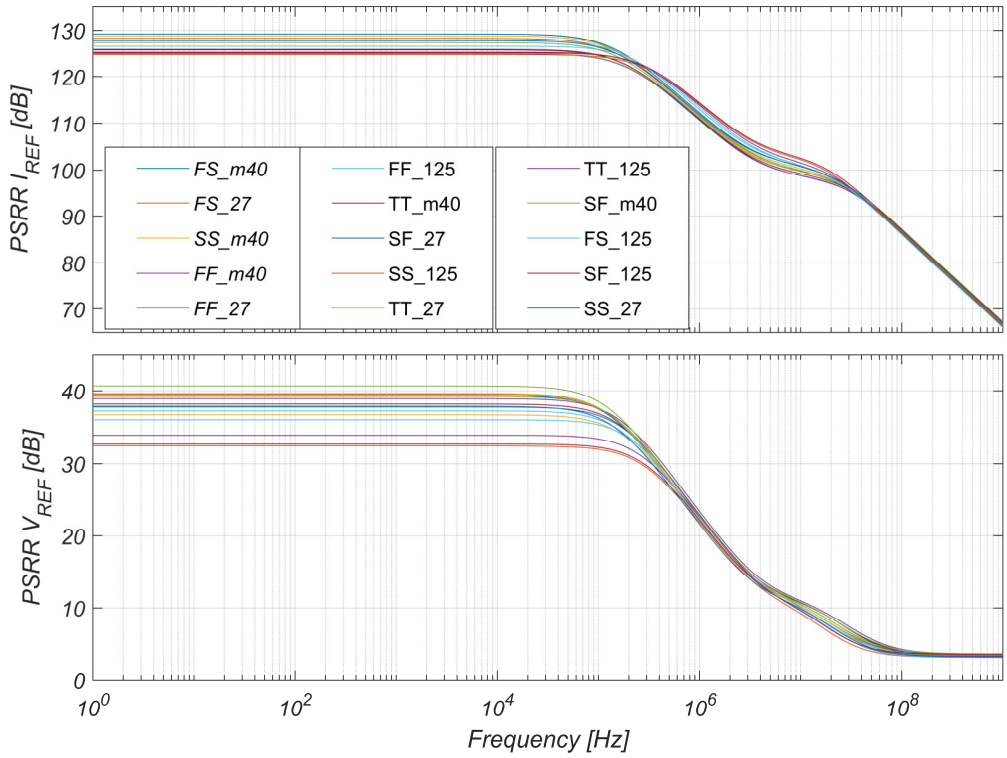


Figure 11. Post-layout simulated PSRR of the voltage and current reference source for all process corners and edge temperatures at supply voltage 1.2 V.

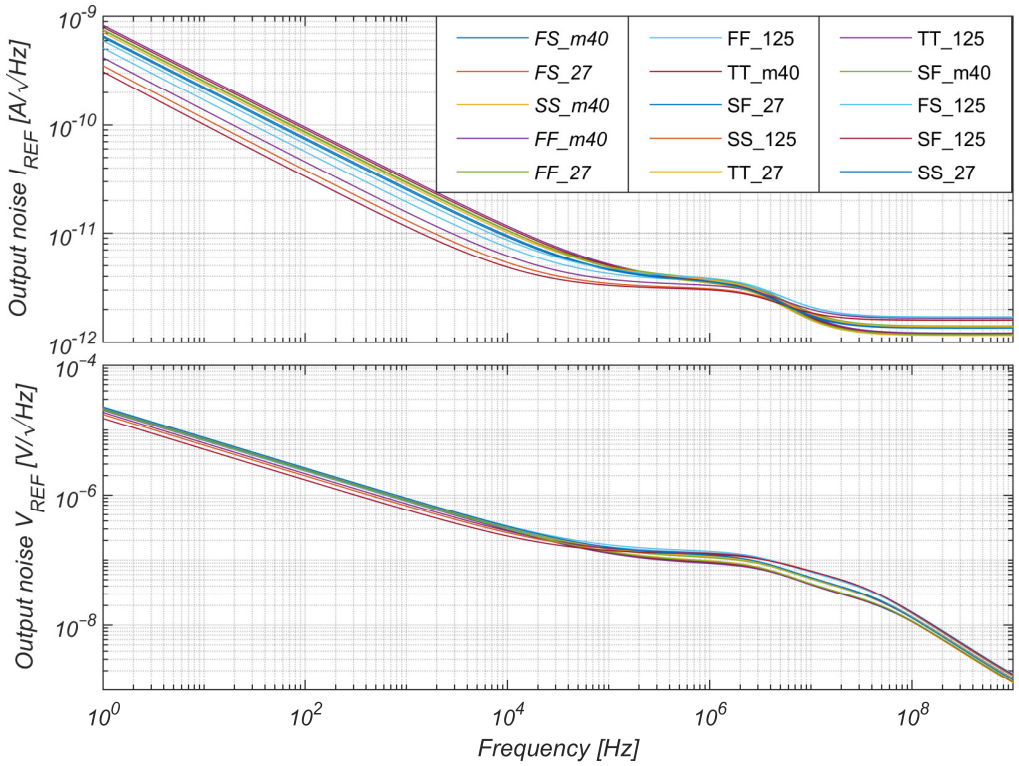


Figure 12. The spectral density of output noise from reference voltage and current source for all process corners and edge temperatures at supply voltage 1.2 V.

The power supply rejection ratio (PSRR) as well as output noise, without any filtering capacitors, of I_{REF} and V_{REF} are shown in Figures 11 and 12.

The output voltage and current noise characteristics presented in Figure 12 show that in example implementation of the proposed circuit, the noise performances are affected at a lower frequency by 1/f noise due to the small area of the gate in transistors M_5 and M_7. The designers could increase the area of these pairs, if possible, to decrease 1/f noise. However, the noise reduction at low frequencies in the presented architecture is mainly accomplished by operation in the subthreshold region by all MOSFETs. The 1/f (flicker noise) is generally lower in the subthreshold region of a MOSFET transistor. This is because, in the subthreshold region, the drain current is significantly lower compared to the region above the threshold. Since flicker noise is closely related to the current flowing through the transistor, a lower current results in less noise. Flicker noise in MOSFET transistors is caused by charge trapping and release at the interface between the semiconductor and the oxide layer, leading to current fluctuations in the channel. In the subthreshold region, where the transistor operates with very low current (lower current density), these fluctuations have a smaller overall impact on the total current, thus reducing the flicker noise. In contrast, in the above-threshold region, where the current is higher, flicker noise becomes more prominent. The equivalent output noise in the presented novel source architecture is comparable with the state of the art.

4.2. Measurement Results of the Example Implementation of a Novel Current–Voltage Source

The circuit was designed using the Virtuoso Schematic and Layout Editor tools. The simulations and analysis were performed with the Spectre simulator and ADE tools. The parasitic elements were extracted with the Calibre PEX. The presented circuit was manufactured and measured. The voltage and current reference source are marked in Figure 13. The circuit is meant to provide a stable reference voltage level and bias current for the RF Front-End in the GNSS (Global Navigation Satellite System) chipset. The details of the reference source topography in the manufactured silicon die are hidden by dummy-fill metal, and that is why it is not visible on the probe station.

The reference voltage–current source was fabricated in the MPW Service shuttle run. The bare dies were connected by DC needles on the Cascade Summit 12000B-AP probe station. The samples were measured separately one by one using an Agilent B1500A semiconductor-device analyzer. The analyzer was equipped with a B1517A high-resolution source/monitor unit (HRSMU) with multiple, multipurpose sources. One of them was configured in Force mode in order to supply the circuit under test, and two others were used in Sense mode to measure the reference output voltage and current, respectively. The voltage measurement input resistance of HRSMU was 10 TΩ.

The measurement results are presented in Figure 14 in the form of I_{REF} and V_{REF} distribution among 90 dies. The experimental results show that the spread between dies in reference current and voltage values is not worse than MC simulation results. The small shift in global process parameters across all manufactured chips is visible in lower output current and higher output voltage in comparison to the MC post-layout simulations results. However, it is still smaller than the simulated process corner sensitivity.

The example implementation of the proposed circuit, which is presented in Section 4, was designed to provide I_{REF} with high PSRR and small output noise in the active mode of SoC at the cost of power consumption. However, the proposed architecture of the reference voltage–current source was also designed for low-power applications without sacrificing some of the key performance. The low-power implementations are summarized in Table 4 as design Nos. 1, 8 and 9. The key parameters in those implementations were 22 ppm/°C, 72.4 ppm/°C and 31.5 ppm/°C respectively for TC. The wide supply voltage range was also ensured. The total power consumption of fabricated design No. 8 is only 29.7 nW, which was dedicated for low-power medical devices. The power reduction of the proposed solution is possible but with a compromise in AC parameters like PSRR and output noise.

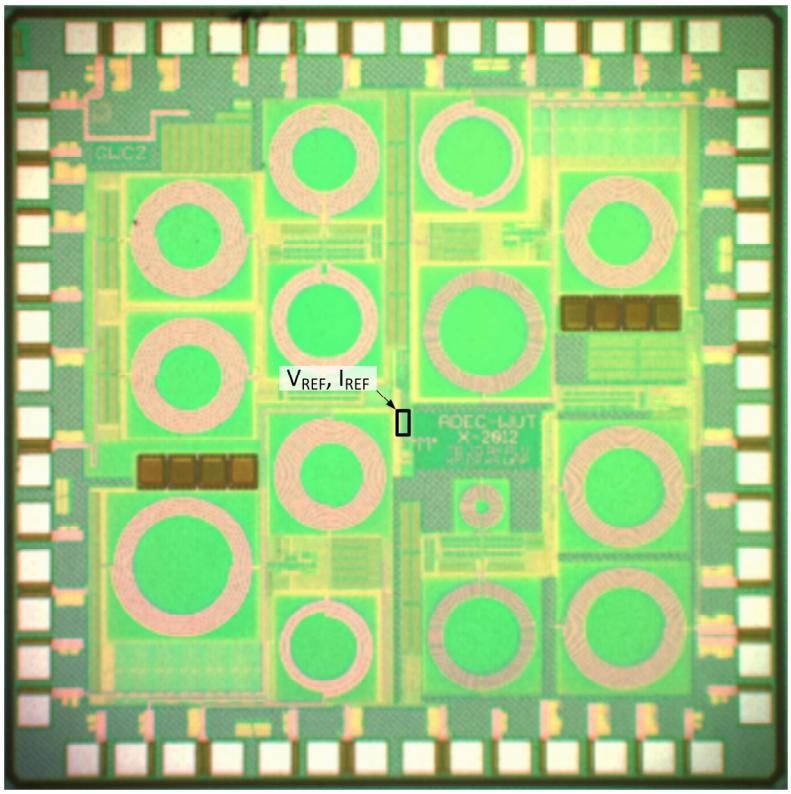


Figure 13. Microphotography with reference voltage and current source as a part of GNSS RF Front-End.

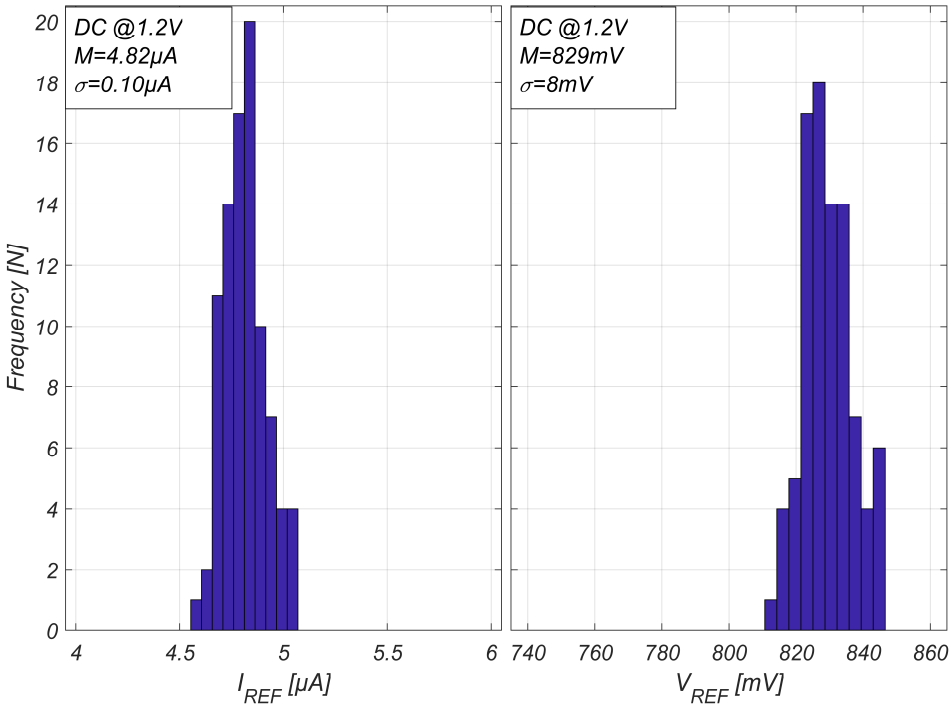


Figure 14. Histogram of I_{REF} and V_{REF} measured on 90 manufactured silicon dies at 27 °C and supply voltage 1.2 V.

The proposed novel voltage–current reference source was implemented in ten different designs for seven different CMOS technologies, and the obtained parameters are summarized in Table 4. Designs No. 7 (presented above in detail) and No. 10 were implemented

as a simultaneous two-in-one voltage–current reference source. The described architecture is silicon-proven in submicron and nanometer technologies—designs 4, 5, 7, 8, 9, 10. The measurements of the manufactured chips confirmed their correct operation and agreed with the simulation results, although in some cases, the variations in the output value were larger than expected.

Table 4. Parameters of the designed voltage and current reference sources at typical process corner, 27 °C, and nominal supply. Designs not marked by * or ** present post-layout simulation results.

No.	Technology	V_{REF} [V] I_{REF} [A]	I_{DD} [A]	V_{DD} [V]	TC [ppm/°C]	Process Sens. [%]	Line Sens. [%]	Settling [s]	Area [μm^2]
1	ATMEL 0.5 µm *	1.105 V	351 n	1.4–7.0	22.0	±9.0	±2.7	–	–
2	IBM 180 nm RF	1.25 V	3.21 µ	1.4–2.0	52.3	±3.8	±1.2	2.2 µ	14,900
3	IBM 180 nm HV	1.248 V	13.1 µ	1.4–2.0	213	±2.9	±1.8	2.0 µ	30,700
4	SMIC 180 nm **	1.244 V	31.6 µ	1.4–3.63	210	±1.0	±1.5	16.6 µ	1900
5	LFoundry 150 nm **	1.137 V	24.5 µ	1.8–3.63	104	±0.69	±0.6	6.9 µ	13,300
6	UMC 130 nm (1)	784 V	13.2 µ	0.9–2.0	40.7	±5.2	±0.8	513 n	1000
7	UMC 130 nm (2) **	829 mV 4.82 µA	14.46 µ	0.9–2.0	118 280	±5.2 ±7.4	±0.9 ±4.0	4.7 µ	1200
8	UMC 90 nm (1) **	409 mV	270 n	0.9–3.3	72.4	±3.7	±3.0	16.3 µ	1100
9	UMC 90 nm (2) **	337 mV	9.0 n	0.7–3.3	31.5	±5.2	±1.5	81.9 µ	1300
10	UMC 90 nm (3) **	659 mV 845 nA	5.7 µ	1.0–2.0	53.5 185	±7.2 ±15	±1.2 ±0.9	80 µ	8200

* pre-layout simulation results. ** measurement results.

5. Conclusions

The parameters of the representative design Nos. 5, 7, and 9 from Table 4 are compared with other published voltage and current reference sources in Table 5. The presented novel only-CMOS circuit that simultaneously performs the functions of a voltage and current reference source without the use of passive devices or BJTs is comparable with other published achievements in the state of the art in terms of key parameters like PVT sensitivity with small silicon area and power consumption kept.

In general, the high robustness of the proposed circuit in response to PVT variations and device mismatch is confirmed by simulations and measurements. It achieves a good trade-off between the key parameters, such as power consumption, silicon area and PVT stability. The power consumption can go below 30 nW for 3.3 V supply voltage (design No. 9). In the presence of the process corners variations, the untrimmed mean temperature coefficient across all the designed reference voltage and current sources is 115 ppm/°C in the temperature range between −40 °C and 125 °C and it is still comparable with the state of the art. The presented architecture shows low sensitivity (the average of 5.5%) of output reference voltage and current to CMOS process variations and device mismatch. The presented examples of implemented reference source designs prove the transferability of this architecture between different technologies and nodes.

The easy integration in standard CMOS technology in a very small silicon area without the need to use highly resistive resistors is the key feature of the proposed circuit. For these reasons, the described solution is already used in many wireless and low-power mixed-signal integrated circuits. Moreover, the design solution of the voltage reference source proposed in the article is referred to by inventors from global EDA/CAD vendors in their patent applications [28].

Potential improvements to the presented solution could include an extra AC start-up circuit with a capacitor to speed up V_{REF} and I_{REF} settling time in all PVT corners. This will be necessary for applications that switch very often between active and sleep modes. The exemplary implementation in Figure 5 contains only basic start-up, which is good enough in this particular design, where SoC raises the reference source immediately after battery replacement and the user does not care about long settling time. The future work will focus on the implementation of the proposed architecture in FD-SOI technologies to check the

potential usage of the back-gate bias technique for further PVT stabilization of the reference source and potential usage for post-production auto-tuning.

Table 5. Summarized performance of the proposed voltage and current reference source and comparison with the state-of-the-art simulated and measured reference source solutions.

Source	Process	V_{REF} [V] I_{REF} [A]	I_{DD} [A]	V_{DD} [V]	TC [ppm/°C]	Process Sens. [%]	Line Sens. [%]	Settling [s]	Area [μm^2]
This work (5)	150 nm **	1.137 V	24.5 µ	1.8–3.63	104	±0.69	±0.6	6.9 µ	13,300
This work (7)	130 nm **	829 mV 4.82 µA	14.46 µ	0.9–2.0	118 280	±5.2 ±7.4	±0.9 ±4.0	4.7 µ	1200
This work (9)	90 nm **	337 mV	9.0 n	0.7–3.3	31.5	±5.2	±1.5	81.9 µ	1300
[17]	65 nm	6.45 µA	47 µ	2.6–3.63	55	±3.0	-	-	7000
[10]	90 nm	718 mV	1.3 µ	1.05–1.35	101	-	±4.1	-	-
[18]	90 nm **	771 mV	173 n	1.6–3.6	40	±2.6	±1.9	-	30,000
[19]	90 nm	724 mV	18.7 µ	1.0–1.2	83	±3.9	-	-	19,910
[13]	130 nm	319 mV	80 n	0.5	2.2	±7.8	-	-	250
[20]	130 nm **	798 mV	26 µ	1.0–2.0	6.64	±0.8	±0.2	-	20,000
[21]	130 nm	602 mV	60 µ	1.2	2.2	±1.4	-	-	-
[22]	130 nm **	501 mV	300 n	0.7–1.8	29.3	±4.8	±0.2	-	23,000
[23]	130 nm **	50.2 µA	-	1.2	29	±0.3	-	-	38,000
[24]	150 nm **	90 µA	-	1.0	257	±5.0	-	-	38,000
[25]	180 nm **	144 µA	83 µ	1.0	185	±7.0	-	-	-
[26]	180 nm **	54.1 µA	700 µ	1.8	47.4	-	-	-	55,000
[27]	180 nm	2.03 µA	7.1 µ	1.0	45	±15	-	-	-

** measurement results.

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