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23.5–27.5 GHz Band Doherty Power Amplifier Integrated Circuit Using 28 nm Bulk CMOS Process Based on Dynamic Power Dividing Network

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Abstract: This paper presents a Doherty power amplifier (DPA) integrated circuit (IC) designed to have enhanced gain, efficiency, and AM-AM characteristics through a dynamic power dividing technique, which can control the power dividing ratio according to the input power. Since this multi-purpose dynamic power dividing network also provides the phase offset and impedance matching at the interstage network needed for appropriate DPA operation, the active IC area could be reduced. To verify the proposed technique and its analysis, the DPA was implemented with a 28 nm bulk CMOS process for the fifth-generation (5G) new radio (NR) millimeter-wave frequency band of 23.5–27.5 GHz. The measured results showed a gain of 20.3–21.9 dB, saturated output power of 14.0–15.2 dBm, power added efficiency (PAE) of 22.8–26.7% at the peak power, and PAE of 14.6–17.6% at the 6 dB output power back-off (OBO).

Keywords: Doherty power amplifier; millimeter-wave (mm-wave); CMOS; output power back-off extension technique

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1. Introduction

The demand for high data rates in wireless communication systems has led to the development of modulated signals, which have high peak-to-average power ratio (PAPR) and wide signal bandwidth. However, due to the increasing PAPR, power amplifiers (PAs) should be operated with a large output power back-off (OBO) level for linearity, thereby resulting in efficiency degradation. To overcome this efficiency degradation, the Doherty power amplifier (DPA) has been used where such linear PAs are needed due to its advantage of having a wide range of high efficiency even at large OBO levels [1–27].

Meanwhile, there are many challenges in designing DPA ICs compared to conventional linear PA design. The DPA load network, which is composed of multiple quarter-wave transmission lines with various forms of its equivalent circuit, tends to be bulky. Compared to a single Class-AB PA, the DPA also has its power gain almost halved at the low input power, when the peaking amplifier is biased to a Class-B or -C, since the DPA power dividing network splits the input power equally between the carrier and peaking amplifiers. It can cause poor AM-AM characteristics with a Class-B or -C peaking amplifier as well. Linearization techniques such as digital pre-distortion (DPD) are not always available in DPA IC applications, and therefore, DPA ICs should have tolerable linearity on their own. As a result, the peaking amplifier is operated, with a deep Class-AB condition in many cases, for the linear operation of the overall DPA and with a little sacrifice of the potential efficiency improvement at large OBO levels.

In recent studies, DPAs have been designed to operate at millimeter-wave (mm-wave) frequencies to meet the requirements of the 5G NR communication standards [4–9]. The increased mm-wave carrier frequency allows the 5G NR modulated signal to have

a higher data rate even with a relatively lower fractional bandwidth, compared to the sub-6 GHz systems. However, DPA design at mm-wave frequencies can be very challenging due to limitations such as device speed or high insertion loss of impedance matching networks. Degradation of the DPA main stage power gain will reduce the overall efficiency, and many of the efficiency improvement techniques used at lower frequencies cannot be applied.

Multi-way and multi-stage techniques will have low power gain due to the multi-branch power dividing networks, and asymmetric DPAs will have to select the trade-off of reduced power gain or poor AM-AM characteristics in many cases. Increasing the peaking periphery for efficiency improvement in itself will not be as successful as at sub-6 GHz frequencies since the performance downgrading of enlarged transistors is more critical at mm-wave. There are also reported works that focus on extending the DPA OBO range, even with symmetric transistors, through matching complex impedances at the DPA power combining node [10,19]. But these methods do not fundamentally solve the issue since DPAs at mm-wave cannot depend on DPD, and the peaking amplifier bias cannot be lowered as desired.

In this paper, a dynamic power dividing network is proposed, which has intentionally removed the isolation between the carrier and peaking amplifiers in order to use the variation of the input impedance of the peaking amplifier according to input power. The dynamic power dividing network is designed to drive more power to the carrier amplifier at the low input power level while driving more power to the peaking amplifier at the peak power level. This can improve the trade-off situation between the AM-AM and overall efficiency of the Doherty power amplifier. Since it has uneven power dividing at the low and peak power levels, the AM-AM can be flattened even when the peaking amplifier is put at a lower bias, which results in high efficiency.

As a result, this dynamic power dividing can enhance the power gain, especially at the low input power level, even while flattening the overall AM-AM characteristics. The improved AM-AM characteristics allow the peaking amplifier to have a deeper operation class toward Class-B or -C, which results in efficiency improvement and also opens the possibility of benefitting from applying various OBO extension techniques. The proposed DPA consists of a single drive amplifier that drives both the carrier and peaking amplifiers through the dynamic power dividing network, which was implemented at the interstage network. The appropriate phase offset, which was needed between the carrier and peaking amplifiers for load modulation and for the in-phase power combining at the load network, was also realized in the dynamic power dividing network, which made the overall topology compact.

For verification of the proposed dynamic power dividing network and its advantages in DPA operation, a DPA IC was designed with a 28 nm bulk CMOS technology for the 5G frequency band of 23.5–27.5 GHz. The simulated and measured performances will be provided and compared to previous related works.

2. Design of the Proposed DPA

2.1. Design of the Dynamic Power Dividing Network

Figure 1a shows a schematic diagram of the dynamic power dividing network proposed in this paper. It is implemented at the interstage of the 2-stage DPA and distributes the input power to the carrier and peaking amplifiers. While the conventional DPAs have used power dividers, such as a Wilkinson power divider or a quadrature hybrid, to achieve high isolation between the carrier and peaking amplifiers, the proposed dynamic power dividing network was designed to deliberately weaken the isolation and to use the nonlinear input impedance of the peaking amplifier for better performance. Z_{C_in} and Z_{P_in} of Figure 1 represent the input impedances of the carrier and peaking amplifiers, respectively. The input impedance of the peaking amplifier, Z_{P_in}, goes through a large transition while input power increases due to the nonlinear input capacitance, while Z_{C_in} of the carrier amplifier has relatively small variation over the input power [3]. Therefore, the transition

of Z_{P_in} can be utilized to provide different power dividing ratios at the DPA low and peak power levels by controlling design parameters of the interstage transformer, phase offset, and the subsidiary impedance matching network.

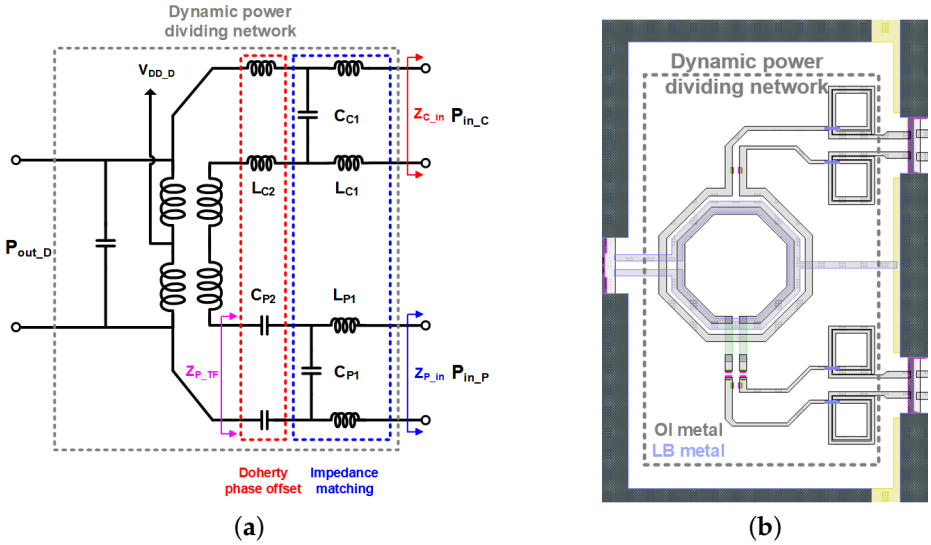


Figure 1. Proposed dynamic power dividing network: (**a**) Schematic; (**b**) Layout.

Figure 2 shows various dynamic power dividing ratios and simulated performances that were obtained from the dynamic power dividing networks with three combinations using differently optimized components compared to the conventional case using a hybrid power divider. The power dividing ratio (P_{in_C}/P_{in_P}) in Figure 2a represents the ratio of the power delivered into the carrier amplifier to the power delivered into the peaking amplifier while increasing the input power from the drive stage. Cases 1 and 2 have the peaking amplifier biased to Class-B and have the dynamic power division applied. The difference of the power ratio between the low and peak power levels is designed to be more than 3 dB for cases 1 and 2 as shown in Figure 2a. At peak power, case 1 has equal power division to the carrier and peaking amplifiers, and case 2 has 1 dB more power driven to the peaking amplifier at the peak power. Case 3 has the dynamic power division applied but has the peaking amplifier biased to Class-AB, and therefore, the variation of the power dividing ratio is low. Case 4 is the conventional case where the peaking amplifier is biased to Class-AB, and no dynamic power dividing is applied.

It can be seen in Figure 2a that the relatively large transition of Z_{P_in} can considerably boost the gain at the low power levels for cases 1 and 2 compared to cases 3 and 4, along with improvement of PAE resulting from the Class-B bias as shown in Figure 2b. Meanwhile, the AM-AM characteristics can be improved when appropriately more input power is driven to the peaking amplifier at the peak power level. Case 1, which has equal power delivered to the carrier and peaking amplifiers at the peak power level, shows the poorest AM-AM characteristics, as shown in Figure 2c. Case 2 has more input power to the peaking amplifier by 1 dB at the peak power level, but has slightly unfavorable AM-AM characteristics compared to the conventional case 4 due to the deeper class of the peaking amplifier. Case 3 shows good AM-AM characteristics, but it has lower PAE compared to cases 1 and 2 since it has more input power to the Class-AB peaking amplifier at the peak power level. The relationship of efficiency and dynamic range of power division is presented in Table 1.

In this paper, case 2 was selected and designed for the DPA configuration. Case 2 has advantages in enhanced power gain using the large variation of the power division ratio by more than 3 dB according to the input power level and in high efficiency with the Class-B peaking amplifier. The AM-AM characteristics are maintained at an acceptable level since it has uneven power drive by about 1 dB to the peaking amplifier at the peak power level. Figure 3 presents the simulated overall gain and PAE of the proposed DPA for

case 2 compared to the conventional DPA. Both cases were designed with an identical load network and a transistor configuration for the same saturated output power. Compared to the conventional case, case 2 exhibited 3.6 dB higher power gain, 4.1%p higher PAE at an OBO of 6 dB, and 3.3%p higher PAE at the peak power while maintaining good AM-AM characteristics.

Table 1. Case comparison of the dynamic power dividing network.

Case	Bias	Efficiency	Dynamic Range
Case 1	Class-B	25%	3.5 dB
Case 2	Class-B	25%	3.5 dB
Case 3	Class-AB	22%	1.0 dB
Case 4	Class-AB	20%	0.3 dB

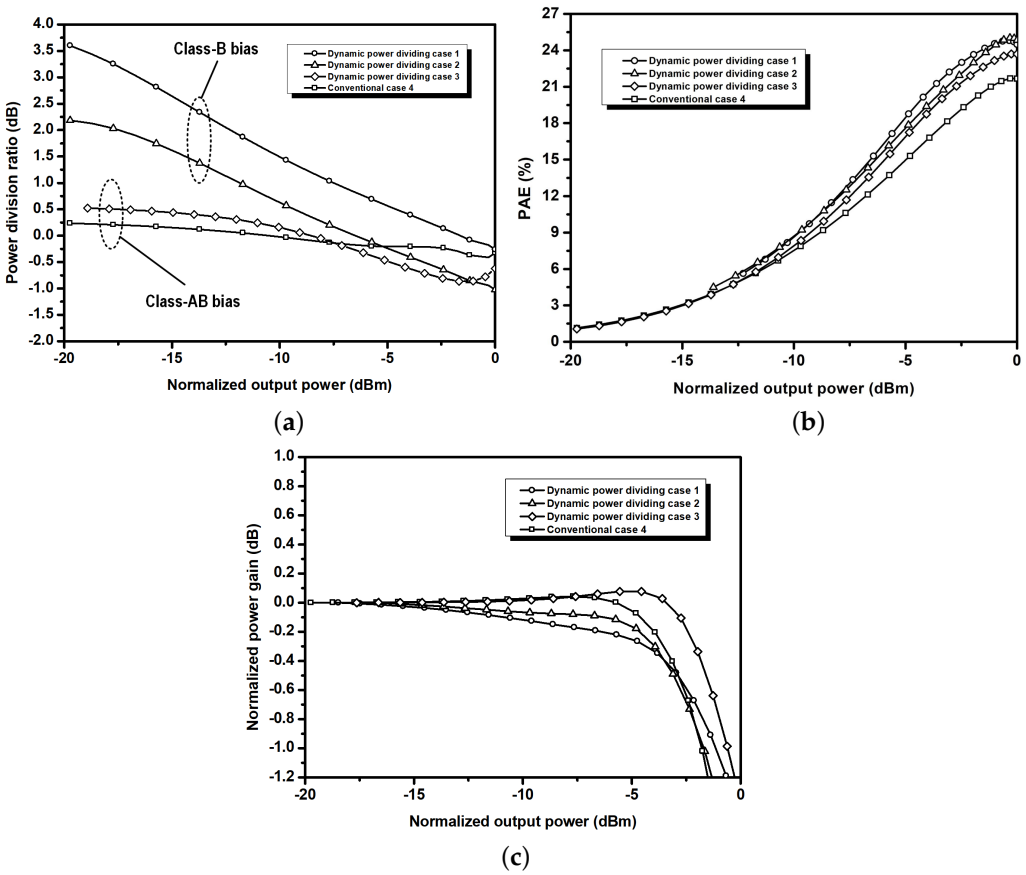


Figure 2. Three cases of the dynamic power dividing network compared to the conventional power divider: (**a**) Power dividing ratio; (**b**) Overall PAE; (**c**) AM-AM characteristics.

Figure 4 shows the design parameters of the interstage transformer used for the dynamic power dividing network. The interstage transformer was designed with a single primary turn with two secondary turns, which can feed the carrier and peaking amplifiers. Therefore, three coupling coefficients are formed between the separate turns, along with three values of self inductances. Altering the coupling coefficients of the interstage matching network would provide different power dividing ratios to achieve the various cases shown in Figure 2. For Case 2, the coupling coefficient between the driver-carrier and driver-peaking paths k21 and k31 had nearly equal values, with a little uneven drive to the carrier path as shown in Figure 4b. This set of values slightly boosts the power gain of the DPA low power operation and can still maintain favorable AM-AM when Z_{P_in} in Figure 1 is appropriately matched to Z_{P_TF} through the T-section matching network, using C_{P2}-C_{P1}-L_{P1}. The

T-section matching network L_{C2}-C_{C1}-L_{C1} of Figure 1 is also optimized to provide the DPA with the required phase offset and proper impedance matching for Z_{C_in}.

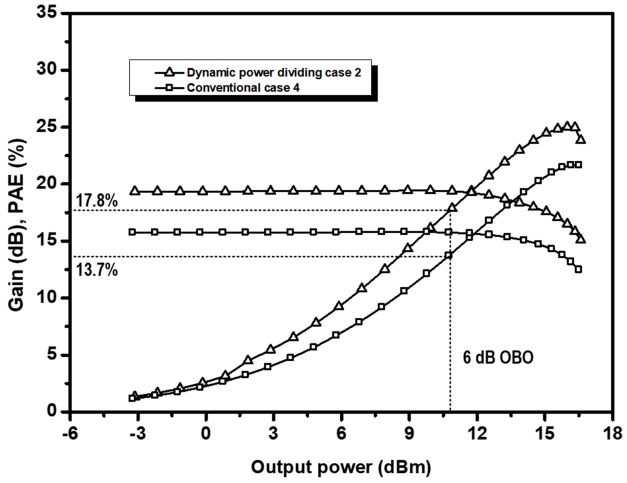
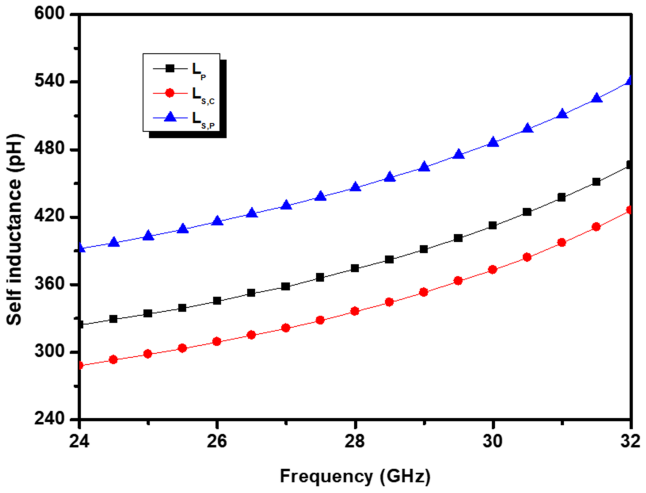
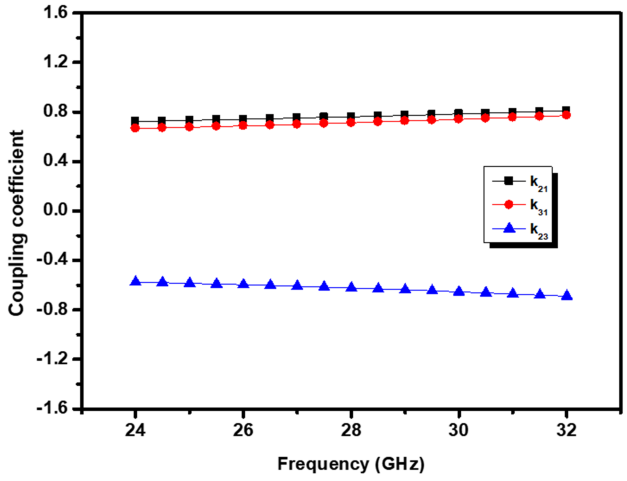


Figure 3. Large signal performance comparison with and without the dynamic power dividing network.



(**a**)



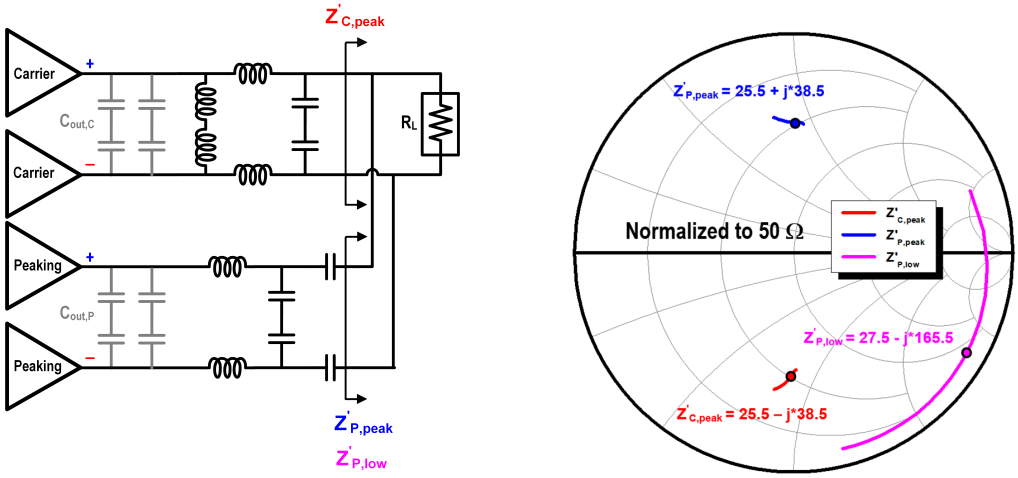
(**b**)

Figure 4. Design parameters of the interstage transformer: (**a**) Self inductance of the driver primary turn, carrier path secondary turn, and peaking path secondary turn; (**b**) Coupling coefficients.

2.2. Design of the DPA Load Network

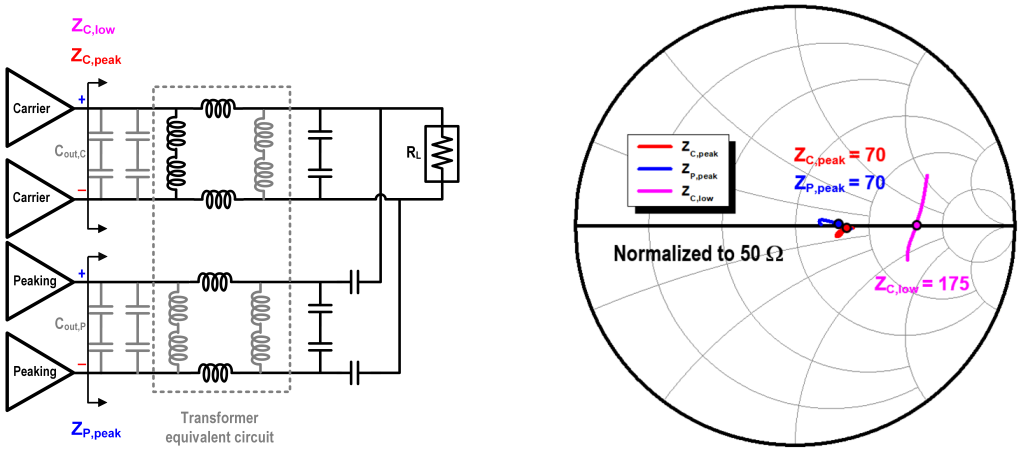
The dynamic power dividing network also affects the load design methodology due to its advantages in maintaining good AM-AM characteristics. Since there is more margin lowering the peaking amplifier bias with dynamic power dividing applier, it is more beneficial when the DPA load network is designed to have a wide OBO range. In this paper, the OBO extension method is applied to the DPA load network design since the dynamic power divider can relieve the burden on linearity when the peaking amplifier is required to have a deeper operation class for extended high-efficiency range.

Figure 5 presents the schematic and simulated results of the load network used in this design. The impedances at the power combining node are controlled to achieve the desired OBO extension. Figure 5b shows the impedance values at the center frequency for $Z'_{C,low}$, $Z'_{C,peak}$, and $Z'_{P,peak}$. Based on the design method through multiple backoff parameters presented in [10], the virtual stub (VS) parameter θ_k is 16.8°, and the outphased current combining (OCC) parameter $\Delta\theta$ is 56.5°. This set of backoff parameters will result in modulating the carrier load impedance 2.51 times higher for an OBO range of 7.02 dB. The load network is initially based on lumped components to match the required impedances, then are converted into transformer-based networks as shown in Figure 6.



(**a**) (**b**)

Figure 5. The proposed DPA load network: (**a**) Lumped model equivalent circuit; (**b**) Simulated impedances at the power combining node for 24–32 GHz.



(**a**) (**b**)

Figure 6. Practical implementation of the DPA load network: (**a**) Transformer equivalent circuit conversion; (**b**) Simulated impedances at the transistor current source planes for 24–32 GHz.

The schematic of the load network in Figure 6 is designed by adding additional shunt inductors and tuning shunt capacitor values to form a pi-type transformer equivalent circuit. The load network can, therefore, be implemented simply only with transformers and additional capacitors. Figure 6b shows the simulated results of the load impedances presented at the current source plane of the carrier and peaking amplifiers with the proposed DPA load network. The simulated values are well matched to the optimum load impedance of 70 Ω at peak power and 175 Ω at low power. The load modulation ratio result of 2.5 also agrees well with the original intention described in Figure 5.

Figure 7a presents the full schematic of the proposed DPA with the dynamic power dividing network. Unit transistor size with a gate length of 30 nm and unit gate width of 1 × 20 µm was selected, and a total of 6-unit transistors were used for one half of a differential cell. The differential cell was used identically for the drive and main stages to minimize the source degeneration effect and was supplied with a drain voltage of 1 V and a quiescent current of 10 mA. Cross-coupled capacitors were applied to neutralize the gate-to-drain capacitance at the fundamental frequency for higher gain and stability. The second harmonic impedance termination is realized using a resonance by adding a shunt inductor at the virtual ground made by shunt capacitors across the differential port.

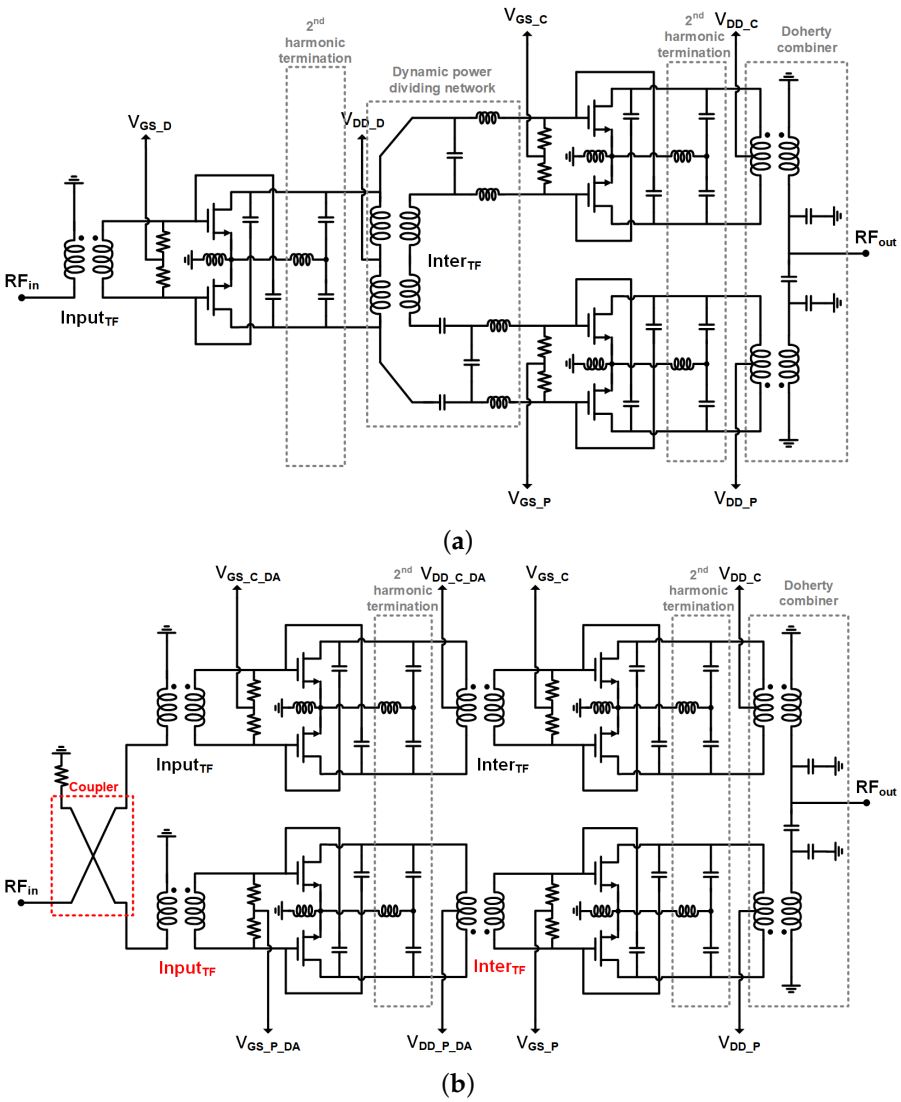


Figure 7. Full schematics of the DPAs with the following: (**a**) The proposed dynamic power dividing network; (**b**) A conventional dual-driven DPA using a hybrid coupler.

When compared to the conventional DPA that has dual-drive amplifiers for the carrier and peaking amplifiers, as shown in Figure 7b, the proposed DPA has two fewer transformers using a single drive amplifier. In addition, compared to the conventional case, which has an isolated power divider, the proposed DPA can have a smaller size since the dynamic power dividing network has a simplified structure including the phase offset line and impedance matching networks.

3. Implementation and Measurement Results

Figure 8 shows the photograph of the fabricated DPA IC using Samsung's 28 nm bulk CMOS technology. The DPA IC has an active area of 0.55 mm^2 and was evaluated by probing after chip-on-board (CoB) assembly. Figure 9 presents the simulated and measured small-signal characteristics of the proposed DPA. The small-signal measurements showed a gain of higher than 20 dB at the frequency band of 23.5–27.5 GHz.

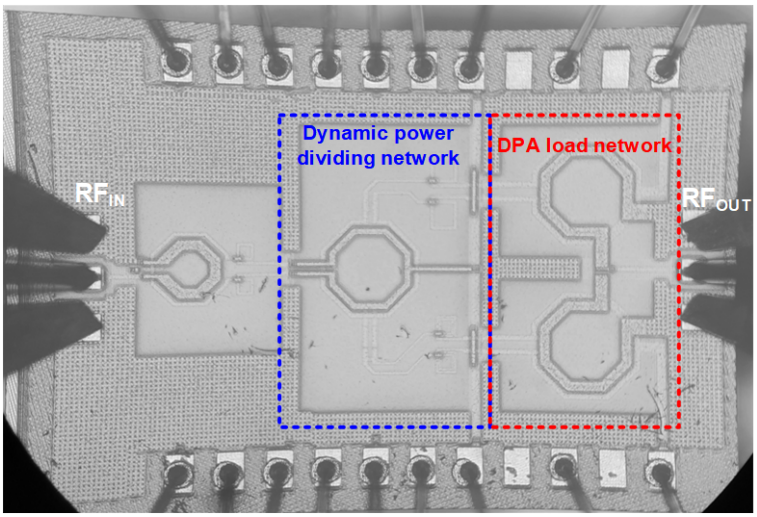


Figure 8. Micro-photograph of the implemented DPA IC.

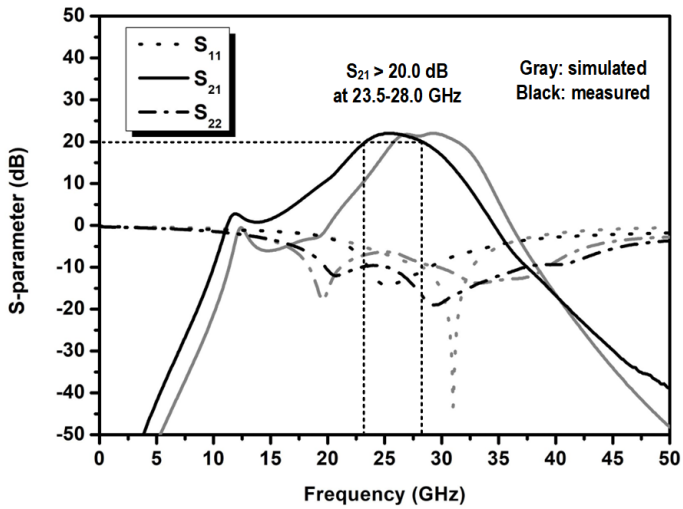


Figure 9. Simulated and measured S-parameters of the proposed DPA.

Figure 10 shows the measurement results using a continuous wave (CW) signal for the frequency range of 23.5–27.5 GHz. Figure 10a shows the measured power gain according to the output power, which shows saturated output power of 14.0–15.2 dBm at the targeted frequency band. Figure 10b presents the measured PAE performances, which are 22.8–26.7% at the peak output power and 14.6–17.6% at the 6 dB OBO. The measured CW performances show good agreement with the simulated results presented in Figure 3.

The measured results of the proposed DPA were compared to the state-of-the-art mm-wave PA ICs designed using CMOS technologies on Table 2. As intended through the dynamic power dividing technique, the designed DPA showed high power gain due to the gain boosting effect of direct power dividing. The proposed DPA also exhibited high efficiency levels at 6 dB OBO resulting from the OBO extension technique applied at the load network design.

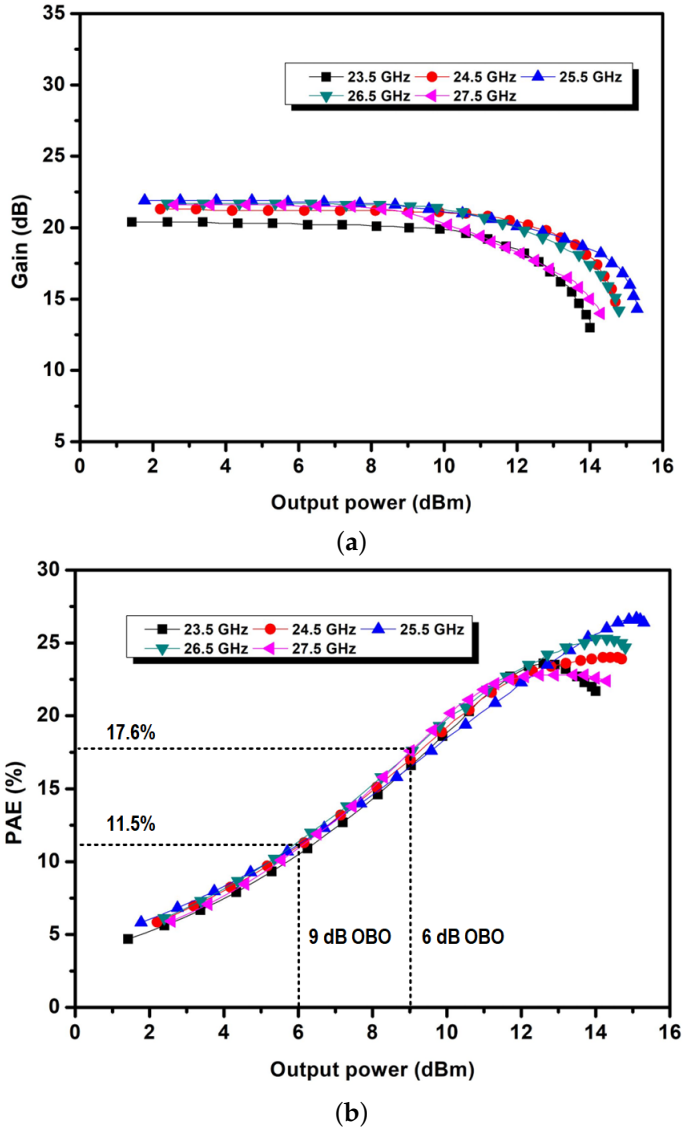


Figure 10. Measurement results using a CW signal at 23.5–27.5 GHz: (**a**) Power gain; (**b**) PAE.

Table 2. Comparison with state-of-the-art mm-wave CMOS PA ICs.

Ref.	Freq. (GHz)	Gain (dB)	P_{sat} (dBm)	PAE_{peak} (%)	$PAE_{6\text{-dB OBO}}$ (%)	Core Area (mm^2)
[4]	26	16.2	18.73	33.2	17.3	0.094
[5]	28	15.8	15.6	41	25	0.24
[6]	30	20	16.6	34.2	11.2 *	0.1
[7]	26	19	21.3	26.1	12.8	0.6
[8]	26	20	20.7	22.3	11.7	0.77
This work	25.5	21.9	15.3	26.7	17.6	0.55

* Graphically estimated.

4. Discussion and Conclusions

In this paper, a dynamic power dividing network, which utilizes the nonlinear input capacitance of the Class-B peaking amplifier, was designed to improve the power gain and efficiency of the DPA by removing the isolation characteristics of the power divider. The dynamic power dividing network was designed to drive more power to the carrier amplifier at the low power level and to drive more power to the peaking amplifier at the peak power level. Compared to previous works, the proposed design can have higher power gain since more power is sent to the carrier amplifier at low power. The efficiency at large OBO levels is also improved, compared to the conventional case, since the peaking amplifier bias can be lowered even while maintaining AM-AM through uneven power drive.

Also, the dynamic power divider makes the overall DPA more compact as it has a simplified structure with fewer transformers needed for impedance matching, compared to the conventional dual-drive topology, and it has the phase offset line merged into the impedance matching at the interstage network. For verification, the proposed DPA was designed for the targeted frequency band of 23.5–27.5 GHz and implemented with a 28 nm bulk CMOS technology. The measurement results exhibited a power gain of as high as 21.9 dB, saturated output power of 15.3 dBm, and PAEs of 26.7% and 17.6% at the peak output power and the 6 dB OBO, respectively, at the center frequency. The proposed DPA exhibited superior gain and efficiency performances at a given OBO level to the previously published CMOS DPA ICs at the mm-wave frequency band.

Author Contributions: Conceptualization, Y.C.C.; methodology, Y.C.C.; software, S.B.; validation, Y.C.C., S.B., and Y.Y.; formal analysis, Y.C.C.; investigation, Y.C.C.; resources, K.C.H.; data curation, K.-Y.L.; writing—original draft preparation, Y.C.C.; writing—review and editing, K.C.H., K.-Y.L., and Y.Y.; visualization, Y.C.C.; supervision, Y.Y.; project administration, Y.Y.; funding acquisition, Y.Y. All authors have read and agreed to the published version of the manuscript.

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