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A 23–29 GHz GaN Low-Noise Amplifier with Drain-to-Source Coupling Feedback

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Abstract: In this paper, a four-stage gallium nitride (GaN) low noise amplifier (LNA) using coupled-line (CL) feedback in a 0.15- μm GaN-on-SiC process is proposed. The electromagnetic coupling feedback between the drain and source of each transistor is employed to generate an additional signal path for neutralization, which enhances gain and improves stability performance. A series transmission line-capacitor-transmission line (TL-C-TL) network is introduced between stages of the LNA for wider band interstage matching. The measured results show that the designed LNA achieves a 3-dB bandwidth of 23.6 to 29.8 GHz, a peak gain of 23.7 dB at 25.8 GHz, and a minimum noise figure (NF) of 2.2 dB at 27.8 GHz. The output-referred 1-dB compression point (OP1dB) is 13 dBm. The total power consumption of the LNA is 200 mW.

Keywords: gallium nitride (GaN); low noise amplifier (LNA); coupled-line (CL) feedback



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1. Introduction

Fifth-generation (5G) communication has been developing rapidly in the past few years, and it provides low delay and a high data rate for various applications [1]. The low-noise amplifier (LNA) is an important component of the 5G RF front-end, which determines the sensitivity and dynamic range of the receiver. As the first amplifier following the antenna, the LNA is required to have a sufficiently high gain and a low noise figure (NF) [2].

In recent years, LNAs have mainly been designed and fabricated using CMOS and GaAs processes. CMOS LNAs have the advantages of low cost, low power consumption and high integration. P. Qin et al. [3] presented a compact wideband LNA utilizing the transformers for bandwidth extension based on the source degeneration. The LNA, fabricated using a 65-nm CMOS process, achieves a 3-dB bandwidth spanning from 15.8 to 30.3 GHz, and a minimum noise figure of 3.3 dB. Erkut Gurol et al. [4] introduced a two-mode, feedback-controlled LNA developed using 130-nm CMOS silicon-on-insulator (SOI) technology. The LNA indicates a high linearity in the IIP3 value from -1.5 to $+5$ dBm at 25 GHz. On the other hand, the LNAs based on GaAs have the advantages of high gain and ultra-low NF at high frequencies. Z. Wang et al. [5] presented an 18.7–36.5-GHz GaAs LNA with a diode-based adaptive bias circuit to improve the linearity and drain current. The measured gain and minimum NF were 15.9 dB and 1.5 dB, respectively. However, LNAs based on CMOS and GaAs are easy to damage at high-power inputs, requiring additional limiter circuits, which contribute to the higher total NF of the receiver [6].

Due to the high breakdown electric field and high electron saturation velocity, the gallium nitride (GaN) high electron mobility transistor (HEMT) device is a good candidate for LNA applications. Moreover, the high-power handling ability of GaN makes it possible for LNA to remove the additional limiter circuits, which avoids introducing excess noise and lowers the total NF of the receiver [7]. Thus, GaN HEMT has unique advantages in LNA applications.

Several GaN LNAs in 5G millimeter-wave bands with good performance have been recently reported. Hyunbae Ahn et al. [8] described a 26–30 GHz GaN LNA which employed a series inductor to enhance stability. The demonstrated design achieved a gain of 20.2 dB and an NF of 2.4–2.5 dB. The design attained a μ -factor up to 7.7 at the operating frequency. L. Pace et al. [9] presented a Ka-band GaN LNA with 1.5 dB NF. By optimizing the DC bias point and geometry, the LNA achieved only 150-mW power consumption. Hailiang Liu et al. [10] proposed a 23–31 GHz high-gain GaN low-noise amplifier using T-type matching networks and multiple feedback techniques. Z. Dai et al. [11] introduced a low-power and high-gain GaN LNA, operating at Ka-band, which can achieve a gain of 34–37 dB with a continuous wave of more than 2 W over 24 h. F. Thome et al. [12] demonstrated a broadband GaN transceiver integrated with a three-stage LNA. The stand-alone LNA yields an NF of 1.5–2.4 dB from 25 to 40 GHz.

Among these well-designed LNAs, source degeneration is a commonly used technique that helps to improve stability and simultaneous noise and input matching (SNIM). However, its effect on stability improvement is limited. Also, when the LNA works near the cut-off frequency (f_T) of the transistor, the gain degradation due to source degeneration is unbearable. The gate-to-drain capacitor (C_{gd}) of the transistor is regarded as one of the main reasons for gain and stability degradation because it couples the input circuit and output circuit in potentially deleterious ways [13]. To mitigate the undesirable effects of C_{gd} , many efforts have been made such as cross-coupled capacitors [14,15] and transformer feedback [16,17]. However, the cross-coupled capacitors can only be applied in differential structures, and the transformer feedback technique usually demands multiple metal layers.

In this paper, we present a GaN LNA fabricated in a 0.15- μ m GaN process for 5G applications. The epitaxial layers of the GaN HEMT are grown on a 100- μ m SiC substrate. The GaN HEMT devices utilized in this work exhibit excellent performance metrics, making them highly suitable for high-frequency and low-noise applications. The devices have a measured breakdown voltage of 120 V, ensuring robust operation in high-voltage environments. The devices also demonstrate a maximum transconductance of 425 mS/mm, indicating strong control over channel current with gate voltage variation. Furthermore, the maximum drain current reaches 985 mA/mm, providing ample current handling capability. The f_T of the GaN HEMT in the process is about 33.8 GHz. Since the LNA aims to operate in the band that is close to the f_T of the HEMT, a four-stage common source structure is adopted and a drain-to-source feedback (DSFB) technique using a coupled line (CL) is proposed to enhance gain with source degeneration and improve stability. In addition, an improved π -type network including a series transmission line-capacitor-transmission line (TL-C-TL) network is applied for wideband interstage matching. The proposed LNA can achieve competitive characteristics of high gain, low NF and high stability.

This paper is organized as follows. Section 2 describes a detailed analysis of the LNA including the proposed DSFB technique using CL, interstage matching network (ISMN), and the overall design of the implemented circuit. Section 3 illustrates the measurement configuration and compares the simulated and measured results. Section 4 gives the conclusion of this paper.

2. Circuit Design

To achieve the high gain and low NF, a four-stage cascade common-source structure is utilized in this work. Figure 1 shows the schematic of the proposed LNA. The transistor size of $2 \times 50 \mu\text{m}$ is selected for all stages after the trade-off between low noise and high gain. A drain voltage of 5 V is applied and a drain current of 10 mA is identically chosen as the bias point for each stage considering maximum gain (G_{max}), minimum noise figure (NF_{min}) and power consumption. The DC voltages are fed to drain and gate through transmission lines (TLs), which also work as RF chokes and short stubs in impedance matching networks.

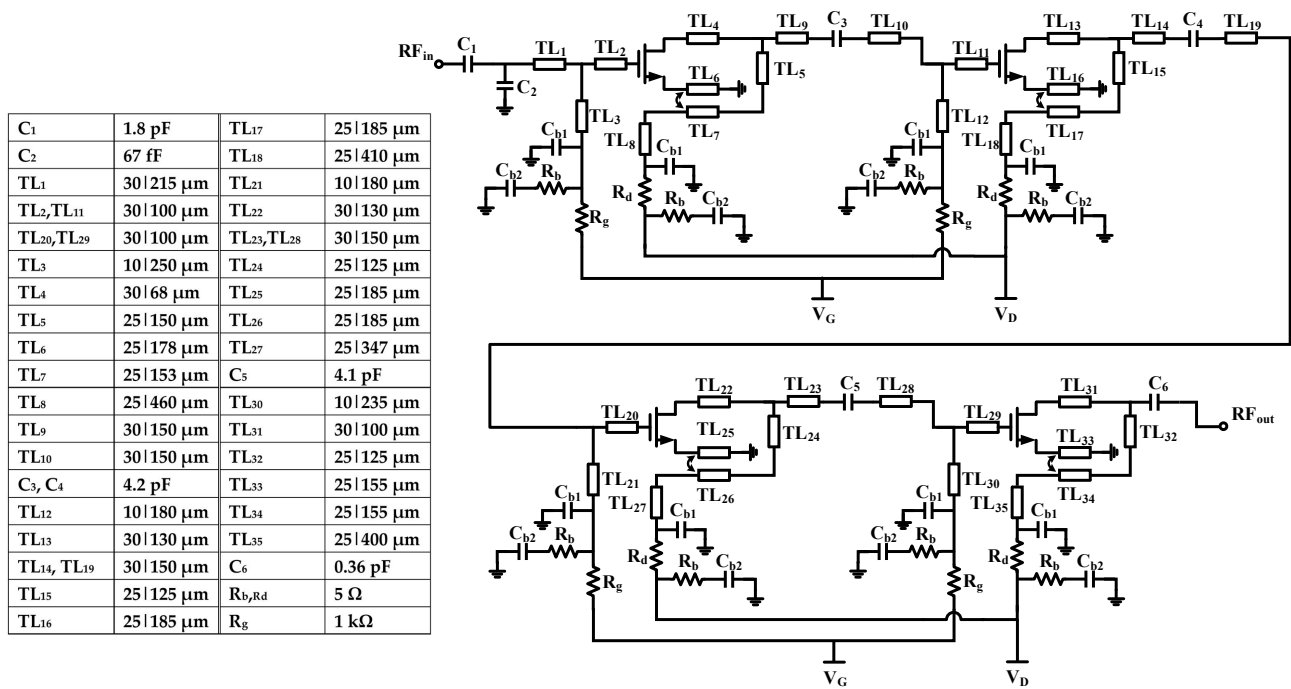


Figure 1. Schematic of the proposed LNA.

Bypass networks including a resistor (R_b) and two capacitors (C_{b1} and C_{b2}) are introduced near the DC pads to enhance the isolation of the RF choke. Instability at low frequencies can lead to the oscillation of the LNA due to external low-frequency interference, thereby affecting its normal operation. Thus, a small resistor (R_d) of 5 Ω is added to the drain bias network to improve low-frequency stability. In wireless communication and radar systems, receivers may encounter high-power interference signals or environmental noise that suffers from nonlinear distortion or damage due to excessive input signals. Therefore, a large resistor (R_g) of 1 k Ω is added to the gate bias network to improve survivability under high input power by limiting gate current. The input matching is realized by an asymmetric network consisting of a series capacitor (C_1), a shunt capacitor (C_2), two series TLs (TL₁ and TL₂) and the shunt stub (TL₃) of the first-stage gate. The input matching network is aimed at achieving a good balance between NF and input return loss.

To obtain high gain, low NF and high gain flatness at the same time, the four stages are designed with different performance focuses. The first stage is designed with the minimum NF because it contributes most to the overall noise according to Friis' Equation. Since the gain of the first stage is not sufficient to effectively suppress noise, the second and third stages are designed to achieve high gain around the center frequency and still keep moderate NF. The last stage is designed to improve gain flatness by providing high gain at high frequency and low gain at low frequency, which balances the uneven distribution of gain in the previous stages.

TLs are applied in the source of each transistor as source degeneration to improve impedance matching and stability. Furthermore, the TLs of the drain and source of each stage are coupled together to form a coupled line (CL), providing feedback from the drain to the source. By adjusting the coupling coefficients and coupling lengths of the CLs, the gain and stability of the LNA can be improved. Moreover, a π -type network composed of shunt TL and series TL-C-TL is proposed as three ISMNs to expand the matching bandwidth.

2.1. Drain-to-Source Coupled-Line Feedback Analysis

To improve the gain and stability performance of the LNA simultaneously, a neutralization technique utilizing DSFB is proposed, which cancels the signal through C_{gd} by adding an additional signal path. The signal flowing through the additional signal path neutralizes the signal on C_{gd} , which increases forward gain and reverse isolation.

The additional signal path is realized by CL in the proposed LNA. When two unshielded TLs are placed in parallel and close enough to each other, the signal can be coupled between the lines due to the interaction of the electromagnetic fields. The voltage response can be calculated by applying an even–odd mode analysis. Figure 2a shows the structure of the coupled line and the even–odd mode stimulus.

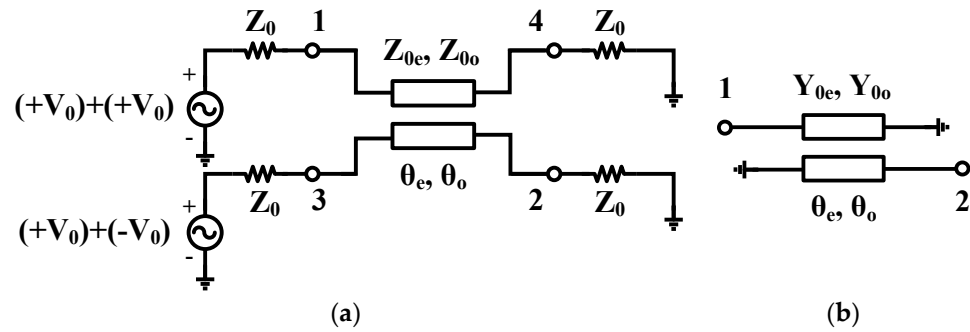


Figure 2. (a) Schematic of the 4-port CL coupler. (b) CL unit with two ports being grounded.

When all ports are connected with a load of Z_0 , apply a pair of $\pm V_0$ to ports 1 and 3, respectively, and the voltage relationship between port 3 and port 4 and V_0 can be derived as Equations (1) and (2):

$$\frac{V_3}{V_0} = \frac{jC \tan \theta}{\sqrt{1 - C^2} + j \tan \theta} \quad (1)$$

$$\frac{V_4}{V_0} = \frac{\sqrt{1 - C^2}}{\sqrt{1 - C^2} \cos \theta + j \sin \theta} \quad (2)$$

In Equations (1) and (2), $C = (Z_{0e} - Z_{0o}) / (Z_{0e} + Z_{0o})$ and $Z_0 = \sqrt{Z_{0e} Z_{0o}}$, where Z_{0e} and Z_{0o} are the characteristic impedances of the CL for even mode and odd mode, respectively. θ is the electrical length of the CL.

When port 3 and port 4 are short to ground, as shown in Figure 2b, the signals transmitted to port 3 and port 4 are completely reflected. In this case, the four-port coupler degenerates into a two-port CL unit, and the Y-Parameters of the CL unit are obtained from Equations (3) and (4).

$$Y_{11} = Y_{22} = -j \frac{Y_{0o} + Y_{0e}}{2} \cot \theta \quad (3)$$

$$Y_{12} = Y_{21} = -j \frac{Y_{0o} - Y_{0e}}{2} \csc \theta \quad (4)$$

where $Y_{0o} = 1/Z_{0o}$ and $Y_{0e} = 1/Z_{0e}$, which are the characteristic admittances of the coupled line for the odd mode and even mode, respectively. The two-port CL unit exhibits bandpass characteristics. The Y_{0o} and Y_{0e} can be adjusted by tuning the width and space of the CL. θ is influenced by the operating frequency and the length of the CL. By increasing the width of the CL, both Y_{0o} and Y_{0e} can be increased, while reducing the line spacing leads to a larger difference between the two. Furthermore, θ is adjusted not only by modifying the physical length of the line but also by considering its frequency dependence, especially across a wide bandwidth. These adjustments help to optimize the performance across the desired frequency range.

Figure 3 reveals the equivalent parameters of a CL with 150- μm length, 20- μm width and 5- μm space. It can be seen that the equivalent self-inductance (L_{eq}), mutual inductance (M_{eq}), Q-factor and coupling coefficient (k) at 26 GHz are around 100 pH, 70 pH, 60 and 0.68, respectively.

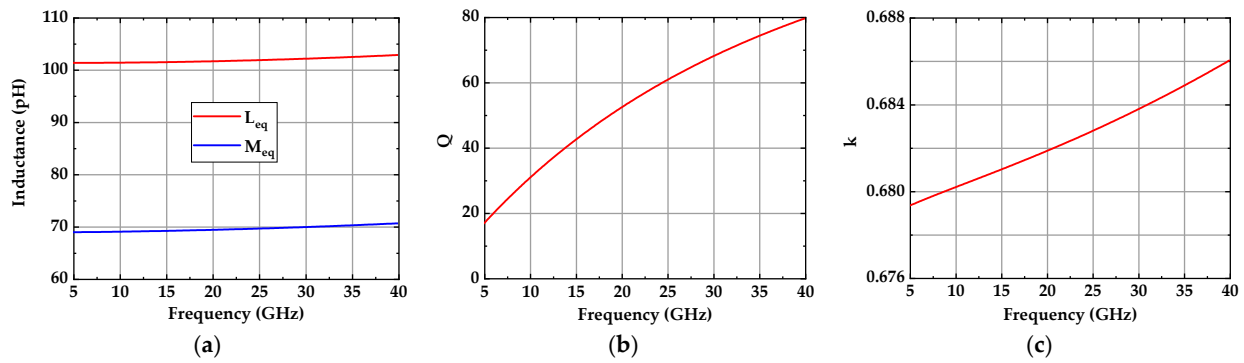


Figure 3. (a) The equivalent self-inductance and mutual inductance. (b) Q-factor. (c) Coupling coefficient.

For a symmetric CL, the hybrid parameters (H-parameters) can be obtained by Equations (5)–(7).

$$H_{11} = s(1 - k^2)L_{eq} \quad (5)$$

$$H_{12} = -H_{21} = -k \quad (6)$$

$$H_{22} = \frac{1}{sL_{eq}} \quad (7)$$

The CL unit is suitable for weak coupling applications such as feedback. In the proposed LNA, it is utilized to build an additional signal path and neutralize C_{gd} for gain and stability enhancement, as shown in Figure 4a. By coupling part of the drain choke TL (TL₇) with the source degenerative TL (TL₆), a portion of the output signal is fed back to the input loop through the CL to counteract the Miller effect of C_{gd} . The 3D view of the single stage with CL feedback is illustrated in Figure 4b. They are designed by the same top metal layer of the process. The green metal traces stand for the MET1 layer and the orange shape represents the back from the ground.

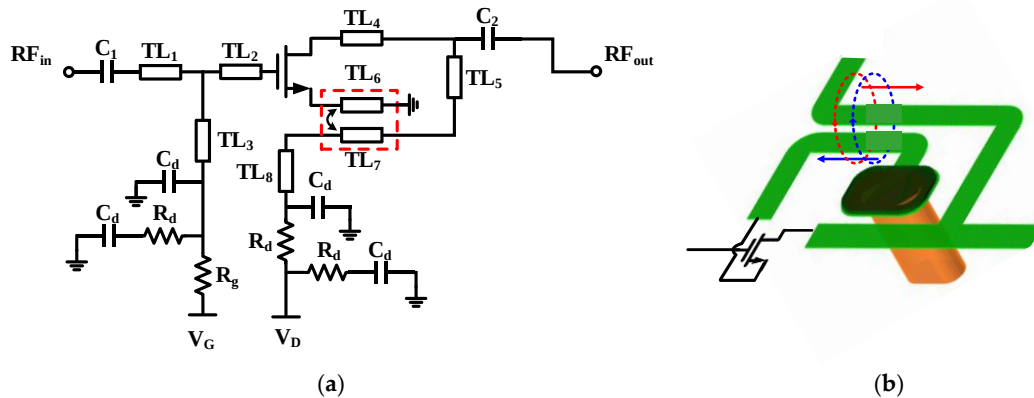


Figure 4. (a) Single stage with drain-to-source CL feedback. (b) Three-dimensional view of the CL in a single stage.

The currents flowing from the drain and the source enter the coupling line TL₆ and TL₇ in the opposite direction, excite a magnetic field in the opposite direction around the coupling line, and establish magnetic coupling between the input and output. When the input voltage increases, the voltage at both ends of the coupling line increases, raising the source voltage, causing the gate-source voltage (v_{gs}) of the transistor to decrease, weakening the increase in input voltage, which neutralizes the positive feedback effect of the gate-drain impedance at a specific frequency range, and increases the real part of the transistor input impedance, thus having a good improvement effect on gain and stability.

Figure 5 illustrates the small-signal model of the transistor with the DSFB neutralization technique. In Figure 5, Z_s and Z_L represent the source and load impedance. $\overline{I_{n,g}^2}$ and $\overline{I_{n,d}^2}$ represent the gate-induced noise and the drain channel thermal noise. Z_{gs} and Z_{gd} represent the gate-source and gate-drain impedance.

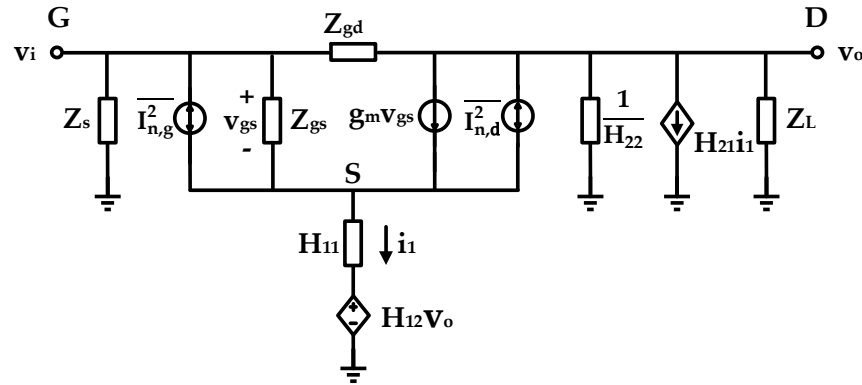


Figure 5. Small signal model of single stage.

From the small signal model, it can be observed that there are two reverse signal flows. One is the signal flow through C_{gd} and the other is the signal created by the CL feedback. The feedback intensity can be controlled by the length, width and space of the CL. The transfer functions of the C_{gd} signal path and the CL signal path are derived as follows:

$$F_{C_{gd}} = \frac{Z_s \parallel (H_{11} + g_m Z_{gs} H_{11} + Z_{gs})}{Z_{gd} + Z_s \parallel (H_{11} + g_m Z_{gs} H_{11} + Z_{gs})} \quad (8)$$

$$F_{CL} = \frac{H_{12} (Z_{gs} \parallel Z_{gd})}{Z_{gs} + Z_s \parallel Z_{gd} + H_{11} + g_m Z_{gs} H_{11}} \quad (9)$$

Set $F_{C_{gd}} = -F_{CL}$, and the neutralization condition can be obtained by Equation (10).

$$H_{21} = \frac{Z_{gs}}{Z_{gd}} \quad (10)$$

When the H_{21} of the CL satisfies Equation (10), the C_{gd} of the transistor can be totally neutralized. However, the design of CLs should also consider the overall performance of the LNA. In particular, impedance matching is influenced by the CL, as the width, length and spacing of the CLs need to be carefully tuned to ensure that the input/output impedance of each stage closely approximates the conjugate of output/input impedance of the preceding/following stages. Additionally, the coupling length of the CL is constrained by source degeneration feedback. If the coupling length is too long, excessive source degeneration can occur, which cancels out the neutralization technique and leads to a reduction in gain. Taking into account neutralization, impedance matching and source degeneration, the parameters of the CLs of each stage are designed as shown in Table 1.

Table 1. Summary of the characteristics of the CLs designed for each stage.

Stage	Width	Effective Coupling Length	Space	Odd/Even Mode Impedance
stage 1	25 μm	68 μm	10 μm	57.3/121.8 Ω
stage 2	25 μm	100 μm	10 μm	54.7/127.7 Ω
stage 3	25 μm	100 μm	10 μm	54.7/127.7 Ω
stage 4	25 μm	75 μm	10 μm	56.4/123.8 Ω

The precise tuning of coupling coefficients and feedback paths is critical for optimizing performance. The variations in fabrication may impact the accuracy of these parameters, and reproducibility across different manufacturing runs can be affected by slight variations in the physical dimensions of the feedback network and coupled lines. To reduce this sensitivity, the tuning parameters and the layout have been optimized to minimize the impact of process variations and simulated potential fabrication tolerances to ensure uniform performance.

The performance improvement of the single-stage unit after coupling is revealed in Figure 6 under the condition of equal length of source and drain lines. Figure 6a shows the gain enhancement with DSFB. To exclude the influence of the matching network, the comparison of G_{max} is supplemented as a reference. The simulated results also imply that DSFB contributes to higher isolation, as shown in Figure 6b. Moreover, stability is improved with DSFB, as can be seen in Figure 6c. Before introducing DSFB, the μ -factor is less than 1 from 6.7 GHz to 21.6 GHz. After introducing DSFB, the μ -factor is greater than 1 across the whole frequency band, indicating that the circuit becomes unconditionally stable. The additional feedback structure usually brings NF degradation, while the proposed DSFB barely deteriorates the NF, as shown in Figure 6d. This is because the gain enhancement suppresses the noise contribution of the CL.

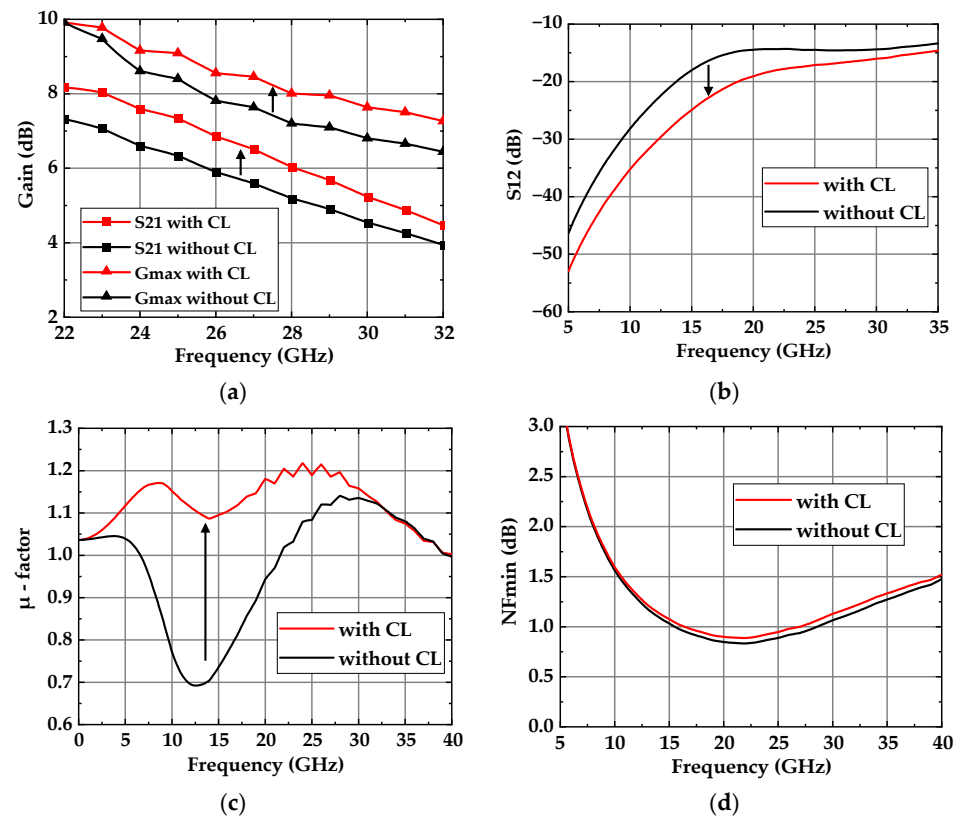


Figure 6. (a) Gain enhancement with coupling. (b) Isolation enhancement with coupling. (c) Stability improvement with coupling. (d) Comparison of NF_{min} before and after coupling.

2.2. Wide Bandpass Interstage Matching Network

The common source structure with inductive degeneration is an inherently narrow-band circuit topology for LNA applications [18,19]. The narrowband characteristic of the topology can be attributed to the sharp variation of impedance with frequency. Compared with first-order LC networks shown in Figure 7a, the π -type matching network is extensively adopted in the traditional designs for its broadband advantage, as pictured in Figure 7b. However, the traditional π -type matching network has a limited impact on the high-frequency impedance. A widely used technique for bandwidth extension is increasing

the order of matching networks which requires adding more reactive components, such as inductors and capacitors, to the network, as revealed in Figure 7c. Although this method can effectively broaden the bandwidth, it significantly increases the loss.

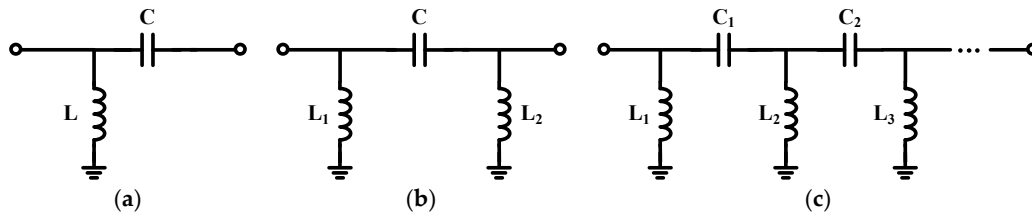


Figure 7. Traditional matching networks (a) First-order LC network. (b) π -type network. (c) High-order network.

To address this challenge, a novel wide bandpass interstage matching network (ISMN) is proposed which enhances the matching bandwidth without increasing the network order. A series TL-C-TL configuration is integrated into the proposed ISMN, as illustrated in Figure 8.

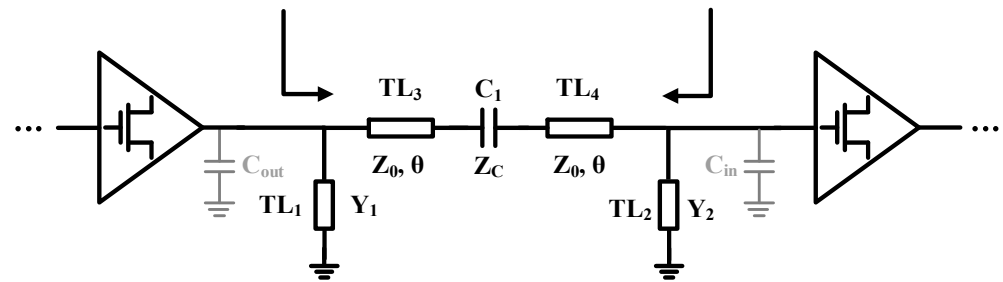


Figure 8. The proposed interstage matching network.

Compared with the traditional matching network, the proposed ISMN consists of two shunt stubs, a series capacitor and two series TLs. The two shunt stubs (TL_1 , TL_2) resonate with the output capacitor and input capacitor (C_{out} , C_{in}), respectively, forming a bandpass filtering network together with the series TL-C-TL. The series TLs are strategically connected on both sides of the series capacitor to achieve wideband matching by effectively converging the impedance. The series TL-C-TL network operates like a stepped impedance matching network, introducing multiple resonance points for matching at various frequencies, enhancing broadband performance. The capacitor (C_1) compensates for high-frequency impedance mismatches, helping to fine-tune the network's impedance. By gradually adjusting the characteristic impedance of the transmission lines and the capacitance values, the network can incrementally match the load impedance to the source impedance. This gradual impedance transformation minimizes the reflection coefficient, ensuring more efficient signal transmission across a wide frequency band. Due to no additional branches being introduced, the ISMN possesses lower loss compared to higher-order networks.

The ISMN can be regarded as a cascade of five two-port networks. As a result, it can be described by the ABCD matrix as written in Equation (11).

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{ISMN} = \begin{bmatrix} 1 & 0 \\ Y_1 & 1 \end{bmatrix} \begin{bmatrix} \cos\theta & jZ_0\sin\theta \\ \frac{j\sin\theta}{Z_0} & \cos\theta \end{bmatrix} \begin{bmatrix} 1 & Z_C \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \cos\theta & jZ_0\sin\theta \\ \frac{j\sin\theta}{Z_0} & \cos\theta \end{bmatrix} \begin{bmatrix} 1 & 0 \\ Y_2 & 1 \end{bmatrix} \quad (11)$$

Once the ABCD parameters of the network are calculated, the S_{21} of the network can be obtained by the A-to-S transfer function shown in Equation (12).

$$S_{21} = \frac{2}{A + \frac{B}{Z_0} + CZ_0 + D} \quad (12)$$

Therefore, the transfer function of the ISMN can be calculated by Equation (13).

$$S_{21} = \frac{4Z_0}{e^{j \cdot 2\theta} [4Z_0 + 2Z_C + (Y_1 + Y_2)(2Z_0^2 + Z_0 Z_C)] + Y_1 Y_2 Z_0^2 Z_C (1 + 2\cos\theta) + 2jY_1 Y_2 Z_0^3 \sin\theta + (Y_1 + Y_2)Z_0 Z_C} \quad (13)$$

where Z_0 and θ are the characteristic impedance and the electrical length of the TLs. Y_1 and Y_2 are the admittance of the shunt stubs. Z_C is the impedance of the capacitor.

The matching bandwidth can be tuned by adjusting the length of the series TL. Figure 9 demonstrates the S_{11} of the single stage with the interstage network with different lengths of TLs.

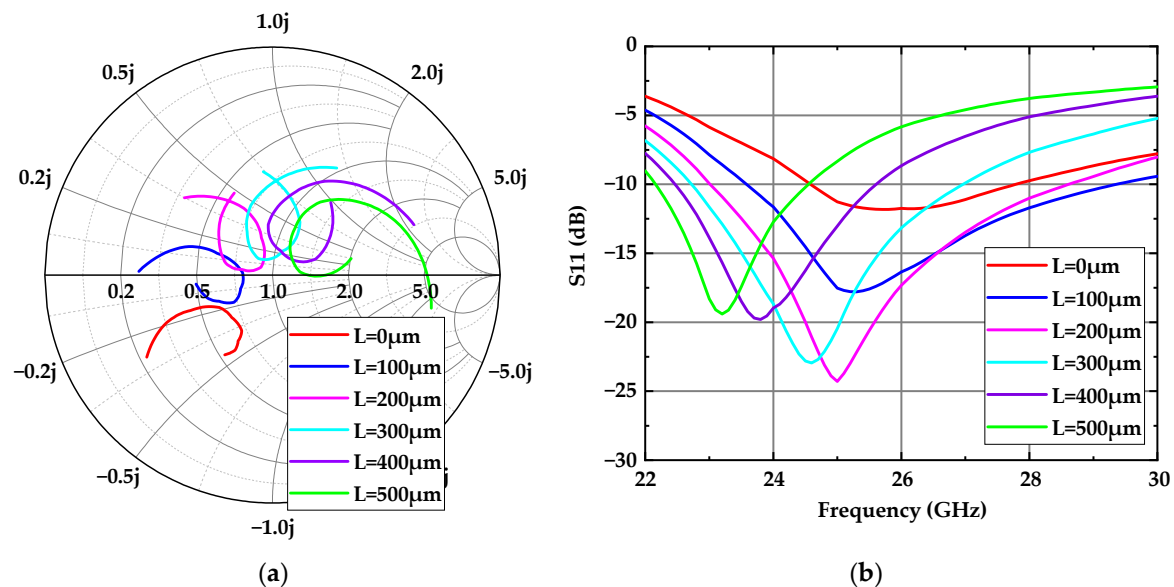


Figure 9. Input reflection coefficient of the transistor using the proposed ISMN with different lengths of series TL. (a) On the Smith Chart. (b) The same S_{11} is expressed in decibels versus gigahertz.

As revealed in Figure 9, the proposed ISMN helps to converge the input impedance of the single stage, and a wide band can be achieved when an appropriate length of TL is chosen. Moreover, compared with the high-order matching network, the proposed matching network exhibits lower loss, which contributes to lower NF in the LNA design.

3. Measurement Results

The chip microphoto of the proposed LNA is shown in Figure 10, with an area of $3.7\text{ mm} \times 1.2\text{ mm}$ including pads. The entire layout including all the passive devices such as TLs, capacitors and resistors was simulated using an EM simulator. The input and output ports were designed to have a 50-ohm impedance to ensure optimal signal integrity and matching across the system.

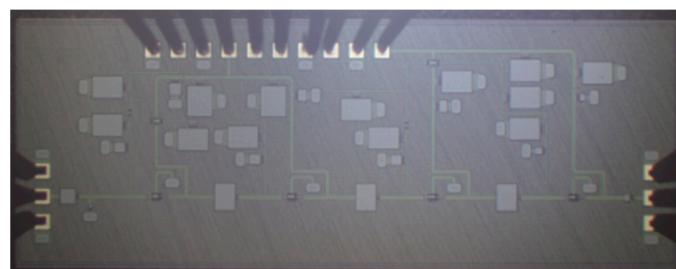


Figure 10. Chip microphoto of the proposed LNA.

The fabricated chip was measured on wafer using a Cascade Microtech Summit 12000 Probe Station and Formfactor RF GSG-150 wafer probes from the United States. The LNA draws a current of 40 mA from the supply at a V_{DD} of 5 V. The gate and drain bias voltages are applied through a DC probe card. To acquire the performance of the LNA, the S-parameters, NF and output-referred 1-dB compression point (OP1dB) were measured with a Keysight PNA-X N5247B vector network analyzer. Before measuring, the S-parameter calibration was conducted with the Short-Open-Load-Through (SOLT) method, and the noise calibration was conducted using NoiseWave NW346V noise source. The measurement configuration is illustrated in Figure 11.

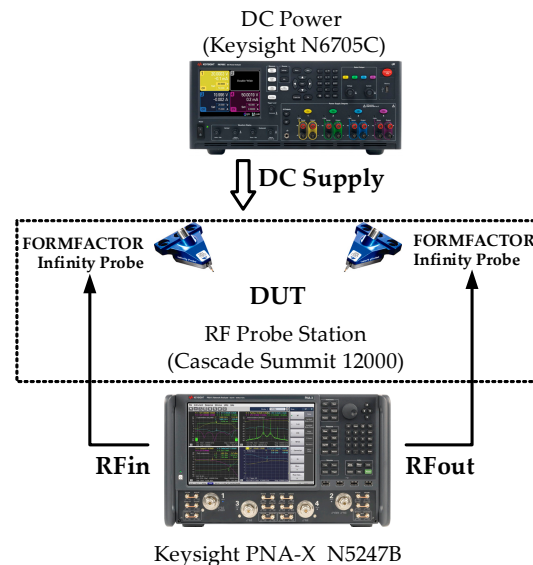


Figure 11. Measurement configuration.

Figure 12 is the simulated and measured S-parameters of the LNA, which include the small signal gain (S21), the input and output return losses (S11 and S22) and the reverse isolation (S12). The gain achieves the maximum value of 23.7 dB at 25.8 GHz with a 3-dB bandwidth of 23.6 GHz to 29.8 GHz. It is observed that the overall measured gain is about 3 dB lower than the simulation, which may be due to the inaccuracy of active device models. The measured S11 is under -10 dB from 19.9 GHz to 29 GHz, and S22 is under -10 dB from 9.3 GHz to 28.2 GHz. The measured return losses are slightly different from the simulation, which can be attributed to the deviation of electromagnetic simulations. The S12 data are lower than -40 dB across the whole frequency range. The excellent reverse isolation performance helps to make the LNA unconditionally stable.

Figure 13 shows the simulated and measured NF. The LNA exhibits a minimum NF of 2.2 dB at 27.8 GHz, and the NF is lower than 3.0 dB in the frequency band of 23.6 GHz to 29.8 GHz. The measured NF shows about 1-dB degradation compared to the simulation, owing to the deviations of the noise parameter model.

The linearity performance of the LNA is plotted in Figure 14, with an OP1dB of 13 dBm at the center frequency of 25.8 GHz. It can be seen that the in-band OP1dB changes from 11 dBm to 14 dBm, which demonstrates great power handling ability and high linearity with limited power consumption.

To evaluate the stability of the LNA, the μ -factor is simulated and measured, as illustrated in Figure 15. The measurement results show that the μ -factor can achieve a peak value of 12.2 at 11.9 GHz, and is greater than 1 over the frequency range of 0–40 GHz, which not only ensures the stability of LNA in the operating frequency band but also keeps it unconditionally stable when dealing with the input signal in a wide frequency band.

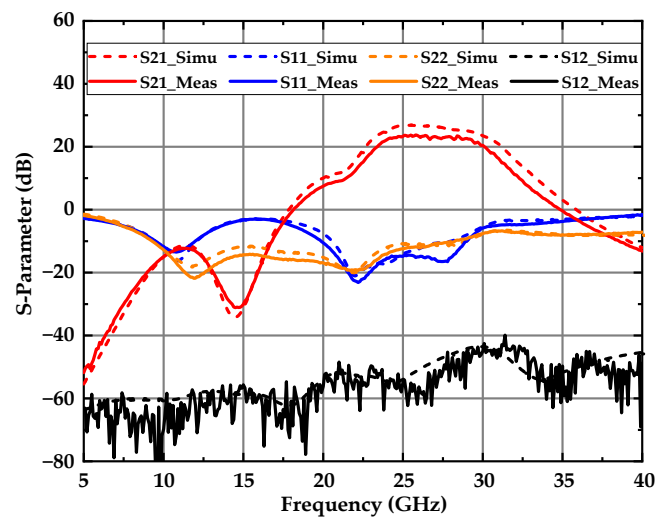


Figure 12. Simulated and measured S-parameters of the LNA.

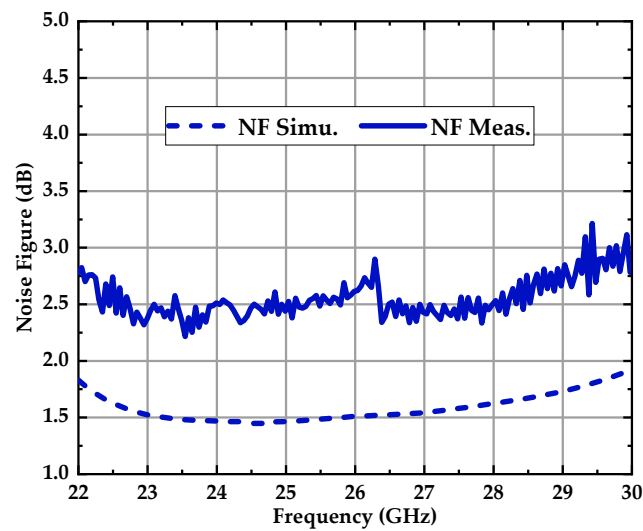


Figure 13. Simulated and measured NF of the LNA.

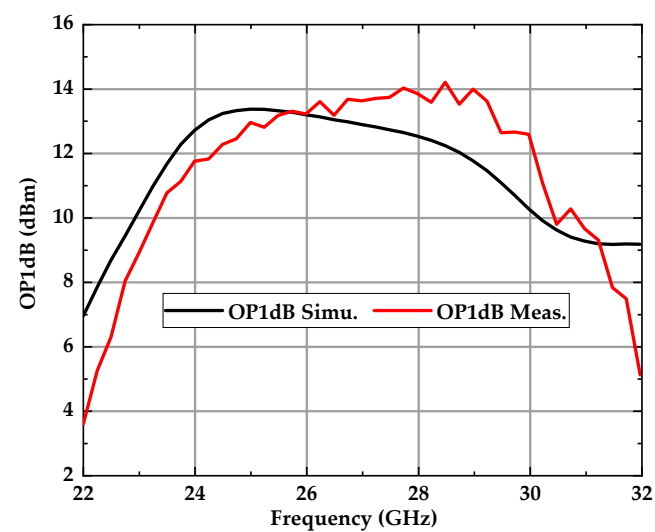


Figure 14. Simulated and measured OP1dB of the LNA.

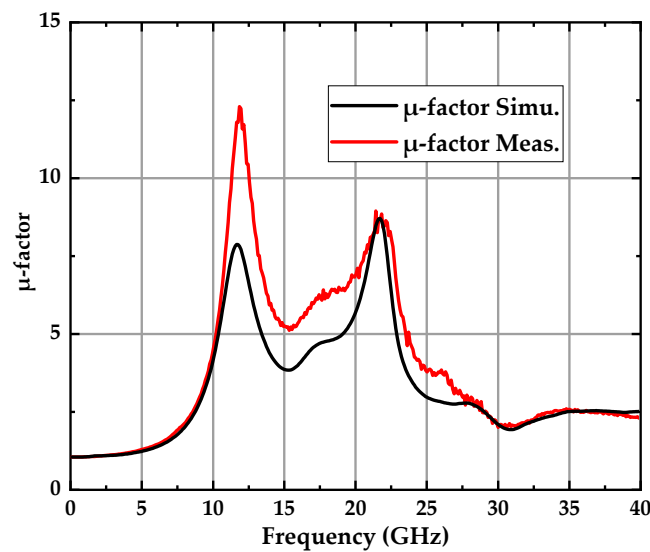


Figure 15. Simulated and measured μ -factor of the LNA.

Table 2 summarizes the performances of the proposed LNA and compares them with other recently reported LNAs based on GaN, GaAs and CMOS. It is obvious that the proposed LNA can achieve good gain and low power consumption, while also exhibiting competitive NF and linearity with a medium chip area.

Table 2. Performance summary and comparison.

Reference	This Work	[3]	[4]	[5]	[8]	[9]	[20]	[21]	[22]
Technology	0.15- μ m GaN-on-SiC	65-nm CMOS	0.13- μ m CMOS SOI	0.1- μ m GaAs	0.15- μ m GaN-on-SiC	0.1- μ m GaN-on-Si	0.15- μ m GaN-on-SiC	0.12- μ m GaN-on-SiC	0.1- μ m GaN-on-Si
Frequency (GHz)	23.6–29.8	15.8–30.3	22–28	18.7–36.5	26–30	27–31	27–31	33–41	18–56
Gain (dB)	23.7	10.2	13.2	15.9	20.2	20	19.6	15	21.5
NF (dB)	2.2–3.0	3.3–5.7	3.07	1.5–2.1	2.42–2.56	1.5	3.7–3.9	3–4	2.2–4.4
OP1dB (dBm)	13	N.A.	3	15	17.2	16	N.A.	13	10
Area (mm ²)	4.44	0.18	1.7	0.96	2.66	3	4.08	0.7	4.8
Power (mW)	200	12.4	32.67	66	320	150	430	280	1400
FoM *	11.02	10.76	3.73	25.43	1.75	6.46	0.63	0.91	5.81

$$* \text{FoM} = \frac{\text{Gain(abs.)} \times \text{BW(GHz)}}{(\text{F} - 1) \times \text{Pdc(mW)}}$$

4. Conclusions

In this paper, a GaN LNA with DSFB based on a coupled line is implemented in a commercial 0.15- μ m GaN-on-SiC process. The prototype LNA can achieve a high gain while maintaining good stability. The shunt stubs at the drain and source are coupled to form a feedback signal path which neutralizes the C_{gd} of the transistors, and therefore improves the gain and stability of the LNA. A bandpass interstage network including series TL-C-TL is adopted, which realizes wideband matching. The measured results show that the presented LNA realized a stable gain of 20.7 to 23.7 dB across the frequency range of 23.6 to 29.8 GHz. The measured in-band NF and OP1dB were 2.2–3.0 dB and 11–14 dBm, respectively. In addition, the LNA can achieve unconditional stability in the frequency range of 0–40 GHz. The whole chip occupies a 4.44 mm² area with 200 mW of power consumption at 5 V of supply voltage.

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