

Article

Design and Optimization of High Performance Multi-Step Separated Trench 4H-SiC JBS Diode

Jinlan Li ^{1,*} , Ziheng Wu ¹ , Huaren Sheng ¹, Yan Xu ¹ and Liming Zhou ²

¹ College of Information Engineering, Yangzhou University, Yangzhou 225009, China; mz120220965@stu.yzu.edu.cn (Z.W.); mz120230973@stu.yzu.edu.cn (H.S.); mz120230964@stu.yzu.edu.cn (Y.X.)

² Yangjie Electronic Technology Company Ltd., Yangzhou 225009, China; liming.zhou@21yangjie.com

* Correspondence: jinlanli@yzu.edu.cn

Abstract: In this paper, a novel 3300 V/40 A 4H-SiC junction barrier Schottky diode (JBS) with a multi-step separated trench (MST) structure is proposed and thoroughly investigated using TCAD simulations. The results show that the introduction of MST expands the Schottky contact area, resulting in a decrease in the forward voltage drop. Furthermore, the combination of the deep P⁺ shielded region and the central P⁺ region effectively reduces the leakage current, leading to a 43.7% increase in the blocking voltage compared to conventional 4H-SiC JBS. The effects of the step depth (d_s) and the width of the central P⁺ region (w_m) on the device performance are analyzed in depth. In addition, a multi-step trenched linearly graded field-limiting rings (MTLG-FLR) termination ensures a more uniform electric field distribution, and the terminal protection efficiency reaches up to 90%, which further enhances the reliability of the terminal structure.

Keywords: 4H-SiC junction barrier Schottky (JBS); multi-step trench; trench FLR; electric field; blocking voltage



Citation: Li, J.; Wu, Z.; Sheng, H.; Xu, Y.; Zhou, L. Design and Optimization of High Performance Multi-Step Separated Trench 4H-SiC JBS Diode. *Electronics* **2024**, *13*, 4143. <https://doi.org/10.3390/electronics13214143>

Academic Editor: Francesco Driussi

Received: 24 September 2024

Revised: 18 October 2024

Accepted: 18 October 2024

Published: 22 October 2024



Copyright: © 2024 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

1. Introduction

Large-diameter 4H-SiC wafers with low defect density have been commercialized and applied in power devices [1]. Compared with Si-based power devices, SiC power devices have attracted more and more attention in the application market due to their faster switching speeds, better thermal stability and higher efficiency [2]. In particular, SiC power devices show great potential in high-voltage application scenarios such as new energy vehicles, power transmission and electric locomotive traction, etc. However, the current commercial SiC diodes are primarily utilized in the low-to-medium voltage range; the design and development of high-voltage devices still face severe challenges [3–6].

In medium-voltage and high-voltage applications, the balance between the forward voltage drop (V_F) and leakage current is critical. For traditional planar junction barrier Schottky (JBS) diodes, the shielding effect of the Schottky barrier region under the reverse voltage depends on the depth of the P⁺ regions [7–12]. Although narrowing the width of the Schottky region can reduce the leakage current, it leads to an increase in V_F of a diode. Recently, various improved structures based on 4H-SiC JBS diodes have been proposed and studied. The floating junction JBS (FJ-JBS) diode optimizes the reverse electric field distribution and enhances the device breakdown voltage by introducing additional PN junctions within the drift layer, while maintaining low on-state resistance [13]. H. Yuan et al. have optimized the trade-off between breakdown voltage (V_{BR}) and specific on-resistance ($R_{on,sp}$) of a 1200 V FJ-JBS diode by simulation, achieving a BFOM (Baliga figure of merit) of up to 8.16 GW/cm². However, this structure exhibits a high degree of sensitivity to the doping of the epilayer, significantly increasing the difficulty in achieving the desired ion implantation process. The Super Junction JBS (SJ-JBS) diode incorporates a periodic arrangement of P and N layers, offering multiple current conduction pathways during

forward biasing, while simultaneously optimizing the electric field distribution under reverse voltage conditions. This approach provides a solution to the trade-off problem between forward and reverse characteristics [14]. B. Wang et al. have successfully prepared a SJ-JBS diode with a V_{BR} of 1920 V and a $R_{on,sp}$ of $1.2 \text{ m}\Omega\cdot\text{cm}^2$ by substrate thinning. The structure still faces many challenges, the most significant of which is its complex manufacturing process and high cost, potentially resulting in reduced yield rates and device reliability. The P-type retrograde-implanted JBS (RP-JBS) diode embeds a lightly doped P^+ region beneath the P^+ region of the conventional JBS structure. This design deepens the PN junction, reducing the electric field at the Schottky interface and effectively lowering capacitance by widening the space-charge region. Furthermore, Y. L. Zhang et al. have proposed the use of RP-JBS to achieve a leakage current of $0.2 \text{ }\mu\text{A}$ at 1200 V [15]. However, although these new structures have improved their performance, they are mainly reported in the medium-voltage field and are limited by high process complexity and poor reliability. In contrast, the trench JBS (TJBS) diode is commercially achievable due to its simple process and excellent performance [16–18]. By flexibly designing the deep P^+ region, it can effectively reduce the leakage current and improve the blocking voltage while maintaining a low forward voltage drop. Therefore, the multi-step trench JBS diode could have great potential for high-voltage applications. In addition, an effective edge-termination technique results in electric field distribution that is more uniform at the edge of the device, thereby enabling the device to approach the ideal breakdown voltage capability of the epilayer used. Many researchers have studied edge termination technologies, such as field limiting rings (FLR), field plates, junction termination extensions and some combined structures [19–21]. These techniques help reduce the reverse leakage current and improve the reliability of the device. Therefore, the optimization of terminal technology is also indispensable.

In this paper, the novel MST-JBS diode is proposed; low forward voltage drop and high breakdown voltage are achieved through the optimization of TCAD simulation. Furthermore, the multi-step trench linearly graded FLR (MTLG-FLR) terminal structure is designed to further enhance the stability and reliability of the device.

2. Device Design and Simulation

Figure 1a,b shows a 3D structure of the 4H-SiC JBS and 4H-SiC MST-JBS diodes, respectively. The P^+ implanted regions in both JBS and MST-JBS diodes account for 50% of the active area. The anode of both diodes features a Schottky contact with the drift region–SiC interface, as well as an ohmic contact with the P^+ interface. The 4H-SiC MST-JBS diode has a three-step trench structure with a central P^+ region, forming a Schottky contact with both the trench sidewall and the drift region. The two structures have a width of $7 \text{ }\mu\text{m}$ and a substrate doping concentration of $1 \times 10^{18} \text{ cm}^{-3}$. For 4H-SiC, the epilayer thickness (T) can be expressed as follows:

$$T = \frac{\epsilon E_c(N_D)}{qE_c} - \sqrt{\left[\frac{\epsilon E_c(N_D)}{qN_D}\right]^2 - \left[\frac{2\epsilon V_{BR}}{qN_D}\right]} \quad (1)$$

where V_{BR} represents the breakdown voltage of the device; q denotes the elementary charge; and ϵ stands for the dielectric constant of 4H-SiC. The critical electric field (E_c) and its relationship with the epilayer doping concentration (N_D) can be determined using the following expression

$$E_c = 2.49 \times 10^6 \times \frac{1}{[1 - 0.25 \log(N_D \times 10^{-6})]} \quad (2)$$

Based on the Formulas (1) and (2), and assuming a junction terminal efficiency of 70%, the values for T and N_D of the epilayer in the 3300 V MST-JBS diode could be optimally set to $35 \text{ }\mu\text{m}$ and $2 \times 10^{15} \text{ cm}^{-3}$, respectively. In the MST structure, the P^+ region has a doping concentration of $1 \times 10^{18} \text{ cm}^{-3}$, and the width of the central P^+ region is 0 to $1 \text{ }\mu\text{m}$.

The width of each step is $0.5 \mu\text{m}$; the step depth (d_s) is 0.2 to $0.6 \mu\text{m}$. In the simulation, the depth of the P^+ region is consistent with the step depth. The specific parameters are presented in Table 1.

Table 1. Device parameters used in simulation.

N_D	Epilayer doping	$2 \times 10^{15} \text{ cm}^{-3}$
N_P	P^+ region doping	$1 \times 10^{18} \text{ cm}^{-3}$
T	Epilayer thickness	$35 \mu\text{m}$
d_s	Depth of each step	$0.2\text{--}0.6 \mu\text{m}$
w_s	Width of each step	$0.5 \mu\text{m}$
w_m	Width of middle P^+ region	$0\text{--}1 \mu\text{m}$

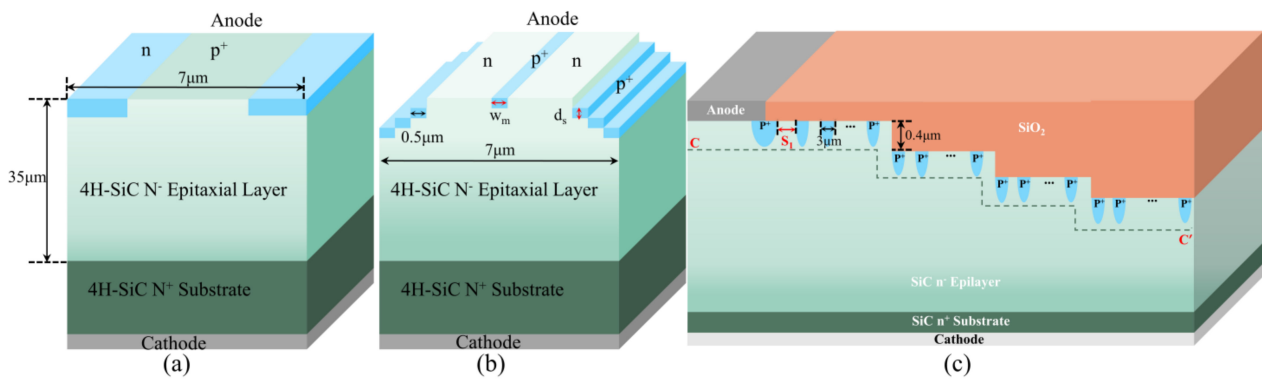


Figure 1. The 3D cell structure of (a) 4H-SiC JBS, (b) 4H-SiC MST-JBS, and (c) 4H-SiC MTLG-FLR.

A novel multi-step trench linearly graded FLR (MTLG-FLR) termination was used, as shown in Figure 1c. The linearly graded FLR structure is formed subsequent to the multi-step trench structure formation to ensure that the MTLG-FLR has a larger junction depth. This edge termination structure combines the strengths of both linearly graded FLR and trench structures, providing more uniform electric field distribution to ensure high breakdown voltages. The terminal structure is set up in three steps, with each step having a depth of $0.4 \mu\text{m}$. The depth and width of the P^+ rings are $0.4 \mu\text{m}$ and $3 \mu\text{m}$, respectively. The spacing design rule of the MTLG-FLR is described as $S_n = S_1 + 0.1(n - 1)$, where S_1 is the spacing between the main junction and the first ring. There are five linearly graded P^+ rings on each step, totaling 20 rings in all. The 4H-SiC MST-JBS structure design and optimization is conducted using Sentaurus TCAD 2017.

In 4H-polytype SiC materials, the presence of dopant atoms, characterized by their relatively high ionization energies, typically leads to difficulty in achieving complete ionization under room temperature conditions. Thus, the phenomenon of incomplete ionization of impurities must be taken into account during the simulation. The model used in the Sdevice to account for incomplete ionization is as follows:

$$N_D = \frac{N_{D,0}}{1 + G_D(T) \exp\left(\frac{E_{F,n} - E_C}{kT}\right)} \quad (3)$$

$$N_A = \frac{N_{A,0}}{1 + G_A(T) \exp\left(-\frac{E_{F,p} - E_V}{kT}\right)} \quad (4)$$

where $G_D(T)$ and $G_A(T)$ signify the temperature-dependent ionization factors, while $N_{D,0}$ and $N_{A,0}$ denote the concentrations of substitutional donors and acceptors, respectively. $E_{F,n}$ and $E_{F,p}$ correspond to the quasi-Fermi levels associated with electrons and holes, respectively. 4H-SiC exhibits a bandgap width of 3.2 eV , and the variation of the bandgap (ΔE_g) can significantly impact its performance. Therefore, it is essential to incorporate this

consideration into the simulations. The physical model integrated into the simulation is addressed as follows:

$$\Delta E_g = E_{ref} \left[\ln \left(\frac{N_D}{N_{ref}} \right) + \sqrt{\left(\ln \left(\frac{N_D}{N_{ref}} \right) \right)^2 + 0.5} \right] \quad (5)$$

where E_{ref} and N_{ref} are 9×10^{-3} eV and 1×10^{17} cm $^{-3}$, respectively. The fundamental physical models used in the simulation also include effective intrinsic density, models for mobility, impact ionization, barrier tunneling and anisotropic material properties. Recombination models include carrier generation recombination, Auger recombination and Shockley–Read–Hall recombination model. Additionally, the Okuto–Crowell model and Caughey–Thomas model were also considered.

3. Results and Discussion

Figure 2a,b shows the influence of varying the width of the central P⁺ region (w_m) on the simulated forward and reverse I–V characteristics of 4H-SiC MST-JBS diodes. The V_F is defined as the voltage drop at the forward-biased current of 40 A, and the V_{BR} defined as the reverse voltage at a current of 10 μ A. As illustrated in Figure 2a, when w_m is increased from 0 μ m to 1 μ m, the reduction of the Schottky contact area leads to an increase in current density at a constant current level of 40 A. This, in turn, causes more collisions between electrons and the lattice, thereby reducing the electron mobility. Consequently, the equivalent resistance of the device increases significantly, leading to the forward voltage drop to rise from 2.0 V to 3.2 V. In Figure 2b, it is worth noting that the leakage current of 4H-SiC MST-JBS, without the central P⁺ region, rapidly increases with the reverse voltage due to the ineffectiveness of the barrier shielding layer. Conversely, the deep barrier created by the multi-step trench structure, in conjunction with the shielding layer formed by the central P⁺ region, effectively shields the Schottky junction and reduces the surface electric field. As w_m increases from 0.25 μ m to 1 μ m, the blocking voltage remains stable, while the leakage current gradually decreases. Consequently, the MST-JBS diode can achieve a higher blocking voltage while maintaining a significantly lower level of leakage current. Therefore, considering the influence of the central P⁺ region on the forward current and the reverse breakdown voltage, the width is optimized to 0.5 μ m. This demonstrates the effectiveness of optimizing the width of the central P⁺ region as a key parameter for improving MST-JBS diode forward performance.

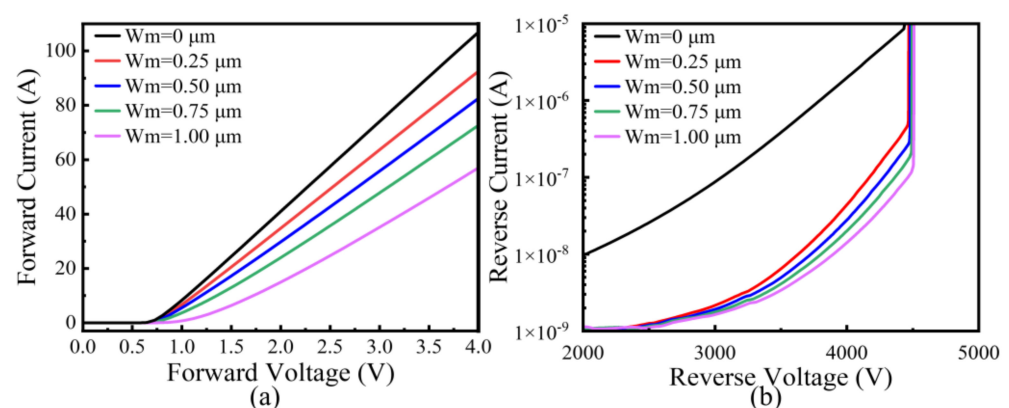


Figure 2. The simulated (a) forward characteristics and (b) reverse leakage current of 4H-SiC MST-JBS diodes as functions of the width of the central P⁺ region.

Figure 3a shows the simulated V_F and V_{BR} as functions of the step depth of the P⁺ region of 4H-SiC MST-JBS diodes. The results show that as the d_s increases from 0.2 to 0.6 μ m, the V_F exhibits a linear increase from 2.0 V to 2.92 V. Additionally, as

illustrated in the inset of Figure 3a, the $R_{on,sp}$ increases correspondingly from $12.8 \text{ m}\Omega\cdot\text{cm}^2$ to $18.7 \text{ m}\Omega\cdot\text{cm}^2$. However, the breakdown voltage exhibits a trend of increasing first and then decreasing. Figure 3b shows the distribution of electric field intensity along AA' in the 4H-SiC MST-JBS diode in Figure 3d. It is obvious that as the d_s increases, the breakdown voltage is effectively improved due to the notable reduction in the electric field intensity on both sides of the central P⁺ region. It is indicated that under a high reverse bias, the depletion layer formed by the shallow depth of the P⁺ region does not effectively shield the Schottky junction, leading to an excessively high surface electric field. Thus, the d_s is $0.2 \text{ }\mu\text{m}$ in the 4H-SiC MST-JBS diode, resulting in a breakdown voltage of approximately 2150 V. This is attributed to the increased effect of image forces resulting in a lowering of the effective barrier height, which subsequently promotes more electrons to flow over the lower barrier explained by the thermionic field emission theory. Furthermore, under high electric field conditions, the excessive carriers tunnel through the lowered Schottky barrier. Thus, a combination of thermionic field emission and field emission contributes to reverse leakage currents, which leads to premature breakdown at the central P⁺ region of the device, as shown in Figure 3e. Figure 3c shows the distribution of electric field intensity along the BB' as the d_s increases. It is found that as the d_s further increases, the electric field concentration effect gradually shifts from the device surface towards its interior. The intensified effect observed along the lowest edge of the P⁺ region in the BB' direction results in device breakdown, as shown in Figure 3f. Furthermore, when the d_s is excessively deep, it causes a decrease in the thickness of the drift layer, which in turn decreases the breakdown voltage. However, when the d_s is $0.4 \text{ }\mu\text{m}$, the deep potential barrier shielding layer plays a crucial role in effectively reducing the high surface electric field. Additionally, this appropriate depth design minimizes the loss of drift layer thickness and significantly alleviates the detrimental impact of the electric field concentration effect on device performance under reverse voltage conditions. Therefore, the uniform distribution of electric field within the active region of the 4H-SiC MST-JBS diode can be achieved by adjusting the d_s as a key parameter. As a result, in order to achieve higher reverse breakdown voltage and lower forward voltage drop requirements, the optimal d_s is determined to be $0.4 \text{ }\mu\text{m}$, resulting in a V_{BR} of 4480 V and a V_F of 2.4 V.

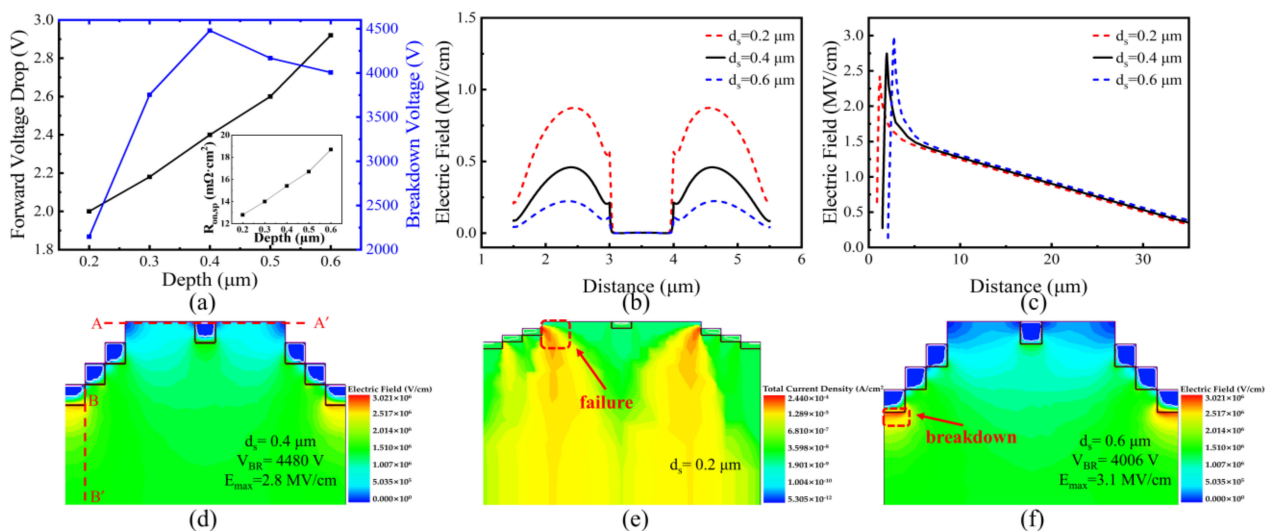


Figure 3. (a) The simulated forward voltage drop and reverse breakdown voltage of 4H-SiC MST-JBS diodes are functions of the d_s . The inset shows the variation of $R_{on,sp}$ with d_s . (b) Electric field distribution in MST-JBS along A-A'. (c) Electric field distribution in MST-JBS along B-B'. (d) Schematic of the cross-sectional electric field distribution under reverse voltage condition. (e) Current density distribution with $d_s = 0.2 \text{ }\mu\text{m}$ at breakdown. (f) Electric field distribution with $d_s = 0.6 \text{ }\mu\text{m}$ at breakdown.

Figure 4a shows the simulated forward characteristics of 4H-SiC MST-JBS and conventional 4H-SiC JBS diodes. Both structures have a cell width of 7 μm ; all parameters are consistent. It can be observed that under forward bias, the voltage drop of the 4H-SiC MST-JBS diode is 2.4 V, which is slightly lower than that of the 4H-SiC JBS diode. Figure 4b shows the 3D simulation results of the current density distribution for the 4H-SiC MST-JBS, with particular emphasis on the Schottky contact located on the trench sidewall. It can be observed that the forward performance of the device is enhanced by expanding the Schottky contact area, which provides an additional path for current flow and promotes a wider and more uniform current distribution. Therefore, current crowding is minimized, resulting in a decrease in the forward voltage drop and an increase in current-carrying capacity. Figure 4c shows the simulated reverse characteristics of 4H-SiC MST-JBS and conventional 4H-SiC JBS diodes. Under reverse bias conditions, the breakdown voltage of the 4H-SiC MST-JBS diode reaches approximately 4480 V, marking a substantial improvement of approximately 43.7% over the conventional JBS diode. Moreover, the leakage current performance of the 4H-SiC MST-JBS is outstanding, with values several orders of magnitude lower than those of the JBS diode at 3300 V. This is attributed to the multi-step trench P^+ region and the central P^+ region, which form a PN junction with the N epilayer, effectively shielding the Schottky barrier and significantly suppressing its lowering. In contrast, the JBS diode suffers a shallow P^+ region, which contributes to a more rapid deterioration of device performance under high reverse bias conditions. Consequently, the MST-JBS diode exhibits excellent electrical properties under high voltage conditions, rendering it a promising candidate for high-voltage power electronics applications exceeding 3300 V.

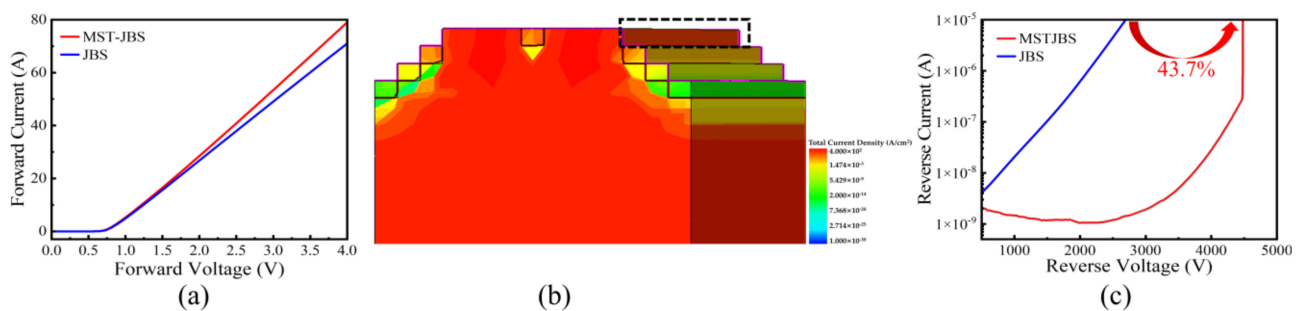


Figure 4. (a) The simulated forward characteristics of JBS and MST-JBS diodes. (b) Current density distribution of a MST-JBS diode. (c) Reverse leakage current of JBS and MST-JBS diodes.

4. Termination Design and Analyze

A multi-step trench linearly graded FLR termination structure is designed and optimized based on simulation, as shown in Figure 1c. For the conventional FLR structure, the breakdown voltage of the termination is highly dependent on the size of the ring spacing. More rings are needed to reduce the electric field peak due to the narrow spacing. Similarly, when the spacing is large, the field-limiting rings fail to expand the depletion layer outward. Therefore, the high electric field at the main junction of the device, caused by the curvature effect, is often not effectively mitigated. The introduction of the MTLG-FLR termination structure results in a much higher protection efficiency. Figure 5a shows the comparison of the reverse I-V characteristics between the MTLG-FLR structure and a conventional FLR structure with a uniform spacing of 2.5 μm . The total length of the FLR is consistent with that of the 1.8 μm S_1 of the MTLG-FLR structure. The results indicate that the FLR structure exhibits a reverse breakdown voltage of 3380 V. In contrast, the breakdown voltage of the MTLG-FLR structure is increased by 20% ($\text{S}_1 = 1.8 \mu\text{m}$). The increase in breakdown voltage observed in the device can be attributed to the combination of two key factors, including the linear variation in the spacing between FLR and the multi-step trench structure of the termination. Thus, the electric field distribution within the MTLG-FLR terminal region is more uniform.

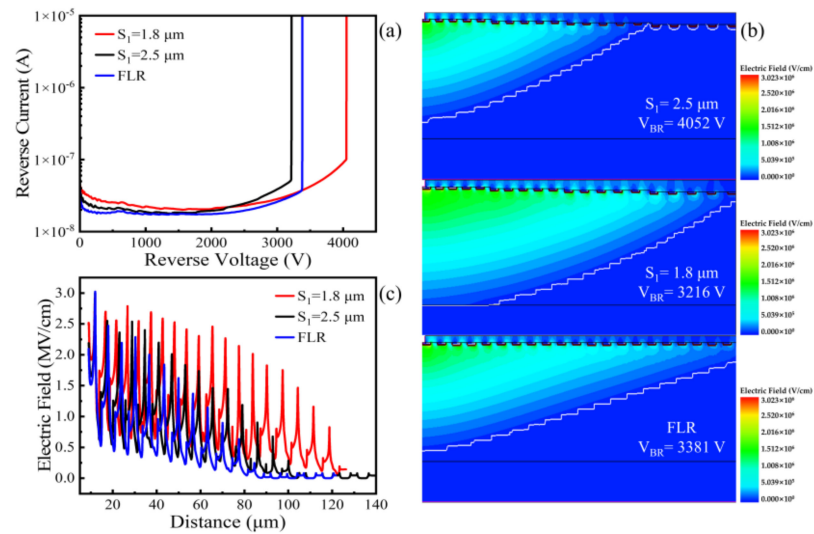


Figure 5. (a) Simulated reverse I–V characteristics for MTLG-FLR structures and conventional FLR structure. (b) Electric field distribution under reverse breakdown of MTLG-FLR structures and conventional FLR structure. (c) Electric field distributions along C–C' for MTLG-FLR structure with $S_1 = 2.5 \mu\text{m}$ and $S_1 = 1.8 \mu\text{m}$, respectively, and the conventional FLR structure.

Figure 5b illustrates the electric field distribution under reverse breakdown of the MTLG-FLR structures with different S_1 and the conventional FLR structures. As the reverse bias at the main junction increases to a level where the depletion region extends to the first floating limiting ring, holes in the first ring flow out of the main junction by the electric field. Then, the junction surface of the first ring transitions from being electrically neutral to a small amount of negative charge. This accumulation of negative charge generates an electric field at the surface, which is opposite to the electric field that exists between the main junction and the first ring. Thus, the electric field intensity in the region is weakened by reducing the electric field near the main junction. Furthermore, the MTLG-FLR structure is equivalent to modulating the lateral concentration distribution in the terminal region. The device has a high doping concentration internally, which gradually decreases outwards. This effectively reduces the high electric field at the main junction while avoiding electric field peaks at the outer ring. Figure 5c shows the electric field distribution along the CC' cross-section of the MTLG-FLR structures at breakdown. When S_1 is set to $2.5 \mu\text{m}$, the MTLG-FLR structure exhibits the highest electric field concentration at the main junction. Due to the large spacing, the external P^+ rings fail to play an effective role, ultimately resulting in premature breakdown. On the contrary, when S_1 is reduced to $1.8 \mu\text{m}$, all the rings of both the MTLG-FLR and conventional FLR structures contribute to the overall performance. The surface electric field distribution of the MTLG-FLR is more uniform compared to that of the conventional FLR. Consequently, the MTLG-FLR structure enhances the effectiveness of the field limiting ring by improving the uniformity of the electric field distribution. This, in turn, leads to an increase in the reliability of the terminal structure.

Figure 6 shows a comprehensive comparison of the specific on-resistance and BFOM ($\text{BFOM} = 4V_{BR}^2/R_{on-sp}$) for the device proposed in this paper, as well as the results reported in the references [19,22–27]. The detailed performance parameters are also summarized in Table 2. As illustrated in Figure 6a, at a voltage of 4.48 kV, the R_{on-sp} obtained from theoretical calculations is approximately $10 \text{ m}\Omega \cdot \text{cm}^2$. The results reveal that the MST-JBS structure exhibits a R_{on-sp} of $15.4 \text{ m}\Omega \cdot \text{cm}^2$, which is notably closer to this theoretical limit value compared to that of other diodes. This indicates that under forward bias, the MST-JBS has the lowest conduction losses, which can reduce energy losses and enhance the overall efficiency of the system. The BFOM reflects the trade-off between the specific on-resistance of the device and its blocking capability. A higher BFOM value signifies that lower on-resistance can be achieved at a specified voltage. The results indicate that the BFOM of

the MST-JBS has achieved 5.21 GW/cm², which is significantly higher than that of other devices. Combining the above results, it is evident that the MST-JBS structure demonstrates remarkable effectiveness in achieving an optimal balance between forward conduction performance and reverse blocking capability. This balance significantly enhances the overall performance of the device, making it a prominent candidate in the field of high voltage devices.

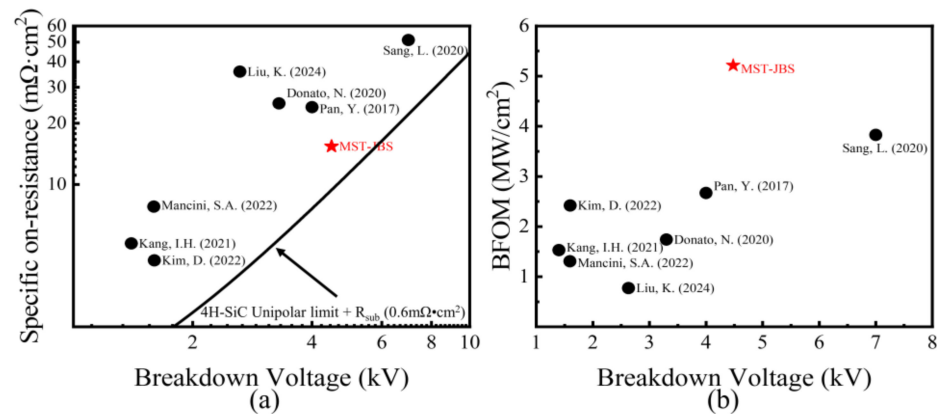


Figure 6. (a) Trade-off between V_{BR} and R_{on-sp} , as well as (b) the trade-off between V_{BR} and the BFOM value of the devices in this paper, as along with the results reported in the references [19,22–27].

Table 2. Performance parameters used in Figure 6.

Reference	Device Structure	V_F (V)	V_{BR} (kV)	R_{on-sp} (mΩ·cm ²)	BFOM (GW/cm ²)
[19]	JBS	1.8 (30 A)	4	23.98	2.67
[22]	JBS	2.0 (20 A)	3.3	25	1.74
[23]	JBS	1.73 (10 A)	1.59	7.79	1.31
[24]	PiN	3.58 (100 A/cm ²)	2.63	35.8	0.77
[25]	JBS	/	7	51.2	3.83
[26]	JBS	1.9 (370 A/cm ²)	1.4	5.14	1.53
[27]	JBSFET	/	1.6	4.24	2.42
Our work	MST-JBS	2.4 (40 A)	4.48	15.4	5.21

5. Conclusions

In this paper, a novel 3300 V/40 A MST-JBS diode with MTLG-FLR termination has been designed and thoroughly analyzed. The introduction of the MST structure in the active region has successfully overcome the inherent limitation of P⁺ region depth in traditional JBS devices. The simulation results demonstrate that the MST-JBS structure utilizes the deep P⁺ region formed by the multi-step trench structure and tightly connects with the depletion layer of the central P⁺ region, achieving a more effective electric field shielding effect. Furthermore, the additional Schottky contacts on the sidewalls actively contribute to forward conduction, effectively optimizing the forward current distribution characteristics of the device and further enhancing its overall performance. The optimized MST-JBS diode exhibits superior forward and reverse characteristics, including a forward voltage drop of 2.4 V, a reverse breakdown voltage of 4480 V, which is a significant 47% improvement over conventional JBS diodes, and extremely low leakage current. This structure not only maintains good forward characteristics but also effectively enhances the reverse characteristics, providing a solution to the trade-off issue between the forward and reverse characteristics of medium- and high-voltage devices. Furthermore, the MTLG-FLR termination structure is introduced, which effectively uniformizes the electric field distribution, surpassing that of the FLR structure by 20%. Therefore, an MST-JBS diode with MTLG-FLR termination greatly expands the applicability of the device in high-voltage applications and significantly enhances its stability and durability.

Author Contributions: Writing-conceptualization and editing, J.L. and Z.W.; software processing and data collation, Z.W., H.S. and Y.X.; validation, J.L. and Z.W.; funding acquisition and writing-review and editing, J.L., Z.W. and L.Z. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the National Natural Science Foundation of China (grant number 62104208 and YZLYJF2020PHD073).

Data Availability Statement: Data are included in the article.

Conflicts of Interest: Author Liming Zhou was employed by the Yangji Electronic Technology Company Ltd. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

References

- Wang, W.; Lu, X.; Wu, X.; Zhang, Y.; Wang, R.; Yang, D.; Pi, X. Chemical-mechanical polishing of 4H silicon carbide wafers. *Adv. Mater. Inter.* **2023**, *10*, 2202369. [\[CrossRef\]](#)
- Takaya, H.; Misumi, T.; Fujiwara, H.; Ito, T. 4H-SiC Trench MOSFET with low on-resistance at high temperature. In Proceedings of the 2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD), Vienna, Austria, 13–18 September 2020; pp. 118–121.
- Wu, J.P.; Ren, N.; Sheng, K. Design and experimental study of 1.2 kV 4H-SiC merged PiN Schottky diode. In Proceedings of the 2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD), Shanghai, China, 19–23 May 2019; pp. 203–206.
- Deng, X.; Xu, X.; Li, X.; Li, X.; Wen, Y.; Chen, W. A novel SiC MOSFET embedding low barrier diode with enhanced third quadrant and switching performance. *IEEE Electron. Device Lett.* **2020**, *41*, 1472–1475. [\[CrossRef\]](#)
- Zhang, Y.L.; Zhang, J.; Ma, H.P.; Chi, Y.Q.; Tian, H.R.; Liu, J.H.; Liu, Q.B.; Chen, Z.G.; Zhang, Q.J. Failure mechanism of 4H-SiC junction barrier Schottky diodes under harsh thermal cycling stress. *Microelectron. Reliab.* **2022**, *136*, 114630. [\[CrossRef\]](#)
- Yue, Y.; Zhu, H.; Liu, X.; Song, Y.; Zuo, X. First-principles study on non-radiative carrier captures of point defects associated with proton generation in silica. *Aip. Adv.* **2021**, *11*, 015214. [\[CrossRef\]](#)
- Li, M.B.; Cao, F.; Hu, H.F.; Li, X.J.; Yang, J.Q.; Wang, Y. High single-event burnout resistance 4H-SiC junction barrier Schottky diode. *IEEE J. Electron. Devices Soc.* **2021**, *9*, 591–598. [\[CrossRef\]](#)
- Meli, A.; Muoio, A.; Trotta, A.; Meda, L.; Parisi, M.; La Via, F. Epitaxial growth and characterization of 4H-SiC for neutron detection applications. *Materials* **2021**, *14*, 976. [\[CrossRef\]](#) [\[PubMed\]](#)
- Lynch, J.; Yun, N.; Sung, W. Design considerations for high voltage SiC power devices: An experimental investigation into channel pinching of 10kV SiC junction barrier schottky (JBS) diodes. In Proceedings of the 2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD), Shanghai, China, 19–23 May 2019; pp. 223–226.
- Tiwari, A.K.; Antoniou, M.; Lophitis, N.; Perkins, S.; Trajkovic, T.; Udrea, F. Retrograde p-well for 10-kV class SiC IGBTs. *IEEE Trans. Electron. Devices* **2019**, *66*, 3066–3072. [\[CrossRef\]](#)
- Zhang, Y.L.; Liu, P.; Lei, G.Y.; Zhang, Q.J. 1.2-kV Low-Barrier 4H-SiC JBS Diodes by Virtue of P-Implants Across Dead Field of Current Flow. *IEEE Trans. Electron. Devices* **2023**, *70*, 4293–4302. [\[CrossRef\]](#)
- Niu, X.; Sang, L.; An, Y.; Wu, P.; Zhang, W.; Liu, R.; Du, Z.; Li, C.; Wei, X.; Yang, Y. Effect of overlap region for schottky metal and field oxide on the electrical characteristics of 6500 V/50A 4H-SiC JBS diodes. *J. Cryst. Growth* **2023**, *603*, 127009. [\[CrossRef\]](#)
- Yuan, H.; Wang, C.; Tang, X.; Song, Q.; He, Y.; Zhang, Y.; Zhang, Y.; Xiao, L.; Wang, Y.; Wu, Y.; et al. Experimental study of high performance 4H-SiC floating junction jbs diodes. *IEEE Access* **2020**, *8*, 93039–93047. [\[CrossRef\]](#)
- Wang, B.; Wang, H.; Wang, C.; Ren, N.; Guo, Q.; Sheng, K. Design and fabrication of 1.92 kV 4H-SiC super-junction SBD with wide-trench termination. *IEEE Trans. Electron. Devices* **2021**, *68*, 5674–5681. [\[CrossRef\]](#)
- Zhang, Y.L.; Liu, P.F.; Zhang, J.; Ma, H.P.; Liu, J.H.; Liu, Q.B.; Chen, Z.G.; Zhang, Q.J. 1.2-kV 4H-SiC JBS diodes engaging p-type retrograde implants. *IEEE Trans. Electron. Devices* **2022**, *69*, 6963–6970. [\[CrossRef\]](#)
- Yuan, J.; Guo, F.; Wang, K.; Liu, N.; Wu, C.; Yang, B. Demonstration of an 1200V/20A 4H-SiC Multi-Step Trenched Junction Barrier Schottky Diode. In Proceedings of the 19th China International Forum on Solid State Lighting & 2022 8th International Forum on Wide Bandgap Semiconductors (SSLCHINA: IFWS), Suzhou, China, 7–10 February 2023; pp. 1–3.
- Dou, W.; Song, Q.; Yuan, H.; Tang, X.; Zhang, Y.; Zhang, Y.; Xiao, L.; Wang, L. Design and fabrication of high performance 4H-SiC TJBS diodes. *J. Cryst. Growth* **2020**, *533*, 125421. [\[CrossRef\]](#)
- Yin, J.; Chen, S.; Chen, H.; Li, S.; Fu, H.; Liu, C. Design space of GaN vertical trench junction barrier schottky diodes: Comprehensive study and analytical modeling. *Electronics* **2022**, *11*, 1972. [\[CrossRef\]](#)
- Pan, Y.; Tian, L.; Wu, H.; Li, Y.; Yang, F. 3.3 kV 4H-SiC JBS diodes with single-zone JTE termination. *Microelectron. Eng.* **2017**, *181*, 10–15. [\[CrossRef\]](#)
- Deng, X.; Xu, S.; Zhang, B.; Zeng, L.; Li, C.; Wu, J.; Li, J. A near ideal edge termination technique for ultrahigh-voltage 4H-SiC devices with multi-zone gradient field limiting ring. In Proceedings of the 2018 1st Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia), Xi'an, China, 16–18 May 2018; pp. 144–148.

21. Yuan, H.; Liu, Y.; He, Y.; Hu, Y.; Zhang, T.; Tang, X.; Song, Q.; Zhnag, Y.; Zhnag, Y.; He, X.; et al. Characteristic and robustness of trench floating limiting rings for 4H-SiC junction barrier Schottky rectifiers. *IEEE Electron. Device Lett.* **2020**, *41*, 1056–1059. [[CrossRef](#)]
22. Donato, N.; Udrea, F.; Mihaila, A.; Knoll, L.; Romano, G.; Kranz, L.; Antoniou, M. Single and repetitive surge current events of 3.3 kV-20 A 4H-SiC JBS rectifiers: The impact of the anode layout. In Proceedings of the 2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD), Vienna, Austria, 13–18 September 2020; pp. 198–201.
23. Mancini, S.A.; Jang, S.Y.; Chen, Z.; Kim, D.; Lynch, J.; Liu, Y.; Raghothamachar, B.; Kang, M.; Agarwal, A.; Mahadik, N.; et al. Static Performance and Reliability of 4H-SiC Diodes with P⁺ Regions Formed by Various Profiles and Temperatures. In Proceedings of the 2022 IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA, 27–31 March 2022; Volume 62.
24. Liu, K.; Zhang, Z.; Tang, X.; Yuan, H.; Zhang, Y.; Liu, Y.; Han, C.; Zhou, Y.; Du, F.; Wang, Z.; et al. Experimental and Simulation Study of Single-Event Leakage Current Degradation and Damage Mechanism in 4H-SiC PiN Diodes. *IEEE Trans. Electron. Devices* **2024**, *71*, 4891–4896. [[CrossRef](#)]
25. Sang, L.; Tian, L.; Li, J.; Niu, Y.; Jin, R. Effect of P⁺ region design on the fabrication of 6500 V 4H-SiC JBS diodes. *J. Cryst. Growth* **2020**, *530*, 125317. [[CrossRef](#)]
26. Kang, I.H.; Seok, O.; Moon, J.H.; Na, M.K.; Kim, H.W.; Kim, S.C.; Bahng, W.; Kim, N.K. Design and Fabrication of 1.2 kV/10A 4H-SiC Junction Barrier Schottky Diodes with High Current Density. *Trans. Electr. Electron. Mater.* **2021**, *22*, 115–120. [[CrossRef](#)]
27. Kim, D.; Jang, S.Y.; DeBoer, S.; Morgan, A.J.; Sung, W. An optimal design for 1.2 kV 4H-SiC JBSFET (junction barrier Schottky diode integrated MOSFET) with deep P-well. *IEEE Electron. Device Lett.* **2022**, *43*, 785–788. [[CrossRef](#)]

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.