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Communication

The Optimization of Program Operation for Low Power Consumption in 3D Ferroelectric (Fe)-NAND Flash Memory

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Abstract: This paper proposes an optimized program operation method for ferroelectric NAND (FE-NAND) flash memory utilizing the gate-induced drain leakage (GIDL) program and validated through simulations. The program operation was performed by setting the time for the unselected cell to reach the pass voltage (V_{pass}) to 0.1 µs, 0.2 µs, and 0.3 µs, respectively. As the time for the unselected word line (WL) to reach V_{pass} increases, the channel potential increases due to a decrease in the electron–hole recombination rate. After the program operation, the threshold voltage (V_{th}) shift of the selected cell and the pass disturb of the unselected cells according to the V_{pass} condition were analyzed. Consequently, there was a more significant change in V_{th} among selected cells compared to the time for unselected cells to reach V_{pass} as 0.1 µs. The findings of this study suggest an optimal program operation that increases slowly and decreases rapidly through the variation of V_{th} according to the program operation. By performing the proposed program operation, we confirmed that low-power operation is achievable by reducing the WL voltage by 2 V and the bit line (BL) voltage by 1 V, in contrast to the conventional GIDL program.

Keywords: three-dimensional FE-NAND flash memory; gate-induced drain leakage; channel potential; program scheme; pass disturb; low power

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1. Introduction

Semiconductor technology is pivotal in modern society, serving as an indispensable foundation across diverse fields. As the demand for semiconductors continues to surge, NAND flash memory technology and performance are constantly evolving, with innovations that encompass enhanced speed, increased density, and reduced power consumption [1–9]. Nevertheless, 2D NAND flash memory is continuously being replaced by 3D NAND flash memory due to technical obstacles such as limited cell density, interference, finite lifespan, and persistent downscaling challenges [10–14]. Moreover, 3D NAND flash memory surpasses 2D NAND flash memory in both performance and capacity, and researchers continue to explore new structures and innovative technologies in the realm of 3D NAND flash memory [15]. The introduction of FE-NAND flash memory aimed to address the issue of high program voltage (V_{PGM}) associated with the charge-trap flash (CTF) structure [16,17]. Ferroelectric field-effect transistors (FE-FETs) fabricated using hafnia-based ferroelectrics are attracting attention as next-generation memory devices due to their low operating voltage, excellent data retention, and fast switching speed.

It has intrinsic, non-volatile memory properties due to its two stable polarization states that can be switched. In addition, it has the advantage of being compatible with existing complementary metal oxide semiconductor manufacturing processes, and the conformal deposition of ferroelectric films is possible even in vertical structures such as 3D

NAND flash memory through atomic layer deposition. Accordingly, research is continuing on 3D FE-NAND flash memory, which adds a ferroelectric thin film to the gate stack of existing NAND flash cells [18]. This study is concerned with the GIDL erase method employed in the CTF structure that was adapted for use in the program operation of FE-NAND flash memory cells [19]. Implementing the GIDL program makes it feasible to perform normal memory operations while maintaining the conventional 3D NAND flash memory structure and wiring method despite the distinctive operational traits of FE-NAND. Furthermore, even in multi-string operation, GIDL can be selectively generated for the BL to be programmed, thereby enabling the same program operation as the conventional 3D NAND flash memory structure.

In this study, we employed the Synopsys Sentaurus Technology computer-aided design (TCAD) tool to analyze the V_{th} of the selected cell and the pass disturb of the unselected cell, depending on the time required for the unselected WL to reach the V_{pass} during the GIDL program operation [20]. In addition, we proposed optimal voltage conditions for the program operation proposed here. Therefore, we confirmed that low-power program operation is achieved by reducing the WL voltage by 2 V and the BL voltage by 1 V, compared with the conventional GIDL program.

2. Structure of the Proposed Program Operation

Figure 1 shows a cross-sectional view of FE-NAND flash memory, which was generated using Synopsys Sentaurus structure editor. The configuration includes memory transistors for WL_0, WL_1, and WL_2, along with string select line (SSL) and ground select line (GSL) transistors. Here, WL_1 represents the selected cell. As detailed in Figure 1 and in Table 1, the structure comprises SiO_2, Poly-Si, HfO_2, and a metal gate. The cross-section in Figure 1 was simulated as a gate-all-around (GAA) structure using the cylindrical command. In addition, models were employed to consider doping concentration dependence, high field saturation, trap scattering mobility, and Trap-Assist-Tunnel (TAT) effects in the device simulations. Also, simulations of the V-NAND structure's operation included the utilization of Shockley–Read–Hall (SRH), Schenk band-to-band recombination, and tunneling models.

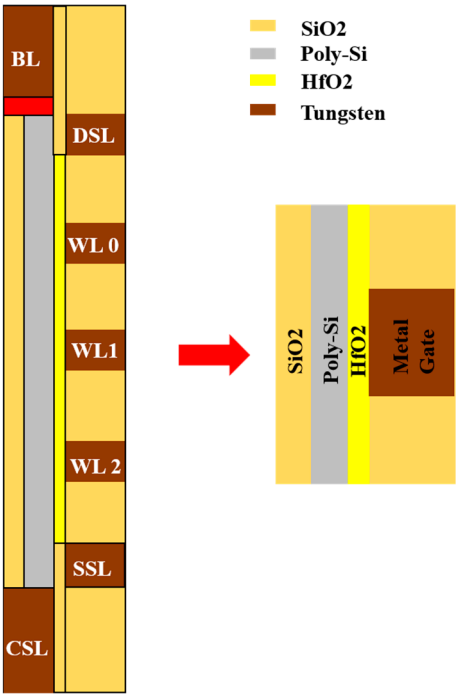


Figure 1. Cross-sectional view of the 3D FE-NAND structure.

Table 1. Parameters of FE-NAND.

Parameters	Value
SiO_2 thickness	20 nm
Poly-Si channel thickness	20 nm
HfO_2 thickness	10 nm
Gate length (WL, SSL, GSL)	40 nm
Spacer length	40 nm
Selected cell	WL_1

Figure 2 shows a voltage–timing diagram for each node employed in the GIDL program operation of the FE-NAND flash memory. The duration for the unselected cell to reach V_{pass} was configured as follows: Case 1 with 0.1 µs, Case 2 with 0.2 µs, and Case 3 with 0.3 µs. When a voltage of V_{PGM} = 10 V is applied to the selected BL and V_{cc} = 2 V is applied to the SSL, the channel potential increases. Selective programming was achieved by applying GND to the selected WL, V_{pass} = 7 V to the unselected WL, and GND to the GSL.

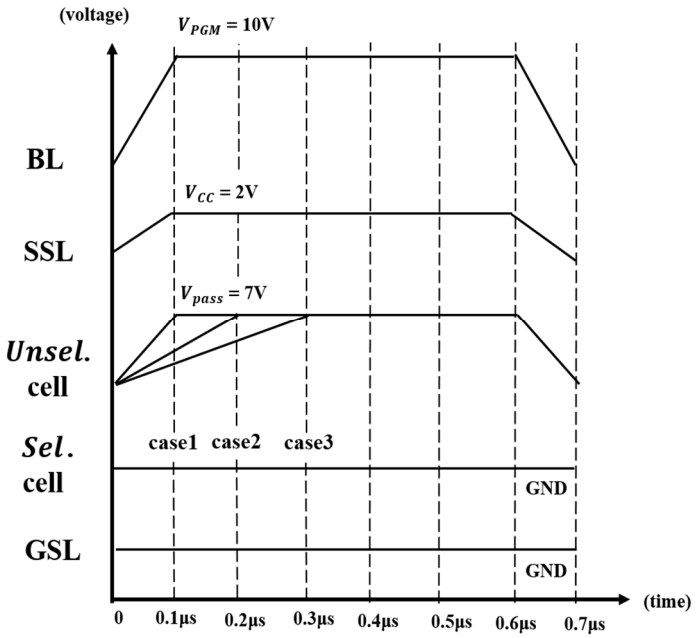
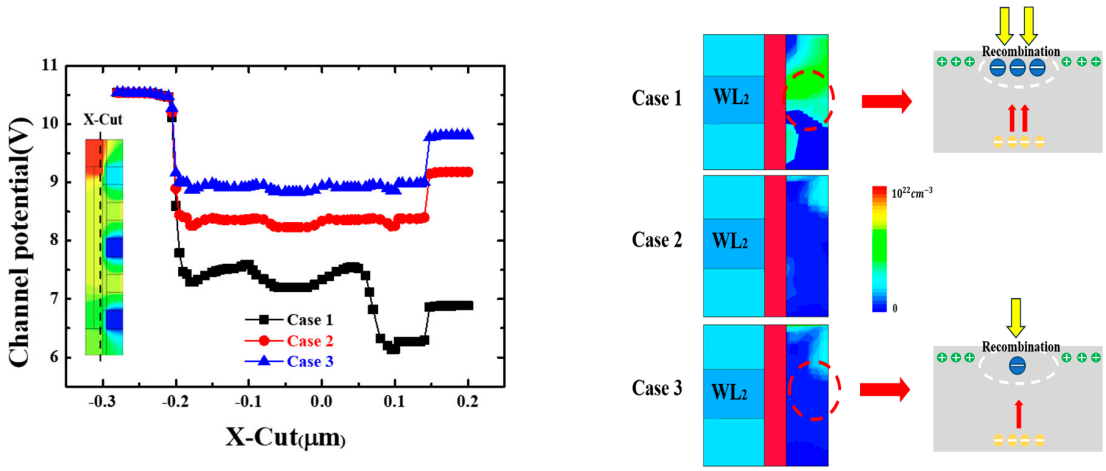


Figure 2. The program operation of the FE-NAND flash memory using GIDL.

3. Simulation Results

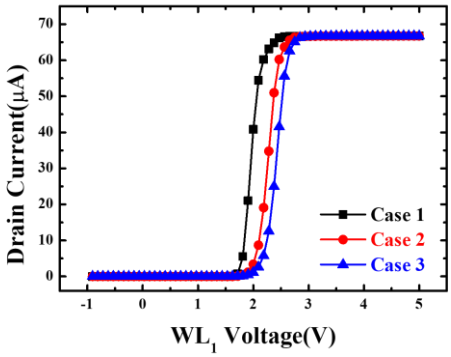
Figure 3a shows the channel potential of the selected string at 0.5 µs during program operation in Case 1, Case 2, and Case 3. The channel potential of the selected string increases sequentially in the order of Case 1, Case 2, and Case 3. Figure 3b presents the channel recombination rates in Case 1, Case 2, and Case 3 during the program operation at 0.1 µs. This explains why the channel potential is highest in Case 3 [21–23]. In Case 1, the recombination rate is the highest, and it progressively decreases towards Case 2 and Case 3. When the unselected cell operates at 0.1 µs, Case 3 exhibits the lowest V_{pass}. A higher V_{pass} leads to a reduction in electron and hole density within the channel due to recombination, ultimately resulting in a decrease in the channel potential.



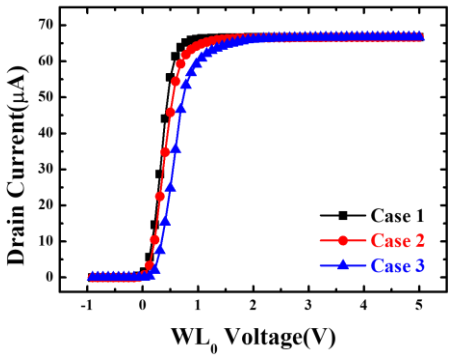
(**a**) (**b**)

Figure 3. Phenomenon in the channels during the operation of the program for Case 1 (BL = 10 V, WL = 7 V), Case 2 (BL = 10 V, WL = 7 V), and Case 3 (BL = 10 V, WL = 7 V): (**a**) selected string channel potential (**b**) for each case channel recombination rate at 0.1 μs.

Figure 4a represents the I−V curve of the selected cell (WL_1) measured at 0.6 μs after programming in all cases. V_{th} increases from 1.789 V in Case 1 to 2.211 V in Case 3. As the channel potential increases during the GIDL program, the potential difference with the selected cell also increases, resulting in it being most programmed in Case 3. Figure 4b,c show the pass disturb of unselected cells (WL_0, WL_2) measured at 0.6 μs after program operation in all cases [24–26]. The V_{th} shifted more in both adjacent cells from Case 1 to Case 2 and Case 3. In the Case 3 programming, a pass disturb of 0.18 V was observed in WL_0, and a pass disturb of 0.17 V occurred in WL_2.

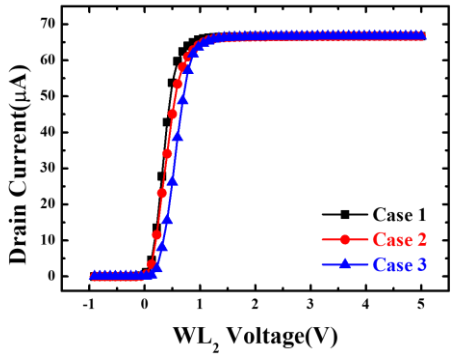


(**a**)



(**b**)

Figure 4. *Cont.*

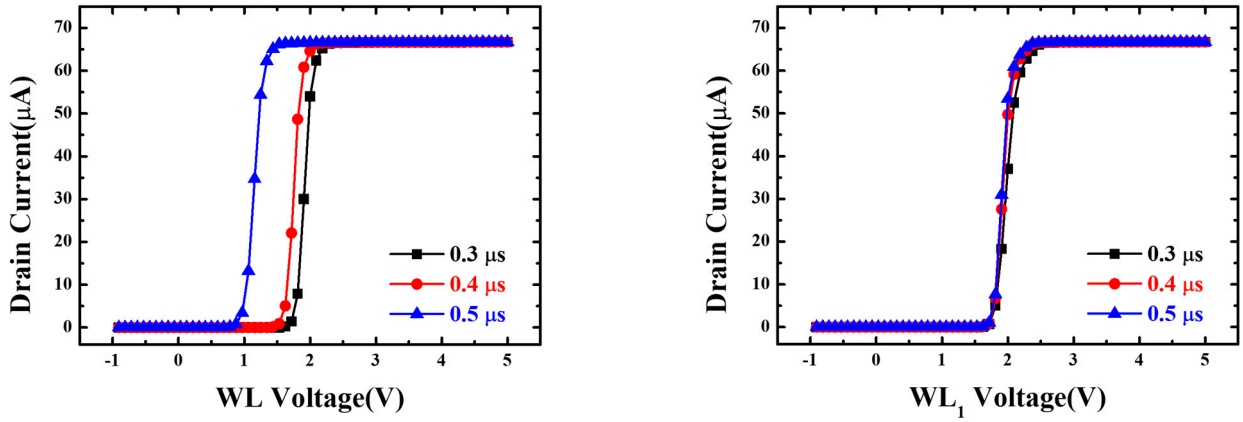


(**c**)

Figure 4. Comparison of I−V curves for different proposed Cases: (**a**) changes in the V_{th} of the selected cell; (**b**,**c**) changes in pass disturb for adjacent unselected cells.

The following results were obtained by comparing to the conventional method of 0.5 μs. In this case, the time for the unselected cell to reach V_{pass} was fixed at 0.1 μs, and then the timing at which V_{pass} decreases was varied to 0.3 μs and 0.4 μs. This approach is in contrast to the proposed program operation method.

Figure 5a represents the I−V curve of the selected cell, measured at 0.6 μs after programming in all cases. As previously mentioned, it was confirmed that there was no effect on V_{th}, as the recombination rate remained consistent. Figure 5b presents the pass disturb of an unselected cell, measured at 0.6 μs after program operation in all cases. Based on the measurement results, the most significant shift in V_{th} occurs when V_{pass} decreases at 0.3 μs. As the decrease time becomes faster, a smaller value of V_{pass} is applied within the same time frame. This results in an increased potential difference, subsequently leading to a higher pass disturb.



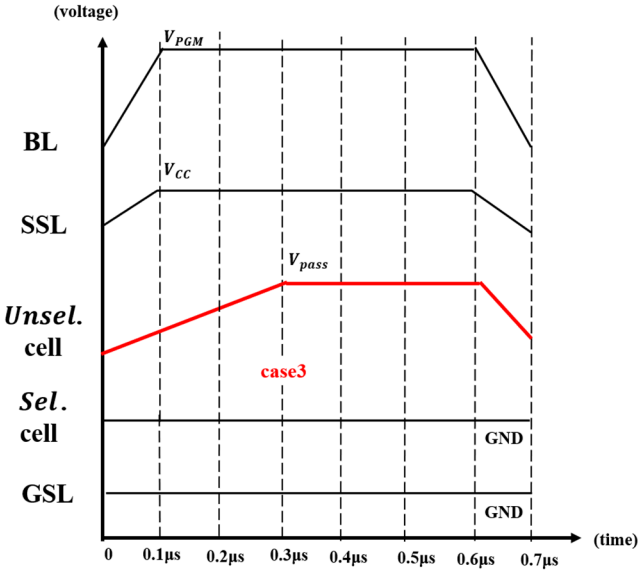
(**a**) (**b**)

Figure 5. Comparison of I−V curves based on the decreasing time while keeping V_{pass} arrival time fixed at 1 μs: (**a**) changes in the V_{th} of the selected cell; (**b**) changes in pass disturb for unselected cells.

Hence, in contrast to the proposed program operation method, an analysis conducted at various time points when V_{pass} decreases after reaching the unselected cell revealed that the shift in the V_{th} of the selected cell had a negligible impact, while the pass disturb due to a substantial V_{th} shift in the unselected cell had a significant effect.

It has been confirmed that low-power program operation is achievable by implementing Case 3, as proposed in this paper. Therefore, the optimal BL/WL voltage conditions during low-power program operation were found by analyzing the program of the selected cell and the disturb of the adjacent unselected cell while reducing it by 1 V increments using TCAD simulation.

Figure 6a,b show the Case 3 timing graph and table of the disturbance of the V_{th} of the selected cell and the adjacent unselected cell during the program operation according to the WL/BL voltage by applying the Case 3 method. In the Case 1 program operation, where the time for the unselected cell to reach V_{pass} is 0.1 µs, corresponding to conventional GIDL program operation, the V_{th} of WL_1 is 1.789 V, and the V_{th} shift due to disturb on WL_0 and WL_2 is 0.129 V and 0.135 V, respectively. Subsequent TCAD simulations confirmed that WL = 5 V and BL = 9 V are the optimal voltage conditions for low-power program operation in the proposed Case 3 during GIDL program operation.



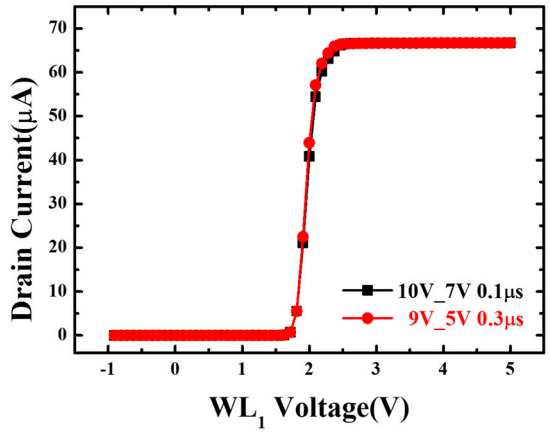
(**a**)

BL \ WL		7V	6V	5V	4V
10V	Program	2.219	2.184	2.138	2.097
	Disturb	0.29	0.73	1.18	1.51
9V	Program	1.792	1.793	**1.792**	1.791
	Disturb	0.137	0.127	0.173	0.458
8V	Program	0.465	0.86	1.339	1.547
7V	program	0.116	0.121	0.127	0.134

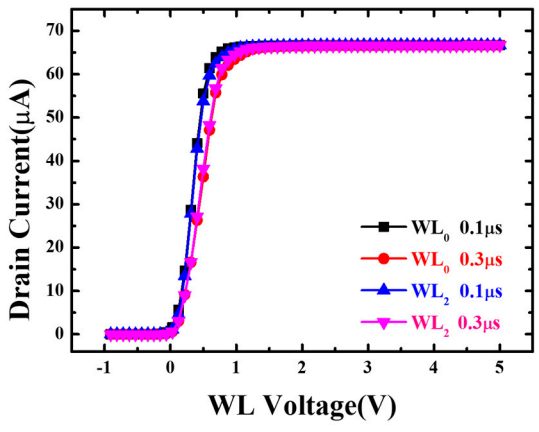
(**b**)

Figure 6. A simulation measuring program and disturb while gradually reducing WL and BL voltages by 1 V each, using the optimized approach: (**a**) Case 3; (**b**) table. The table indicated the optimal voltage conditions.

In Figure 7a,b, a comparison is made between the selected cell and I−V curves of WL_0 and WL_2 under the conditions of BL = 10 V and WL = 7 V, representing Case 1, which corresponds to conventional GIDL program conditions, which were made after program operation was performed in Case 3 under the conditions of BL = 9 V and WL = 5 V.



(**a**)



(**b**)

Figure 7. Comparison of I−V curves between Conventional Case 1 (BL = 10 V, WL = 7 V) and the optimized approach, Case 3 (BL = 10 V, WL = 7 V): (**a**) changes in the V_{th} of the selected cell; (**b**) changes in pass disturb for unselected cells.

As depicted in Figure 7a, it is evident that there is nearly the same degree of change in V_{th}. Specifically, V_{th} = 1.792 V is observed during optimal voltage condition program operation using the Case 3 method, whereas V_{th} = 1.789 V is seen during conventional GIDL program operation. Furthermore, Figure 7b presents a graph comparing the application of an optimal voltage in the programming process using the Case 3 method with the pass disturb of the unselected cell adjacent to the conventional GIDL program. The analysis revealed that the program disturb increased compared to the conventional GIDL program. However, the increase in disturb, approximately 0.05 V, does not pose significant operational issues. Therefore, the proposed program operation has optimized low-power functionality compared to the conventional FE-NAND operation [19].

4. Conclusions

In this study, to optimize the programming method in the 3D FE-NAND flash memory structure, the GIDL program was applied. The voltage applied to the unselected cell was then analyzed under different cases. With an increase in the time it takes for the unselected cell to reach V_{pass}, the electron–hole recombination rate decreases while the channel potential increases. Consequently, the V_{th} of the selected cell increased, and the pass disturb of the unselected cell also escalated. In conclusion, we confirmed that the program effect is most pronounced in Case 3, characterized by the increase of channel potential. On the contrary, it was observed that as the time for the voltage to drop after reaching V_{pass} increases, there is a corresponding increase in the occurrence of pass disturb. Hence, it was established that controlling the V_{pass} time to slowly increase and rapidly decrease yielded the optimal outcome for low-power program operation. Subsequently, following the optimized programming method, BL/WL voltage was reduced by 1 V through TCAD simulation. As a result of these simulations, it was affirmed that low-power program operation could be achieved by lowering the WL voltage by 2 V and the BL voltage by 1 V compared to the conventional GIDL program operation. Therefore, it is expected that this study will make effective contributions when transitioning from the CTF V-NAND structure to the FE-NAND structure in the future.

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Data Availability Statement: Data is contained within the article.

Conflicts of Interest: The authors declare no conflicts of interest.

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