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Review

Hardware Testing Methodologies for Wide Bandgap High-Power Converters

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Abstract: Wide bandgap (WBG) power semiconductor devices are increasingly replacing silicon IGBTs in high-power and high-voltage power electronics applications. However, there is a significant gap in the literature regarding efficient testing methodologies for high-power and high-voltage converters under constrained laboratory resources. This paper addresses this gap by presenting comprehensive, hardware-focused testing methodologies for high-power and high-voltage WBG power semiconductor-based converter bring-up before the control validation phase steps in. The proposed methods enable thorough evaluation and validation of converter hardware, including device switching characteristics, driving circuit functionality, thermal management performance, insulation integrity, and sustained operation at full power. We utilized the double pulse test (DPT) to characterize switching performance in a two-level phase leg configuration, extract circuit parasitics, and validate magnetic components. The DPT was further applied to optimize gate driving circuits, validate overcurrent protection mechanisms, and measure device on-resistance. Additionally, a multicycle test was introduced to rapidly assess steady-state converter performance and estimate efficiency. Recognizing the critical role of thermal management in high-power converters, our methodologies extend to the experimental extraction of key thermal parameters—such as junction-to-ambient thermal resistance and thermal capacitance—via a heat loss injection method. A correlation method between temperature sensor measurements and junction temperature is presented to enhance the accuracy of device temperature monitoring during tests. To ensure reliability and safety, dielectric withstand tests and partial discharge measurements were conducted at both component and converter levels under conventional 60 Hz sinusoidal and high-frequency PWM waveforms. Finally, we highlight the importance of testing converters under full voltage, current, and thermal conditions through power circulating tests with minimal power consumption, applicable to both non-isolated and isolated high-power converters. Practical examples are provided to demonstrate the effectiveness and applicability of these hardware testing methodologies.

Keywords: silicon carbide (SiC); dynamic characterization; double pulse test (DPT); thermal impedance extraction; partial discharge (PD) measurements; power cycling test

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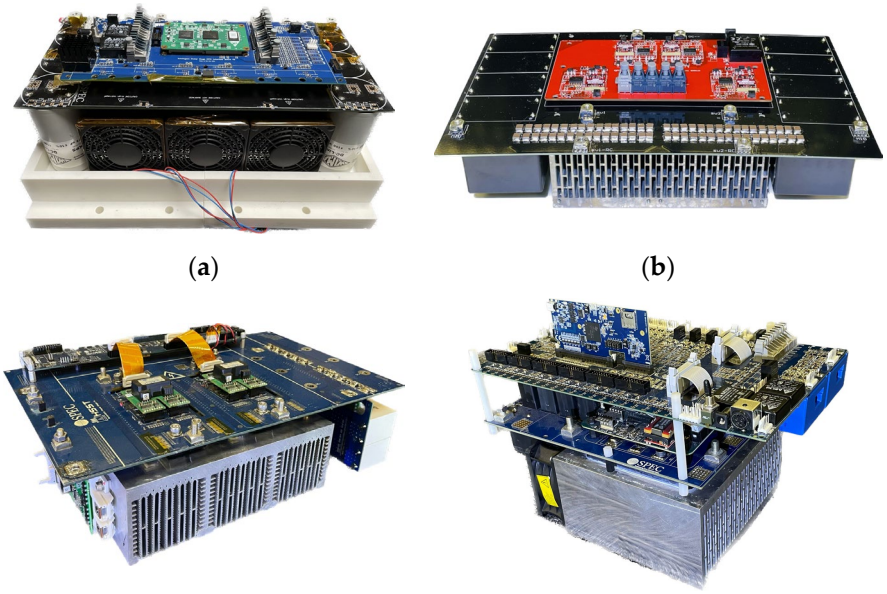
1. Introduction

Wide bandgap (WBG) power semiconductor devices such as silicon carbide (SiC) and Gallium nitride (GaN) are very attractive in high-power applications because of the significantly reduced losses compared with their Si counterparts [1–5]. They are now being commercially introduced at various voltage and current ratings, enabling power conversion applications from kilowatts to megawatts in solar and wind [6,7], battery energy storage systems [8], smart grids [9], electric vehicles [10–12], data centers [13], consumer electronics, and so on.

Due to the superior capability of these devices, researchers with limited resources or experience can also develop very high-power converter prototypes. However, once the high-power converter is designed and assembled, bring-up and validation of the hardware

design become challenging because they require many lab resources such as high-power DC and AC power supplies, heavy-duty resistive loads, and facility electric grid capacity. Also, if tested using resistive load, the test could result in substantial energy waste. For example, the power consumed running a 100 kW resistive load test for one hour may be enough to supply a typical US household for 3–4 days. Therefore, there is a need to validate WBG high-power converters with higher energy efficiency and with limited lab resources [14–20].

The Power Electronics Power Stage (PEPS) is the most critical part of a high-power converter, which generally incorporates power semiconductor devices, the busbar, gate driving circuits, and thermal management components. Figure 1 illustrates a few examples of SiC high-power WBG PEPSs developed. These PEPSs are fundamental units for high-power WBG converters deployed across diverse applications, including grid-forming PV systems, intelligent grid-tied converters, and electric vehicle DC fast chargers [21–23].



(**a**) (**b**) (**c**) (**d**)

Figure 1. Examples of Power Electronics Power Stages (PEPSs). (**a**) 1200 V/4.3 mΩ SiC six-phase power stage. (**b**) 2400 V/7 mΩ SiC full-bridge power stage. (**c**) 1200 V/7.3 mΩ SiC full-bridge plus IGBT full-bridge power stage. (**d**) 900 V/2.5 mΩ three level power stage.

This paper outlines the testing methodologies employed by the authors to bring-up and validate high-power WBG PEPS hardware. The proposed evaluation methods are summarized in Figure 2. This comprehensive testing approach assesses critical aspects, including switching characteristics, driving circuit functionality, thermal management performance, insulation levels, and continuous operation at full power capacity. We utilized the double pulse test (DPT) to characterize the power semiconductor switching behavior, extract parasitic parameters, and validate the magnetics. Furthermore, the DPT serves to optimize gate driving circuits, validate overcurrent protection mechanisms, and measure device on-resistance. In addition to the DPT, we introduced multicycle tests designed to evaluate steady-state performance and estimate efficiency swiftly. Our testing methods extended to experimental verification of key thermal parameters, recognizing the critical importance of thermal management in high-power/high-voltage converters. This verification includes junction-to-ambient thermal resistance and thermal capacitance extraction through heat loss injection. A correlation method between temperature sensor measurements and junction temperature is presented to enhance the accuracy of device temperature monitoring during tests.

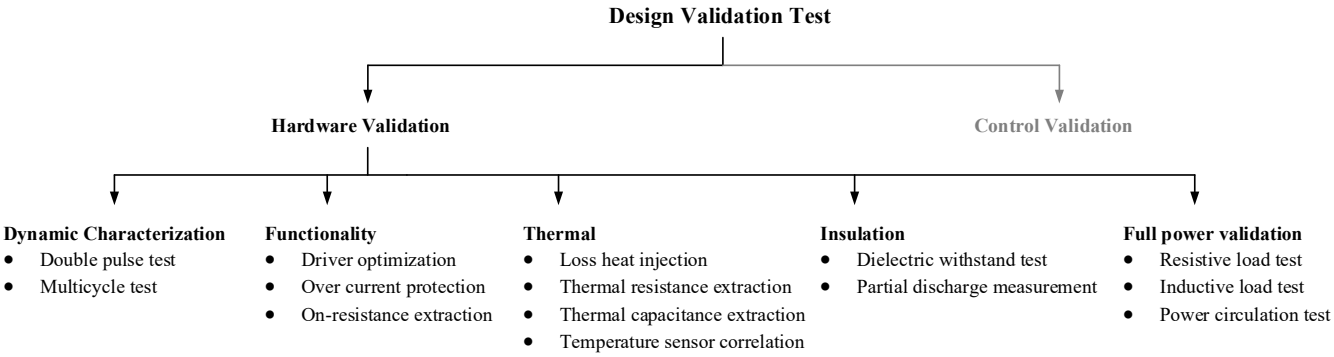


Figure 2. Summary of the design evaluation test.

To ensure the insulation reliability of the converters, our methodology incorporates dielectric withstand tests and partial discharge measurements. These tests serve to verify insulation integrity at both component and system levels. Finally, we underscore the significance of testing converters under full voltage, current, and thermal conditions in power circulation tests. These testing methodologies enable a comprehensive evaluation of the converter's thermal management, testing it to its maximum voltage/current/thermal rating and estimating its efficiency while placing minimal requirements on the power supply, load, passive components, and facility electric grid capacity. These testing methodologies are universally applicable to all high-power converters except where the semiconductor and packaging difference between Si and SiC devices stands out.

2. Switching Characteristics Evaluation

2.1. Double Pulse Test Using the Two-Level Phase Leg Switching Cell

The Double Pulse Test (DPT) is widely used to evaluate a device's switching performance, extract parasitic inductance, validate the gate signal integrity, tune the gate driving circuits, and verify the over-current protection function. A typical DPT test setup is shown in Figure 3. One of the two semiconductors is the device under test (DUT); it can be the top switch or the bottom switch. Since the top switch typically has a much worse common mode noise problem, it is recommended to test the top switch to ensure the integrity of the converter and the gate drive circuit's ability to suppress the noise and false trigger. The other switch in the DPT is parallel to an inductor and acts as the freewheeling switch. Compared with using a freewheeling diode, the freewheeling switch can use the same device as the DUT and works in the third quadrant as a synchronous rectifier, mimicking the operation condition of a real converter. An accurate positive/negative gate driving voltage is also necessary since it changes the device's properties. The DPT is suggested to be tested at no less than 1.5× the current rating at the designed bus voltage in case of a corner case in system operation. The inductor's saturation current needs to be higher than the maximum current in the DPT, so using an air-core inductor is a good practice for DPT. The turn-to-turn capacitance of the inductor can bring an undesired oscillation and hence needs to be minimized. The DPT can also operate with the real magnetics to be used in the system, such as the boost inductor, or short the secondary side of the transformer and work as an inductor; however, the current will be limited by saturation. Once the inductor is constructed and characterized, changing the DUT conduction time T_s can tune the switching current at a certain bus voltage. The pulse energy is mainly from the DC link capacitor C_{DC}. Thus, the power supply can set a less than 1 A current limitation, or an additional contactor, S_1, can be added to disconnect the setup from the power supply after the capacitor bank is charged. Adding energy release resistor R_B and contactor S_2 is optional for safety purposes.

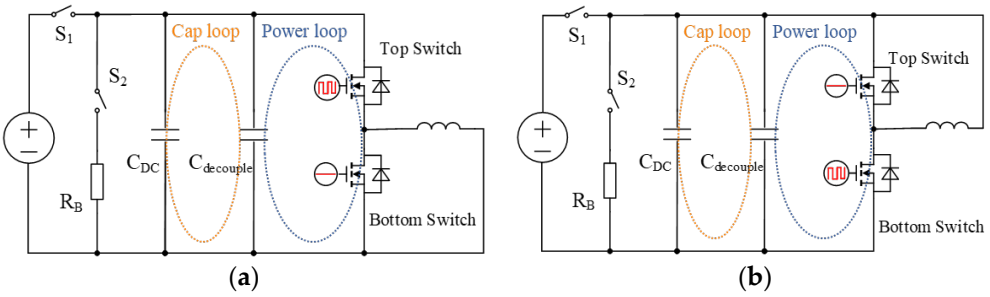


Figure 3. Test setup for double pulse test (DPT). (**a**) Bottom side DPT. (**b**) Top side DPT.

A typical double pulse test waveform is presented in Figure 4; gate-source voltage (V_{gs}), drain-source voltage (V_{ds}), and load inductor current I_L are plotted. The desired switching current can be set by adjusting the pulse width t_1 and t_2. The inductor current after each pulse can be calculated by Equations (1) and (2). Four switching points can be captured, which are: turning on at zero load current; turning off at I_{L1}; turning on at I_{L1}; and turning off at I_{L2}. In most cases, turning on/off at I_{L1} is the test objective, so the second pulse t_2 should be as short as possible to avoid the undesired high turn-off current I_{L2}. This characterization therefore mimics the switching performance of a hard switching converter.

$$I_{L1} = \frac{V_{ds}}{L} \cdot t_1 \tag{1}$$

$$I_{L2} = \frac{V_{ds}}{L} \cdot t_1 + \frac{V_{ds}}{L} \cdot t_2 \tag{2}$$

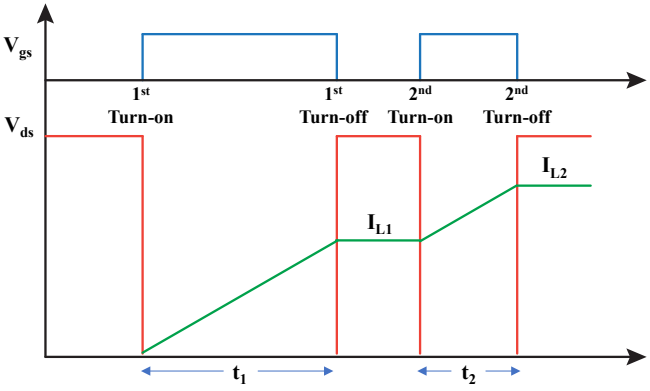


Figure 4. Typical waveform for a double pulse test.

In the DPT, the first turn-on happens at zero load current. Since the load current is zero, the measured DUT current represents the freewheeling switch's reverse current when it is charged from zero volts to the full voltage. This feature can be used to estimate the freewheeling switch's capacitance C_{oss} and stored charge Q_{oss}. The accuracy of this measurement is affected by the parasitic capacitance of the PCB board and the load inductor. Therefore, having the load inductor capacitance characterized separately is needed in order to improve the accuracy of the Q_{oss} measurement.

Since WBG power devices are much faster, a decoupling DC capacitor placed very close to the device is desirable to minimize the device voltage overshoot during the turn-off switching. The decoupling capacitor is recommended to provide more than 250 times the device's internal C_{oss} in [24]; a lower ESL is also desired for better performance. The main DC-link capacitor C_{DC} also needs enough capacitance to ensure each switching dynamic happens at the same voltage; otherwise, the bus voltage will drop, and the second pulse is not characterized at a lower voltage, especially when a current is very high. The parasitic inductance in the entire power commutation loop greatly influences the switching

waveform; a higher loop inductance will contribute to a higher voltage overshoot during the turn-off transients. The power loop inductance L_p can also be quickly calculated by Equation (3); C_{PCB} and C_{probe} are the parasitics induced by the PCB and probes. f is the resonance frequency after turn-off.

$$L_p = \frac{1}{4\pi^2 f^2 \left(C_{oss} + C_{PCB} + C_{probe}\right)} \tag{3}$$

The measurement equipment and correct probe connection points are also critical in the DPT test. The voltage and current measurement equipment must have sufficient bandwidth to capture a high-resolution waveform that can then be used to calculate the switching losses. The equivalent bandwidth of the rising edge and falling edge can be estimated from the rising time (t_r) and falling time (t_f) as $f_{eff} = 0.35/\min(t_r, t_f)$, and the measurement system bandwidth should be at least 3–5 times higher than the maximum equivalent bandwidth of the switching events [25]. A coaxial shunt resistor is claimed to be a high bandwidth solution [26,27]; still, it will increase the loop inductance by at least 2.2 nH, nearly 10% of the total loop inductance for optimized TO-247-based SiC converters, or even 100% for surface-mounted GaN device based converters. A non-invasive current measurement such as a Rogowski coil probe is desired. The lower bandwidth of an off-the-shelf Rogowski coil is the downside for very fast switching cases. Some high-bandwidth Rogowski coils have been researched but not commercialized [28–30]. Rogowski coils can be used in a converter hardware setup where the footprint for the coaxial shunt resistor does not exist. However, the measurement result might be compromised if a high-current conductor (such as the inductor terminal) is placed nearby. Additionally, the bandwidth and size of Rogowski coils are often limited by the availability of commercial options on the market.

Alignment for V-I measurement is essential in loss calculation since a slight difference in probes' propagation delay can cause a significant switching loss calculation error. For example, a 1 ns delay can generate over 80% measurement error with a fast-switching WBG device [25]. Many of the V-I misalignment methods require additional calibration fixtures or components; thus, directly de-skewing by using the DPT waveform is very attractive [31]. The fast-rising device current will cause a voltage dip on V_{ds} during the turn-on, where $\Delta V = L_p \times (dI/dt)$. The V_{ds} and I_d can be aligned using two points; the starting point of the V_{ds} decay should match with the current rise, and the maximum I_d with the maximum voltage dip. A detailed example of V-I alignment is given in the next section with experimental waveforms.

2.2. Understanding a Double Pulse Test Waveform

In a complete converter with a large DC link capacitor, two loops are actually formed, as shown in Figure 5. One is the inner power loop that defines the overshoot voltage and switching loss; the other is the capacitor loop between the small decoupling capacitor and the bulky DC link capacitor. The power loop inductance includes the device's internal inductance, mainly determined by the lead and bond wire, and the external inductance, which is the loop inductance on the busbar. As shown in Figure 5, the power loop introduces a high-frequency oscillation during device switching, and the capacitor loop brings in a lower-frequency oscillation between the decoupling capacitor and the DC link capacitor.

A typical bottom-side DUT DPT waveform is given in Figure 6, where a TO-247 packaged SiC MOSFET (Infineon IMZA120R007M1H (Neubiberg, Germany) [32]) is tested at 800 V and up to 175 A. CH3 is the V_{gs} of the DUT. CH2 shows the drain-source voltage for the DUT directly measured on the lead (closest point to the die in the MOSFET package); CH2 is measured by 800 MHz passive probe TPP0850. CH4 also shows the drain-source voltage for the DUT but is measured on the power terminals on the busbar, which is relatively far away from the die; CH4 is measured by a THDP0200 200 MHz differential probe (Tektronix, Beaverton, OR, USA). CH5 is the drain current, where a TRCP0300

30 MHz Rogowski current probe (Tektronix, Beaverton, OR, USA) is placed around the drain lead of the MOSFET. CH7 presents the current on the inductor, measured by TCP0150. CH6 measures the current in the capacitor loop, which is the sum of the MOSFET drain current, and the current goes into the decoupling capacitors; CH6 is measured by the Rogowski current probe. Figure 6a clearly shows the measured V_{ds} during turn-off is significantly lower if the measurement point is far from the die in the MOSFET package. This result also suggests that measuring the V_{ds} of a SiC power module is less accurate since the power module's drain terminal is far from the die inside the module. Actual device stress is higher.

Figure 6b illustrates the waveform for the first turn-on; it can validate the switching characteristics for soft switching topologies and measure the real Q_{oss} by integrating the measured current. The V-I measurements can be deskewed using the second turn-on waveform under a heavier load condition, as is shown in Figure 6c. Figure 6d shows the second turn-off where the highest overshoot voltage is present. The switching loss during the turn-on and turn-off can be calculated by integrating the V-I overlap during the switching transient. The gate resistance can also be optimized using the double pulse test, trading off between switching speed, loss, overshoot voltage, gate loop stability, and EMI.

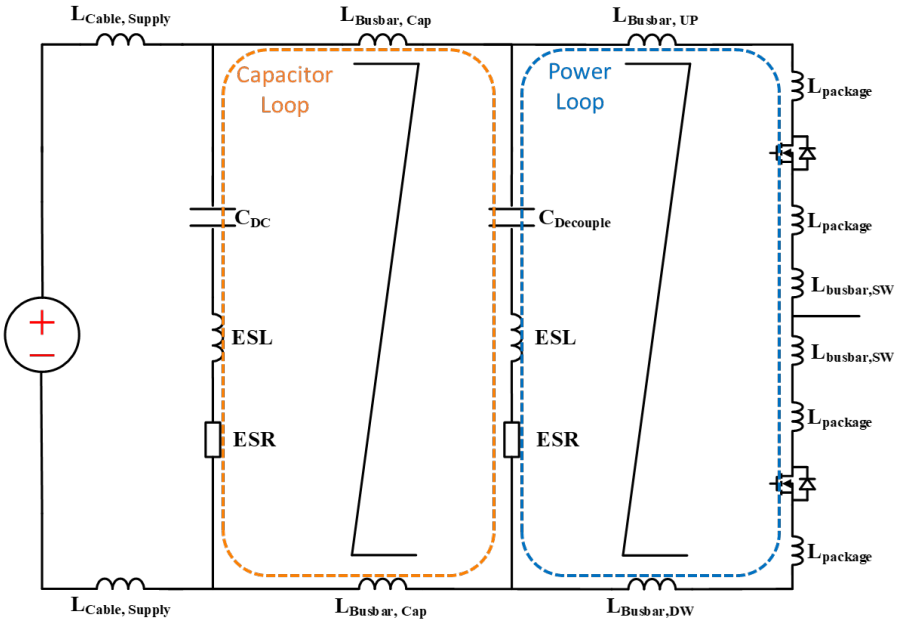


Figure 5. Commutation loop inductance.

The power commutation loop inductance directly impacts the switching loss and voltage overshoot; much research has studied power loop inductance extraction methodologies. The loop inductance can be accurately extracted by Q3D simulation, measured by equipment, or experimentally tested [33–36]. Extracting power loop inductance and capacitor loop inductance through the DPT waveform is very attractive because of its easy implementation. Using the DPT waveform in Figure 6 as an example, the turn-off resonant frequency f_{osc} was measured to be 51.4 MHz, the SiC MOSFET C_{oss} was 420 pF from the datasheet [32], and ignoring all other parasitic capacitance and using Equation (3), the power loop inductance was estimated to be 22.8 nH. This could be revalidated using the V_{ds} voltage dip during the second turn-on or overshoot voltage at the second turn-off. As shown in Figure 6d, the maximum dI/dt was measured to be 6.9 A/ns, the overshoot voltage was 154 V, L_p was calculated to be 22.3 nH by $\Delta V = L_p \times (dI/dt)$. Similar results are shown in Figure 6c, where the maximum dI/dt was measured to be 4.6 A/ns while the V_{ds} dip was 102.8 V, and the L_p was calculated to be 22.3 nH. These three methods find similar results despite measurement error, ignored parasitic capacitance, and inaccurate C_{oss}. The capacitor loop inductance can also be extracted using the decoupling capacitor value and oscillation frequency f_{cap}. For example, in Figure 6a

the capacitor loop inductance is estimated to be 22.2 nH with a 408 nF decoupling capacitor value and 1.69 MHz resonant frequency.

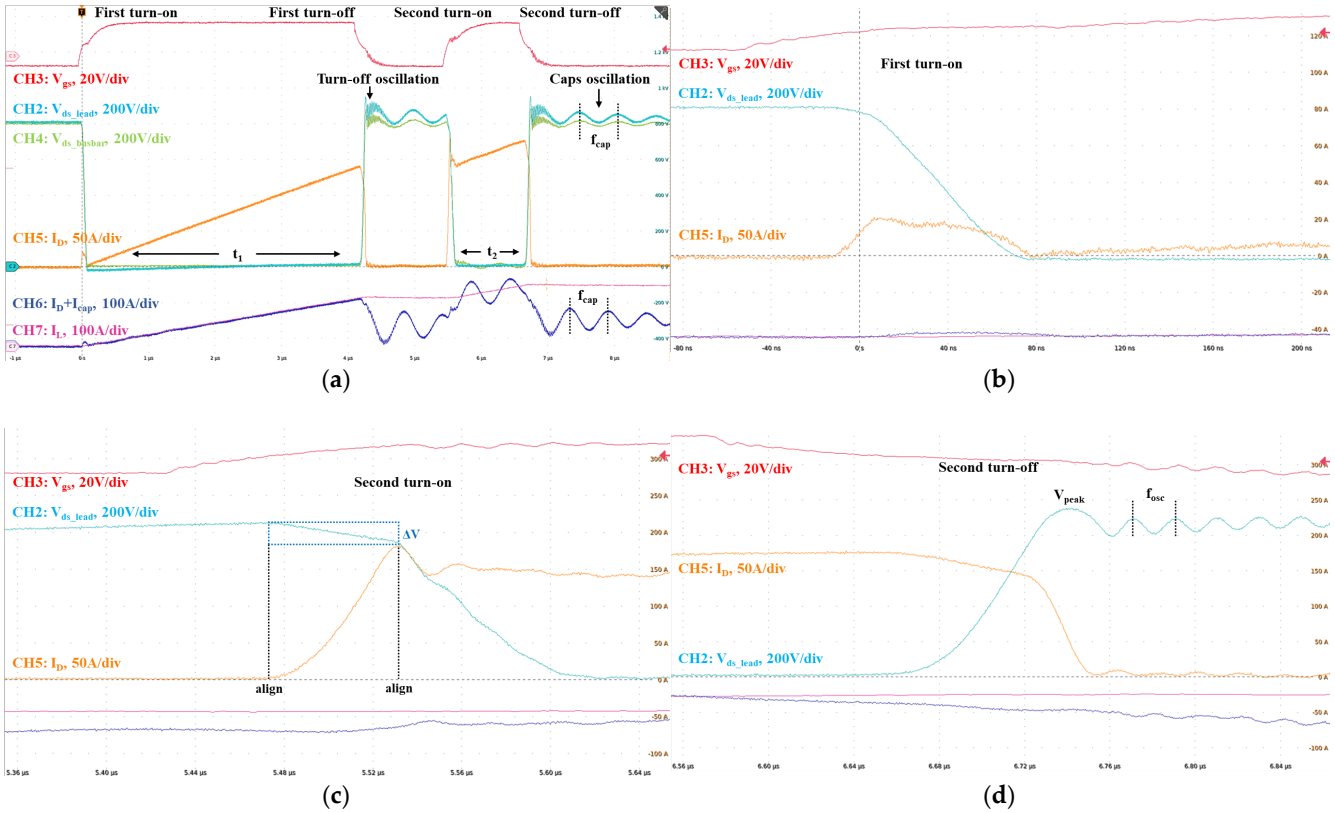


Figure 6. Typical switching waveform for double pulse test. (**a**) Double pulse test with 800 V bus voltage. (**b**) Zoomed-in waveform for the first turn-on at 0 A. (**c**) Zoomed-in waveform for the second turn-on at 138 A. (**d**) Zoomed-in waveform for the second turn-off at 175 A.

2.3. Multicycle Test

The Multicycle Test (MCT) is an essential step for powering up the converter after evaluating the switching performance in the DPT and before continuous operation. In the MCT, the complete converter is connected to a resistive load and runs at the rated voltage and current for several line cycles (60 Hz for grid-connected or a few kHz for motor drives). Limiting the number of cycles to a small value, such as 5–100 line cycles, ensures no need to worry about heating the load or the converter (using thermal capacitance); the resistive load bank can be much smaller than required in continuous tests. The converter may not need to be attached to a fully functioning cooling system. The number of cycles needs to be small so that device heating is not a concern. The MCT can provide validation of the auxiliary voltage power supply unit and driving circuit reliability since the switching pulse number is significantly increased over the DPT (e.g., ten 60 Hz line cycles contain 10 k pulses at a 60 kHz switching frequency). False turn-on/off of the switch and shoot-through should be checked during this stage.

An MCT test example is in [37,38]: a 500 kW inverter was tested to full voltage/current rating while connected to a few kW resistive load and running five line cycles. The converter's efficiency could be estimated by integrating the data from the oscilloscope. However, this efficiency is the upper limit of the converter's real efficiency because the operating temperature is close to room temperature. Once the converter runs continuously and heats up in a steady state, the semiconductor conduction loss and switching loss will increase, and many other passive components and traces will also all become lossy, reducing the steady state efficiency.

2.4. Functionality Validation

Smart functionalities integrated into a high power converter have been extensively researched and are suggested to be a necessary feature for high-power WBG converters [39–42]. These functions include protection circuits, temperature sensing, current sensing, voltage sensing, and online health monitoring. Validating these functions can also take advantage of the DPT's flexible voltage and current control. Figure 7 presents an online voltage measurement and over-current (OC) protection circuit [43]; the circuit consists of a gate driver internal current source, a low-voltage Zener diode D_Z, and a high-voltage Schottky diode D_B. The protection current threshold can be calculated by Equation (4), where V_{DESAT} is the comparator voltage inside the gate driver, and I_{CS} is the current source current. The measurement voltage V_M can be represented by Equation (5), where V_{DB} is the diode D_B voltage. Figure 8 presents a verification of the overcurrent protection function in a DPT. The overcurrent protection was triggered at 88 A, while the current increased to 149 A (determined by t_2 as shown in Figure 4) if the overcurrent protection was disabled.

$$I_{D,max} = (V_{DESAT} - V_{DB} - V_{DZ} - R_1 \cdot I_{CS}) / R_{dson} \tag{4}$$

$$V_M = V_{DB} + R_{dson} \cdot I_D \tag{5}$$

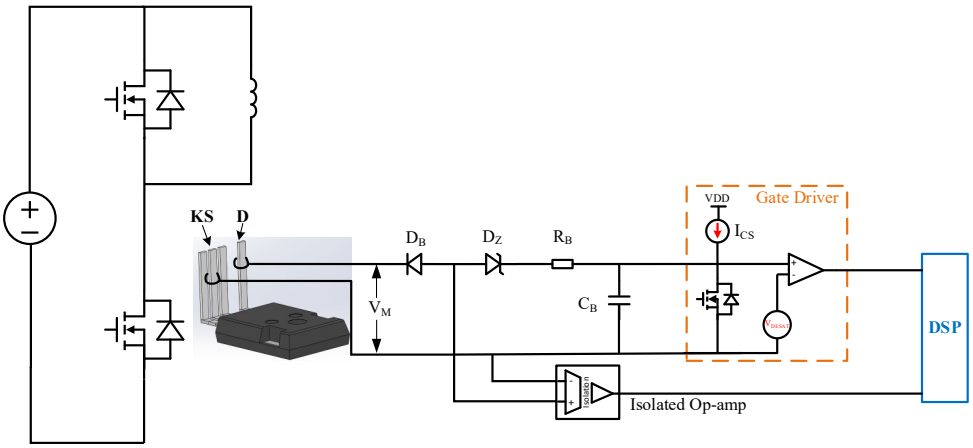


Figure 7. A gate driver integrating online voltage measurement and overcurrent protection circuit.

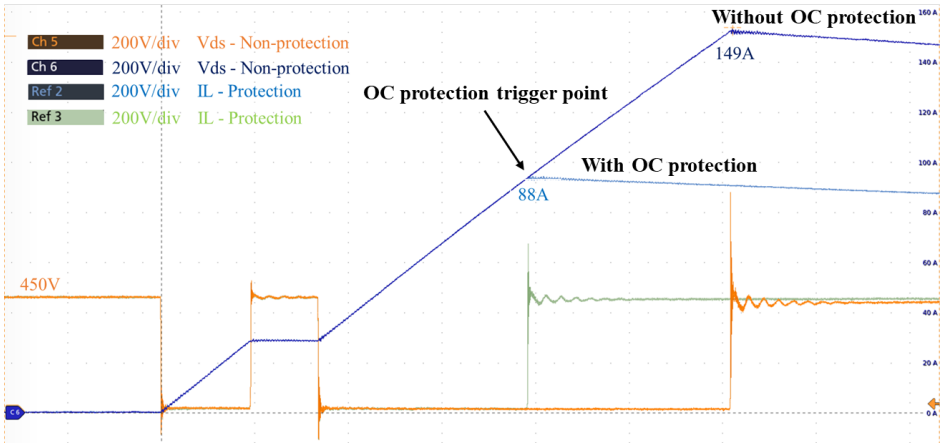


Figure 8. Overcurrent protection validation in double pulse test.

The device's on-resistance can also be extracted during the DPT by using the circuits shown in Figure 7. A Digital Signal Processor (DSP) read 50 VM samples in a DPT. The results are plotted with the device current measured by a TCP0150 current probe, as shown

in Figure 9. The on-resistance could then be calculated as 7.8 mΩ to 8.3 mΩ at 24 °C room temperature, matching well with the datasheet (UnitedSiC, UF3SC120009K4S (Qorvo, Greensboro, NC, USA)) [44].

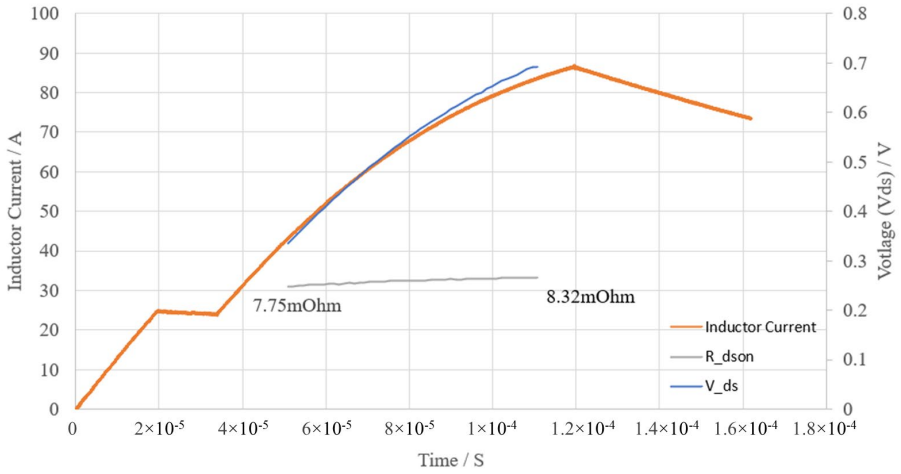


Figure 9. On-resistance extraction in double pulse test.

3. Thermal Management Evaluation

3.1. Heat Injection for Thermal Management Evaluation

Thermal management defines a high-power converter's current and power rating; evaluating the thermal performance is necessary before any high-power continuous test. The thermal impedance can be modeled by a simplified thermal network equivalent circuit model, such as the Cauer model, also known as the continued-fraction circuit (Figure 10a), and the Foster model, also known as the partial-fraction circuit (Figure 10b). The Cauer model reflects the physical setup of the thermal resistance and thermal capacitances. In contrast, the Foster model is an analytical model for thermal parameters calculation; individual RC elements of the Foster model do not represent the layer sequence, and the network nodes do not have any physical correlation [45,46].

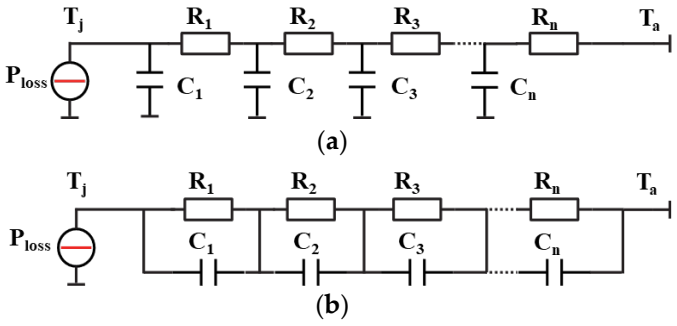


Figure 10. Thermal network equivalent circuit models. (**a**) Cauer model. (**b**) Foster model.

To evaluate the thermal performance, the easiest way to generate a fixed amount of heat is to inject current in the reverse conduction direction of the converter by swapping the connection with the DC busbar (Figure 11a); all the phase legs across the same busbar will be paralleled in reverse conduction. This method works well with SiC and GaN devices since they all include an internal body diode. This method does not work for the Si IGBT or a SiC module with antiparallel diodes since the current will flow in the antiparallel diode, and the actual switch die thermal performance will not be tested. The reverse conduction method is also not suitable for a cascode SiC or GaN FET unless a stacking die structure is used.

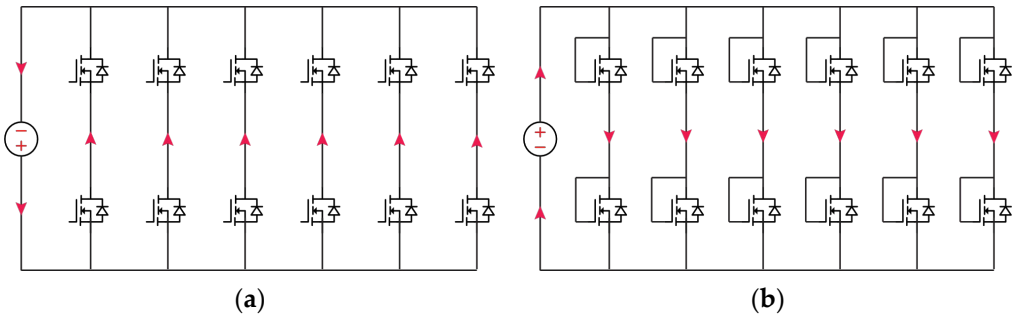


Figure 11. Loss injection for thermal management evaluation of a six-phase power stage. (**a**) Reverse conduction for loss injection. (**b**) Forward conduction for loss injection.

During reverse current conduction, the SiC or GaN junction is heated up, and the steady state junction to the ambient thermal resistance ($R_{th} = R_1 + R_2 + \ldots R_n$) can be extracted when applying the necessary thermal management condition (forced air or liquid cooling). The DC power supply can be a lower voltage DC source and only needs to provide the sum of the devices' reverse conduction voltage drop. However, there are several limitations to the reverse conduction test. The first is that if there are several phase legs on the same busbar, the current required will be higher. Thus, this method needs a lower voltage but very high current power supply. Another problem is that the reverse conducting current may exceed the current rating of the busbar and power connector since most busbars have a lower DC link current capacity than the sum of phase legs. For example, the 1200 V/4.3 mΩ SiC six-phase power stage in [23] is supposed to see less than 100 A DC bus current; however, when injecting 1000 W loss to the PEPS in reverse conduction, the total current from all six phases exceeds 400 A, which heats up the busbar, power connectors, and cables significantly. Power supply at this rating is rarely available in most labs.

The loss can also be injected into the converter by forward conduction of the power semiconductor. However, the WBG device often has relatively low on-resistance, requiring a substantially higher current to generate the same loss, and the gate driver circuits need to be functioning in the test. One alternative option is to short the gate and drain and let the device operate as a diode in the forward direction (Figure 11b). This method is more effective for devices with low reverse conduction voltage drop, such as cascode SiC FETs and GaN. An example is given in Figure 12, where four devices are connected in series and have different thermal resistance. The voltage drop on each device is around 5.2 V when the drain and gate are shorted in forward conduction; the current is 7 A when 36 W loss is injected into the device. However, when it is in reverse conduction, the voltage drop is around 0.9 V, which requires 5.8 times higher current to inject the same loss, bringing in higher current capacity requirements for both the power supply and the busbar.

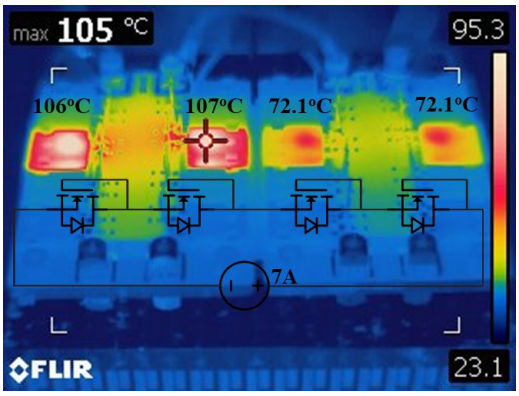


Figure 12. Thermal camera image in a forward conduction loss heat injection test.

3.2. Dynamic Thermal Impedance Extraction

It is also essential to extract thermal capacitance from the actual hardware, especially for junction temperature estimation when there is a load current surge. This test can utilize temperature-sensitive electrical parameters (TSEP), such as the V_{sd} of the device. The V_{sd} at a certain current can be correlated to the device's junction temperature. The thermal capacitance can be extracted by the following steps as described in [43]: first, correlation of the V_{sd} at 0.1 A from 25 °C to 150 °C needs to be obtained using a thermal chamber or hot plate, as shown in Figure 13; this can be obtained with a single device without attaching to any thermal management components, and the V_{sd} can be read by a digital controller or other voltage measurement methods. Typically, the V_{sd} changes linearly with the temperature when the current is constant, as shown in Figure 14.

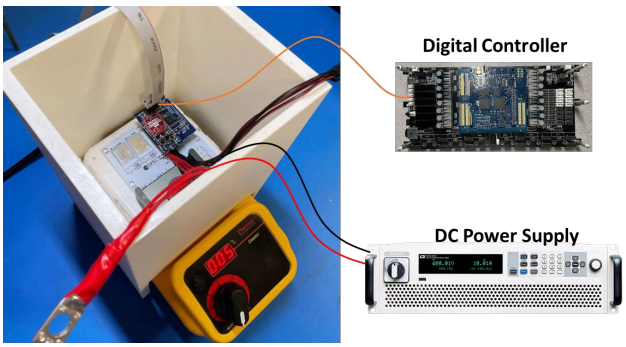


Figure 13. Example for temperature calibration.

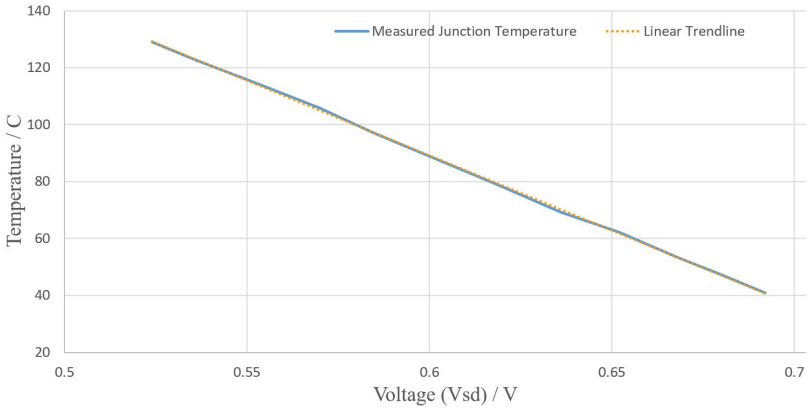


Figure 14. V_{sd} measurement at varies T_j.

After collecting the T–V_{sd} data, the MOSFET should be attached to its full thermal management system to extract its thermal impedance with the actual cooling condition. Heat the device to a higher temperature by reverse current conduction at a high current level, and then quickly step down the power supply current to 0.1 A. Record the voltage V_{sd} change with time. This represents the cooling down of the converter and each voltage point corresponding to a temperature vs. time data point. The thermal impedance can then be extracted by curve fitting to Equation (6) and Equation (7) and extracting the C_n and R_n from its Foster model as in Figure 10b. An example of a typical waveform for thermal impedance extraction is shown in Figure 15. The device heats up in 23 A reverse conduction; then the current is step changed to 0.1 A. The cooling curve is captured by an oscilloscope. Convert each voltage point to a temperature using the T–V_{sd} curve captured earlier.

$$Z_{th}(t) = \sum_{i=1}^{n} R_i\left(1 - e^{-\frac{t}{R_1 C_1}}\right) \quad (6)$$

$$T_j(t) = P_{loss}(t) \cdot Z_{th}(t) + T_a \quad (7)$$

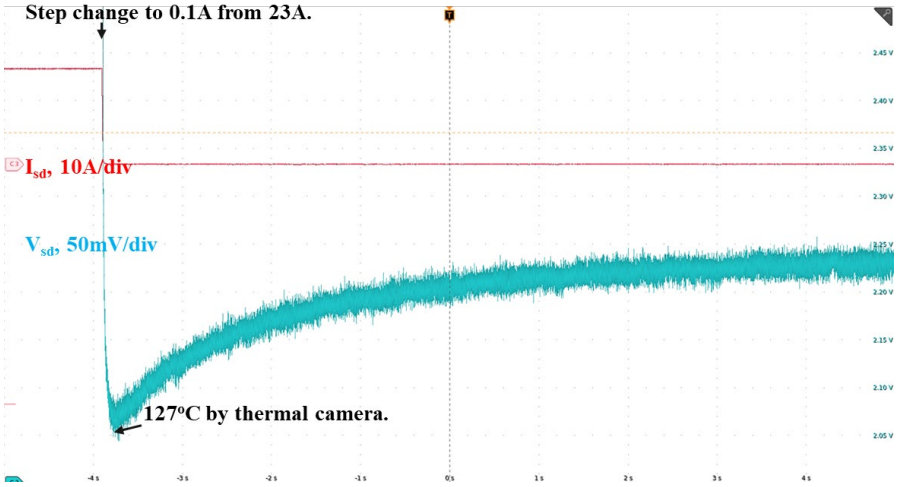


Figure 15. A typical waveform for thermal impedance extraction.

The dynamic thermal impedance extraction method can be extended to establish a correlation between the junction temperature and external temperature sensors located near the power semiconductors, such as built-in NTC thermistors, thermocouples, and thermal cameras used in the experiments. This correlation process mirrors the dynamic thermal impedance extraction approach. After obtaining the T–V_{sd} data, the devices are heated in reverse conduction to various temperatures, followed by step changes at each temperature level. This allows for plotting the temperature sensor versus junction temperature curve, as illustrated in Figure 16.

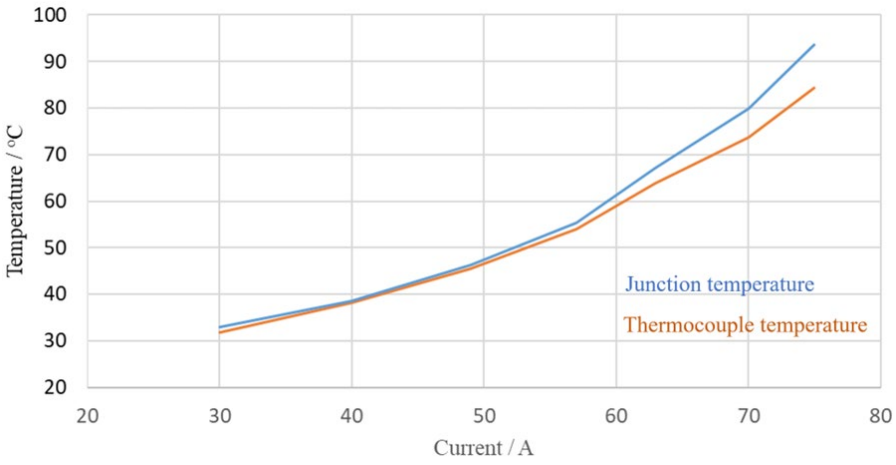


Figure 16. Correlation curve between thermocouple and junction temperature.

4. Insulation Evaluation

4.1. DC Dielectric Withstand Test

High-voltage converters must validate their insulation at both the component and system levels, including power semiconductor-to-heatsink insulation, busbar insulation, and transformer insulation. The dielectric withstand test, commonly known as the high potential (hi-pot) test, applies high voltage to assess insulation levels and must be conducted on all hardware to ensure safe operation before any high-voltage testing. While some commercial equipment is dedicated to the hi-pot test, it can also be quickly performed in the lab when a dedicated hi-pot machine is not available. A simplified approach involves using a high-voltage, low-current DC power supply with the Device Under Test (DUT) connected in series with a high-resistance blocking resistor (R_B) and a low-resistance sensing resistor (R_S) to observe the leakage current. An example of this dielectric withstand test for an Insulated

Metal Substrate (IMS) of a SiC power module is shown in Figure 17, with the measurement results presented in Figure 18. In the test setup, all copper plates on the single-layer IMS power module were connected to the same voltage potential, and the assembly was placed in series with the blocking resistor to the power supply. The power supply's ground terminal was connected to the aluminum substrate of the IMS. The voltage was gradually increased in 100 V increments, and the voltage across a 110 kΩ sensing resistor was measured to extract the leakage current. The sample exhibited repetitive leakage current pulses as the voltage rose from 2627 V to 2722 V, with a dV/dt of approximately 1.2 V/ms, indicating that the insulation capability is below 2.6 kV. This remains adequate for a 1200 V power module, which typically operates at a bus voltage of 800 V.

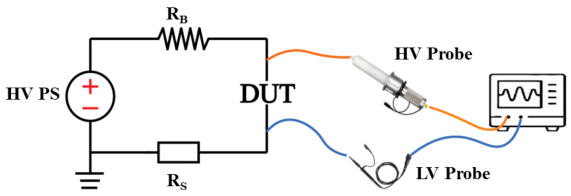
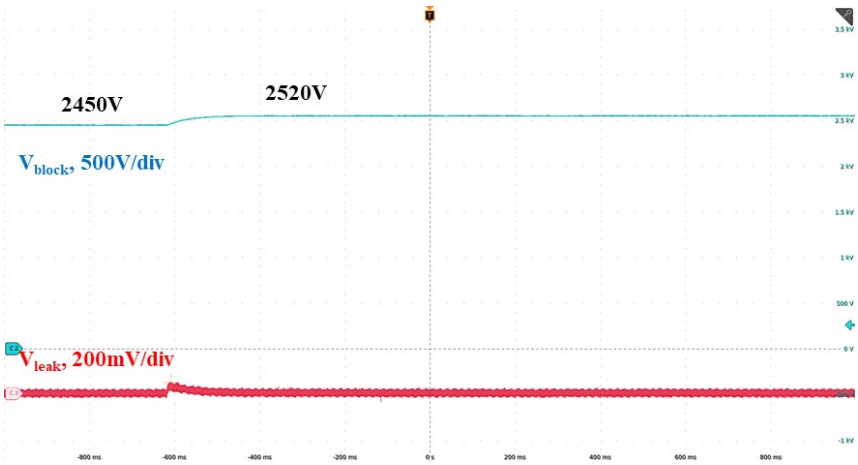
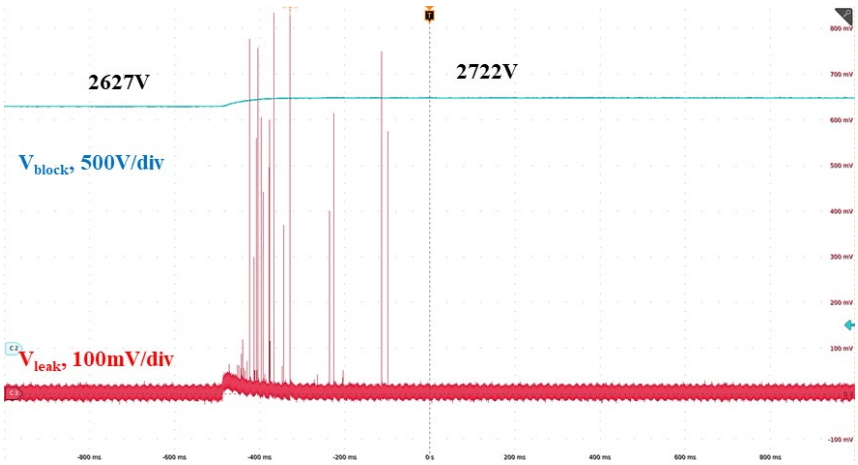


Figure 17. Test setup for DC dielectric withstand test.



(**a**)



(**b**)

Figure 18. Dielectric withstand test result. (**a**) Voltage increasing from 2450 V to 2520 V. (**b**) Voltage increasing from 2627 V to 2722 V.

4.2. 60 Hz Sinusoidal Partial Discharge Measurement

Partial Discharge (PD) is a phenomenon often occurring in insulation system defects (cavities), which can significantly affect lifetime and reliability. Many industry standards and regulations mandate PD tests for power electronics converters. Compliance with these standards is essential for ensuring the safety and reliability of electrical systems [47–50]. The most common PD test is to measure under a 60 Hz sinusoidal waveform. An example circuit diagram of the 60 Hz sinusoidal waveform PD test setup for a medium-frequency transformer (MFT) is shown in Figure 19 [51]. It includes a high-voltage power supply, a C-L-3C filter, a high-frequency current transformer (HFCT), and a PD detector. The PD measurement device's frequency band is 100 kHz to 500 kHz, consistent with the IEC 60270 standard [52]. The cable terminals and high-voltage inductor are placed in transformer oil baths to minimize PD from cable termination and inductor terminals. The discharge pulses sensed by the HFCT are recorded and processed by the PD detector (Doble PD Smart) and transferred to a computer for monitoring and visualization. As all interconnections are appropriately terminated, this setup can conduct both AC and DC PD tests up to 30 kV with a background noise level of 5 pC.

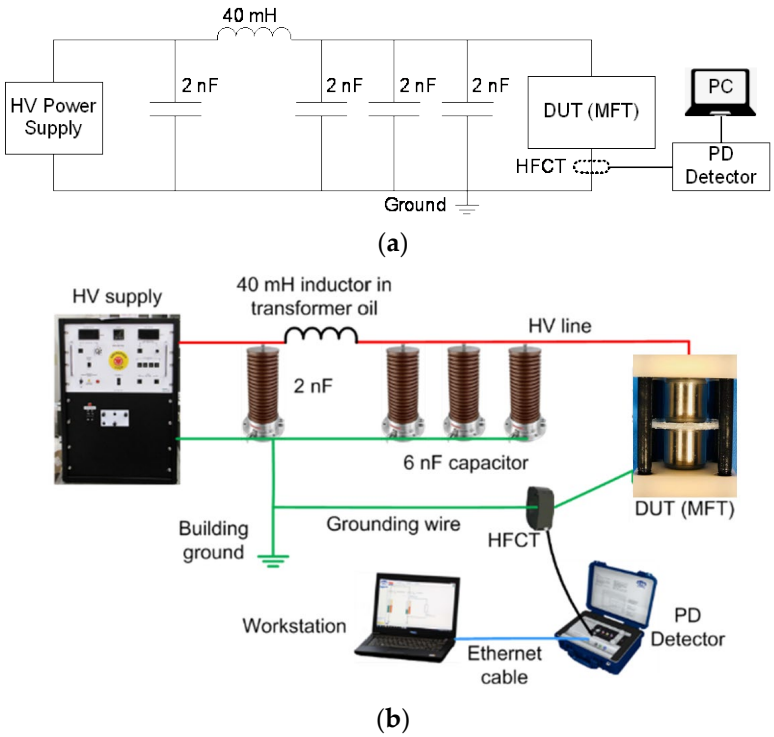


Figure 19. Circuit diagram of a 60 Hz sinusoidal waveform PD test platform. (**a**) Circuit diagram. (**b**) Hardware setup.

Figure 20 shows the PD test process under a 60 Hz sinusoidal waveform. The orange curve represents the applied voltage RMS value, and the blue curve is the PD charge magnitude. Continued PD happens when the voltage reaches 2.7 kV RMS. Figure 21 shows a PD pattern diagram under AC 60 Hz peak-to-peak 7.6 kV voltage. It is a typical internal PD pattern with a maximum charge of around 400 pC.

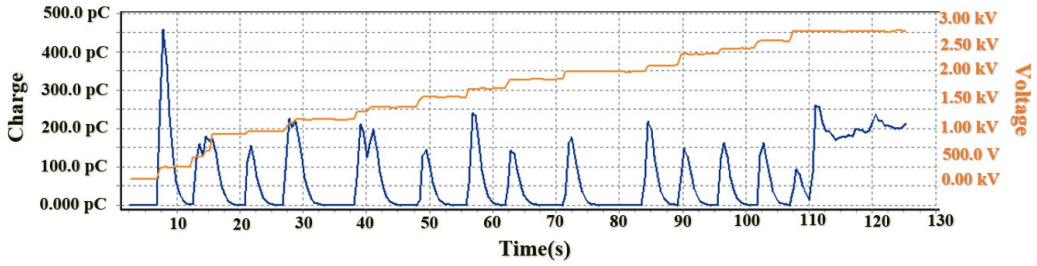


Figure 20. PD test at 60 Hz sinusoidal waveform (orange: applied voltage; blue: PD charge).

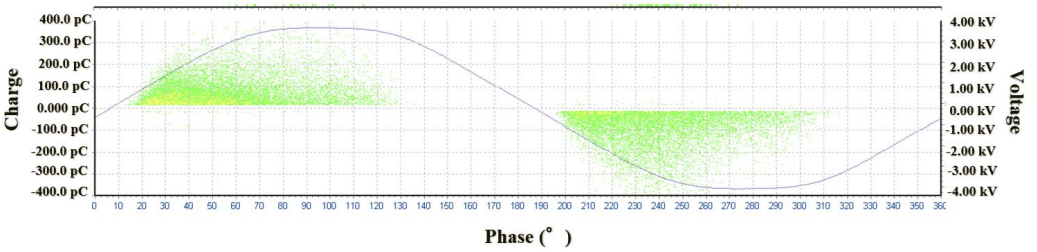
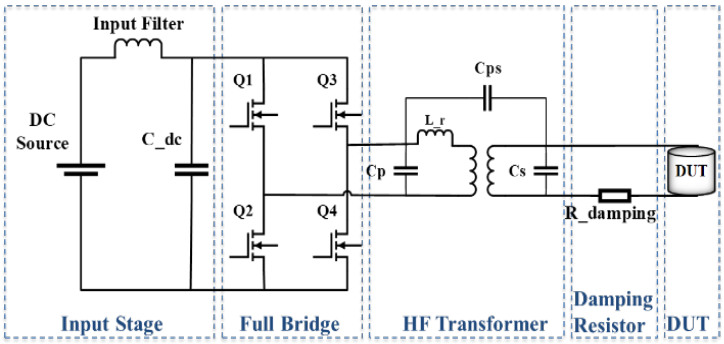


Figure 21. PD pattern diagram at AC 60 Hz peak-to-peak 7.6 kV.

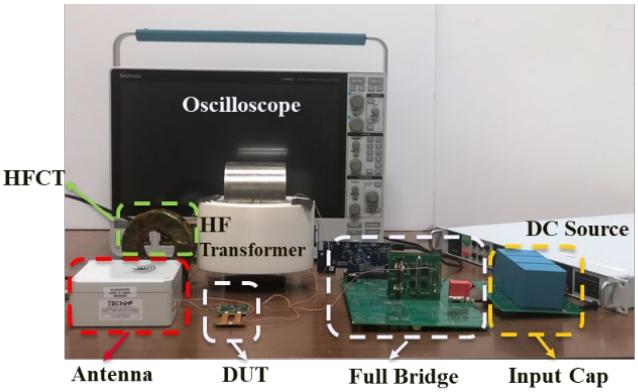
4.3. High-Frequency PWM Partial Discharge Measurement

With the development of wide bandgap power devices, higher voltage and high-frequency square wave voltages are applied in power electronics systems, challenging lifetime and reliability. There is a high demand to characterize PD under high-frequency PWM voltage stress with fast switching speed and high dV/dt. A high-voltage PWM waveform PD test platform is illustrated in Figure 22 [53]. It consists of a GaN-based full-bridge converter with a DC voltage source, a step-up transformer, a variable damping resistor, and the DUT. The full-bridge inverter generates a low-voltage PWM wave, which is then stepped up by the step-up transformer. A variable damping resistor controls the output voltage dV/dt and quality factor. This GaN-based full-bridge inverter is realized using 600 V GaN FET (TI LMG3410R050) and controlled by a Digital Signal Processor (DSP). The step-up transformer is designed with amorphous magnetic cores with a turns-ratio of 1:12.5; 3D printed Acrylonitrile Butadiene Styrene (ABS) bobbins are used to construct the winding structure. A high-bandwidth HFCT (Pearson 6585, Palo Alto, CA, USA, 6585) and an antenna (Techimp TEM antenna, Marlborough, MA, USA) are used for PD signal detection. The TEM antenna and HFCT have bandwidths of 100 MHz–3 GHz and 400 Hz–250 MHz, respectively. The setup was tested at higher than ±5 kV to verify the background noise level (which can affect the sensitivity of PD detection).

Figure 23 shows the test waveforms under 20 kHz and up to 7 kV peak-to-peak PWM pulses for a DUT. Using the experimental data, the PD pattern diagram is plotted. The red dots represent PD pulses, which are located at the rising and falling edges of the PWM waveform.



(**a**)



(**b**)

Figure 22. A high-frequency high-voltage PWM waveform PD test platform. (**a**) Circuit diagram. (**b**) Hardware setup.

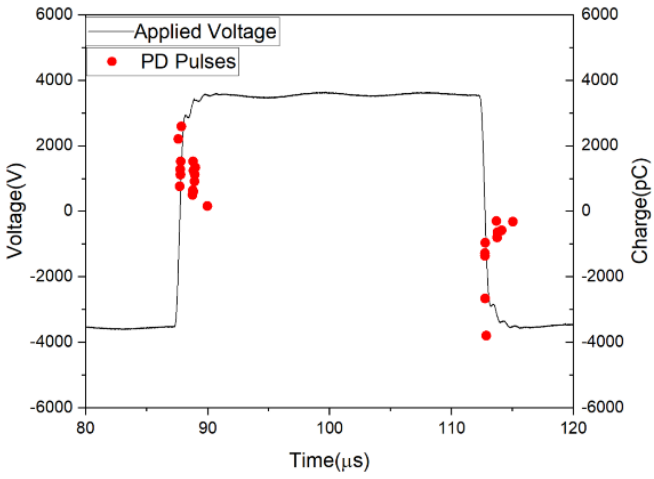


Figure 23. PD pattern diagram under 20 kHz 7 kV peak-to-peak PWM waveform.

5. Full Power Validation

WBG high-power converters must be tested under their full voltage, current, and thermal stress. Ideally, this can be performed quickly by connecting the converter to a resistive load. However, this will require a high-power supply and high power load bank with cooling capability. In many labs this is not feasible. In some cases, the facility's electric grid capacity is also an issue. The resistive load test also causes environmental hazards (heating the space) and wastes much energy, so it should be avoided. Testing the converter with circulating or regenerative power is an attractive solution.

5.1. Circulating Test for Three-Phase Inverter

A three-phase converter/inverter can be configured and tested with inductive load. In this case, the DC power supply only provides the losses (Figure 24). Low-frequency (60 Hz) inverter output voltage is applied to the inductor; hence, this test will require three high current and high inductance-value inductors. These kinds of inductors may not be available in most labs. For example, testing a 480 V/75 kVA three-phase inverter to its full power condition requires an inductor with above 8 mH, which will be huge and heavy. Since the power factor is zero in this test, the tested efficiency and thermal performance also differ from actual cases where the power factor is high.

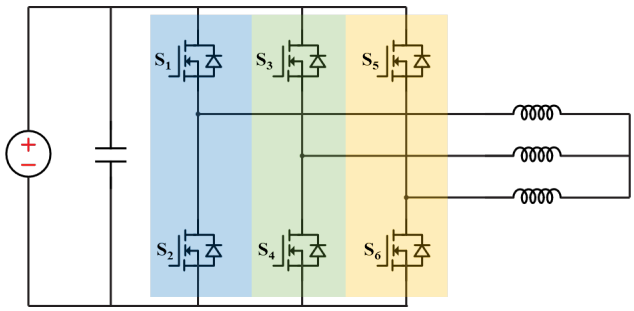


Figure 24. Inductive load three-phase circulating test.

Another way to achieve a full-power test is to circulate the power between converters (also called a back-to-back test or pump-back test) for a single-phase inverter [16,17] or between two three-phase inverters [18,19], as shown in Figure 25. In this case, the voltage applied to the inductor is the difference between two inverter output voltages. Thus, a much smaller inductance can be used.

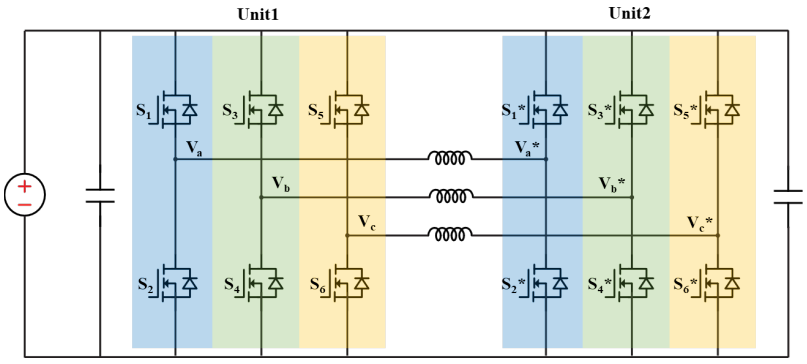


Figure 25. Configuration of the six-phase leg pump-back circulating test.

The test can be performed using an open-loop or closed-loop control. The current can be adjusted by changing the phase shift (θ in Figure 26) between the two legs on the same inductor while maintaining a fixed modulation index. Efficiency can be accurately measured since the DC supply provides only the losses; hence, each converter's losses can be estimated to be half of the DC supply power.

The requirement for power supply is much lower since the WBG power converter usually has higher than 98% efficiency. Testing two 100 kVA inverters only requires a power supply of less than 4 kW. The inductor losses are included in this estimation and can be subtracted if the inductor loss can be estimated separately. High DC link capacitance should be in place for a single-phase test due to the low-frequency AC component. In six-phase leg tests, the two inverters operate as three switching cells, so there is a 120-degree phase difference between three units, and the DC voltage ripple is canceled out more by the balanced three-phase current. Eight states for each switching cell are presented in Figure 27, while Figure 28 presents typical open-loop experimental waveforms.

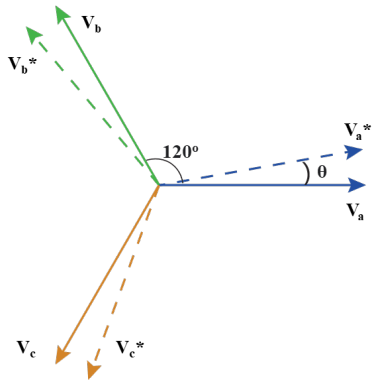


Figure 26. Phasor diagram for pump-back circulating test.

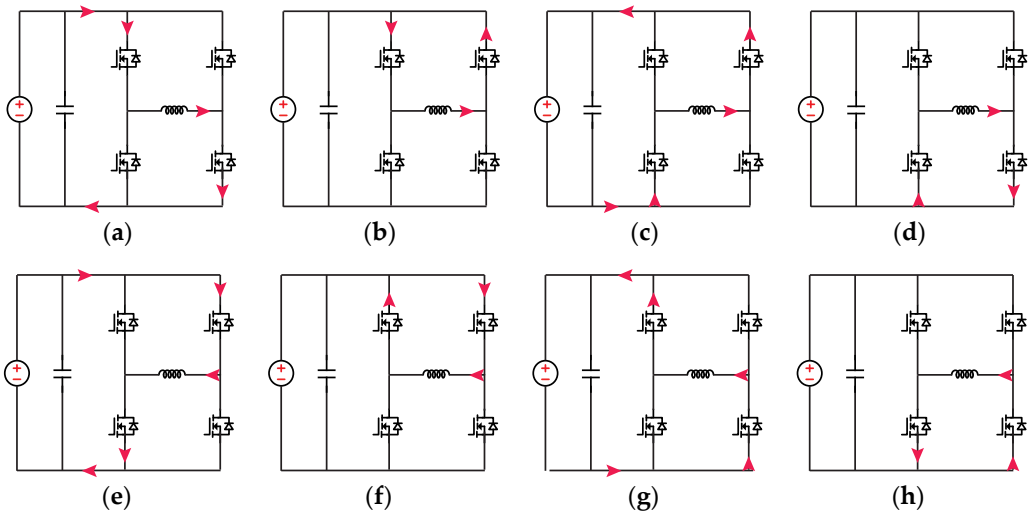


Figure 27. Switching states in the pump-back circulating test. (**a**) inductor current increases. (**b**) freewheeling through top devices. (**c**) inductor current decreases. (**d**) freewheeling through bottom devices. (**e**) inductor current increases in the reverse direction. (**f**) freewheeling through top devices. (**g**) inductor current decreases. (**h**) freewheeling through bottom devices.

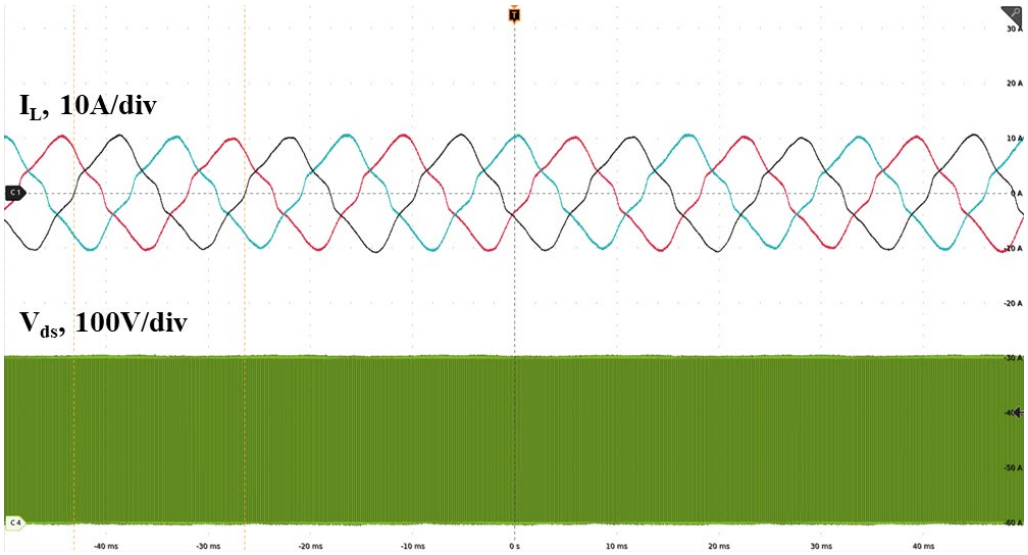


Figure 28. Typical experimental waveform for a circulating test (three inductor current on the top; device drain-source voltage on the bottom).

5.2. Circulating Test for Isolated Converter

Many high-voltage and high-power converters, such as Solid-State Transformers (SST), often employ a modular configuration [5,9,54–56] using many identical cells or submodules. Each submodule needs to be pre-validated before any system-level integration. A pump-back circulating power test can be utilized to validate isolated submodules with a 1:1 conversion ratio, such as a DAB or a CLLC. In this case, both the power electronics power stage and the magnetics are evaluated under the desired operation condition. Reference [55] presents an example test of a 200 kW SiC submodule in a Dual Active Bridge (DAB) converter and CLLC resonant converter using the configuration shown in Figure 29a. The tested converter demonstrated 99.6% at 200 kW; hence, the DC power supply needs to provide very little power during the test. Testing AC-AC SST submodules is discussed in detail in [56], using a circuit like in Figure 29b.

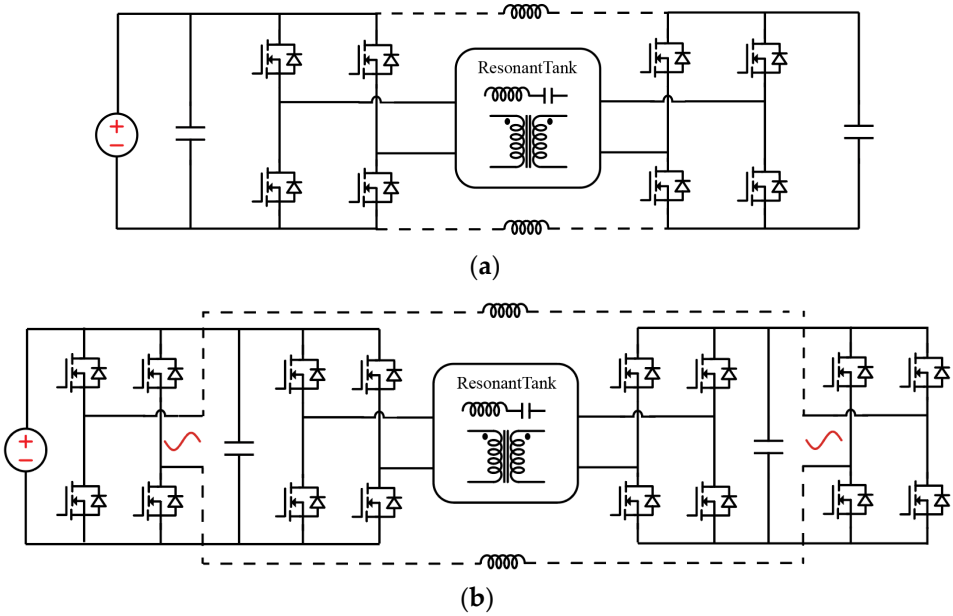


Figure 29. Pump-back circulating test for isolated converters. (**a**) Pump-back test for isolated DC-DC converter. (**b**) Pump-back test for isolated AC-AC converter.

6. Conclusions

This paper fills a critical knowledge gap in hardware testing methodology for emerging WBG-based high-power converters. The proposed testing methodology is essential for new hardware development and validation, offering a comprehensive framework for assessing various aspects of a high-power converter, including switching characteristics, driving circuit functionality, thermal management performance, insulation levels, and continuous operation at full power capacity.

The double pulse test (DPT) is an important platform for power semiconductor device switching performance and switching loss characterization, C_{oss} and Q_{oss} measurement, optimization of gate driving circuits, assessing magnetics components, validation of overcurrent protection mechanisms, and measurement of device on-resistance. Heat loss injection and accurate temperature sensing, which are essential for extracting key thermal parameters with actual cooling conditions for high-power converters, are also discussed in detail. A correlation method between temperature sensor measurements and junction temperature is presented to enhance the accuracy of device temperature monitoring during converter operation.

Dielectric withstand tests are introduced to ensure converter reliability and safety, verifying insulation at both component and system levels. This verification extends to partial discharge measurements under conventional 60 Hz sinusoidal stress and high-

frequency square wave voltage stress. The significance of testing converters under full voltage, current, and thermal conditions is discussed with a focus on the power circulating test for both isolated and non-isolated converters, which minimizes electricity consumption and equipment requirement, underscoring the practical effectiveness and applicability of the proposed testing methodologies.

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