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A Compact Broadband Rectifier Based on Coupled Transmission Line for Wireless Power Transfer

Yan Liu ^{1,*}  and Gang Xie ^{1,2}¹ College of Electrical and Power Engineering, Taiyuan University of Technology, Taiyuan 030024, China; xiegang@tyut.edu.cn² Shanxi Key Laboratory of Advanced Control and Equipment Intelligence, Taiyuan University of Science and Technology, Taiyuan 030024, China

* Correspondence: liuyan0067@link.tyut.edu.cn

Abstract: Wireless Power Transfer (WPT) can effectively solve the problem of autonomous power supply for low-power devices. Rectifier is the key component in WPT technology. In this paper, a novel impedance matching network for the broadband rectifier is proposed. This impedance matching network compensates for the diode impedance and reduces its impedance change when the frequency or input power changes. The passive boosting mechanism utilizing coupled transmission lines (CTLs) improves the power conversion efficiency (PCE) of the diode in the low power region. The structure is especially optimized for low-power device applications. For validation, a broadband rectifier operating at 1.9–3 GHz is fabricated and measured. The structure fabricated on the Rogers 4003 substrate with a thickness of 1.508 mm and the diode is HSMS2860. The DC voltage V_{out} on the load ($R_L = 1300 \Omega$) was measured. The results show that at 0 dBm, the PCE keeps more than 60% at 1.98–3 GHz. The peak PCE of 79.6% is obtained at 4 dBm. The compact size of the broadband rectifier is 19 mm × 21 mm. This broadband rectifier for low input power ranges can be applied to WPT technology.

Keywords: broadband; coupled transmission line; energy harvesting (EH); radio frequency (RF); rectifier; wireless power transfer (WPT)



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1. Introduction

Wireless power transmission (WPT) has received increasing attention as it enables powering devices over long distances [1–3]. The rectifier is an important part of determining the power conversion efficiency (PCE) of the WPT system. High PCE and compactness are research priorities in the design of rectifiers [4,5].

In recent years, many rectifiers have been proposed. These works have focused on single-band [6–9] and multi-band rectifiers [10–14]. The structure presented in Ref. [6] achieves PCE of more than 80% at 2.45 GHz at 25 dBm. A multi-band rectifier with a single impedance matching network is proposed by Halimi et al. [10]. A single-band rectifier is first designed and then converted to dual-band and tri-band by adding transmission lines (TLINs). The structure can work at common bands such as 1.95 GHz and 5.8 GHz. A dual-band rectifier is suggested in Ref. [11]. Using a half-wavelength transmission line (HWTL) in the matching network to increase the operational band. At 3.5 GHz and 5.8 GHz, the PCE is 42.3% and 54.9%, when the input power is 0 dBm. However, most of these structures show narrow-band characteristics and low PCE in other operational bands. Some broadband rectifiers have been designed [15–20]. The 1.6–3.0 GHz range covers many applications such as WIFI, 4G, ISM, and other applications. In Ref. [15], a two-stage impedance matching network is proposed. PCE over 70% from 1.80 to 2.72 GHz at 19.5 dBm. The broadband rectifier presented by He et al. Ref. [16] achieves PCE more than 70% at 2.1–3.3 GHz with an input power of 14 dBm. A compact wideband rectifier

is proposed in Ref. [20]. The structure consists of a multilayer printed circuit board. The center frequency is 12.795 GHz and the fractional bandwidth is 40.33%.

However, these structures are not suitable for low input power. Since the input voltage to the diode must be greater than the threshold voltage in order for the diode to start, the diode loss is the biggest limiting factor in the rectifier circuit's inability to achieve high efficiency at low input power. In order to improve the PCE at low input power, studies have been carried out in Refs. [21,22]. Ref. [21] enhances PCE by increasing the efficiency of each part of the rectifier and by using a low-loss dielectric substrate and reducing diode losses. Ref. [22] achieves high pce by controlling the diode temperature and lowering the threshold voltage.

Coupled transmission lines (CTLs) have been shown in studies to have the effect of expanding the bandwidth [23] and filtering out the harmonics [24]. In this paper, we use additional properties of CTLs. CTLs are combined with TLINs to realize impedance matching over a wide frequency band. On the other hand, CTLs realize passive voltage enhancement, effectively increase the RF signal voltage amplitude loaded on the rectifier diode, and improve the diode forward conduction time and reducing diode losses, which improves the PCE at low power levels. For verification, a broadband rectifier operating at 1.9–3 GHz is fabricated and measured. The structure fabricated on the Rogers 4003 substrate with a thickness of 1.508 mm and the diode is HSMS2860. The DC voltage V_{out} on the load ($R_L = 1300 \Omega$) was measured. According to the measurement result, the PCE reaches more than 40% from 1.9 to 3 GHz with a bandwidth of 44.9% at -10 dBm. The RF-DC conversion efficiency of the rectifier remains above 60% with a bandwidth of 41% from 1.98 to 3 GHz at 0 dBm. At 4 dBm, the highest measurement efficiency is 79.6%.

2. Broadband Rectifier Design and Analysis

Figure 1 shows the schematic diagram of the proposed broadband rectifier, which consists of three main parts. The design of these three parts is described specifically next. The DC pass filter can be realized in the conventional method.

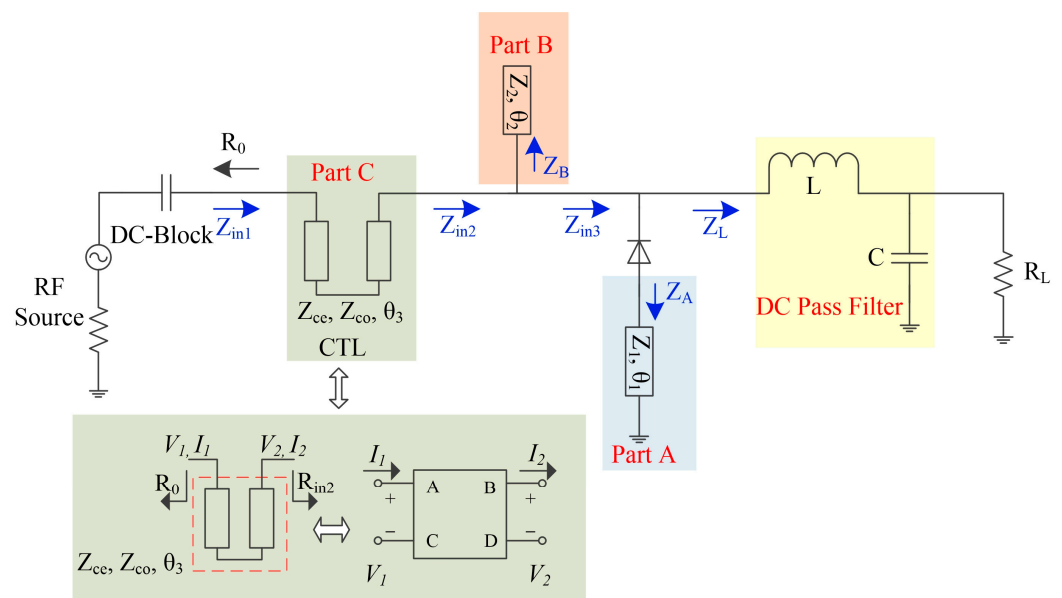


Figure 1. The proposed broadband rectifier.

2.1. Design of Part A

Part A consists of a transmission line. This part realizes the conjugate matching of the input impedance at the lowest and highest frequencies. The lowest and highest operating

frequencies within the wideband are denoted as f_1 and f_2 , respectively. The frequency ratio of f_1 and f_2 is k ($k = f_1/f_2$). The input impedance Z_d at f_1 and f_2 is expressed as:

$$Z_d = \begin{cases} R_{d1} + jX_{d1} \\ R_{d2} + jX_{d2} \end{cases} \quad (1)$$

TLINs labeled as TL₁-TL₂. The characteristic impedance and electron length of the TL₁ are Z_1 and θ_1 . Z_{in3} can be expressed as follows using transmission line theory:

$$Z_{in3}(f_1) = Z_1 \frac{(R_{d1} + jX_{d1}) + jZ_1 \tan \theta(f_1)}{Z_1 + j(R_{d1} + jX_{d1}) \tan \theta(f_1)} \quad (2)$$

$$Z_{in3}(f_2) = Z_1 \frac{(R_{d2} + jX_{d2}) + jZ_2 \tan \theta(f_2)}{Z_1 + j(R_{d2} + jX_{d2}) \tan \theta(f_2)} \quad (3)$$

$\theta(f_1)$ and $\theta(f_2)$ are defined as the electrical length at two frequencies, respectively. $\theta(f_2)$ can be expressed as:

$$\theta(f_2) = k\theta(f_1) = k\theta_1 \quad (4)$$

At f_1 and f_2 , making the real parts of Z_{in3} equal and the imaginary parts are opposite to each other. Thus the impedance at f_1 and f_2 is realized conjugate:

$$Z_{in3}(f_1) = [Z_{in3}(f_2)]^* \quad (5)$$

It follows from (2–5) that

$$\frac{Z_1(R_{d1} - R_{d2})}{R_{d2}X_{d1} - R_{d1}X_{d2}} + \tan((1+k)\theta_1) = 0 \quad (6)$$

$$\frac{Z_1(X_{d1} + X_{d2})}{Z_1^2 - R_{d1}R_{d2} - X_{d1}X_{d2}} + \tan((1+k)\theta_1) = 0 \quad (7)$$

From (6) and (7), the parameters of TL₁ can be solved as:

$$Z_1 = \sqrt{R_{d1}R_{d2} + X_{d1}X_{d2} + \frac{X_{d1} + X_{d2}}{R_{d2} - R_{d1}}(R_{d1}X_{d2} - R_{d2}X_{d1})} \quad (8)$$

$$\theta_1 = \frac{1}{k+1} \left\{ \arctan \left[\frac{Z_1(R_{d1} - R_{d2})}{R_{d2}X_{d1} - R_{d1}X_{d1}} \right] + n\pi \right\} \quad (n = 1, 2, \dots) \quad (9)$$

Part A can be verified by calculating Z_1 and θ_1 . As shown in Figure 2a, Z_{in3} on a wideband is calculated using the impedance change formula. The real part of Z_{in3} is about 30. The imaginary part is essentially symmetrical at the center frequency.

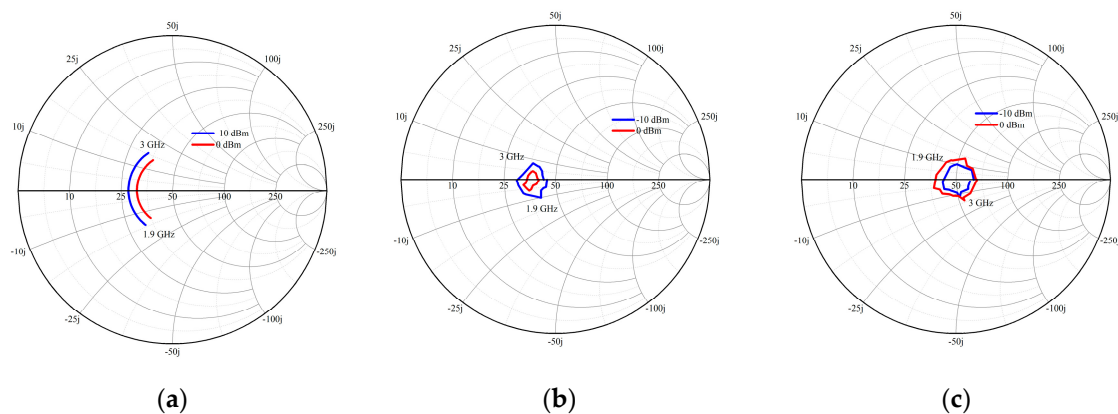


Figure 2. Design principles of the broadband input impedance matching network: (a) Design A; (b) Design B; (c) Design C.

2.2. Design of Part B

Part B consists of an open stub with characteristic impedance Z_2 and electrical length θ_2 . This part is used to eliminate the imaginary part of Z_{in3} and keep the real part unchanged. The input impedance of Z_B can be expressed as:

$$Z_B(f) = -jZ_2 \cot \theta_2(f) \quad (10)$$

According to part A, Z_{in3} at f_1 and f_2 can be expressed as follows:

$$Z_{in3}(f_1) = R_3 - jX_3 \quad (11)$$

$$Z_{in3}(f_2) = R_3 + jX_3 \quad (12)$$

To eliminate the imaginary part of Z_{in3} by adding an open stub:

$$Z_B(f_1) = -jZ_2 \cot \theta_2 = jX_3 \quad (13)$$

$$Z_B(f_2) = -jZ_2 \cot(k\theta_2) = -jX_3 \quad (14)$$

From (13) and (14) calculate Z_2 and θ_2 :

$$\theta_2 = \frac{\pi}{1+k} \quad (15)$$

$$Z_2 = X_3 \tan(k\theta_2) \quad (16)$$

Z_{in2} is defined as:

$$Z_{in2} = \frac{1}{\frac{1}{Z_{in3}} + \frac{1}{Z_b}} \quad (17)$$

The results show that the real part of Z_{in2} and Z_{in3} are the same and the imaginary part is close to 0. Figure 2b shows the performance of Z_{in2} in the Smith Chart for different input power levels. The curves are close to the real axis and are compressed within a smaller region. The part C realizes further matching of the source impedance with the diode input impedance.

2.3. Design of Part C

Part C consists of a CTL. The coupling of two transmission lines results from the interaction of their respective electromagnetic fields when they are in close proximity. The coupling effect varies at different frequencies. Since the imaginary part of Z_{in2} is zero, only the real part R_{in2} of Z_{in2} needs to be considered. CTLs have more design freedom because they have many design parameters. The Z_{in2} can be changed during the design process by adjusting the width, gap distance and electrical length of the CTL. Impedance matching is realized in two frequencies according to Ref. [25]. Then, they are matched and adjusted within the bandwidth. Figure 1 shows a schematic diagram of the parameters of the CTL. The matrix of the CTL can be expressed as:

$$A = D = \frac{Z_{ce} - Z_{co} \tan^2(\theta_3)}{Z_{ce} + Z_{co} \tan^2(\theta_3)} \quad (18)$$

$$B = \frac{2Z_{ce}Z_{co}j \tan(\theta_3)}{Z_{ce} + Z_{co} \tan^2(\theta_3)} \quad (19)$$

$$C = \frac{2j \tan(\theta_3)}{Z_{ce} + Z_{co} \tan^2(\theta_3)} \quad (20)$$

At f_1 and f_2 , Z_{in2} is converted to Z_{in1} by a CTL.

$$Z_{in1} = \frac{A_{f_1} V_2 + B_{f_1} I_2}{C_{f_1} V_2 + D_{f_1} I_2} = \frac{A_{f_1}(Z_{in2}) + B_{f_1}}{C_{f_1}(Z_{in2}) + D_{f_1}} \quad (21)$$

$$Z_{in1} = \frac{A_{f_2} V_2 + B_{f_2} I_2}{C_{f_2} V_2 + D_{f_2} I_2} = \frac{A_{f_2}(Z_{in2}) + B_{f_2}}{C_{f_2}(Z_{in2}) + D_{f_2}} \quad (22)$$

Z_{in1} is the source impedance of the rectifier. The CTL parameters Z_{co} , Z_{ce} , θ_3 can be solved by (18–22):

$$Z_{co} = \frac{\sqrt{4Z_{in}R_0 \tan^2 \theta_3}}{2 \tan^2 \theta_3} = \frac{\sqrt{Z_{in}R_0}}{\tan \theta_3} \quad (23)$$

$$Z_{ce} = Z_{co} \tan^2(\theta_3) = \sqrt{Z_{in}R_0} \tan \theta_3 \quad (24)$$

$$\theta_3 = \frac{\pi}{1+k} \quad (25)$$

After obtaining the initial parameters of the CTL and further fine-tuning is performed using ADS simulation software to get a better match on the wideband. The input impedance is obtained by part C as shown in Figure 2c. The curves remain essentially the same at -10 dBm and 0 dBm, indicating that the rectifier can operate over a wide input power range.

At low power input, the load voltage of the rectifier is introduced along the DC path to the diode. When the V_d of the diode is less than or equal to the V_{bi} of the diode, the diode is not turned on because there is not enough energy. According to Ref. [26], a new CTL-based design criterion is used in order to boost the V_d of the diode.

$$G_v = \left| \frac{V_2}{V_1} \right| = \left| \frac{1}{A + \frac{B}{Z_{in2}}} \right| = \left| \frac{(Z_{ce} - Z_{co} \tan^2 \theta_3) Z_{in2} + j2Z_{ce}Z_{co} \tan \theta_3}{j2Z_{in2} \tan \theta_3 + Z_{ce}Z_{co}} \right| \quad (26)$$

G_v represents the voltage gain by introducing a CTL. Substituting the values obtained from (23–25) into (26) obtains $G_v > 1$. This passive voltage boost is used to augment the input voltage, thereby increasing the dc voltage across the diodes.

The design parameters of the proposed structure are obtained from the derivation. To facilitate the rectifier processing, the actual physical lengths and widths are provided in Table 1.

Table 1. Design parameters for the broadband rectifier.

Parameter	Value (mm)	Parameter	Value (mm)
W_1	2.26	L_1	0.76
W_2	3.27	L_2	5.54
W_3	5.85	L_3	5.68
W_4	0.30	L_4	12.23
G	5.00		

3. Implementation and Experimental Results

For verification, a broadband rectifier is designed. The structure fabricated on the Rogers 4003 substrate (Rogers Corporation, Chandler, AZ, USA) ($\tan \delta = 0.0027$, $\epsilon_r = 3.55$) with a thickness of 1.508 mm and the diode type is the Schottky diode HSMS2860. The DC voltage V_{out} on the load ($R_L = 1300 \Omega$) was measured by varying the input power and frequency. The DC-block capacitor is 24 pF. The DC-pass filter consists of a 5 nH inductor and a 24 pF capacitor. Figure 3a shows the layout of the rectifier. Figure 3b shows the fabricated rectifier.

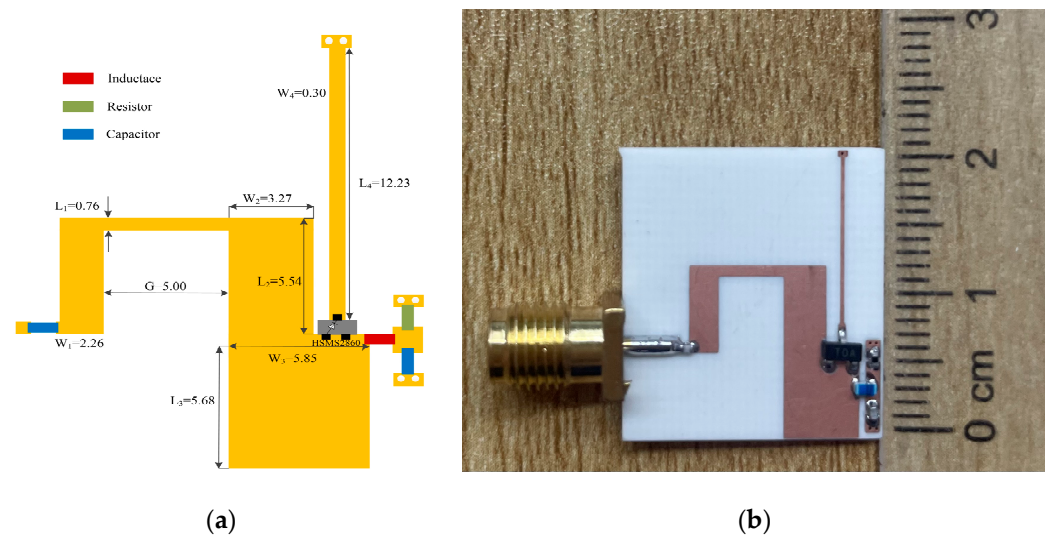


Figure 3. (a) Layout of the proposed rectifier; (b) Fabricated rectifier.

PCE is the ratio of output power to input power, which is represented as:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out}^2}{P_{in} \times R_L} \quad (27)$$

where V_{out} is DC out voltage, R_L is the load, P_{out} is output power, and P_{in} is input power.

Simulated and measured input return loss (S_{11}) at 0 dBm. As shown in Figure 4a, S_{11} is less than -10 dB from 1.85 GHz to 3.0 GHz, which shows the structure performs well over a wideband. The rectifier of the PCE versus frequency at 0 dBm is shown in Figure 4b. The simulated and measured results are essentially identical. In the wide band range of 1.98–3 GHz, the PCE is over 60% and the bandwidth is 41%. The difference between simulated and measured results may be due to processing errors and diode losses.

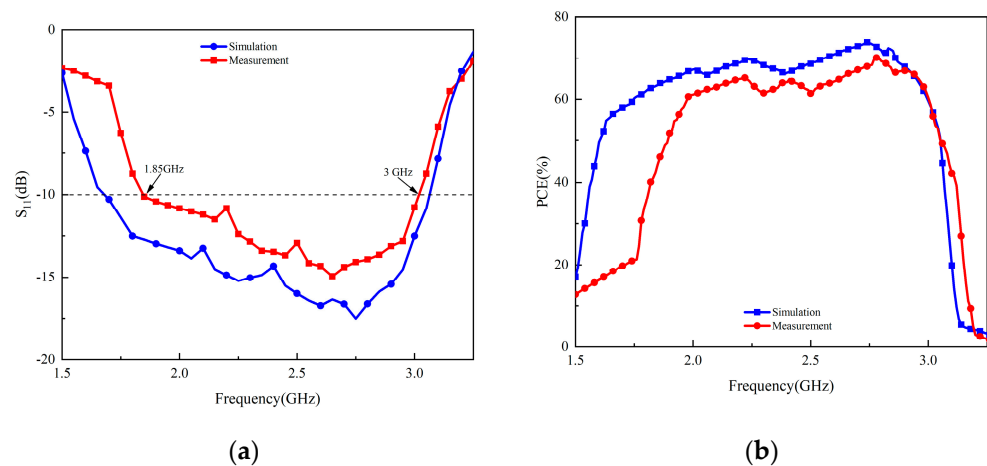


Figure 4. (a) Simulated and measured S_{11} at the input power of 0 dBm; (b) Simulated and measured PCE versus frequency at the input power of 0 dBm.

The PCE versus frequency for different input power levels is shown in Figure 5a. When the input power is -10 dBm, the PCE remains above 40% in the range of 1.9–3 GHz. When the input power is 0 dBm, the PCE remains above 60% in the range of 1.98–3 GHz. The PCE keeps above 70% in the range of 1.97–2.95 GHz at 4 dBm. The broadband rectifier performance is further analyzed. Effect of input power variation on PCE and output voltage when 2.45 GHz is selected in the wide band. The simulation and measurement results are shown in Figure 5b. Input power range from -8.5 dBm to 7 dBm at 2.45 GHz when PCE

over 50%. The measured conversion efficiency is 45.1% at -10 dBm. Output voltage is 240 mV. At 0 dBm, the conversion efficiency is 62.9% and the output voltage is 932 mV. The peak PCE of 79.6% is obtained at 4 dBm with an output voltage of 1.43 V.

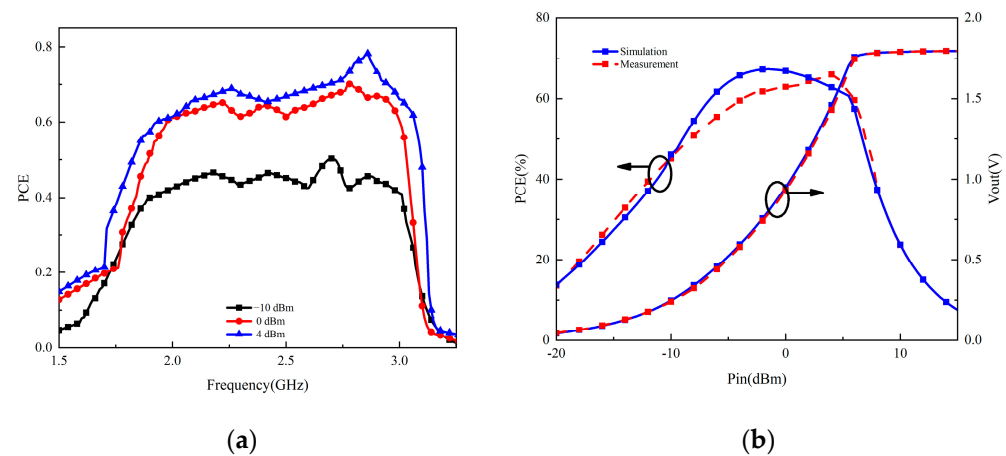


Figure 5. (a) Measured PCE versus frequency with different input power from -10 to 4 dBm; (b) Simulated and measured PCE and Vout versus input power at 2.4 GHz.

Table 2 shows the performance comparison with existing works. The 1.6–3 GHz covers most of the applications, so wideband rectifiers in this range are chosen for comparison. Compared to the existing works, the proposed rectifier has a wide band in the low input power range and maintains the compact size of $19 \text{ mm} \times 21 \text{ mm}$.

Table 2. Performance comparison with the state-of-the-art broadband rectifiers.

Ref.	Size (mm ²)	Substrate	Diode	Frequency (GHz) (PCE > 40% 0 dBm)	Bandwidth	$\eta_{\text{PCE}_{-10\text{dBm}}}$	$\eta_{\text{PCE}_{0\text{dBm}}}$	$\eta_{\text{PCE}_{\text{peak}}}$
[23]	37×10	F4B	HSMS 2860	1.7–2.8	49%	N/A	49% (1.99 GHz)	78.63% (1.99 GHz)
[27]	46×32	TLY-5	HSMS 2860	1.7–2.8	48.9%	N/A	61% (1.85 GHz)	82.5% (1.9 GHz)
[28]	36×35	Rogers 4350	HSMS 2860	1.9–3.1	48%	12% (2.5 GHz)	50% (2.5 GHz)	75.8% (2.5 GHz)
[29]	22.5×22.8	TLY-5	BAT 15-03W	1.8–2.9	47%	28% (2.1 GHz)	64% (2.1 GHz)	82.3% (2.1 GHz)
Ours	19×21	Rogers 4003	HSMS 2860	1.82–3.1	52%	44% (2.9 GHz)	67% (2.9 GHz)	79.6% (2.9 GHz)

4. Conclusions

In this paper, we propose a novel impedance matching network based on CTLs. Impedance matching is achieved by utilizing the design freedom of a single CTL in combination with TLINs. And by realizing G_v greater than 1, it extends the dynamic voltage of the input signal and ensures the conversion efficiency at low power. The design of a broadband rectifier at low input power is realized by this method. For verification, a broadband rectifier is fabricated and measured. The measured results show that at -10 dBm, the PCE keeps more than 40% at 1.9–3 GHz with a bandwidth of 44.9%. When the input power is 0 dBm, PCE above 60% and the bandwidth is 41% at 1.98–3 GHz. The structure is more compact than existing rectifiers and maintains a high PCE over a wide-band.

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