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Design and Experimental Validation of a High-Efficiency Sequential Load Modulated Balanced Amplifier

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Abstract: The purpose of this paper is to present a detailed design procedure for a highly efficient sequential load-modulated balanced amplifier (SLMBA) to provide an in-depth analysis of this complex power amplifier (PA) architecture. SLMBA's basic theory is presented and discussed. An SLMBA with a frequency range from 2.45 GHz to 2.65 GHz was implemented and then measured in order to validate the proposed design methodology. In both saturation and back-off states, the fabricated SLMBA exhibits extremely high efficiency and output power. It delivers a maximum output power of 43~44.4 dBm and a drain efficiency (DE) of 71.6~75% at saturation, a DE of 63.5~66% at 6 dB output back-off (OBO) state, a DE of 61.8~66% at 10 dB OBO state, and a DE of more than 51% at 12 dB OBO state in the targeted frequency band. The achieved results demonstrate the effectiveness of the proposed design procedure.

Keywords: GaN technology; high efficiency; high output power; high OPBO; microwave measurements; power amplifier



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1. Introduction

Spectrum resources are becoming increasingly scarce as a result of the rapid development of modern wireless communication systems. For the purpose of maximizing frequency band utilization, modern communication systems employ complex modulation schemes, which have extremely high peak-to-average power ratios (PAPRs), requiring the power amplifier (PA) module to maintain high efficiency during output-power backoff (OBO) [1,2].

A primary method for improving PA OBO efficiency is the supply modulation (SM) technique [3–6], the load modulation (LM) technique [7–27], and their combination [12]. SM methods, such as envelope tracking (ET) PAs [3–5], suffer from complex system implementation, limited dynamic range, and modulation bandwidth. In recent decades, the LM method has become the primary research focus for improving the efficiency of OBOs. As the most widely used LM architecture, Doherty PAs (DPAs) are narrowband in nature, and their OBO range is limited to 6 dB. Various combinations of load impedance and asymmetrical drain bias voltages have been demonstrated to extend the OBO range of DPA [13–18]. Despite this, the OBO range of DPA is still less than 9 dB, which does not meet the demanding requirements of modern wireless communication systems.

A novel load-modulation architecture, the load-modulated balanced amplifier (LMBA), has recently been reported (see Figure 1) [19–24]. LMBA is theoretically capable of achieving a wider back-off range and a higher efficiency level over a wider frequency range. In a traditional LMBA, there is a control amplifier (CA) and a balanced amplifier (BA) pair, which is connected using quadrature couplers. As a follow-up to the conventional LMBA, a number of different architectures have been proposed, whose OBO range can reach 10 dB, including sequential LMBA (SLMBA) [25], pseudo-Doherty LMBA (PD-LMBA) [26,28],

etc. It should be noted, however, that traditional LMBA and their variants are generally more complex than DPA circuits. In order to provide a more comprehensive design for the complex PA, this work presents a detailed design procedure for a highly efficient SLMBA. The proposed design strategy is successfully validated by experimental characterization of the developed SLMBA prototype, which is based on using gallium nitride (GaN) high-electron-mobility transistor (HEMT) technology that is well-suited for high-power microwave applications [29–34].

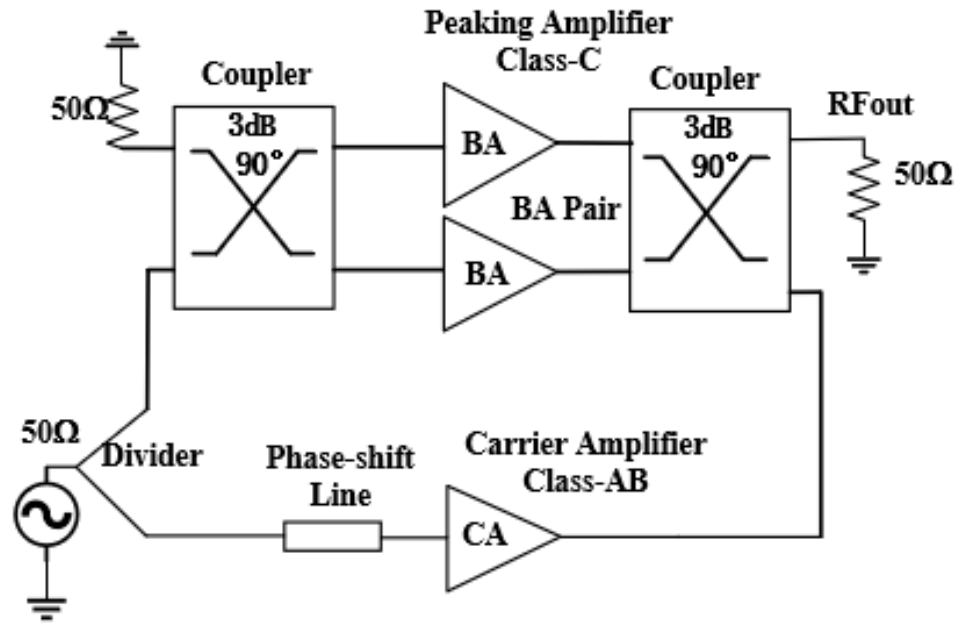


Figure 1. The topology of the SLMBA.

The remainder of the paper is organized as follows: Section 2 provides an introduction to the basic theory of SLMBA. In Section 3, the details of the design procedure and implementation of SLMBA are presented. The experimental results of the developed SLMBA prototype are presented and discussed in Section 4. In Section 5, the conclusions of this study are summarized.

2. Basic Theory of SLMBA

As illustrated in Figure 1, SLMBA consists of a CA and two BAs [26], which are connected by two 3 dB couplers and a power divider. The BA pair consists of two amplifiers operating in deep Class C mode, and the CA operates in Class AB mode. In accordance with [26], the load impedance of CA and BA can be calculated as reported in Equations (1) and (2).

$$Z_{B1} = Z_{B2} = Z_0 \cdot \left(1 + \sqrt{2} \frac{I_c e^{j\theta}}{I_b} \right) \quad (1)$$

$$Z_c = Z_0 \quad (2)$$

where I_b is the amplitude of the BA current, I_c is the amplitude of the CA current, θ is the phase of the control path, Z_{B1} and Z_{B2} are the impedances seen from the BA transistor to the output coupler.

According to Equations (1) and (2), the load impedance of CA is always equal to a fixed value, whereas the load modulation impedance of BA is determined by the current phase and amplitude. It is possible for BA to achieve optimal load impedance with proper control of the phase and amplitude. To further analyze the impedance matching between CA and BA and the performance of SLMBA, the load modulation impedance and performance at different output power levels were examined.

As a result of the different states of CA and BA, SLMBA can appear in three different working states to ensure high efficiency [21]. When the output power falls below the predefined targeted OBO power level, the BA pair does not open. Instead, only the CA operates, thereby determining the output power and efficiency of the entire SLMBA, as shown in Figure 2a. When the output power reaches the saturated output power, the CA enters the saturation state, and the BA becomes active. It is during this period that the output current of the CA reaches its maximum, whereas the output current of the BA increases. Due to the change in the ratio between CA and BA currents, the BA load impedance changes. Therefore, the SLMBA operates at high efficiency in the back-off region, as illustrated in Figure 2b. The saturation of the SLMBA output power occurs simultaneously with the saturation of the CA and BA output powers. This is the case in which the SLMBA reaches its maximum output power. Therefore, the SLMBA is capable of achieving high efficiency over a wide back-off range.

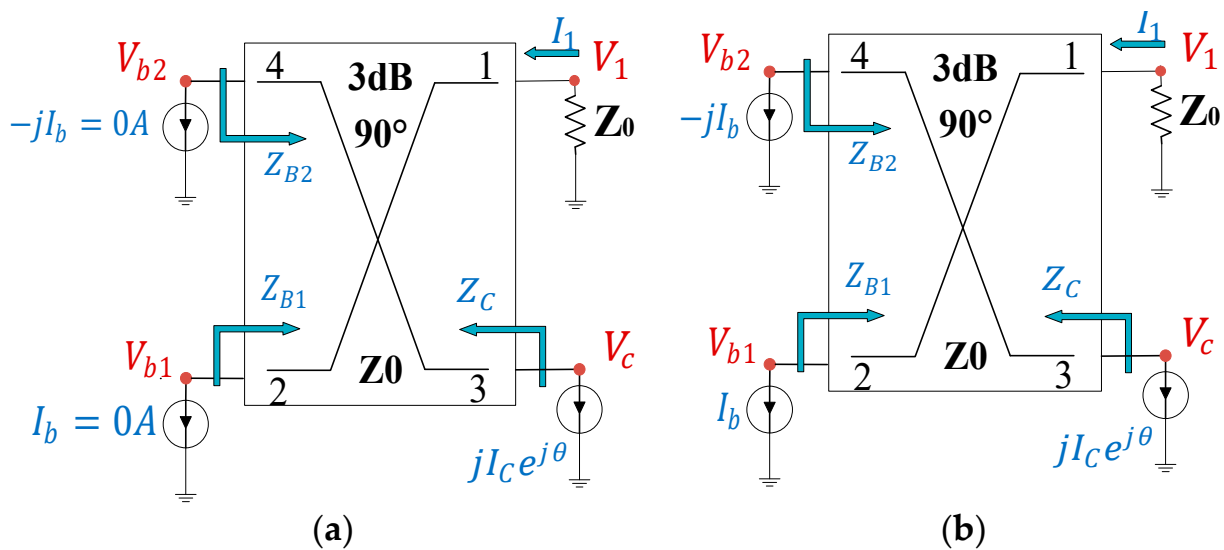


Figure 2. Equivalent schematic of the output combining network of the SLMBA at (a) low output power and (b) high output power.

3. Design of SLMBA

3.1. Design Proposal Analysis

The objective of this work is to design an RF-input SLMBA with a bandwidth ranging from 2.45 GHz to 2.65 GHz with high efficiency using Wolfspeed GaN HEMT devices. In order to achieve a 10 dB OBO range, the CA's saturated output power should be 33 dBm, and the BA's saturated output power should be over 40 dBm. With a gate bias voltage of -2.3 V and a drain bias voltage of 12 V, the CA is configured as a Class AB PA. In contrast, the BA is configured as a Class C PA, with a gate bias voltage of -6.5 V and a drain bias voltage of 28 V. In this design, the Rogers 4350 substrate with a thickness of 0.762 mm is utilized.

As an illustration in Figure 3, the design steps of the SLMBA are as follows: (A) design the CA; (B) design the power divider and 3 dB coupler; (C) design the BAs; (D) connect the components and tune the phase shift line [19–24]. On the other hand, the design steps of a single-ended PA, such as the CA and BA, involve the following steps: (1) finding the quiescent operation point; (2) ensuring PA stability; and (3) matching input and output impedance. Once all the components have been designed, the entire SLMBA is assembled and optimized to meet the target requirements.

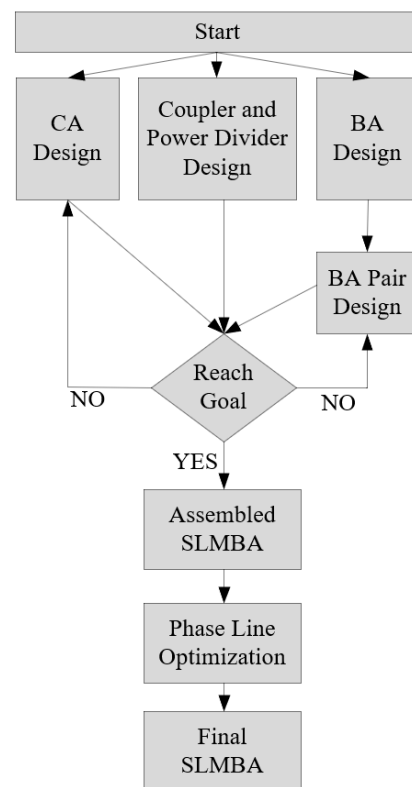


Figure 3. The design steps of the LMBA.

3.2. Design of the CA

According to the theoretical analysis of the SLMBA proposed above, the CA operates in Class AB mode, and a 6 W GaN transistor (CGH40006P) from Wolfspeed is employed in the design of the CA. With an input of 25 dBm, the expected CA power will be 33 dBm, and the DE should be greater than 60%. With the power divider, the CA's input power is around 22 dBm when designed separately.

The quiescent operation of this design is fixed at -2.3 V for the gate source and 12 V for the drain source, resulting in 260 mA for the drain source when in quiescent operation. To ensure that the CA remains stable over the entire target frequency range, a stability network has been included in the design. A $30\ \Omega$ resistor and a 3.6 pF capacitor are used to construct the RC parallel stability network for CA. Figure 4 shows the circuit block diagram with the stability network. Figure 5 illustrates the comparison of the stability coefficient before and after the addition of the stability network. It can be seen from the results that CA stability can be significantly improved. Over the entire frequency range, the stability factor exceeds 1.

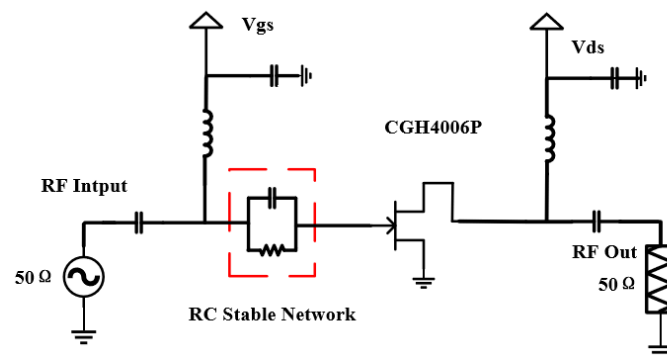


Figure 4. The circuit block diagram of adding the stability network.

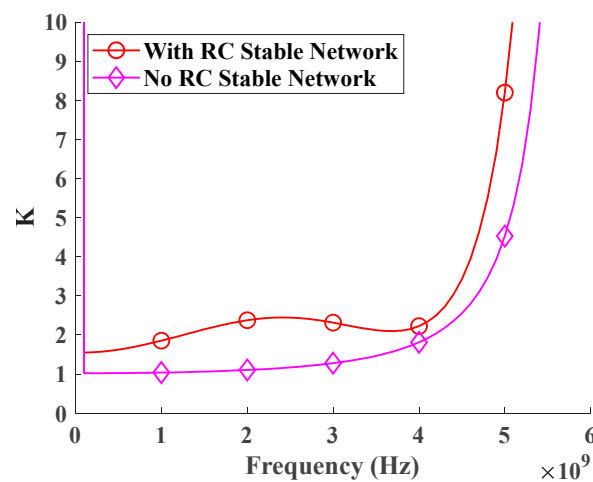


Figure 5. Stability coefficient with and without stable networks.

Once the operation condition has been fixed and the stability network has been tested, the matching network can be designed. To determine the ideal source and load impedances of the transistor for CA circuits, source pull and load pull simulations are conducted.

Figure 6 illustrates the output power and power-added efficiency (PAE) contours for source and load pull simulations using 22 dBm input power. The solid line represents the impedance region where the PAE is over 60%, while the dashed line represents the impedance region where the CA output power is 33 dBm. The area of overlapping impedances is the location of the optimal matching impedance. An illustration of the optimal impedance with maximum PAE at a fixed output power of 33 dBm is provided in Table 1.

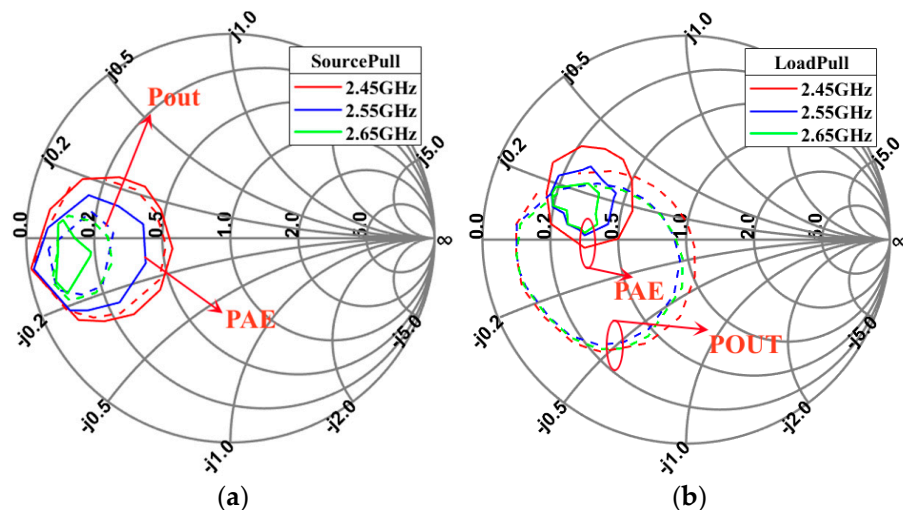


Figure 6. The (a) source and the (b) load pull results with the 22 dBm input.

Table 1. The optimal CA impedance in the target frequency band.

Freq. (GHz)	Load	Source
2.45	$17.2 + j13 \Omega$	$5 + j4 \Omega$
2.55	$15.6 + j10.2 \Omega$	7.3Ω
2.65	$13.1 + j8 \Omega$	$11 - j3 \Omega$

As input and output matching, the second-order Chebyshev low-pass topology is used, along with a center frequency matching method. The optimal impedances

$Z_L = 15.6 + j10.2 \, \Omega$ and $Z_S = 7.3 \, \Omega$ are selected for initial matching. Figure 7a,b illustrate the matching procedure for both load and source impedances. Figure 8 shows CA after matching, and Figure 9 shows the PAE and output power of the circuit with the ideal transmission line. Based on the results, the CA PAE is over 60%, and the output power lies between 32.8 and 34.3 dBm across the target frequency band.

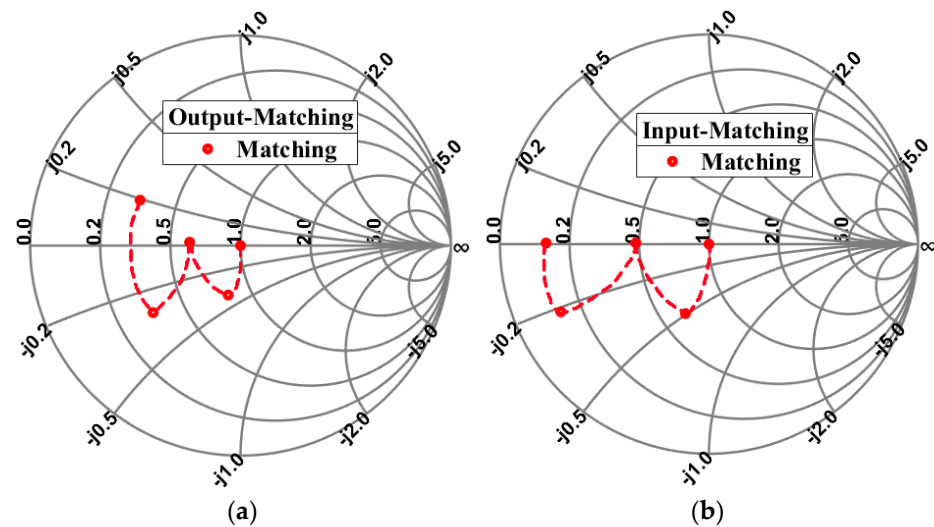


Figure 7. The matching procedure for (a) load and (b) source.

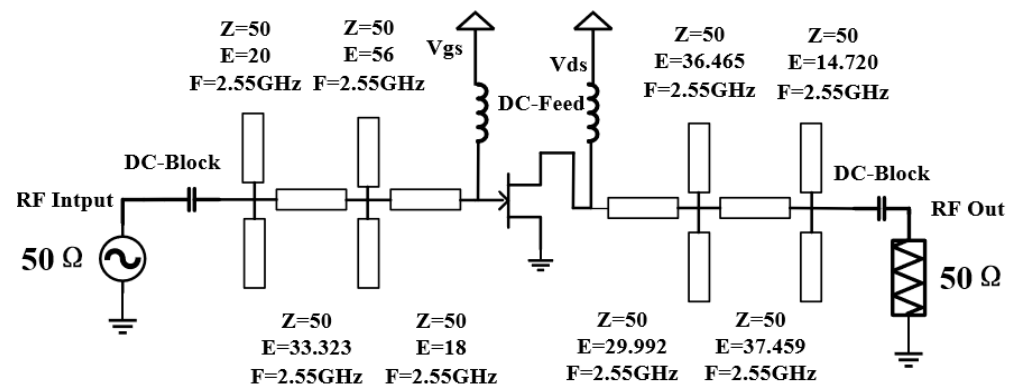


Figure 8. CA circuit with ideal transmission line.

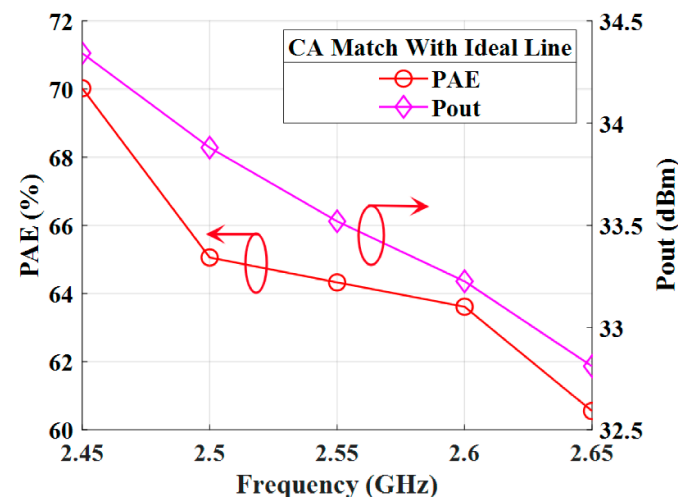


Figure 9. PAE and output power of CA with ideal transmission line.

As shown in Figure 10, a complete CA is shown after replacing the ideal transmission line with a microstrip line and adding the RC stability network and the bonding pad. Figure 11 illustrates the corresponding output power and PAE. Observing the results, the PAE is approximately 60%, and the output power is between 33.1 dBm and 33.6 dBm, which is in line with the requirements.

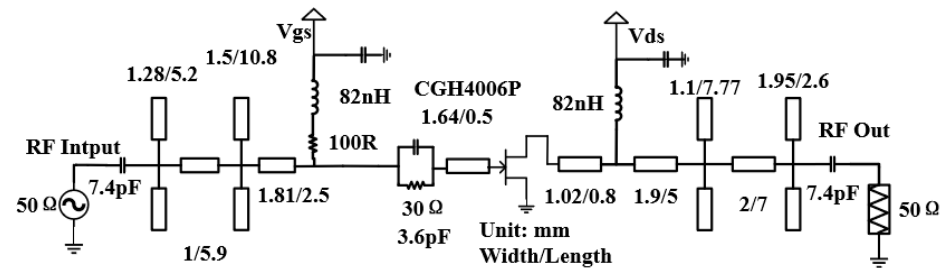


Figure 10. Complete CA circuit with microstrip lines.

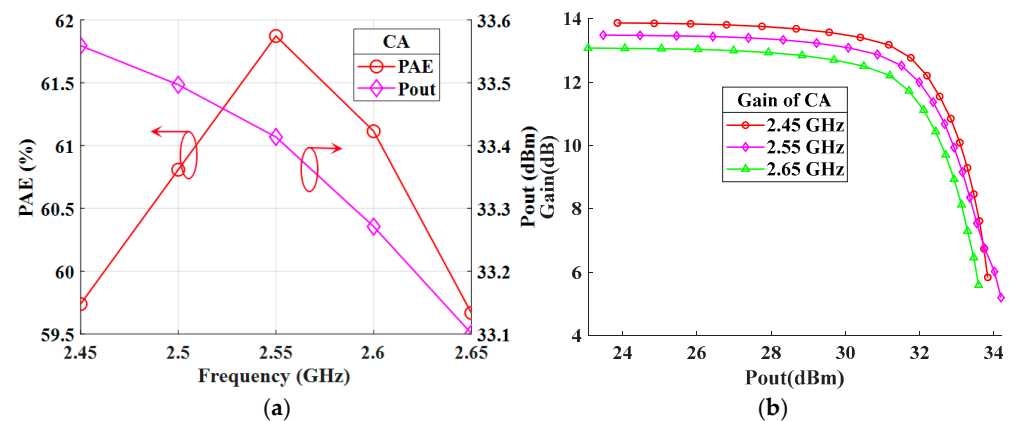


Figure 11. Simulation result of (a) PAE, output power, and (b) gain of CA with microstrip line.

3.3. Design of a 3 dB Couple and Power Divider

Couplers are designed to connect the input and output ports of a BA pair. A block diagram and S-parameter for the designed coupler are shown in Figure 12a,b. The coupler provides an almost constant phase difference between ports 3 and 4, and the power between ports 3 and 4 is equally divided. Figure 13a,b illustrate the S-parameter and block diagram of the power divider. As can be seen, the 3 dB quadrature coupler has been successfully implemented in the target frequency range.

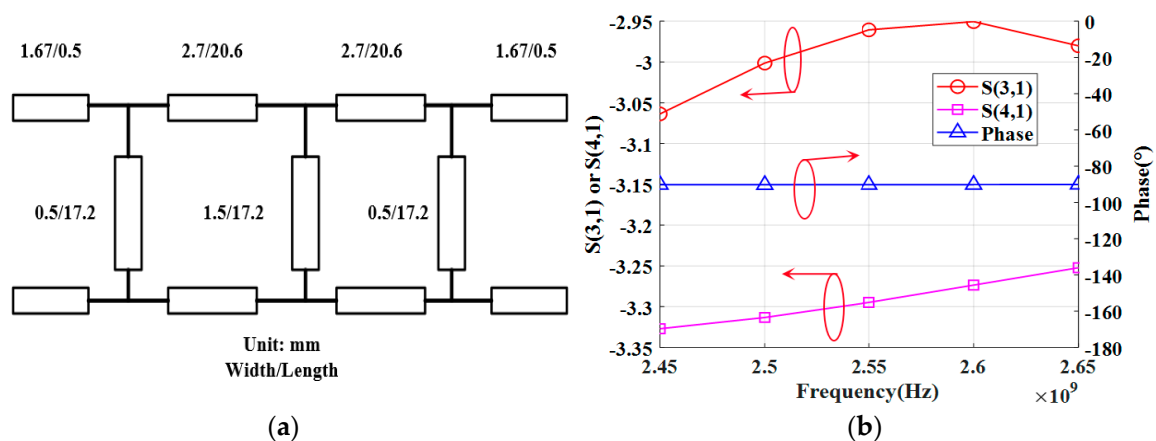


Figure 12. (a) The block diagram and (b) S-parameter of the designed coupler.

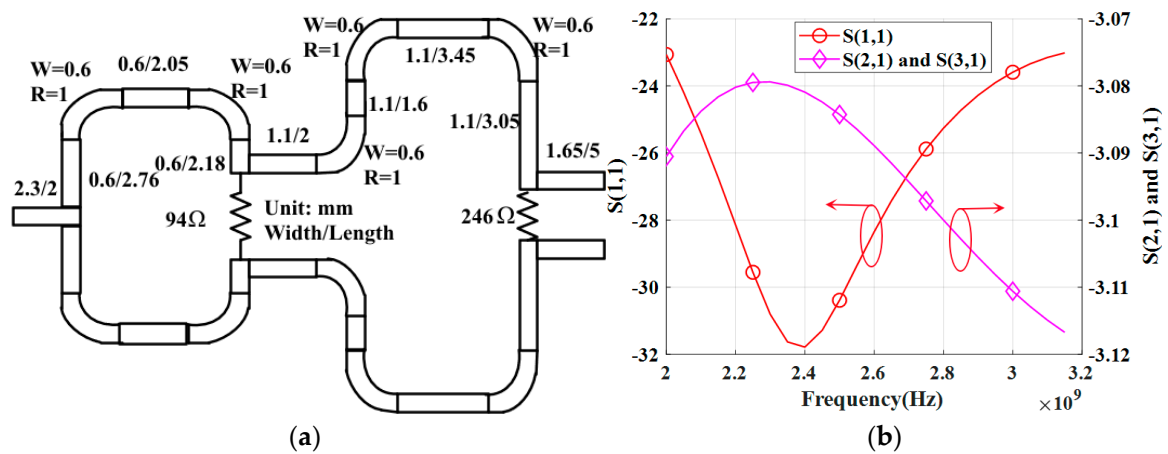


Figure 13. (a) The block diagram and (b) S-parameter of the designed power divider.

3.4. Design of the BAs

A BA pair consists of two identical amplifiers. In order to achieve a peak power of 43 dBm, the 10 W GaN HEMT (CGH400010F) transistor is utilized, and each BA unit must provide an output power of approximately 40 dBm at saturation. It operates in the Class C mode. Therefore, the V_{gs} is biased at -6.5 V and the V_{ds} is biased at 28 V.

BA follows a similar design procedure to CA. In each amplifier, the PAE should be greater than 70%, and the output power should be greater than 40 dBm. The final schematic diagram, simulation output power, and PAE of the designed BA can be seen in Figures 14 and 15. Based on the results, the BA delivers an output power of more than 40 dBm and a PAE of more than 70%, which meets the requirement.

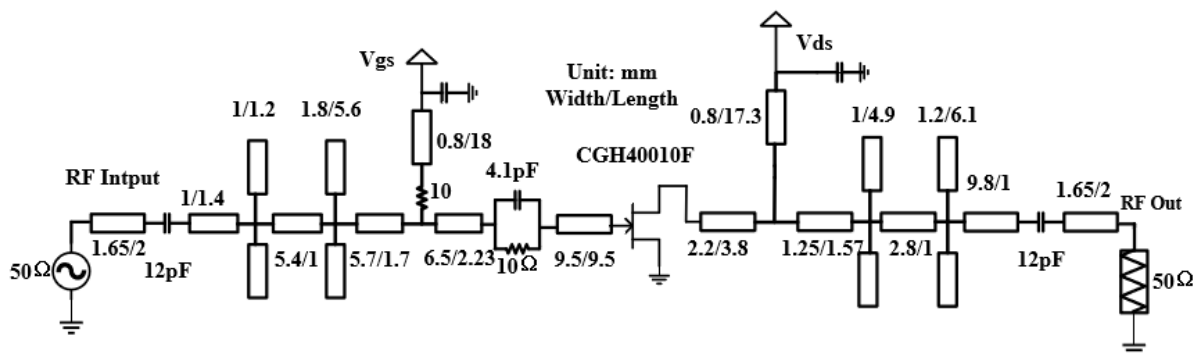


Figure 14. Schematic diagram of the designed BA.

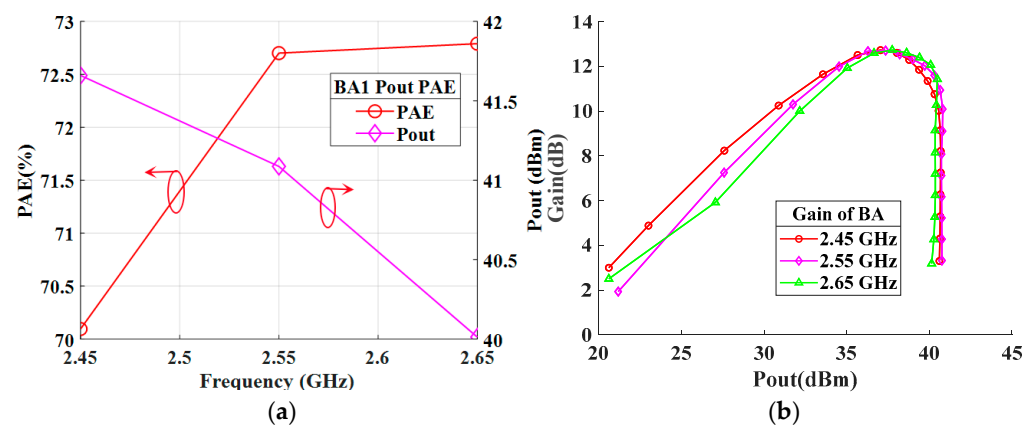


Figure 15. BA (a) output power, PAE, and (b) gain.

By connecting the BAs and the coupler, the block of BA pairs is completed, and the simulation results are shown in Figure 16a. According to the results, performance has decreased, and re-optimization is necessary. Figure 16b illustrates the optimized results, while Figure 17 shows the detailed circuit.

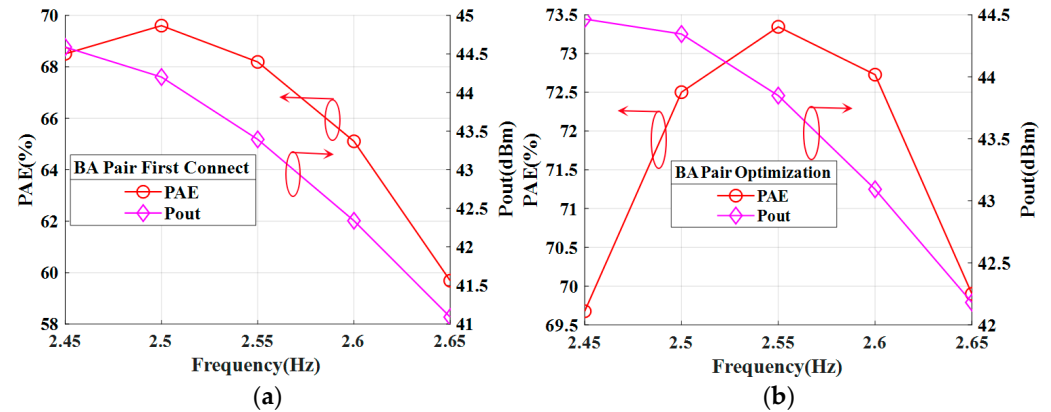


Figure 16. The PAE and output power of the BA: (a) before and (b) after optimization.

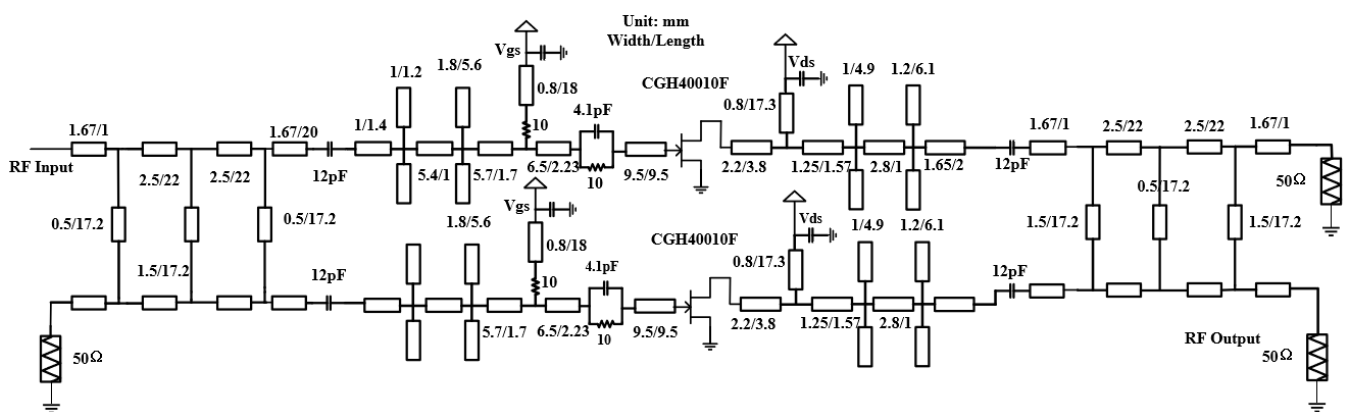


Figure 17. The circuit of BA after the optimization.

3.5. SLMBA Design

As soon as all the different parts have been integrated, the entire SLMBA can be obtained. Figure 18 illustrates the effect of phase shift angles on the performance of SLMBA at 2.55 GHz. It can be seen that the optimal angle for the phase shift line is 135°. Table 2 shows the optimal phase shift angle for different frequencies.

Table 2. The optimal phase shift angle at different operation frequencies.

Frequency	2.45 GHz	2.55 GHz	2.65 GHz
Phase	125°	135°	175°

According to the table, the optimal phase shift line varies with the frequency of operation. Therefore, it is necessary to make a compromise in order to modify SLMBA performance throughout the entire frequency band. In this study, a phase shift line with a 150° angle is used. Figure 19a shows the detailed topology, while Figure 19b shows the performance of the SLMBA.

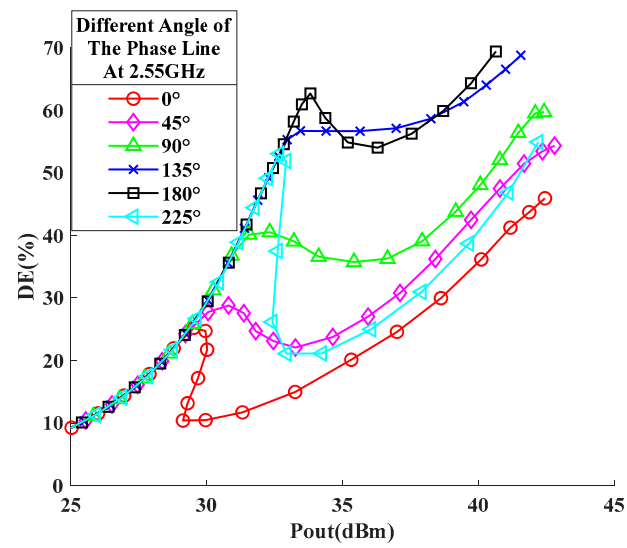


Figure 18. Influence of different phase shift angles on the performance of SLMBA at 2.55 GHz.

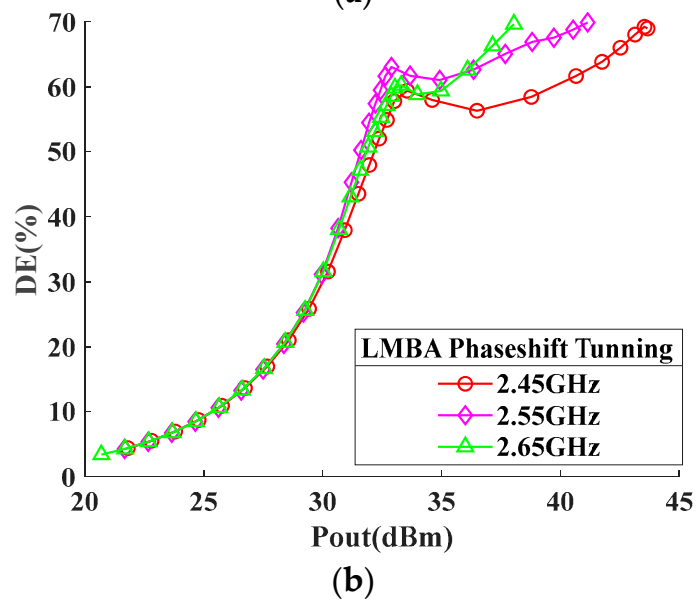
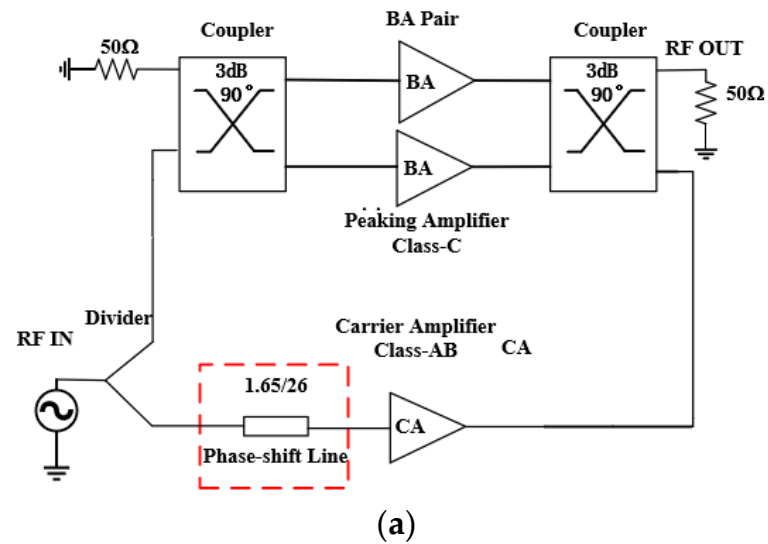


Figure 19. (a) The block of adding the phase shift line and (b) the performance of DE.

According to Figure 19, the DE of the designed SLMBA has been improved at 6 dB OBO; however, the maximum output power has been reduced. Therefore, further optimization is required to improve the performance of the output power. Figure 20 illustrates the final optimized circuit diagram, and Figure 21 illustrates the performance of the SLMBA. The results demonstrate that the SLMBA provides an output power of 42.6 to 43.4 dBm and a DE of 73.2% to 77% at saturation.

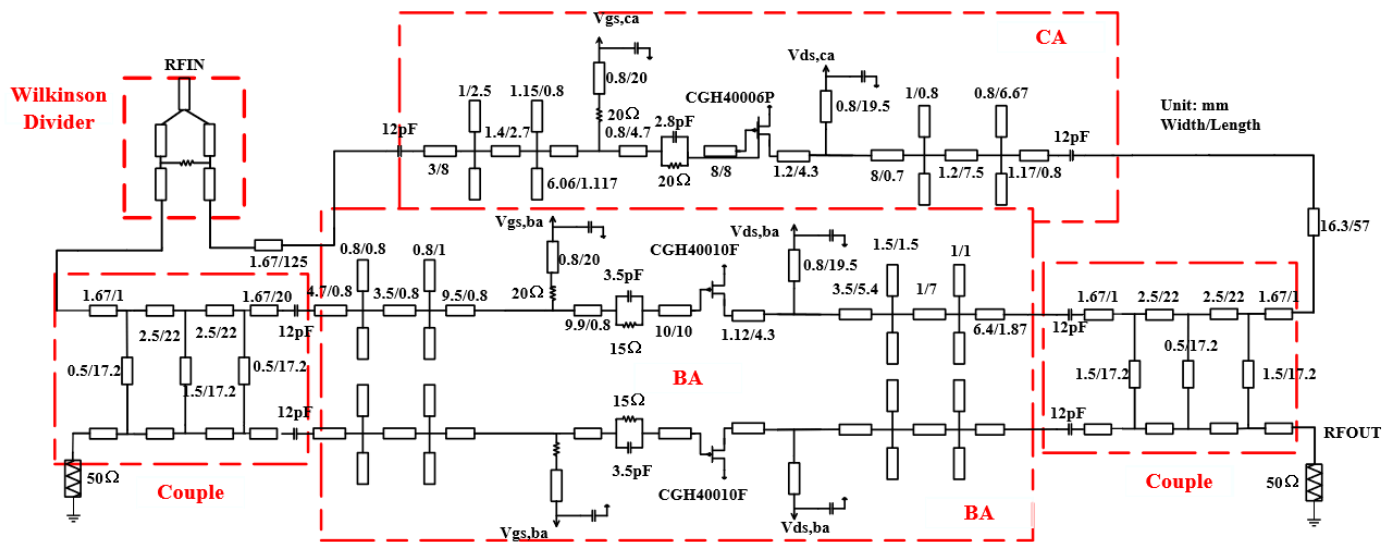


Figure 20. The final circuit diagram.

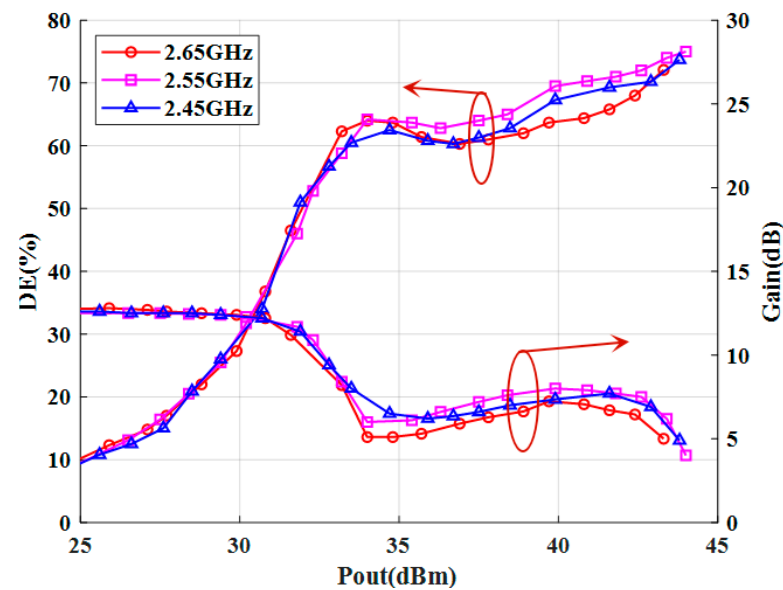


Figure 21. The performance of the SLMBA.

4. Measurement Results

The SLMBA is implemented and tested in order to experimentally validate the proposed design procedure. The fabricated SLMBA is shown in Figure 22, and the measurement results are provided in Figure 23. During the measurements, a vector signal generator was used to generate signals, and a spectrum analyzer was used to measure the output power. SLMBA's entire saturation output power ranges from 43 dBm to 44.4 dBm, and its entire saturation DE ranges from 71.6% to 75% between 2.45 GHz and 2.65 GHz. It delivers a DE range of 63.5% to 66% at 6 dB OBO state, 61.8% to 66% at 10 dB OBO state, and 51% to 52% at 12 dB OBO state.

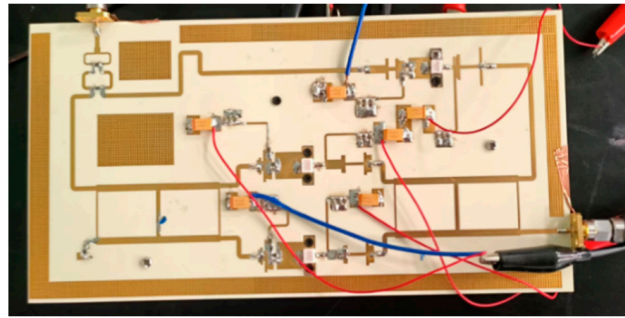


Figure 22. Photograph of the fabricated LMBA.

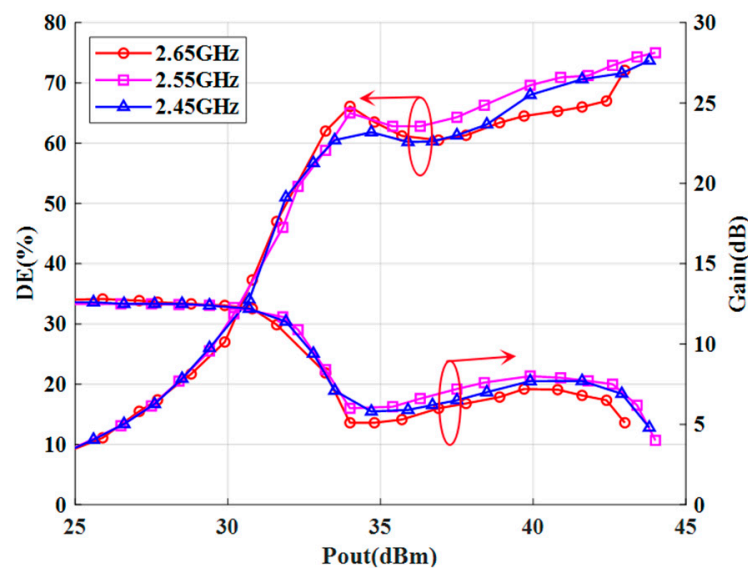


Figure 23. Measured performance of the fabricated LMBA from 2.45 GHz to 2.65 GHz.

A comparison of this work with recent LMBA designs is presented in Table 3. It can be seen from the reported results that this design achieves excellent DE performance, having the highest saturation efficiency, 6 dB OBO efficiency, and 12 dB OBO efficiency while maintaining a high output power at the same time, which shows the effectiveness of the proposed SLMBA design procedure.

Table 3. State of the art of SLMBAS.

Ref./Year	Architecture	Freq. (GHz)	$P_{total,sat}$	DE@ $P_{total,sat}$	DE@HBO(%)	DE@LBO(%)
[35] 2017	RF-Input LMBA	0.7–0.85	42	57–70	39–53 @ 6 dB	35–40 @ 10 dB
[36] 2019	SLMBA	2.4	43	69	NAN	>50 @ 12 dB
[37] 2021	H-LMBA	3.45–3.65	43	50–63	42.3–47 @ 6 dB	42.3–47 @ 9 dB
[21] 2021	TS-LMBA	3.3–3.6	44.5–45	66.9–70.1	51.2–62.1 @ 6 dB	42.2–47.3 @ 10 dB
[38] 2023	RF-Input LMBA	2.0	44.5	67	54 @ 9 dB	52 @ 15 dB
This work	SLMBA	2.45–2.65	43~44.4	71.6~75%	63.5~66% @ 6 dB	51~52% @ 12 dB

5. Conclusions

In this work, a detailed design procedure for an SLMBA was proposed. Based on the optimal matching impedances obtained by the source and load pull methods, the CA and BA were designed and optimized separately. Furthermore, complex phase modulation was

examined and improved for the entire circuit. It can be seen from the reported results that this design achieves excellent DE performance, having the highest saturation efficiency, 6 dB OBO efficiency, and 12 dB OBO efficiency while maintaining a high output power and a higher OPBO at the same time, which shows the effectiveness of the proposed SLMBA design procedure.

Author Contributions: Conceptualization, J.C.; methodology, D.J. and J.C.; software, D.J.; validation, D.J., J.C. and G.C.; formal analysis, J.C.; investigation, D.J.; resources, J.C.; data curation, M.L.; writing—original draft preparation, D.J. and J.C.; writing—review and editing, G.C., M.L. and J.C.; visualization, M.L.; supervision, M.L., G.C. and J.C.; project administration, J.C.; funding acquisition, J.C. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflicts of interest.

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