

Article

Analysis of Power Electronic Traction Transformer under Non-Single Frequency PWM Control

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Abstract: In the context of locomotive traction systems, the power electronic traction transformer (PETT) represents a pivotal component, fulfilling essential functions pertaining to electrical isolation and power control. The majority of existing PETT prototypes employ a combination of a cascade structure and an ISOP structure. The aforementioned scheme effectively reduces the voltage withstand level of the power devices on the input side, yet it also necessitates the utilisation of a greater number of power devices and passive components within the PETT. In order to further reduce the number of power devices used, this paper proposes a new cascaded PETT design. The proposed PETT will adopt a scheme combining a cascade structure and a hardware circuit multiplexing. This paper first analyses the operation principle of the new circuit under non-single frequency PWM control. It then derives the design equations for some hardware parameters and control circuits. Finally, it verifies the effectiveness of the proposed PETT through simulation analysis.

Keywords: power electronic traction transformer; cascaded; hardware circuit multiplexing; non-single frequency PWM control; simulation analysis



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1. Introduction

The power electronic traction transformer (PETT) is regarded as a potential alternative to conventional transformers in locomotive traction systems, offering a number of advantages [1]. These include a reduction in weight and size, enhanced efficiency, and a lower injection of current harmonics into the grid. In 2012, the world's inaugural PETT for locomotives was developed and deployed by ABB in conjunction with Swiss Federal Railways [2,3]. This was followed by a series of comprehensive investigations into the potential of PETT, involving numerous research organisations worldwide, such as ABB [4–6], Alstom [7], Bombardier [8], Siemens [9], etc. These studies led to the development of PETT prototypes and proof-of-concept machines in various forms.

The cascaded PETT has become a typical circuit structure for PETT design [10–16], and a detailed illustration of the specific circuit topology can be found in Figure 1. The PETT illustrated in Figure 1 can be regarded as a combination of a cascaded multilevel AC/DC converter and an isolated DC/DC converter. The input side of the AC/DC converter is connected to the AC traction grid, whereby the AC input is converted into a medium-voltage DC voltage. The DC/DC converter achieves electrical isolation while increasing the frequency of the transformer's transmission voltage, which will result in a significant reduction in the size and weight of the on-board transformer. Furthermore, the incorporation of controllable power devices enhances the intelligence of the locomotive.

As the AC/DC converter is directly linked to the traction network (15 kV/16.7 Hz), the objective is to limit the number of switching devices and reduce the voltage withstand level of these components. In order to achieve this, it is necessary to utilise a CHB structure with 6.5 kV IGBT modules. In order to further reduce the losses in the circuit, the DC/DC converter can be designed as a resonant converter [17–21]. The resonant cavity, which

encompasses L-type, LC-type, and LLC-type configurations, guarantees the zero-current and zero-voltage conduction of the power devices within the DC/DC converter.

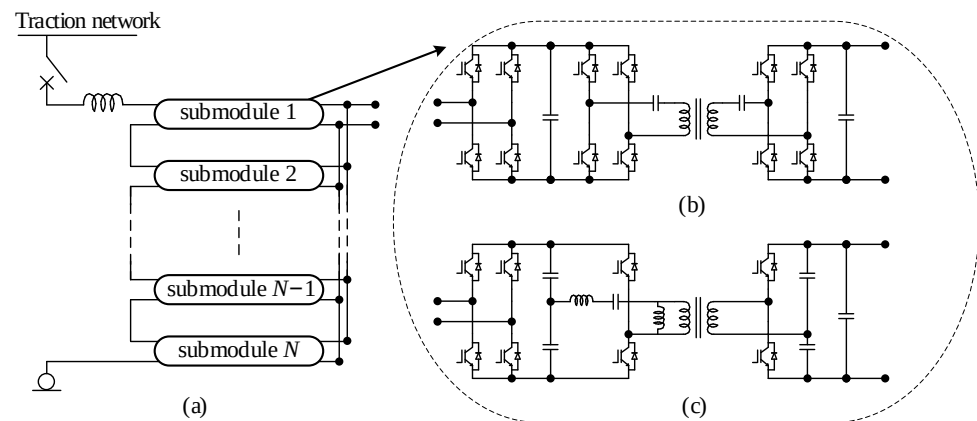


Figure 1. Typical circuit structure of PETT. (a) PETT circuit. (b) Bombardier. (c) ABB.

In order to further reduce the number of power devices employed, a novel PETT is designed in this paper, and the specific circuit structure is shown in Figure 2. In the proposed PETT, the number of power units is N_s . The PETT has the following characteristics:

- (i) Each power unit is an AC/DC converter and contains a medium-frequency transformer (MFT). The principal aspect of the MFT is constituted by a series of cascaded H-bridge modules, which function as alternating current AC/DC converters. The number of H-bridge modules in this configuration is designated as N . On the secondary side of the MFT, one H-bridge module is employed as an AC/DC converter.
- (ii) The two power units collectively constitute a unit group, and there is a distinction between the control signals of these two power units, which will be elucidated subsequently.
- (iii) With regard to feature 2, it is necessary for the number of power units in the PETT to be even.

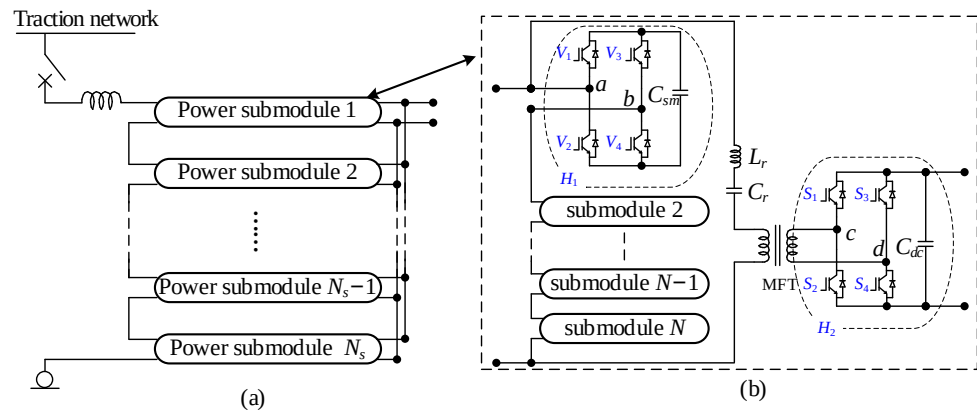


Figure 2. The proposed PETT circuit. (a) The PETT circuit. (b) The internal circuit of a power unit.

The proposed circuit employs a reduced number of switching devices and capacitors in comparison to the conventional circuit illustrated in Figure 1, while maintaining the same input size. This allows for the low-cost design of PETTs. Consequently, novel circuitry offers substantial benefits in terms of reducing the size of PETTs and increasing their power density. The proposed circuit employs a reduced number of switching devices in comparison to the same type of circuit, presented in [22], for the same size of input. In comparison to same type of circuit, outlined in [23], the proposed circuit employs multiple low-voltage-level and low-capacity MFTs in lieu of a single high-voltage and high-capacity MFT. This results in a reduction in the voltage level and capacity of a single MFT, which facilitates the modular and redundant design of PETTs. In comparison with

the same type of circuit, presented in [24], the proposed circuit employs a multi-frequency modulation strategy, which involves a more straightforward control methodology and is more straightforward to implement.

The prevailing design of on-board PETTs still belongs to the multistage conversion type of converter, which requires a large number of active devices and therefore reduces the power density and increases the manufacturing costs. Simplifying the conversion process of PETT is an effective way to improve the power density. In this paper, the method of multi-frequency modulation enables the bridge arm of the CHB circuit to output a fundamental-frequency AC voltage as well as a high-frequency AC voltage, which in turn reduces the number of stages of the power conversion and can effectively reduce the number of components involved and improve the power density. It is valuable in terms of reducing the cost and volume of multilevel PETTs, promoting the development of PETTs, and accelerating the construction of intelligent locomotive traction systems.

2. Analysis of the Proposed PETT

2.1. Analysis of the Working Principle

The H-bridge circuit represents the fundamental circuit structure of PETTs, and an analysis of this circuit is beneficial in terms of researching PETTs. In the case of the H-bridge circuit, under PWM control, the frequency and waveform of the AC-side voltage are in accordance with a modulating waveform [25,26]. The following section will examine the output law of the H-bridge circuit under PWM control, utilising two modulating waves with disparate frequencies and waveforms as illustrative examples. For the purposes of this discussion, the two modulating waves will be denoted as u_{r1} and u_{r2} . The following assumptions will be made:

- (i) The modulating waveform u_{r1} will be taken to be sinusoidal, with frequency f_1 .
- (ii) The modulating waveform u_{r2} will be taken to be a square wave, with frequency f_2 .

In accordance with the aforementioned assumptions, the AC-side voltage of the H-bridge circuit can be decomposed into a sinusoidal voltage component and a square-wave voltage component. For the purposes of discussion, the aforementioned voltage components are henceforth designated u_{f1} and u_{f2} , respectively. It is possible to decouple u_{f1} and u_{f2} and subsequently transmit them independently through the filter circuit due to their differing frequencies. The aforementioned concept may be employed in the redesign of the PETT circuit, illustrated in Figure 1. This entails the replacement of the two series-connected H-bridges on the primary side of the MFT with a single H-bridge, thereby yielding the novel PETT circuit depicted in Figure 2.

The following clarification is provided for the sake of clarity and exposition. In the proposed PETT, the H-bridge on the primary side of the MFT is designated as H_1 , and the H-bridge on the secondary side is designated as H_2 . H_1 is responsible for implementing the AC/DC converter, while also forming a DC/DC converter with the MFT and H_2 . Furthermore, the f_2 should be sufficiently high to provide a high-frequency square-wave voltage on the primary side of the MFT. It can be stated that the multiplexing of the H-bridge circuit is achieved through the utilisation of multi-frequency PWM control, which represents the operational principle of the proposed PETT. It is assumed that the hardware parameters of the cascade sub-modules in Figure 2b are identical and that the switching devices are numbered in accordance with the circuit depicted in Figure 2. It is evident that H_1 comprises switching devices $V_1 \sim V_4$ and capacitor C_{sm} , while H_2 is constituted by switching devices $S_1 \sim S_4$ and capacitor C_{dc} .

The different polarities of the modulating waves allow for the classification of PWM control into unipolar and bipolar types. Each of these control methods possesses distinct advantages and disadvantages, which are contingent upon the specific application. In the case of unipolar PWM control, the AC side of the H-bridge is capable of outputting positive, negative, and neutral levels. In the case of bipolar PWM control, the H-bridge AC side outputs positive and negative levels. It is important to note that the equivalent switching frequency of unipolar PWM control is twice that of bipolar PWM modulation.

Consequently, it is possible to reduce switching losses while simultaneously reducing the total harmonic distortion (THD) of the H-bridge AC-side voltage, which in turn leads to a reduction in the fluctuations in the AC-side input current. In light of the benefits associated with unipolar PWM control, this paper proposes the implementation of unipolar PWM control as the control strategy for PETTs.

Table 1 illustrates the complete set of switching combinations for $V_1 \sim V_4$ under unipolar modulation. Here, a switching signal of “0” indicates that the device is in an off state, while a switching signal of “1” denotes that the device is in an on state. At this time, H_1 exhibits the following characteristics:

- At $u_{ab} > 0$, the value of u_{ab} will switch between u_{sm} and 0, where u_{sm} is the voltage of the capacitor C_{sm} on the DC side of H_1 .
- At $u_{ab} < 0$, the value of u_{ab} will switch between $-u_{sm}$ and 0.

Table 1. Switching combinations of H_1 under unipolar PWM control.

Modal	Switching Device				u_{ab}
	V_1	V_2	V_3	V_4	
1	0	1	0	1	0
2	0	1	1	0	$-u_{sm}$
3	1	0	0	1	u_{sm}
4	1	0	1	0	0

One possible PWM strategy for realising the switching combinations demonstrated in Table 1 is given in Figure 3, and several important waveforms relevant to this strategy are given.

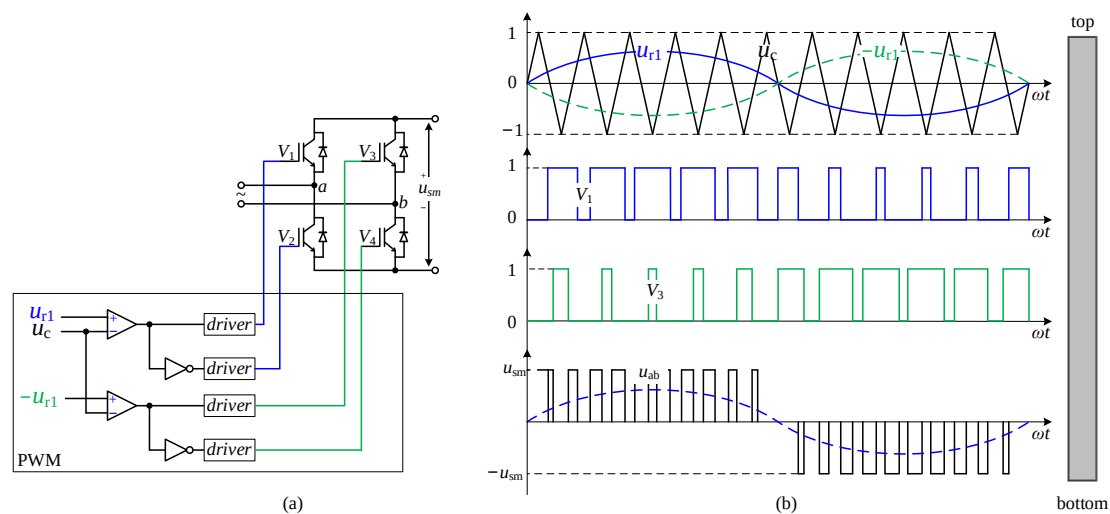


Figure 3. PWM control strategy. (a) Control method. (b) Waveforms under PWM control (from top to bottom); carrier waveform u_c ; and modulating waveform u_{r1} ; control signals of switch V_1 ; control signals of switch V_3 ; and AC-side voltage u_{ab} .

The introduction of a three-valued logic switching function, δ , with $\delta = V_1 - V_3$, allows the voltage u_{ab} and the DC-side current i_{sm} of H_1 to be expressed in terms of the switching function as

$$\begin{cases} u_{ab} = \delta u_{sm} \\ i_{sm} = \delta i_{ab} \end{cases}, \quad (1)$$

where i_{ab} is the base wave current on the AC side of H_1 .

The non-single frequency modulation strategy adopted in this paper allows for the decomposition of the voltage u_{ab} into a sinusoidal AC component u_{f1} and a square-wave AC component u_{f2} . The corresponding switching functions, designated as δ_{f1} and δ_{f2} ,

respectively, enable the expression of the voltage component of u_{ab} and the DC-side current ism as

$$\begin{cases} u_{f1} = \delta_{f1} u_{sm} \\ u_{f2} = \delta_{f2} u_{sm} \\ i_{sm} = \delta_{f1} i_g - \delta_{f2} i_r \end{cases}, \quad (2)$$

where i_g is the grid current at the network side and i_r is the resonant current of the LC resonant circuit.

Figure 4 depicts a partially enlarged representation of Figure 3b for $u_{ab} \geq 0$. It is assumed that the frequency of the triangular carrier u_c is f_s and that its peak value is U_{cm} . The rms value of u_{sm} is denoted as U_{sm} , and it is that $U_{cm} = U_{sm}$. If the modulation ratio of the modulating wave u_{r1} is m_1 , the modulating wave u_{r1} can be expressed as $u_{r1} = m_1 U_{sm} \sin \omega_1 t$.

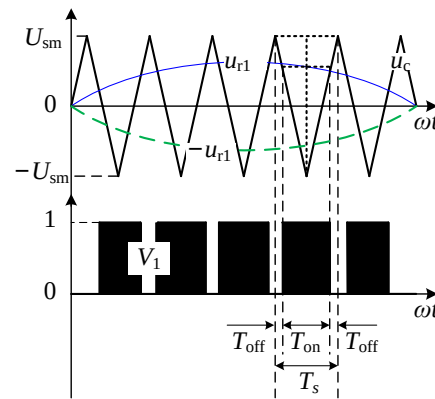


Figure 4. Partial enlargement of Figure 3.

Figure 4 illustrates the relationship between the on-time T_{on} of switch V_1 and the period T_s of the carrier wave. Based on the similarity of triangles, T_{on} satisfies the following relationship with T_s :

$$\frac{T_{on}}{T_s} = \frac{U_{cm} + m_1 U_{sm} \sin \omega_1 t}{2U_{cm}}, \quad (3)$$

The duty cycle function of the switch V_1 when employing u_{r1} modulation is represented as $d_{f1}(V_1)$. By employing Equation (3), it is possible to derive the following equation: $d_{f1}(V_1) = 0.5 + 0.5m_1 \sin \omega_1 t$. Similarly, the duty cycle function of the switch V_3 is represented as follows: $d_{f1}(V_3) = 0.5 - 0.5m_1 \sin \omega_1 t$. If the duty cycle function corresponding to the switching function $\delta f1$ is denoted as d_{f1} , it can be expressed as $d_{f1} = m_1 \sin \omega_1 t$.

If the modulation ratio of the modulating wave u_{r2} is m_2 , the modulating wave u_{r2} can be expressed as

$$u_{r2} = m_2 U_{sm} \sum_{j=1}^{\infty} \frac{4}{j\pi} \sin(j\omega_2 t), \quad (4)$$

where j is an odd number.

In the context of u_{r2} modulation, the duty cycle functions of the switch V_1 and V_3 are designated as $d_{f2}(V_1)$ and $d_{f2}(V_3)$, respectively. By means of Equations (3) and (4), the following can be obtained:

$$\begin{cases} d_{f2}(V_1) = 0.5 + 0.5m_2 \sum_{j=1}^{\infty} \frac{4}{j\pi} \sin(j\omega_2 t) \\ d_{f2}(V_3) = 0.5 - 0.5m_2 \sum_{j=1}^{\infty} \frac{4}{j\pi} \sin(j\omega_2 t) \end{cases}, \quad (5)$$

The duty cycle function corresponding to the switching function δ_{f2} is designated as d_{f2} . This can be obtained through Equation (5):

$$d_{f2} = m_2 \sum_{j=1}^{\infty} \frac{4}{j\pi} \sin(j\omega_2 t), \quad (6)$$

In this paper, open-loop control is used to control H_2 , and the on/off switching devices $S_1 \sim S_4$ are controlled by square-wave pulses with a duty cycle of 0.5. Table 2 shows all the switching combinations of $S_1 \sim S_4$, where a switching signal of “0” means the device is off and a switching signal of “1” means the device is on. The control process is as follows: when $u_{cd} > 0$, S_1 and S_4 are on; when $u_{cd} < 0$, S_2 and S_3 are on.

Table 2. Switching combinations of H_2 .

Modal	Switching Device				u_{cd}
	S_1	S_2	S_3	S_4	
5	1	0	0	1	u_{dc}
6	0	1	1	0	$-u_{dc}$

The introduction of a three-valued logic switching function, σ , with $\sigma = 2S_1 - 1$, allows the voltage u_{cd} and the DC-side current i_{dc} of H_2 to be expressed in terms of the switching function as

$$\begin{cases} u_{cd} = \sigma u_{dc} \\ i_{dc} = \sigma i_{cd} \end{cases}, \quad (7)$$

where i_{cd} is the base wave current on the AC side of H_2 .

If the ratio of the MFT is represented by the symbol N_T , then the voltage and current on the primary and secondary sides of the MFT are satisfied:

$$\begin{cases} N\delta_{f2}u_{sm} = N_T\sigma u_{dc} \\ i_{dc} = N_T\sigma i_r \end{cases}, \quad (8)$$

If the duty cycle function corresponding to the switching function σ is represented by the symbol D , this is expressed as follows:

$$D = \sum_{j=1}^{\infty} \frac{4}{j\pi} \sin(j\omega_2 t), \quad (9)$$

From Equations (6) and (9), it can be demonstrated that $d_{f2} = m_2 D$. Consequently, Equations (2) and (8) can be expressed in terms of the duty cycle function as

$$\begin{cases} u_{f1} = d_{f1}u_{sm} \\ u_{f2} = d_{f2}u_{sm} \\ i_{sm} = d_{f1}i_g - d_{f2}i_r \\ m_2 i_{dc} = N_T d_{f2} i_r \\ m_2 N u_{sm} = N_T u_{dc} \end{cases}, \quad (10)$$

2.2. Current Loop of the Proposed PETT

In this section, the current loop of the proposed PETT under unipolar PWM control is discussed. When $e_g > 0$, the modes of H_1 are mode 3 and mode 4. When the switching combination of H_1 is in mode 3, the voltage across the inductor L_s is less than 0. Depending on the direction of the current i_{ab} , H_1 possesses 2 current loops. Figure 5a,b illustrate the aforementioned two current loops. When the switching combination of H_1 is in mode 4, the voltage across the inductor L_s is greater than 0. At this time, the current loop of H_1 is shown in Figure 5c. The details can be analysed as follows:

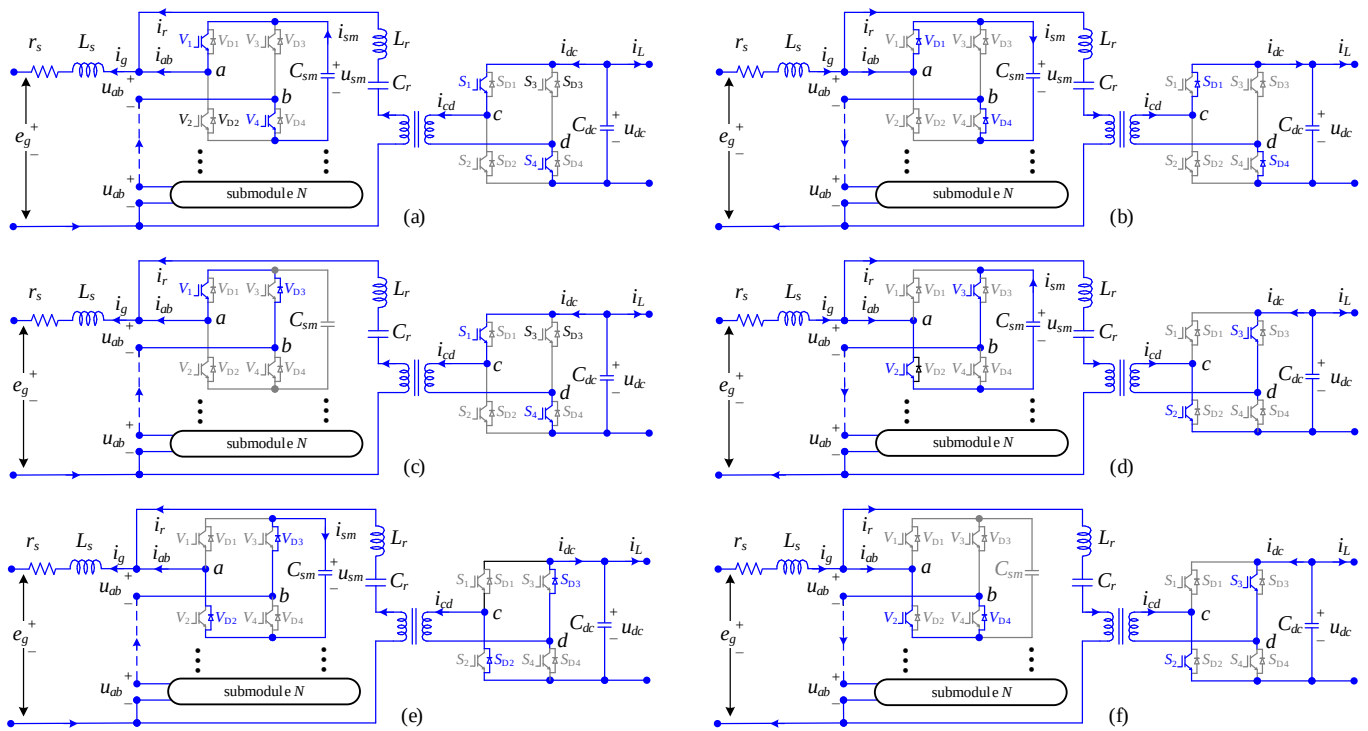


Figure 5. Current loop of the proposed PETT. (a) $i_{ab} < 0$ and V_1, V_4, S_1, S_4 are on. (b) $i_{ab} > 0$ and V_1, V_4, S_1, S_4 are on. (c) $i_{ab} < 0$ and V_1, V_3, S_1, S_4 are on. (d) $i_{ab} > 0$ and V_2, V_3, S_2, S_3 are on. (e) $i_{ab} < 0$ and V_2, V_3, S_2, S_3 are on. (f) $i_{ab} > 0$ and V_2, V_4, S_2, S_3 are on.

In Figure 5a, $i_{ab} < 0$. At this point, the current i_{ab} flows into point b, through V_4 , the capacitor C_{sm} , and V_1 , and subsequently out of point a. In this process, $u_{ab} = u_{sm}$, and the inductor L_s stores energy. The switching combination of H_2 is in mode 5 and $i_{cd} < 0$. At this point, the current flows in from point d, through S_4 , the capacitor C_{dc} , and S_1 , and finally out from point c. In this process, $u_{cd} = u_{dc}$.

In Figure 5b, $i_{ab} > 0$. At this point, the current i_{ab} flows in from point a, through the anti-parallel diode of V_1 , the capacitor C_{sm} , and the anti-parallel diode of V_4 , and finally out from point b. The inductor L_s releases energy. In this process, $u_{ab} = u_{sm}$, and the inductor L_s releases energy. The switching combination of H_2 is in mode 5 and $i_{cd} > 0$. At this time, the current i_{cd} current flows from point c, flows through the anti-parallel diode of S_1 , the capacitor C_{dc} , and the anti-parallel diode of S_4 , and finally out from point d. In this process, $u_{cd} = u_{dc}$.

In Figure 5c, $i_{ab} < 0$. At this point, the current i_{ab} flows in from point b, flows through V_1 and the anti-parallel diode of V_3 , and finally out from point a. In this process, $u_{ab} = 0$. The current loop of H_2 remains the same as in Figure 5a.

When $e_g < 0$, the modes of H_1 are mode 2 and mode 1. When the switching combination of H_1 is in mode 2, the voltage across the inductor L_s is greater than 0. Depending on the direction of the current i_{ab} , H_1 is equipped with 2 current loops. Figure 5d,e illustrate the aforementioned two current loops. When the switching combination of H_1 is in mode 1, the voltage across the inductor L_s is less than 0. At this time, the current loop of H_1 is shown in Figure 5f. The specific analyses are as follows:

In Figure 5d, $i_{ab} > 0$. At this point, the current i_{ab} flows in from point a, flows through V_2 , the capacitor C_{sm} , and V_3 , and finally out from point b. In this process, $u_{ab} = -u_{sm}$ and the inductor L_s stores energy. The switching combination of H_2 is in mode 6 and $i_{cd} > 0$. At this time, i_{cd} flows in from point c, flows through S_2 , the capacitor C_{dc} , and S_3 , and finally flows out from point d. In this process, $u_{cd} = -u_{dc}$.

In Figure 5e, $i_{ab} < 0$. At this point, the current i_{ab} flows in from point b, flows through the anti-parallel diode of V_3 , the capacitor C_{sm} , and the anti-parallel diode of V_2 , and finally

flows out from point a. In this process, $u_{ab} = -u_{sm}$, and the inductor L_s releases energy. The switching combination of H_2 is in mode 6 and $i_{cd} < 0$. At this point, the current i_{cd} flows from point d, through the anti-parallel diode of S_3 , the capacitor C_{dc} , and the anti-parallel diode of S_2 , and finally out from point c. In this process, $u_{cd} = -u_{dc}$.

In Figure 5f, $i_{ab} > 0$. At this point, the current i_{ab} flows in from point a, flows through V_4 and the anti-parallel diodes of V_2 , and finally flows out from point b. In this process, $u_{ab} = 0$. The current loop of H_2 remains the same as it is in Figure 5d.

2.3. Mathematical Modelling of the Proposed PETT

The equivalent circuit of the proposed PETT is shown in Figure 6, where half of the power unit AC-side voltages are $(Nu_{f1} + Nu_{f2})$ and the other half of the power unit AC-side voltages are $(Nu_{f1} - Nu_{f2})$. The loop 1 in Figure 6 is analysed and the KVL equation is written as follows:

$$e_g - r_s i_g - L_s \frac{d}{dt} i_g - N_s Nu_{f1} = 0, \quad (11)$$

where e_g is the traction grid voltage, i_g is the grid input current, L_s is the grid-side filter inductance, N_s is the number of power units, N is the number of sub-modules inside a single power unit, and u_{f1} is the voltage component of the sub-module AC-side voltage with frequency f_1 .

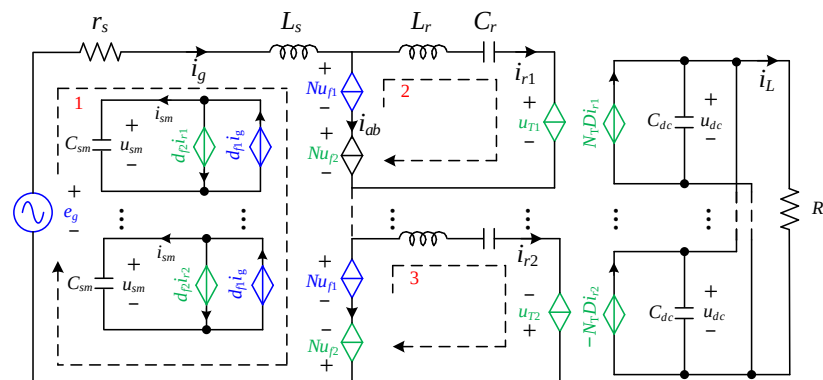


Figure 6. An equivalent circuit of the proposed PETT.

Let us assume that the grid voltage e_g is $e_g = E_m \sin \omega_1 t$ and the voltage component u_{f1} is $u_{f1} = E_{m1} \sin \omega_1 t$. From Equation (11), the first-order linear differential equation can be obtained as follows:

$$i_g'(t) + \frac{r_s}{L_s} i_g(t) = \frac{E_m - E_{m1}}{L_s} \sin(\omega_1 t), \quad (12)$$

The solution to Equation (12) is as follows:

$$i_g(t) = \frac{E_m - E_{m1}}{r_s^2 + \omega_1^2 L_s^2} (r_s \sin \omega_1 t - L_s \cos \omega_1 t) + c_1 e^{-\frac{r_s}{L_s} t}, \quad (13)$$

Considering $i_g(t=0) = 0$, the value of the constant c_1 in Equation (13) can be obtained. Also, the phase angle φ_1 is introduced and satisfied:

$$\begin{cases} \sin \varphi_1 = \frac{r_s}{\sqrt{r_s^2 + \omega_1^2 L_s^2}} \\ \cos \varphi_1 = \frac{\omega_1 L_s}{\sqrt{r_s^2 + \omega_1^2 L_s^2}} \end{cases}, \quad (14)$$

From the preceding analysis, it can be inferred that

$$i_g(t) = \frac{E_m - N_s N E_{m1}}{\sqrt{r_s^2 + \omega_1^2 L_s^2}} \sin(\omega_1 t - \varphi_1) + \frac{E_m - E_{m1}}{r_s^2 + \omega_1^2 L_s^2} L_s e^{-\frac{r_s}{L_s} t}, \quad (15)$$

Equation (15) shows that the steady-state current of i_g does not contain the harmonics associated with f_2 , and the current i_g can be expressed as $i_g = I_m \sin(\omega_1 - \varphi_1)$.

The loop 2 in Figure 6 is analysed and the KVL equation is written as

$$Nu_{f1} + Nu_{f2} - L_r \frac{d}{dt} i_r - u_{cr} - u_T = 0, \quad (16)$$

where u_T is the primary-side voltage of MFT.

Since the resonant frequency of the LC resonant circuit is the same as that of u_{f2} , then L_r and C_r satisfy $L_r C_r = 1/\omega_2$. The following can be obtained:

$$\begin{cases} Nu_{f1} - L_r \frac{d}{dt} i_r - u_{cr} = 0 \\ Nu_{f2} - u_T = 0 \end{cases}, \quad (17)$$

The second-order linear differential equation can be obtained from (17):

$$u''_{cr}(t) + \frac{1}{L_r C_r} u_{cr}(t) = \frac{NE_{m1}}{L_r C_r} \sin(\omega_1 t), \quad (18)$$

The solution to Equation (12) is as follows:

$$u_{cr}(t) = c_2 \sin(\omega_2 t) + c_3 \cos(\omega_2 t) + \frac{\omega_1^2}{\omega_2^2 - \omega_1^2} NE_{m1} \sin(\omega_1 t), \quad (19)$$

The derivative operation on Equation (19) gives the current of the LC filter circuit as

$$i_{r1}(t) = c_2 \omega_2 C_r \cos(\omega_2 t) - c_3 \omega_2 C_r \sin(\omega_2 t) + \frac{\omega_1^3}{\omega_2^2 - \omega_1^2} NE_{m1} C_r \cos(\omega_1 t), \quad (20)$$

Considering $i_r(t=0) = 0$, the value of the constant c_2 in Equation (20) can be determined. Upon the substitution of this value into Equation (20), the result is as follows:

$$i_{r1}(t) = -\frac{\omega_1^3}{\omega_2^2 - \omega_1^2} NE_{m1} C_r \cos(\omega_2 t) - c_3 \omega_2 C_r \sin(\omega_2 t) + \frac{\omega_1^3}{\omega_2^2 - \omega_1^2} NE_{m1} C_r \cos(\omega_1 t), \quad (21)$$

Equation (21) shows that the LC filter current contains harmonics related to f_2 . However, in the actual design, when the angular frequency ω_2 is much larger than ω_1 , and the smaller C_r is selected as the filter capacitor, the coefficients of the first and third terms on the right side of the middle equation of Equation (20) are smaller, and the maximum or minimum value of the current i_r can then be considered to be $I_{rm} = |c_3| \omega_2 C_r$. Considering that the maximum transmitted power satisfies $P_m = 0.5 E_m I_m = 0.5 N_s N E_{m2} I_{rm}$, the value of the constant c_3 can be obtained. Upon the substitution of this value into Equation (21), the result is as follows:

$$i_{r1}(t) = \frac{E_m I_m}{N_s N E_{m2}} \sin(\omega_2 t) + \frac{\omega_1^3}{\omega_2^2 - \omega_1^2} NE_{m1} C_r [\cos(\omega_2 t) - \cos(\omega_1 t)], \quad (22)$$

Similarly, an examination of the analysis of loop 3 in Figure 6 reveals that

$$i_{r2}(t) = -\frac{E_m I_m}{N_s N E_{m2}} \sin(\omega_2 t) + \frac{\omega_1^3}{\omega_2^2 - \omega_1^2} NE_{m1} C_r [\cos(\omega_2 t) - \cos(\omega_1 t)], \quad (23)$$

The presence of time-varying AC quantities in the mathematical model obtained is not favourable for control system design. It is also necessary to transform it into a mathematical model in the dq coordinate system by means of coordinate transformation. For single-phase systems, a virtual orthogonal component must be constructed when performing coordinate transformation. In this paper, we will construct the virtual β -axis orthogonal to the α -axis

by delaying a quarter cycle, then construct the $\alpha\beta$ coordinate system, and finally complete the construction of the dq coordinate system.

The mathematical model of the proposed PETT in the coordinate system of the dq coordinate system is as follows:

$$\begin{cases} L_s \frac{d}{dt} i_d + r_s i_d = e_d - N_s N d_d u_{sm} + \omega_1 L_s i_q \\ L_s \frac{d}{dt} i_q + r_s i_q = e_q - N_s N d_q u_{sm} - \omega_1 L_s i_d \\ C_{sm} \frac{d}{dt} u_{sm} + \frac{m_2 C_{dc}}{N_T} \frac{d}{dt} u_{dc} = d_f i_g - \frac{m_2 u_{dc}}{N_T R_{eq}} \end{cases}, \quad (24)$$

where R_{eq} is the equivalent load of a single power unit, $R_{eq} = R_L / N_s$.

3. Control Strategy of the Proposed PETT

In the field of PWM converter control, the double closed-loop strategy is a well-established approach that offers the benefits of a rapid dynamic response and high interference immunity [27–31]. Typically, this strategy comprises voltage outer-loop control and current inner-loop control. For the PETT circuit under consideration, the double closed-loop control represents a straightforward and effective control strategy.

3.1. Analyse of the Current Inner-Loop Control System

The present loop control circuit is designed in accordance with the specifications set forth in Equation (24). Given the symmetry between the i_q current loop and the i_d current loop, the design method for the latter will be outlined in this section. When the PI controller is employed as the current controller and feedforward control quantities are introduced, the control equation can be designed as follows:

$$\begin{cases} N_s N d_d u_{sm} = e_d - \frac{k_{p1}s + k_{i1}}{s} (i_d^* - i_d) + \omega_1 L_s i_q \\ N_s N d_q u_{sm} = e_q - \frac{k_{p1}s + k_{i1}}{s} (i_q^* - i_q) - \omega_1 L_s i_d' \end{cases} \quad (25)$$

where k_{p1} and k_{i1} are the proportional and integral regulation gains of the current controller, respectively; i_d^* is the command value of the current i_d ; i_q^* is the command value of the current i_q ; and the third term on the right side of the equation is the feed-forward control quantity.

The current loop, illustrated in Figure 7, is constructed in accordance with Equation (25). In Figure 7, $G_1(s)$ is the transfer function of the i_d current controller. $G_2(s)$ is the transfer function of the H-bridge converter under PWM control. $G_3(s)$ is the open-loop transfer function of the system unit. The specific expression for the aforementioned transfer functions is as follows:

$$\begin{cases} G_1(s) = k_{p1} + \frac{k_{i1}}{s} \\ G_2(s) = \frac{1}{T_i s + 1} \\ G_3(s) = \frac{1}{s L_s + r_s} \end{cases}, \quad (26)$$

where T_i is the sampling period of the current loop and is the same as the switching period T_s , meaning that $T_i = T_s$.

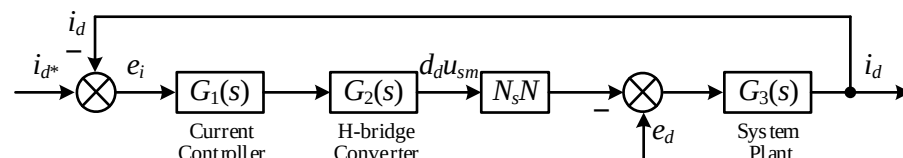


Figure 7. Structure of i_d current loop control system after decoupling.

In the absence of the consideration of e_d , the open-loop transfer function of the i_d current loop can be expressed as follows:

$$F_1(s) = \frac{N_s N}{r_s} \frac{k_{i1}}{s} \left(\frac{1}{T_i s + 1} \right) \left(\frac{k_{p1}}{k_{i1}} s + 1 \right) \frac{1}{\left(\frac{L_s}{r_s} s + 1 \right)}, \quad (27)$$

Equation (27) shows that the i_d current loop comprises two poles, namely, $s_1 = -1/T_i$ and $s_2 = -L_s/r_s$. In the majority of cases, the main pole is identified as s_2 due to the considerable value of f_i . In order to achieve a faster response, it is possible to utilise the controller's zeros in order to offset s_2 . This can be achieved by setting $k_{p1}/k_{i1} = L_s/r_s$. At this juncture, the switching function $F_1(s)$ is as follows:

$$F_1(s) = \frac{N_s N k_{i1}}{r_s} \frac{1}{s(T_i s + 1)}, \quad (28)$$

Then, the closed loop transfer function of the i_d current loop is as follows:

$$G_i(s) = \frac{N_s N k_{i1}}{r_s T_i s^2 + r_s s + N_s N k_{i1}}, \quad (29)$$

3.2. Analysis of the Voltage Outer-Loop Control System

The present loop control voltage is designed in accordance with the specifications set forth in (24). When the PI controller is employed as the voltage controller, the control equation can be designed as

$$d_{f1} i_g = \frac{k_{p2} s + k_{i2}}{s} (u_{sm}^* - u_{sm}) + \frac{m_2}{N_T} \frac{k_{p3} s + k_{i3}}{s} (u_{dc}^* - u_{dc}), \quad (30)$$

where k_{p2} and k_{i2} are the proportional adjustment gain and integral adjustment gain of the voltage u_{sm} controller; k_{p3} and k_{i3} are the proportional adjustment gain and integral adjustment gain of the voltage u_{dc} controller; u_{sm}^* is the command value of the voltage u_{sm} ; and u_{dc}^* is the command value of the voltage u_{dc} .

Considering the preceding analysis, it can be assumed that $i_g = I_m \sin(\omega_1 t - \varphi_1)$ and $i_r = I_{rm} \sin \omega_2 t$. With regard to the DC-side fundamental wave and double frequency fluctuation, the DC-side current component of H_1 can be expressed as follows:

$$d_{f1} i_g = 0.5 m_1 I_m \cos \varphi_1 - 0.5 m_1 I_m \cos(2\omega_1 t - \varphi_1), \quad (31)$$

$$d_{f2} i_r = \frac{2}{\pi} m_2 I_{rm} - \frac{2}{\pi} m_2 I_{rm} \cos(2\omega_2 t) + \frac{1}{2} m_2 I_{rm} \sum_{j=3}^{\infty} \left\{ \frac{4}{j\pi} [\cos(j\omega_2 t - \omega_2 t) - \cos(j\omega_2 t + \omega_2 t)] \right\}, \quad (32)$$

The voltage loop, illustrated in Figure 8, is constructed in accordance with Equation (30). In Figure 8, $G_4(s)$ and $G_6(s)$ are the transfer functions of the u_{sm} voltage controller and the u_{dc} voltage controller, respectively. $G_5(s)$, $G_7(s)$, and $G_8(s)$ are the open-loop transfer functions of the system devices. The specific expression for the aforementioned transfer functions is as follows:

$$\begin{cases} G_4(s) = k_{p2} + \frac{k_{i2}}{s} \\ G_5(s) = \frac{1}{s C_{sm}} \\ G_6(s) = k_{p3} + \frac{k_{i3}}{s} \\ G_7(s) = \frac{1}{L_r C_r s^2 + 1} \\ G_8(s) = \frac{1}{s C_r} \end{cases}, \quad (33)$$

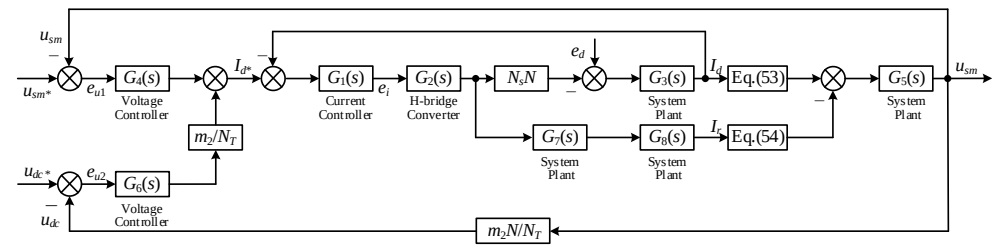


Figure 8. Structure of voltage loop control system.

As illustrated in Figure 8, both Equations (31) and (32) are time-varying links. This introduces challenges in the design of the voltage loop, which can be addressed by considering the maximum proportional gain of the link as a potential replacement. In the absence of the consideration of the e_d , the equivalent structure diagram, as illustrated in Figure 9, is obtained through the simplification of the control structure diagram, as shown in Figure 8. This is achieved through the combination of comparison points, the shifting of the lead point backwards, and the application of series equivalence and parallel equivalence.

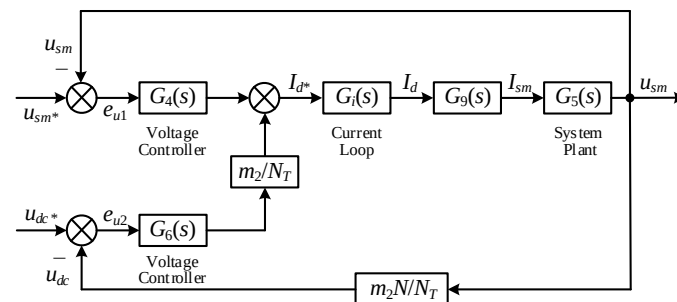


Figure 9. Equivalent structure of voltage loop control system.

In Figure 9, the specific expression of $G_9(s)$ is as follows:

$$G_9(s) = 0.5m_1 - 0.64m_2 \frac{G_7(s)G_8(s)}{NsNG_3(s)}, \quad (34)$$

When $u_{dc}^* = 0$, the open-loop transfer function between the input signal u_{sm}^* and the output signal u_{sm} can be obtained as follows

$$F_2(s) = \frac{G_4(s)G_i(s)G_9(s)G_5(s)}{1 + \frac{m_2^2 N}{N_T^2} G_6(s)G_i(s)G_9(s)G_5(s)}, \quad (35)$$

When $u_{sm}^* = 0$, the open-loop transfer function between the input signal u_{dc}^* and the output signal u_{sm} can be obtained as follows

$$F_3(s) = \frac{m_2 G_6(s)G_i(s)G_9(s)G_5(s)}{N_T + N_T G_4(s)G_i(s)G_9(s)G_5(s)}, \quad (36)$$

3.3. Integrated Control Strategy

In summary, the overall control block diagram of the proposed PETT is presented in Figure 10. The voltage control loop employs PI controllers, while the control voltages u_{sm} and u_{dc} adhere to the prescribed values of u_{sm}^* and u_{dc}^* , respectively. The outputs of the aforementioned controllers are employed as inputs to the current loop following the implementation of requisite arithmetic operations. Subsequently, the modulating signal waveform, designated as d_{f1} , is generated following the completion of the current loop and coordinate transformation. The values of m_2 are then obtained through the operation of u_{sm}^* and u_{dc}^* . This, in turn, generates the aforementioned modulating signal waveform,

designated as d_{f2} . Subsequently, the aforementioned two modulating signals (d_{f1} and d_{f2}) are superimposed, whereupon PWM modulation is performed. The resulting output is the control signal for H_1 . In conclusion, a fixed-frequency square-wave pulse is employed as the control signal for H_2 .

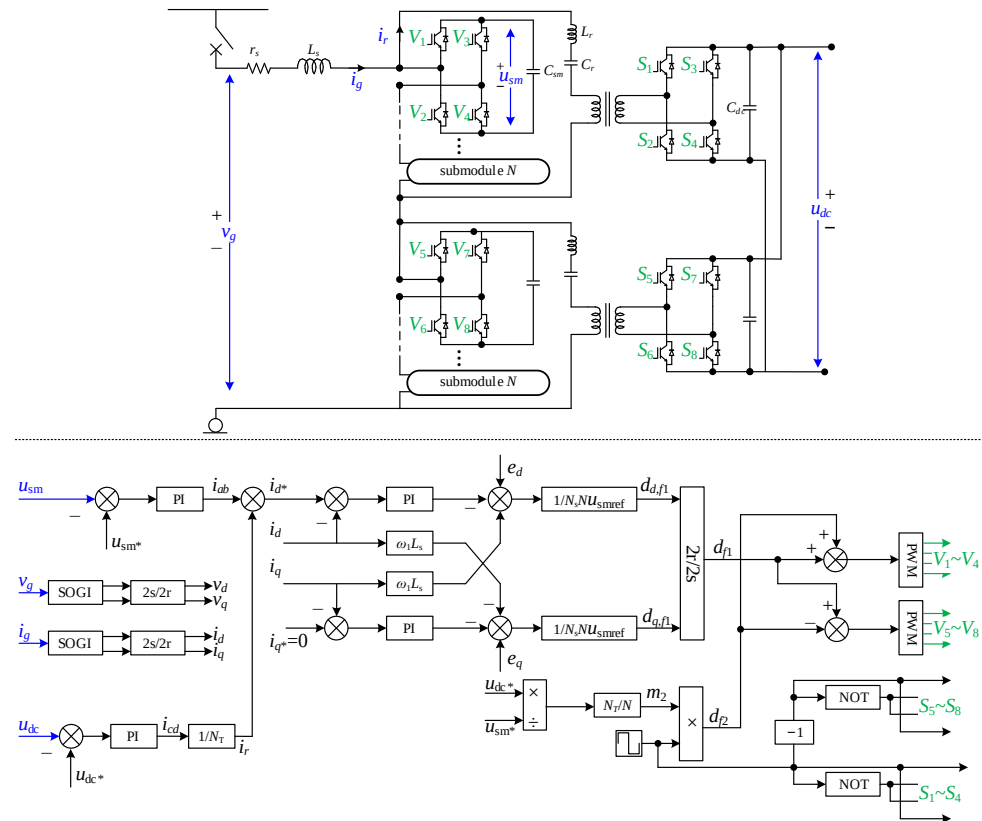


Figure 10. The control strategy adopted for the proposed PETT.

The extensive use of power electronic equipment will inevitably result in an increase in the total harmonic distortion (THD) of the incoming current. Improvements in THD can be achieved through the optimisation of the topology, the enhancement of the hardware performance, and the optimisation of the control algorithm, with the objective of ensuring the power quality. When the proposed PETT adopts the control strategy shown in Figure 10, the PWM control can be combined with the selective harmonic elimination (SHE) technique to eliminate the lower harmonics and reduce the THD value under the traditional PWM control while also ensuring the fundamental amplitude. This method necessitates only minimal alterations to the control circuit and is straightforward to implement. Furthermore, the introduction of a harmonic compensator can serve to mitigate the effects of harmonic currents. By rotating the positive-sequence component of the k th harmonic by $k\omega_1$ while the negative-sequence component rotates by $-k\omega_1$, a mathematical model of the controlled object in the k th harmonic rotating coordinate system is obtained. This model is then used to design the parameters of the harmonic compensator. This scheme necessitates a significant alteration to the control circuit. As the improvement of the THD is not the primary objective of this study, a detailed examination of this topic is not provided here.

3.4. Loss Analysis of the Proposed PETT

A reasonable loss analysis constitutes an essential component of the converter design process. Calculating the power loss of the converter and subsequently predicting the efficiency of the converter facilitates the subsequent optimisation of the converter's efficiency. Concurrently, forecasting the temperature distribution of the switching devices and magnetic components supports subsequent work on the thermal design of the entire

machine. This section presents a discussion of the power loss, including the conduction loss and switching loss, caused by the proposed PETT switching under the control strategy illustrated in Figure 10. The discussion employs an N-channel type IGBT module as a case study.

(i) Conduction loss

Upon the activation of the IGBT module, two distinct operational states are observed: forward conduction and reverse conduction (anti-parallel diode conduction). Figure 11 illustrates the conduction sequence of the switching devices and the current waveforms flowing through the IGBTs and diodes in H_1 under unipolar PWM control.

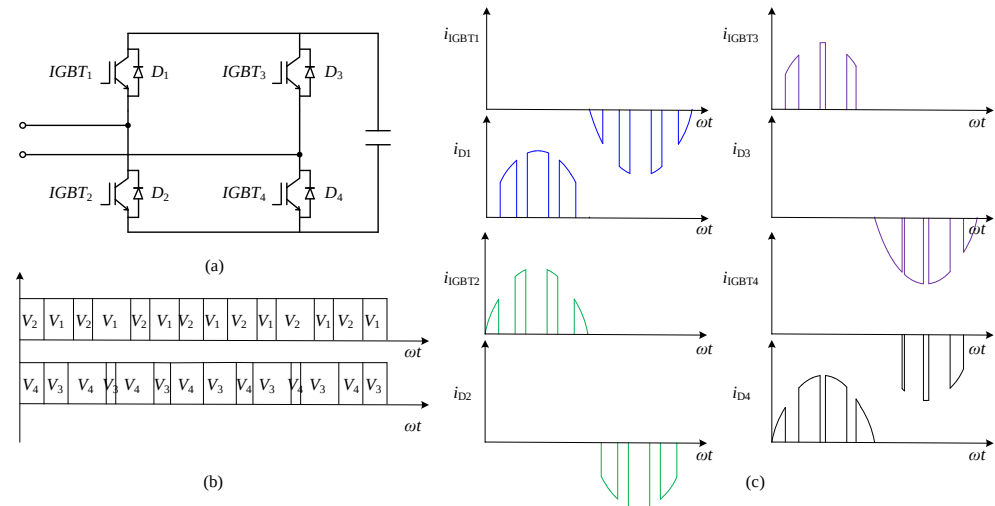


Figure 11. Current waveforms of switching devices in H_1 under unipolar PWM control. (a) H-bridge circuit. (b) Switch conduction sequence. (c) Current waveform of each switching device in one operating cycle.

As illustrated in Figure 11, at each current cycle, both the IGBT and the diode are operational for only half of the cycle. Let us consider first that the conduction loss of a single IGBT when the modulating waveform is sinusoidal (frequency f_1) is as follows:

$$p_{CT,f1} = \frac{1}{T_{f1}} \int_0^{T_{f1}} \frac{1}{2} v_{ce}(t) i_{ce}(t) d_{f1}(t) dt, \quad (37)$$

where T_{f1} is the operating period of the IGBT, $d_{f1}(t)$ is the duty cycle function, $i_{ce}(t)$ is the on-state current, and $v_{ce}(t)$ is the on-state voltage drop. The latter is solved by the following (38):

$$v_{ce}(t) = u_{ce0} + r_{ce} i_{ce}(t), \quad (38)$$

where u_{ce0} and r_{ce} are obtained from the IGBT output characteristic curve provided by the IGBT manufacturer.

It has been previously established that $i_{ce}(t) = I_m \sin(\omega_1 t - \varphi_1)$ and $d_{f1}(V_1) = 0.5 + 0.5m_1 \sin \omega_1 t$. Upon substituting $i_{ce}(t)$ and $d_{f1}(t)$ into (37) and (38), the conduction loss of a single IGBT in one operating cycle is obtained as follows:

$$p_{CT,f1} = \frac{u_{ce0} I_m}{2\pi} + \frac{r_{ce} I_m^2}{8} + \frac{m_1 u_{ce0} I_m}{8} + \frac{m_1 r_{ce} I_m^2}{3\pi}, \quad (39)$$

Similarly, the conduction loss of a single diode in one operating cycle is obtained as follows:

$$p_{CD,f1} = \frac{u_{t0} I_m}{2\pi} + \frac{r_t I_m^2}{8} - \frac{m_1 u_{t0} I_m}{8} - \frac{m_1 r_t I_m^2}{3\pi}, \quad (40)$$

where u_{t0} and r_t are obtained by means of diode output characteristic curves provided by the manufacturer.

Next, let us consider the calculation of the conduction loss of a single IGBT and diode when the modulating waveform is a square wave (frequency f_2). It was previously shown that $i_d(t) = I_{rm} \sin(\omega_2 t)$. The duty cycle function is shown in Equation (5). This information can be used to determine the following:

$$p_{CT,f2} = \frac{u_{ce0} I_{rm}}{2\pi} + \frac{r_{ce} I_{rm}^2}{8} + \frac{m_2 u_{ce0} I_{rm}}{2\pi} + \frac{m_2 r_{ce} I_{rm}^2}{\pi^2} \sum_{j=1} \left[\frac{1}{j^2} - \frac{1}{(j+2)(j-2)} \right], \quad (41)$$

$$p_{CD,f2} = \frac{u_{t0} I_{rm}}{2\pi} + \frac{r_t I_{rm}^2}{8} - \frac{m_2 u_{t0} I_{rm}}{2\pi} - \frac{m_2 r_t I_{rm}^2}{\pi^2} \sum_{j=1} \left[\frac{1}{j^2} - \frac{1}{(j+2)(j-2)} \right], \quad (42)$$

(ii) Switching loss

Switching loss is the loss generated during the turn-on and turn-off process of power electronic devices, including turn-on loss and turn-off loss. Switching losses can be obtained by both estimation and experimental measurement.

Approximating the switching process to be linear, the switching losses are estimated by using the voltage and current values at turn-on or turn-off, as are the rise and fall times. Alternatively, using the manuals provided by the device manufacturers, the switching losses under standard conditions are read and the switching losses are estimated based on the actual temperature, voltage, and current. Let us consider the parasitic parameters in the switching device, including the parasitic capacitance and parasitic inductance. The switching process of the device is not linear, and so the switching loss obtained by the prediction method is incorrect in relation to the actual loss. This also requires that more accurate switching loss predictions should be obtained through experimental calculations in situations where efficiency optimisation is required.

4. Parametric Design of the Proposed PETT

Grid-side inductance L_s affects the value of the DC-side voltage u_{sm} of H_1 and the waveform quality of the input current i_g . In addition, it places a limit on the maximum amount of power that can be transmitted. In the design of inductor L_s , it is essential to consider the metric of transient current tracking.

- (i) When the current i_g crosses zero, the rate of change of the current reaches its maximum value. In order to ensure the rapidity of the current response, the value of the inductor L_s should be as small as possible.
- (ii) Near the peak value of current i_g , harmonic pulsation is at its most serious. In order to suppress the harmonic current, the value of inductor L_s should be as large as possible.

In order to initiate the analysis, two switching cycles were selected: one near the current value of $i_g = 0$ and one near the peak value of i_g . The resulting tracking waveform of i_g is presented in Figure 12. Figure 12a corresponds to one switching cycle in which the value of e_g changes from a negative to a positive value, while Figure 12b corresponds to one switching cycle in which the value of e_g is positive and the value of i_g reaches its peak.

In steady-state conditions, the value of the grid voltage e_g can be considered to be constant at 0 for one switching cycle, as illustrated in Figure 12a. If the effect of r_s is disregarded, the following system of equations is derived:

$$\begin{cases} 0 = L_s \frac{\Delta i_1}{T_1} - N_s N u_{sm} & 0 \leq \omega_1 t < T_1 \\ 0 = L_s \frac{\Delta i_2}{T_2} & T_1 \leq \omega_1 t < T_s' \end{cases} \quad (43)$$

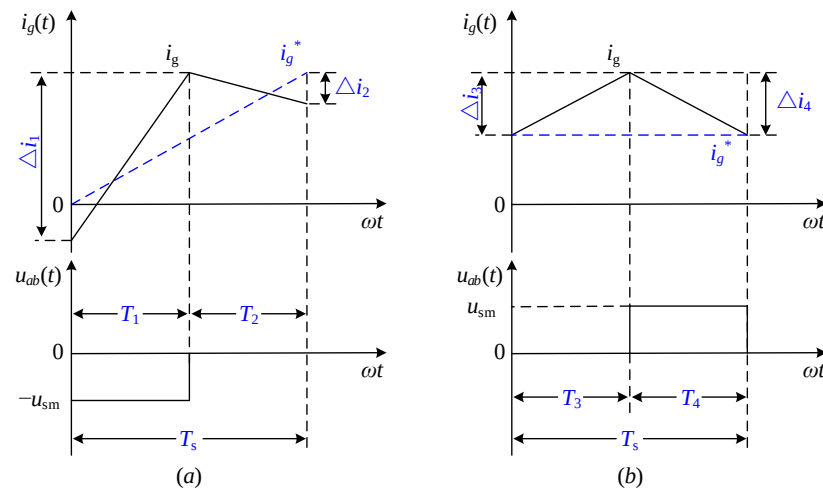


Figure 12. Current tracking waveforms during one switching cycle at special moments. (a) $i_g = 0$. (b) $i_g = i_{gm}$.

In order to facilitate the rapid advancement of the command current by the i_g , it is essential to satisfy the following equation:

$$\frac{||\Delta i_1| - |\Delta i_2||}{T_s} \geq \frac{I_m \sin(\omega_1 T_s)}{T_s}, \quad (44)$$

Since the value of the switching period T_s is sufficiently small, $\sin(\omega_1 T_s)/T_s \approx \omega_1$. The range of values of L_s can be determined by Equations (43) and (44) as follows:

$$L_s \leq \frac{N_s N u_{sm} T_1}{I_m \omega_1 T_s}, \quad (45)$$

In steady-state conditions, the value of the grid voltage e_g can be considered to be constant at E_m for one switching cycle, as illustrated in Figure 12b. If the effect of r_s is disregarded, the following system of equations is derived:

$$\begin{cases} E_m = L_s \frac{\Delta i_3}{T_3} & 0 \leq \omega_1 t < T_3 \\ E_m = L_s \frac{\Delta i_4}{T_4} + N_s N u_{sm} & T_3 \leq \omega_1 t < T_s \end{cases} \quad (46)$$

Considering that $|\Delta i_3| = |\Delta i_4|$ and $T_3 + T_4 = T_s$, the pulsation of current i_g can be obtained from (46) as follows:

$$\Delta i = \frac{N_s N u_{sm} - E_m}{L_s N_s N u_{sm}} E_m T_s, \quad (47)$$

If the maximum value of current pulsation is Δi_{max} , then the range of values of L_s can be determined as follows:

$$L_s \geq \frac{N_s N u_{sm} - E_m}{\Delta i_{max} N_s N u_{sm}} E_m T_s, \quad (48)$$

In conclusion, in order to satisfy the metric of transient current tracking, the value of L_s must satisfy the following inequality:

$$\frac{N_s N u_{sm} - E_m}{\Delta i_{max} N_s N u_{sm}} E_m T_s \leq L_s \leq \frac{N_s N u_{sm}}{I_m \omega_1}, \quad (49)$$

The DC-side capacitor (C_{sm}) of H_1 serves two distinct functions: firstly, it stabilises the DC-side voltage, and secondly, it suppresses the DC-side harmonic voltage. In the case of

H_1 , the instantaneous value component of the input power on the AC side can be expressed as follows:

$$\begin{cases} p_{f1} = \frac{1}{2}m_1u_{sm}I_m - \frac{1}{2}m_1u_{sm}I_m \cos(2\omega_1t) \\ p_{f2} = \frac{2}{\pi}m_2u_{sm}I_{rm} - \frac{2}{\pi}m_2u_{sm}I_{rm} \cos(2\omega_2t) \\ \quad + \frac{2}{\pi}m_2u_{sm}I_{rm} \sum_{j=3}^{\infty} \left\{ \frac{1}{j} [\cos(j\omega_2t - \omega_2t) - \cos(j\omega_2t + \omega_2t)] \right\} \end{cases}, \quad (50)$$

Equation (50) shows that the instantaneous power on the AC side of H_1 consists of two parts, the DC and AC power. Similarly, the instantaneous power on the DC side of H_1 should also consist of two parts, namely, the average power consumed by the load and the ripple power of the ripple current flowing through the capacitor. The instantaneous power on the DC side can be expressed as follows:

$$p_{dc1} = u_{sm}i_{sm} - u_{sm}C_{sm} \frac{d}{dt} \Delta u_{sm}, \quad (51)$$

where Δu_{sm} is the output DC ripple voltage value of H_1 .

It is assumed that the power loss of the IGBT is not considered. In accordance with the law of energy conservation, the instantaneous input power of the H-bridge converter is approximately equal to the instantaneous output power on the DC side. This is expressed as follows:

$$\begin{cases} u_{sm}i_{sm} = \frac{1}{2}m_1u_{sm}i_m - \frac{2}{\pi}m_2u_{sm}i_{rm} \\ u_{sm}C_{sm} \frac{d}{dt} \Delta u_{sm} = -\frac{m_1I_m}{2} \cos(2\omega_1t) + \frac{4m_2u_{sm}I_{rm}}{3\pi} \cos(2\omega_2t) \end{cases}, \quad (52)$$

The integration of both sides of Equation (52) results in the following:

$$C_{sm}\Delta u_{sm} = -\frac{m_1I_m}{4\omega_1} \sin(2\omega_1t) + \frac{2m_2I_{rm}}{3\pi\omega_2} \sin(2\omega_2t), \quad (53)$$

If the maximum allowable pulsation value of u_{sm} is denoted as Δu_{max1} , then $\Delta u_{max1} \geq 2\Delta u_{sm}$ needs to be satisfied. According to Equation (53) the range of values of C_{sm} can be determined as follows:

$$C_{sm} \geq \frac{4m_2I_{rm}}{3\pi\omega_2\Delta u_{max1}} + \frac{m_1I_m}{2\omega_1\Delta u_{max1}}, \quad (54)$$

Similarly, the range of values of C_{dc} can be determined as follows:

$$C_{dc} \geq \frac{4Nm_2I_{rm}}{3\pi\omega_2\Delta u_{max2}}, \quad (55)$$

where Δu_{max2} is the maximum allowable pulsation value of u_{dc} .

5. Simulation Analysis

In order to ascertain the efficacy of the proposed PETT circuit, a 1.2 MW PETT was designed and presented in this paper. The specifications of the traction grid included 15 kV/16.7 Hz. The sub-module had a DC-side voltage of 3.6 kV and a DC output voltage of 1.2 kV. Based on the design methodology outlined in Sections 2–4, the design flow of the main circuit parameters of the proposed PETT is shown in Figure 13. The principal circuit parameters of the PETT can be derived from Figure 13. The fundamental characteristics of the proposed PETT circuit are presented in Table 3.

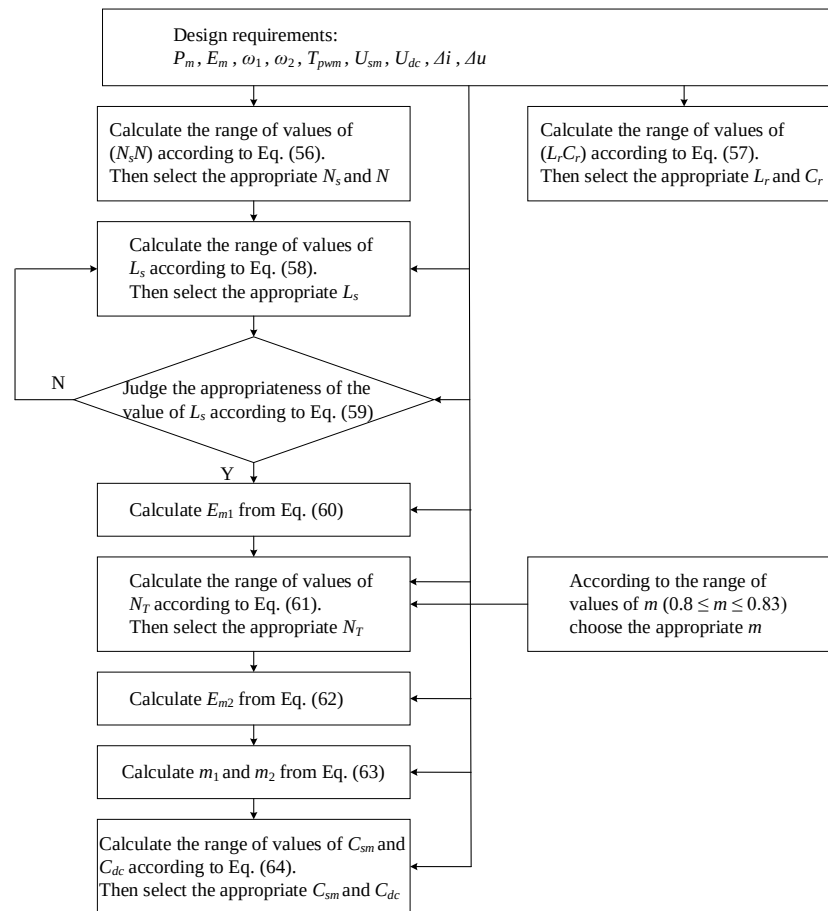


Figure 13. The design flow of the proposed PETT main circuit parameters.

Table 3. Parameters of PETT.

Circuits	Parameter	Values	Parameter	Values
Main circuit	Grid phase voltage RMS v_g	15 kV	Grid frequency f_1	16.7 Hz
	Rated power P_N	1.2 MW	Grid-side inductance L_s	60×10^{-3} H
	Number of PM N_s	2	Number of SM N	4
	Resonant inductance L_r	56.7×10^{-3} H	Resonant capacitance C_r	1×10^{-6} F
	Sub-module capacitance C_{sm}	6×10^{-3} F	Output-side capacitance C_{dc}	24×10^{-3} F
	Transformer ratio N_T	4.8	Resonant frequency f_2	668 Hz
Control Circuit	Control mode of H1	PWM	Control mode of H2	open loop control
	Switching frequency of H1	2 kHz	Switching frequency of H2	2 kHz
	DC-side voltage of H1	3.6 kV	DC-side voltage of H2	1.2 kV

In Figure 13, Equations (56)–(64) are specifically expressed as follows:

$$U_{sm} \geq \frac{E_m}{N_s N}, \quad (56)$$

where E_m is the peak value of the phase voltage, in this case the value of 12,247 V, and U_{sm} is the design value of the sub-module capacitance voltage, in this case the value of 3600 V.

$$L_r C_r = \frac{1}{\omega_2^2}, \quad (57)$$

where ω_2 is the resonant frequency of the filter, which in this case takes the value of 2000 Hz.

$$\frac{N_s N U_{sm} - E_m}{4 P_m N_s N U_{sm} \Delta i} E_m^2 T_{pwm} \leq L_s \leq \frac{N_s N}{2 P_m \omega_1} U_{sm} E_m, \quad (58)$$

where P_m is the maximum transmitted power, which is taken here as 1.2 MW; T_{PWM} is the switching period of H_1 , which is taken here as 10,000 Hz; ω_1 is the frequency of the grid voltage, which is taken here as 16.7 Hz; and Δi is the maximum permissible value of the current ripple, which is taken here as 5%.

$$L_s \leq \frac{E_m \sqrt{(N_s N U_{sm})^2 - E_m^2}}{2 \omega_1 P_m}, \quad (59)$$

$$E_{m1} = \frac{1}{N_s N} \sqrt{E_m^2 + \left(\frac{2 \omega_1 L_s P_m}{E_m} \right)^2}, \quad (60)$$

$$N_T = \frac{m N U_{sm} - N E_{m1}}{U_{dc}}, \quad (61)$$

where U_{dc} is the design value of the output DC voltage of the PETT, which in this case is taken as 1200 V.

$$E_{m2} = \frac{N_T}{N} U_{dc}, \quad (62)$$

$$m_1 = \frac{E_{m1}}{U_{sm}}, \quad m_2 = \frac{E_{m2}}{U_{sm}}, \quad (63)$$

$$\begin{cases} C_{sm} \geq \frac{2 m_2 P_m}{3 \pi \omega_2 U_{sm} \Delta u} + \frac{m_1 P_m}{2 \omega_1 E_m U_{sm} \Delta u} \\ C_{dc} \geq \frac{2 N m_2 P_m}{3 \pi \omega_2 N_s N E_{m2} U_{dc} \Delta u} \end{cases} \quad (64)$$

where Δu is the maximum permissible value of the capacitor voltage ripple, which in this case is taken as 3%.

The PET prototype, designed in accordance with Figure 1 and detailed in Table 4, is compared with the designed PETT in this paper. It is observed that the proposed PETT employs a reduced number of sub-modules, switching devices, capacitors, and MFTs. It is shown that the proposed PETT has the advantage of requiring a reduced number of power devices and passive components under the condition of the same grid voltage, the same IGBT voltage level, and the same output voltage. Furthermore, this advantage is more pronounced when non-high-voltage IGBTs are employed.

Table 4. The cascade PETT design of different structures.

Structure	Specification of PETT	Specification of Switching Devices	Sub-Modules	Number Switching	Capacitors	MFT
Figure 1a	1.2 MW	AC/DC:6.5 kV IGBT	8	96	32	8
Figure 1b	AC: 15 kV/16.7 Hz	DC/DC:3.3 kV IGBT	8	64	48	8
Figure 2	DC: 1.5 kV		8	40	12	2

In order to ascertain the veracity of the designed PETT circuit, a simulation model was constructed and analysed using PLECS 4.2. The simulation parameters are presented in Table 3. The simulation process is as follows: at $0 \leq t < 3$ s, the PETT operates at the rated load. At $3 \text{ s} \leq t < 6$ s, the PETT operates at 80% of the rated load. At $6 \text{ s} \leq t < 9$ s, the PETT operates at 60% of the rated load.

Figures 14–18 show the simulation results of some physical quantities at the primary side of the IF transformer. Specifically, Figure 14 gives the waveforms of current i_g and

voltage e_g at the grid side of the PETT. When the PETT is running stably, the sinusoidal nature of the current is good, the power factor is kept at 1, and the voltage waveform can be tracked. The calculated value of the peak current is 195.96 A at a rated load and the simulation yields a peak value of 202.3 A with an error of 3%. At $t = 3$ s and $t = 6$ s, the sudden change in load causes a short oscillation in the current, which can quickly reach a steady state, and the peak current increases after stabilisation. The results of FFT analysis of the grid side current at rated load are given in Figure 15, which shows a THD of 10.08%.

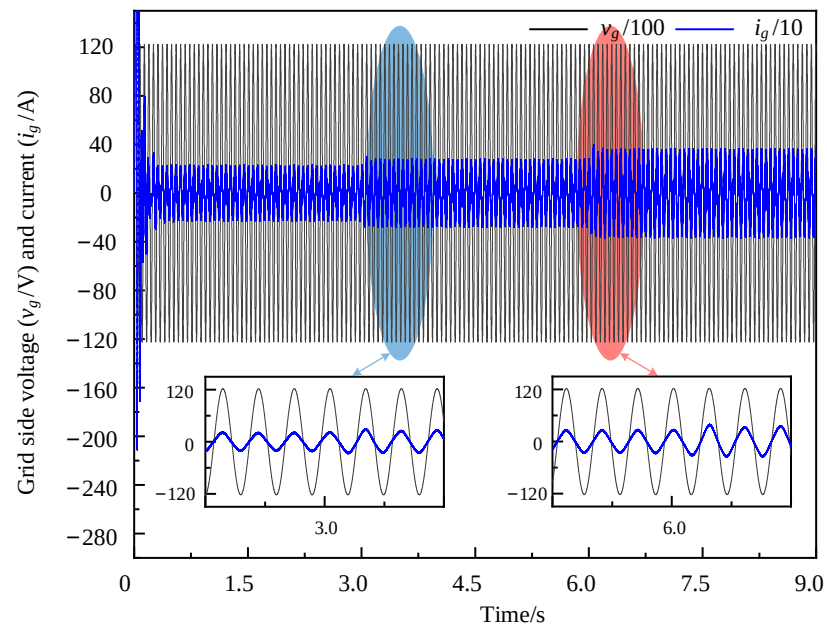


Figure 14. Network-side voltages and currents, and their local magnification.

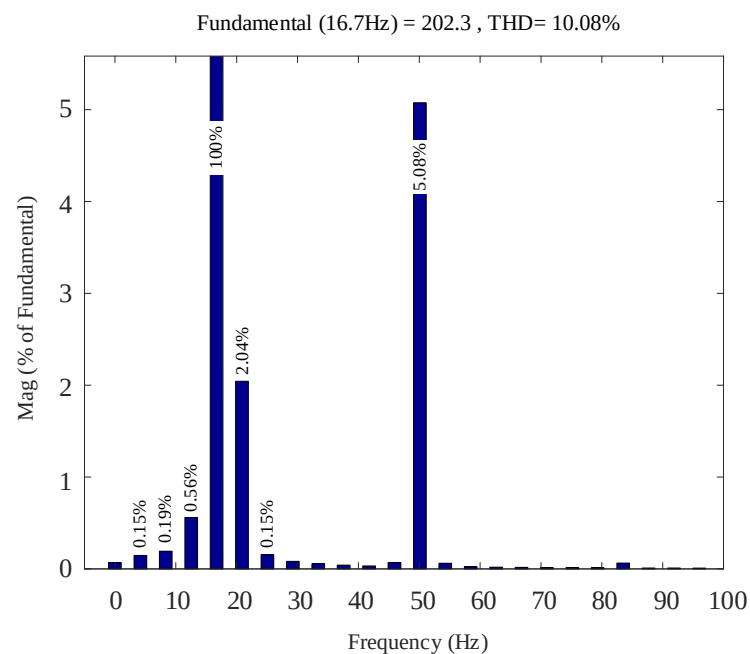


Figure 15. FFT analysis of network-side currents.

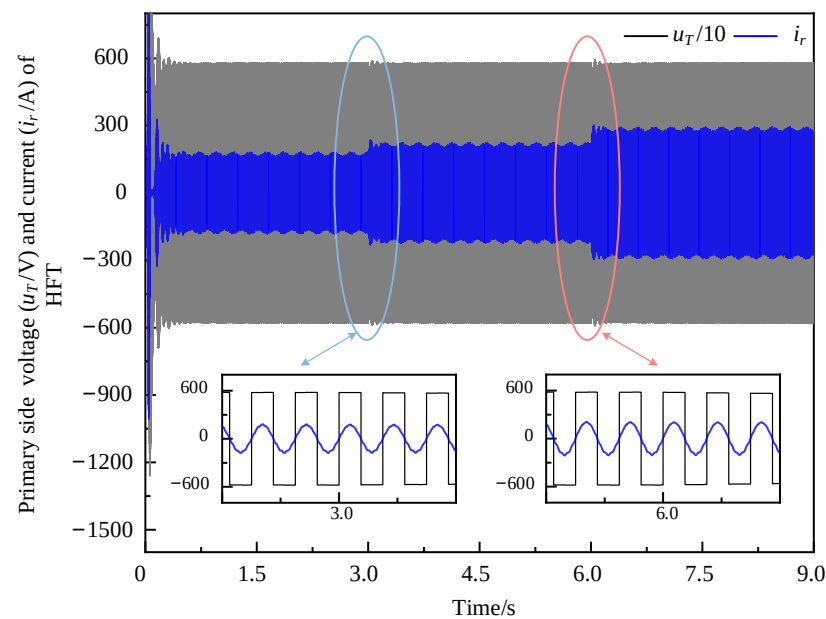


Figure 16. Primary-side voltages and currents of MFT.

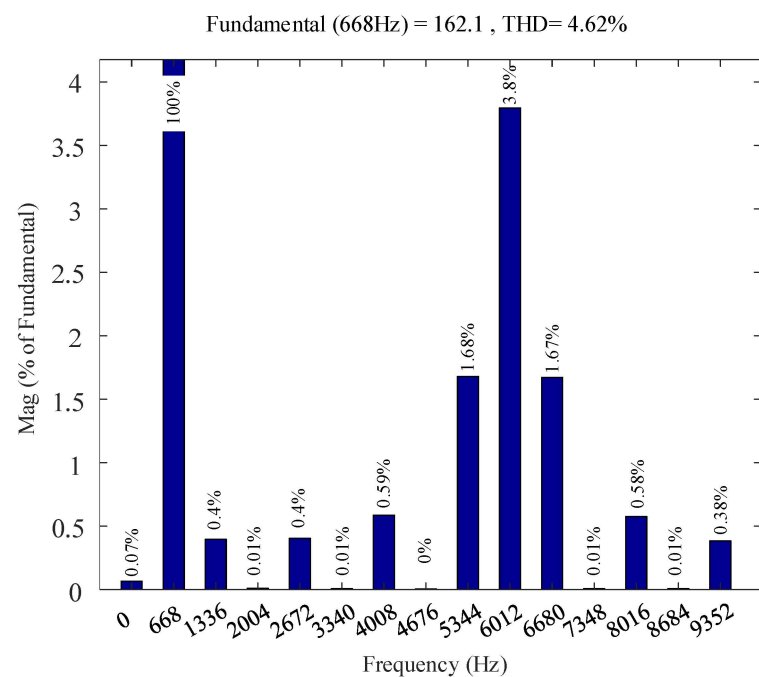


Figure 17. FFT analysis of primary-side currents of MFT.

Figure 16 illustrates the waveforms of the current i_r and voltage u_T at the primary side of the MFT. u_T is a square wave with a frequency of 668 Hz when the PETT is running stably, and the current i_r is of the same frequency and the same phase as u_T . Under the rated load, the peak value of voltage u_T is 5760 V, and the peak value of current i_r is 166 A. At $t = 3$ s and $t = 6$ s, the sudden change in the load causes a brief oscillation in the current, which can quickly reach a steady state. The peak value of the current increases after stabilisation, and the peak value of the voltage remains unchanged after stabilisation. Figure 17 gives the results of FFT analysis of i_r at rated loads, showing a THD of 4.62%.

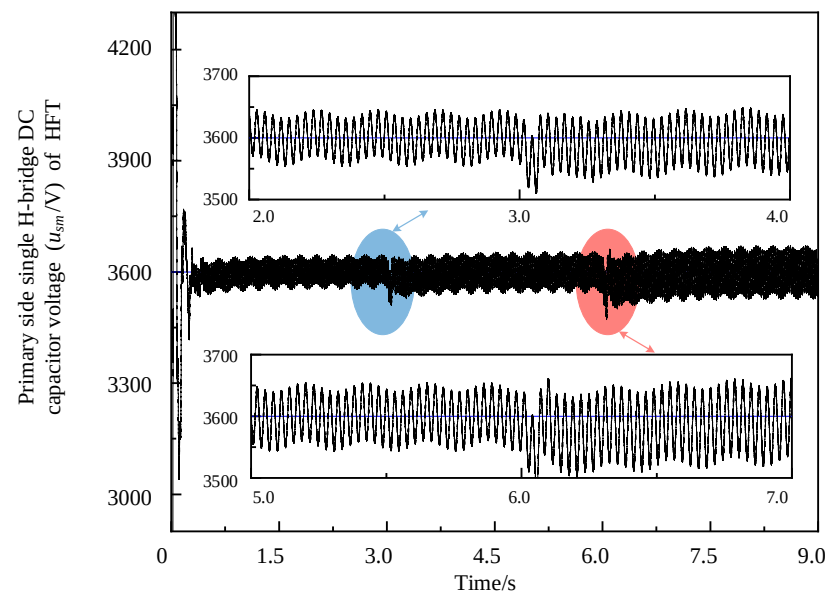


Figure 18. Voltage of capacitor C_{sm} of H_1 .

Figure 18 gives the waveforms of the voltage of capacitor C_{sm} in H_1 . The value of the voltage u_{sm} is 3600 V during the stable operation of the PETT, which agrees with the design value. The ripple of the stabilised voltage is 1.1%, 1.4%, and 1.8% at different operating points. These values meet the design requirements. At the moment of a sudden load change, the u_{sm} stabilises again faster.

Figure 19 shows the waveforms of the voltage of capacitor C_{dc} in H_2 . The value of the voltage u_{dc} is 1200 V during the stable operation of the PETT, which matches the design value. The ripple of the stabilised voltage is 0.50%, 0.58%, and 0.71% at different operating periods, which meets the design requirements. At the moment of a sudden load change, u_{dc} stabilises again faster.

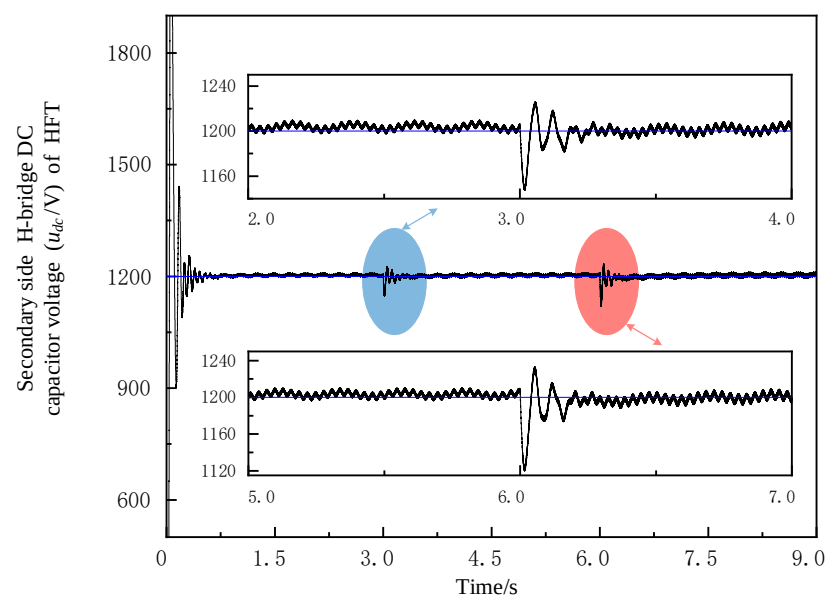


Figure 19. The voltage of capacitor C_{dc} of H_2 .

6. Conclusions

Cascaded PTETTs are considered effective in terms of reducing the number of conventional low-frequency transformers in locomotives, with the advantages of light weight, small size, and high efficiency. However, the issue of the large number of switching devices

and passive components in this type of converter cannot be ignored. In this paper, a novel PETT structure is introduced, and its feasibility is verified by theoretical analysis and simulation. The results show that the proposed PETT can achieve the multiplexing of the H-bridge through effective control, and the voltages at different frequencies are decoupled. The grid-side current can track the grid voltage better and achieve unit power factor operation. The sub-module capacitor voltage and output DC voltage can be better controlled to be in accordance with the design's value and reach the steady state again faster when the load changes abruptly. Finally, the proposed PETT has positive significance, with reduced size and weight in relation to other PETTs and increased the power density.

Voltage equalisation strategies between multiple sub-modules of the proposed PETT will also be explored in the future. In addition, the development of accurate loss models will help to design more efficient PETTs, and these studies will further deepen the research on the proposed PETT and enable the successful use of the prototype on a locomotive.

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