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A 28/56 Gb/s NRZ/PAM-4 Dual-Mode Transmitter with Eye-Opening Enhancement in 28 nm CMOS

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Abstract: This paper presents a non-return-to-zero (NRZ)/4-level pulse amplitude modulation (PAM-4) dual-mode wireline transmitter with an eye-opening enhancement technique to improve horizontal eye-opening. With the eye-enhancement pulse generator and the auxiliary pull-up device in the tail-less current-mode driver, the worst-case horizontal eye-opening increased by 30% in the PAM-4 eye diagram. The power efficiency of the NRZ mode was also improved by completely turning off the LSB path in the differential data path, resulting in only a 31% power efficiency degradation, which is far lower than that of the prior dual-mode transmitters. Fabricated in 28 nm CMOS, the transmitter achieves power efficiency of 1.4 pJ/bit at 56 Gb/s in PAM-4 mode and 1.84 pJ/bit at 28 Gb/s in NRZ mode, respectively.

Keywords: wireline transmitter; eye-opening enhancement; non-return-to-zero (NRZ); 4-level pulse amplitude modulation (PAM-4); dual-mode

1. Introduction

The continuous growth of data-intensive computing has pushed the bandwidth of high-speed wireline links over 50 Gb/s or beyond by utilizing 4-level pulse amplitude modulation (PAM-4) signaling [1–8], which doubles the data rate without increasing the symbol rate. In comparison to conventional non-return-to-zero (NRZ) signaling [9–12], however, using multiple single levels inevitably leads to a reduction in eye-opening. In particular, the reduced horizontal eye-opening due to transitions among multiple non-adjacent levels negatively impacts the timing margin at the receiver, potentially degrading the overall link signal integrity [13–16]. Fundamentally, the reduction in horizontal eye-opening occurs due to the limited transition time between signal levels. To address these issues, there have been several studies that aimed to improve horizontal eye-opening by using custom-designed pulse generators for edge-boosting [2] or programmable pulse width [3]. These techniques have shown improved eye-opening by reducing the transition time, but often require a redundant DC current during the pre-charging phase or this will result in an additional precursor intersymbol interference (ISI) at the transmitter output after channel. This paper presents an improved eye-opening enhancement technique by adding an auxiliary pull-up device in a tail-less CML driver, achieving an average 25% improvement in horizontal eye-opening. Unlike the previous eye-enhancement techniques, our method does not suffer from an extra DC current or a precursor ISI issue.

Another challenge in PAM-4 transmitter design is that the transmitter is commonly required to generate both PAM-4 and NRZ outputs for backward compatibility in typical wireline standards [17–19]. While generating the dual-mode output is not difficult, maintaining good energy efficiency for both modes is not trivial. For example, in [4], all driver slices are utilized in both the PAM-4 mode and NRZ mode. Therefore, the power consumption in both modes stays the same, leading to less energy efficiency in the NRZ mode than in the PAM-4 mode. This seemingly ironic characteristic is not desirable, given that the I/O energy efficiency worsens when the data rate is lower. This work presents a

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Citation: Won, J.; Kim, J. A 28/56 Gb/s NRZ/PAM-4 Dual-Mode Transmitter with Eye-Opening Enhancement in 28 nm CMOS. *Electronics* **2024**, *13*, 3774. https://doi.org/10.3390/electronics13183774

Academic Editor: Costas Psychalinos

Received: 1 September 2024
Revised: 20 September 2024
Accepted: 20 September 2024
Published: 23 September 2024

transmitter data path design that enables a considerable power reduction in NRZ mode for an NRZ/PAM-4 dual-mode transmitter. Experimental results show that the energy efficiency degrades by only 31% as opposed to 100% in both [4,5].

The paper is organized as follows. Section 2 presents the architecture of the transmitter along with our proposed technique for the eye-opening enhancement. Section 3 describes the circuit implementation to realize substantial power savings in NRZ mode. Section 4 presents the measurement results. Section 5 concludes this paper.

2. Transmitter with Eye-Opening Enhancement

Figure 1 shows the overall architecture of the transmitter consisting of a 4-to-1 multiplexing output driver and a differential data path. An on-chip 4-way parallel QPRBS13 pattern generator [20] runs at a 7 GHz clock. The true and complementary 8-bit PRBS outputs, having a 4 UI pulse width, drive the differential data path, in which a PAM-4/NRZ mode selector separates incoming 8-bit data into 4-bit MSB and 4-bit LSB. In the subsequent 1 UI data and eye-boosting pulse generator, the 8-bit data with the 4 UI pulse width is converted to the data with a 1 UI pulse width. In addition, the 1 UI eye-control pulse, which is the key signal to enhance the horizontal eye-opening, is also generated. The pulse generators use three adjacent clocks (CKR, CKD, and CKP in Figure 2) out of four quadrature phase clocks that are generated by an on-chip delay-locked loop (DLL) [21–23]; a quadrature error corrector (QEC) [24–26] is used to adjust the sampling phase to avoid setup time issues. The QEC, which is foreground-calibrated, is implemented using capacitor–DAC-based delay cells. The resulting 1 UI pulse width data and eye-control pulse drive the input of the segmented tail-less current-mode output drivers [6]. The outputs of eight drivers (4 MSB and 4 LSB segments) are combined for a 4-to-1 current-domain multiplexing at the output to relax the bandwidth requirement for each driver [7,9,27].

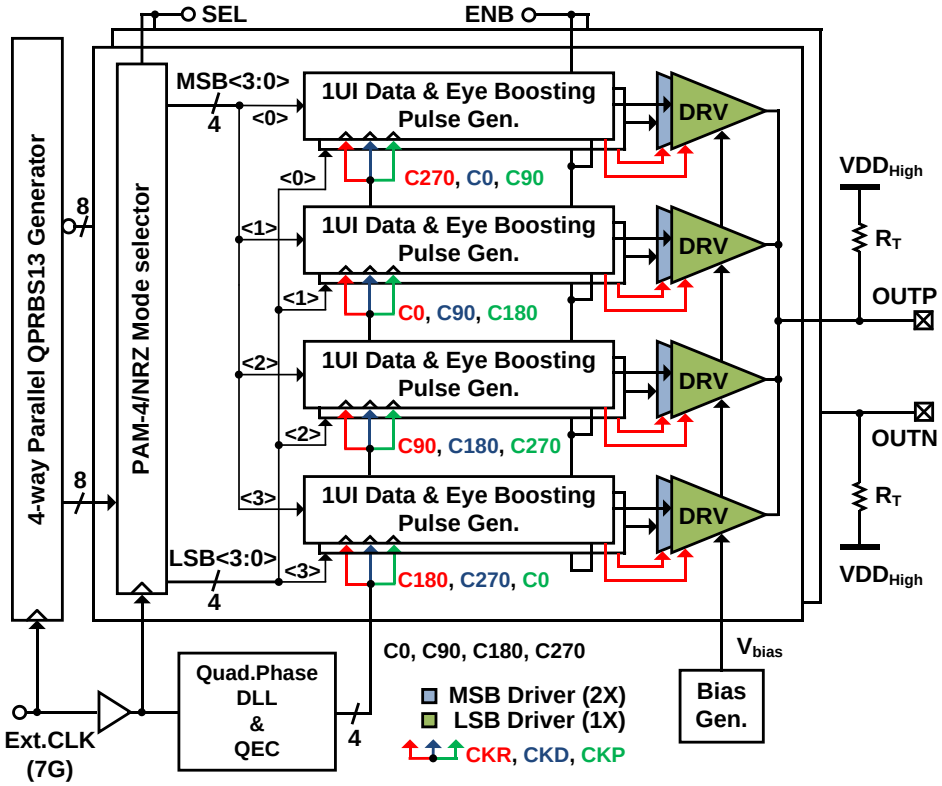

Figure 1. Overall architecture of the transmitter.

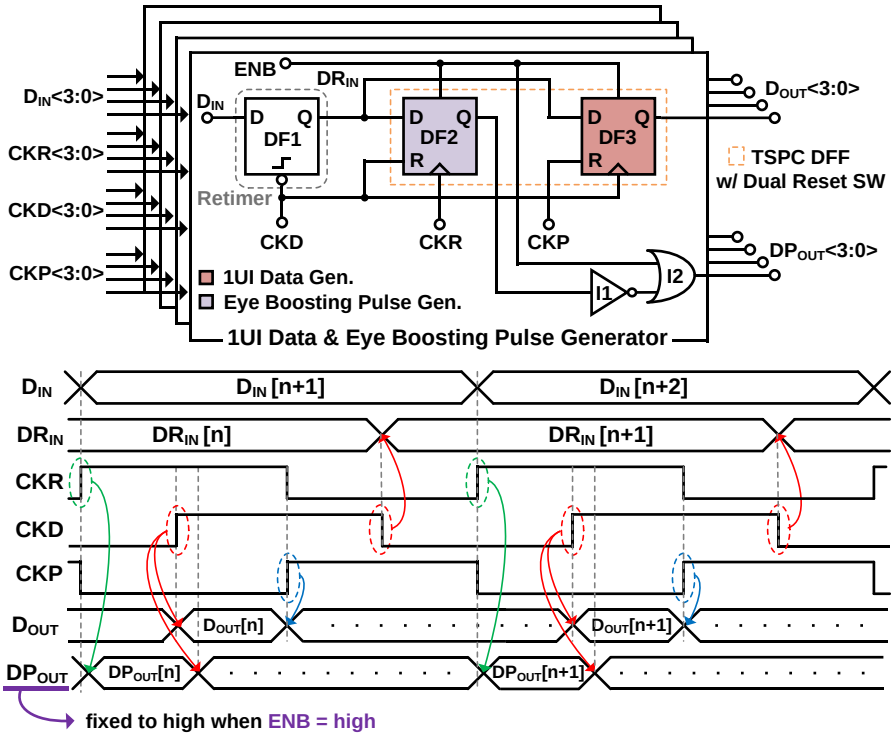

Figure 2. 1 UI data and eye-boosting pulse generator, along with its timing diagram.

The details of the 1 UI data and eye-boosting pulse generator are shown in Figure 2. The DF1 is a negative edge-triggered flip-flop [28] and uses CKD to sample D_{IN}, generating a time-shifted data DR_{IN}. DF2 and DF3 are custom-designed TSPC flip-flops with a programmable reset strength. The 1 UI pulse generating flip-flop, DF3, receives DR_{IN} as an input while using CKP, which is delayed by 1 UI compared to CKD, as the reset clock with which to create D_{OUT}, which has a 1 UI pulse width with a period of 4 UI. The eye-opening enhancement pulse, DP_{OUT}, is generated by DF2, which is clocked by CKR, which is 1 UI ahead of CKD, while the output of DF2 is flipped by an inverter I_1. Therefore, when the ENB signal is low, DP_{OUT} becomes a 1 UI-advanced and inverted replica of D_{OUT}, as shown in the timing diagram in Figure 2. The custom-designed TSPC flip-flop, shown in Figure 3, adopts a dual-strength reset switch scheme, where a faster reset of the QB node is enabled via an extra reset path consisting of M_2 and M_3 when the ENB is low. Figure 4 comparatively illustrates the operation of the horizontal eye-opening enhancement. Figure 4a illustrates the case when the ENB is high, where the additional reset switch in the pulse generator is not activated (grayed out) and the reset strength is nominal. The DP_{OUT} also remains high, because one input from the OR gate I2 is forced to be high. As a result, the auxiliary pull-up device MPX in the tail-less CML driver remains off-state. On the other hand, when the ENB is low, as shown in Figure 4b, the extra reset switch is engaged to speed up the reset. As a result, when D_{OUT} changes from high to low, the faster transition in D_{OUT} leads to the sharper rising edge of OUTN. In addition, when D_{OUT} changes from low to high, the DP_{OUT}, which is a 1 UI-advanced and inverted replica of D_{OUT}, turns on the auxiliary pull-up device, M_{PX}, to keep the Vx node at VDD temporarily, even after DOUT is high, resulting in a slight delay in the falling edge of OUTP. Consequently, the crossing of differential outputs, OUTP and OUTN, occurs when the transition of both signals is sharp, leading to a faster differential rise time. In contrast, when the ENB is high, the crossing of OUTP and OUTN is not properly aligned, resulting in a slower differential rise time. Compared to a single [1] or multi-stage [2] pulse generator for pre-charging the input data pulse at intermediate voltage, our technique does not use mid-level voltages for a faster rise time, thus it does not draw potential DC current in the pre-charge phase. The simulated differential output in the NRZ mode over the process corners, shown in Figure 5,

indicates that the proposed technique yields a considerable 10–90% rise time reduction in the differential output over various process corners (TT, FS, SF).

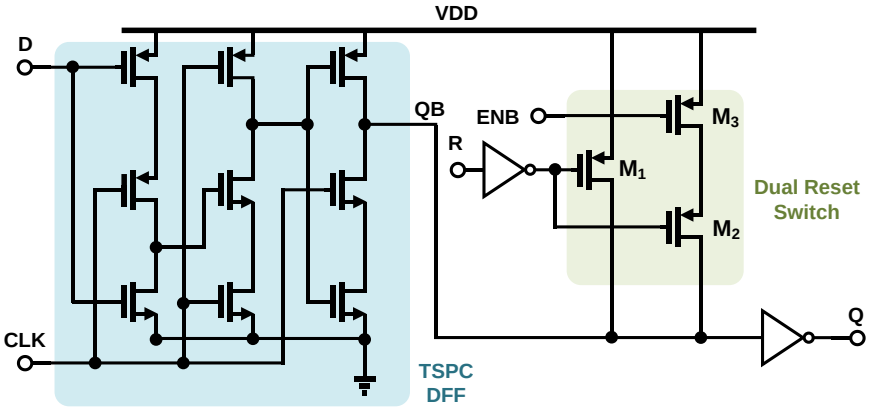

Figure 3. Schematic of TSPC flip-flop with programmable reset strength.

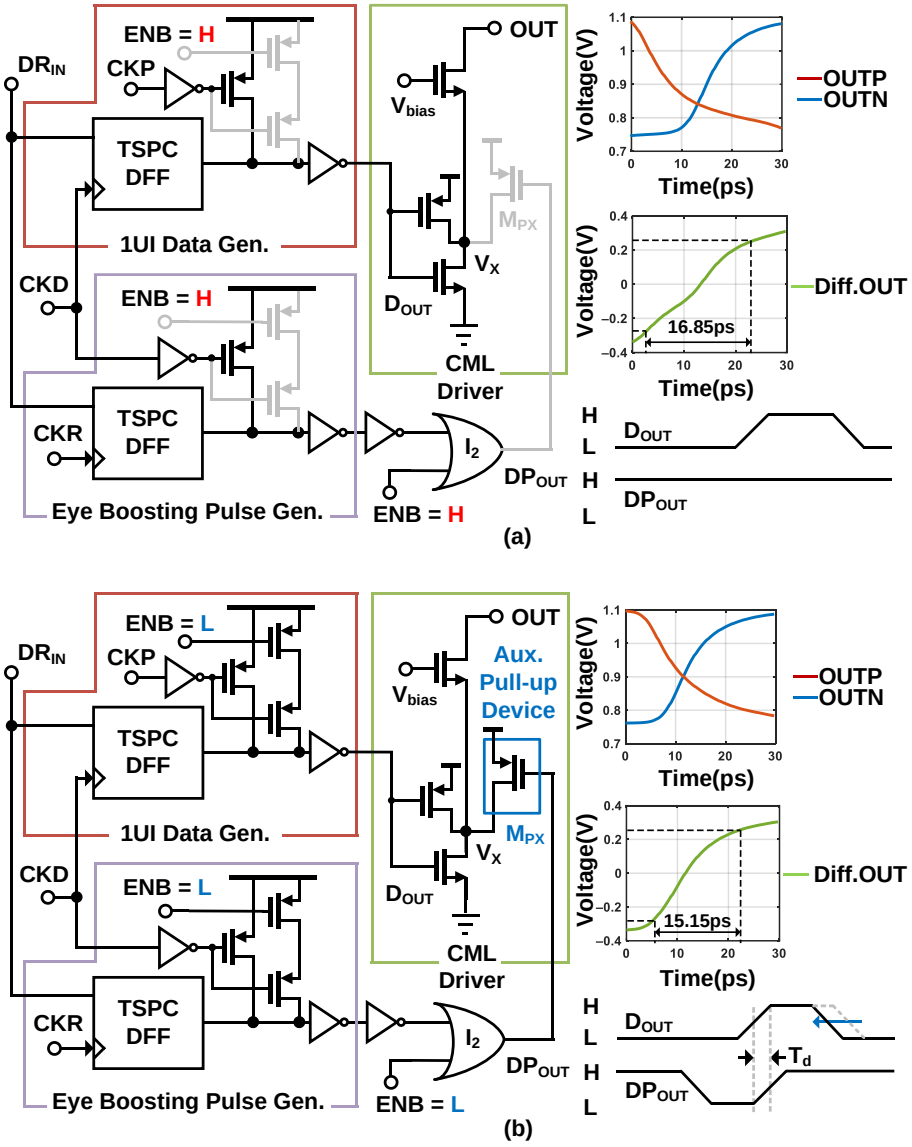

Figure 4. Configuration of the transmitter (half-circuit) when the eye enhancement is: (**a**) off; and (**b**) on.

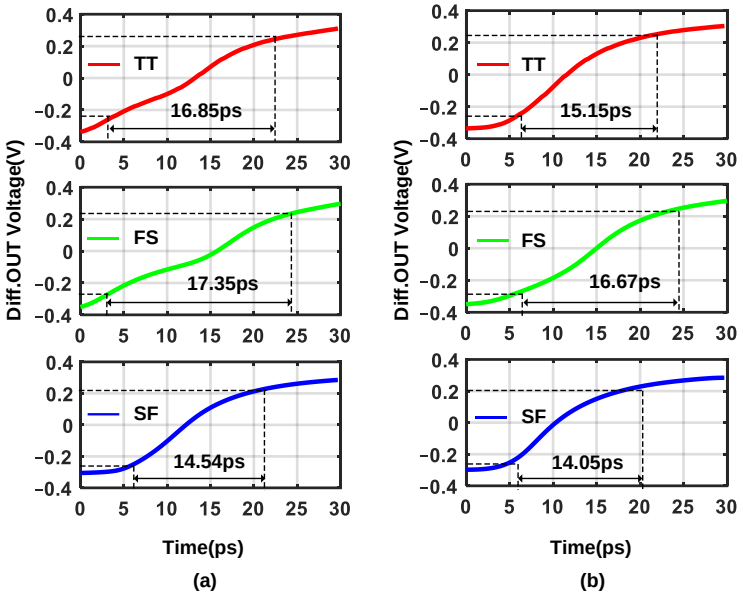

Figure 5. The simulated rise time of the transmitter output in NRZ mode at three corner cases (TT, SF, FS) when the eye enhancement is: (**a**) off; and (**b**) on.

3. Low-Power NRZ/PAM4 Dual-Mode Data Path

Figure 6 displays the details of the mode selector and data path of the transmitter for a dual-mode operation. The transmitter uses a shared differential data path for both NRZ/PAM-4 modes [29], allowing us to completely turn off the LSB data path to enable the power reduction in NRZ mode. The data path circuits, including the register-configurable mode selector, are implemented in CMOS logic to save power. In each mode selector, there are two groups of four active-low reset flip-flops, DFM and DFL, each corresponding to 4-bit wide MSB and LSB data paths. The reset signal of DFL is controlled by an external SEL signal while that of DFM is tied to VDD, so that DFM is never reset.

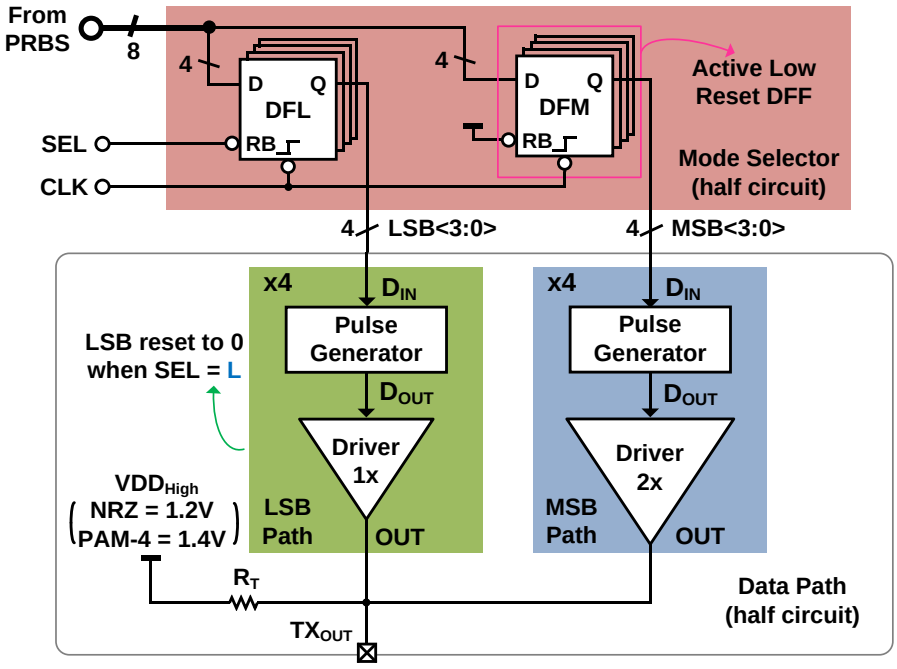

Figure 6. The mode selector and the differential data path for NRZ/PAM-4 dual-mode operation.

When the SEL is high, the transmitter operates in PAM-4 mode and both the MSB and LSB data are simply 1-clock delayed, yielding PAM-4 encoded output when properly combined at the output. In NRZ mode, the SEL is set at low, and the data are only encoded at the MSB path. Meanwhile, both the true and complementary LSB data paths are forced to be low by the DFL. As a result, the 1 UI pulse generator, and all subsequent digital gates in the LSB path, are not active at all and considerable power reduction is attained in NRZ mode.

4. Measurement Results

Figure 7a shows a die photograph of the transmitter. The design is fabricated in a 28-nm CMOS process and occupies an active area of 0.0344 mm^2. The power breakdown of the transmitter and the measurement setup are also shown in Figure 7b,c. In terms of energy efficiency, the PAM-4 and NRZ modes achieve 1.4 pJ/bit and 1.84 pJ/bit, respectively. When the clocking power is excluded, the power consumption in NRZ mode is reduced by 43% compared to the PAM-4 mode. In other words, the energy efficiency degrades by only 31%, which is considerably lower than the 100% degradation in prior works [4,5]. This improvement is mainly ascribed to the differential data path architecture with an option to completely disable the LSB path. Figure 8a shows a measured PAM-4 eye diagram with and without the eye-opening enhancement. When the eye enhancement is disabled, the measured worst-case eye height is 114.2 mV, and the eye width is 0.42 UI. When the enhancement is enabled, the eye widths of all three eyes are improved; the minimum eye width improves by 30% (0.42 UI → 0.55 UI). Figure 8b shows a measured NRZ eye diagram with and without the eye-opening enhancement. The horizontal eye-opening improves by 4% (0.87 UI → 0.9 UI). Note that the horizontal eye-opening improvement in NRZ mode is not as significant, which is expected, because the signal transitions between the binary level in NRZ mode do not cause a serious reduction in the horizontal eye.

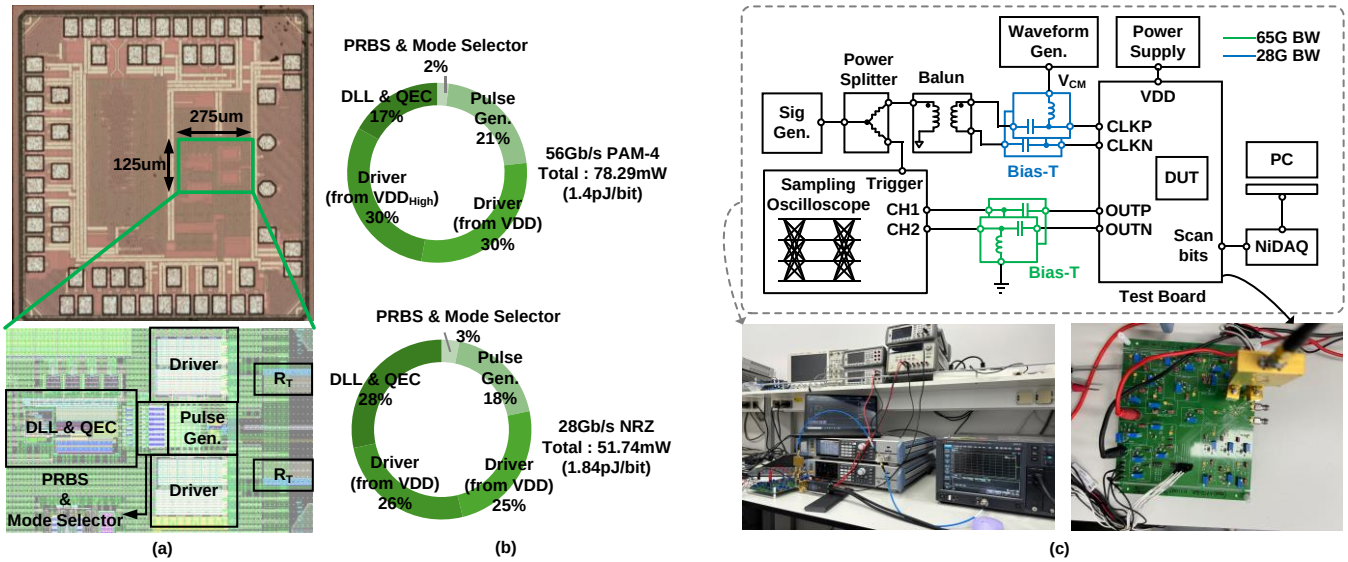

Figure 7. (**a**) Die photo; (**b**) power breakdown of the transmitter; and (**c**) measurement setup.

Table 1 summarizes the performance comparison of this work with recently publish-ed state-of-the-art technology. The proposed transmitter operates at 28 Gs/s symbol rate with NRZ/PAM-4 dual-mode, and the minimum horizontal eye-opening in the 56 Gb/s PAM-4 eye diagram is 0.55 UI, which is the largest when compared to that of the other technology. In addition, this transmitter achieves state-of-the-art power efficiency of 1.4 pJ/bit in PAM-4 mode and 1.84 pJ/bit in NRZ mode (clocking power included), respectively, by reducing unnecessary data path power dissipation for a dual-mode transmitter.

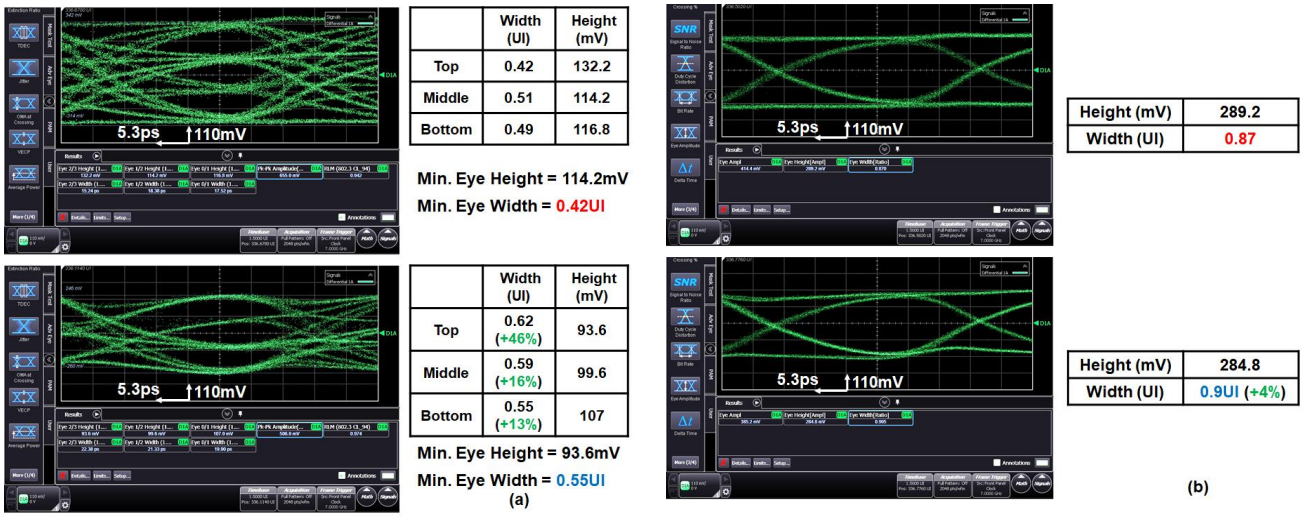

Figure 8. Measurement result of eye diagram when the eye enhancement is (**top**) off and (**bottom**) on: (**a**) at 56 Gb/s PAM-4; and (**b**) 28 Gb/s NRZ.

Table 1. Performance comparison (N/A = Not Applicable).

	This Work		**JSSC'19 [6]**	**ASSCC'20 [8]**	**ISSCC'23 [3]**	**CICC'24 [2]**	**JSSC'20 [4]**		**ISSCC'18 [5]**	
Data Rate (Gb/s)	56	28	64	50	128	128	128	64	112	56
Process (nm)	28		28 (FDSOI)	28	28	28	14		10	
Modulation	PAM-4	NRZ	PAM-4	PAM-4	PAM-4	PAM-4	PAM-4	NRZ	PAM-4	NRZ
Supply (V)	1.1/1.4	1/1.2	1	N/A	N/A	N/A	0.95/1.2		N/A	
Driver	Tail-less CML (w/Aux.device)		SST	CML	CML	Tail-less CML	Tail-less CML		CML	
RLM (%)	97	N/A	>96	>94	N/A	99	98.6	N/A	98.5	N/A
Area (mm^2)	0.0344		0.12	0.214	0.137	0.18	0.048		0.0302	
Efficiency (pJ/bit)	1.4	1.84	2.1	2.87	1.4 *	1.5	1.3	2.7	2.07	4.14
Efficiency (pJ/bit) (w/o clocking)	1.1	1.3	N/A	N/A	0.9	N/A	N/A		1.72 **	3.44 **
Min.Eye Width (UI)	0.56 (56 Gb/s)		0.45 (64 Gb/s)	0.22 (50 Gb/s)	0.18 (128 Gb/s)	0.34 (128Gb/s)	N/A		N/A	

* 4-phase clock generation power is excluded. ** clock distribution, DCC/QEC, local clock buffers are included.

5. Conclusions

This study presented a low-power NRZ/PAM-4 dual-mode transmitter using a tail-less current-mode driver with an eye-opening enhancement technique. Fabricated in 28 nm CMOS, the transmitter operates at 28 Gb/s in NRZ and 56 Gb/s in PAM-4 mode. An eye-width enhancement of up to 30% is achieved by the proposed technique, which can considerably relax the timing budget in PAM-4 links. We believe that the proposed horizontal eye-opening enhancement technique can be used in future research, such as in >100 Gbps transmitter designs or PAM-8 transmitter designs for more advanced processes with minimal modifications, given that circuit structures to enhance horizontal eye-opening are CMOS-compatible. In addition, thanks to the presented low-power data path design for the dual-mode transmitter, the power efficiency degrades by only 31% in NRZ mode. Because wireline transceivers in evolving data centers and communication infrastructures

must operate with backward compatibility, our low-power data path architecture for reducing NRZ-mode power will be crucial to improving the overall power efficiency of future high-speed links. In summary, this work achieves state-of-the-art energy efficiency in dual-mode operation with an average 25% eye-width enhancement, demonstrating the effectiveness of the proposed techniques.

Author Contributions: J.W. and J.K. proposed the architecture. J.W. designed the circuit and made all measurements. J.W. wrote the initial manuscript and J.K. supervised the manuscript. All authors have read and agreed to the published version of the manuscript.

Funding: This work was partly supported by an IITP grant funded by the Korea Government (MSIT) under 2022-0-01171, A Development of Intelligent PHY Interface for High-Speed PIM Data Transfer and National R&D Program through the National Research Foundation of Korea (NRF), funded by the Ministry of Science and ICT (2020M3H2A1078119).

Data Availability Statement: Data are contained within the article.

Acknowledgments: We thank IDEC, KAIST for the CAD tool support.

Conflicts of Interest: The authors declare no conflicts of interest.

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