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# Use of Threshold Median Adjustment to Achieve Accurate Current Balancing of Interleaved Buck Converter with Constant Frequency Hysteresis Control

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**Abstract:** This paper proposes a current balancing loop that is obtained using the threshold median adjustment (TMA-CBL) to achieve the accurate current balancing of an interleaved constant frequency hysteresis (CFH) buck converter. The CFH control is implemented with a frequency phase loop based on a threshold width adjustment (TWA-FPL). To ensure the loop's stability and minimize the steady-state error, a multi-phase, coupled, small-signal model (MPC-SSM) is derived with a consideration of the coupling effect among the multiple phases. Furthermore, the current balancing error is analyzed in detail, with a consideration of the sensing resistance deviations in the loop. Finally, based on a 180 nm BCD process, a four-phase interleaved buck converter is fabricated to verify the effectiveness of the proposed TMA-CBL. The maximum current balancing error is within 0.68% when the sensing resistors are deviated by 5%.

**Keywords:** threshold median adjustment; threshold width adjustment; constant frequency hysteresis; interleaved buck converter; multi-phase coupling effect

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## 1. Introduction

The demand for CPU power supplies continues to grow, necessitating power levels in the range of 100–200 W and slewing rates of ~A/ns [1,2]. In contrast, single-phase linear control buck converters typically achieve only ~A/μs and power levels below 10 W [3,4]. To meet these increasing demands, interleaved hysteresis control buck converters have been proposed [5,6], which significantly enhance the response speed and power output. However, two main challenges arise with this approach:

- The unpredictable switching frequency associated with conventional hysteresis control can lead to severe electromagnetic interference (EMI).
- Current imbalances among the phases reduce both the efficiency and lifespan of the system.

To maintain a constant switching frequency, periodic thresholds, like triangular waveforms or spike pulses, have been introduced into hysteresis control [7–10]. While these methods stabilize the frequency, they struggle to operate effectively over a broad range, potentially causing converter misconvergence. To address this limitation, phase-frequency-error-based methods have been developed to extend the switching frequency range [11–17]. These methods adjust the current-sensing slope, threshold width, or delay time based on the phase frequency error detected by a phase frequency detector (PFD), thereby regulating the switching frequency. However, implementing these constant frequency hysteresis (CFH) controls in interleaved buck converters remains challenging due to the absence of effective current balancing techniques in CFH controls.

The current balancing methods are typically categorized as either passive or active. Passive methods, including coupled inductors, temperature-dependent impedances, and

passive impedance matching techniques [18–21], generally lack precision. For improved accuracy, active methods regulate equivalent impedance through duty cycle adjustments [22]. In some approaches, a single current threshold adjustment loop controls the inductor current for balancing [23–25]. However, these active methods are not well suited for interleaved CFH buck converters due to the dynamic nature of threshold width adjustments, which can inadvertently alter the switching frequency and exacerbate EMI issues. There are two issues in the existing research: 1. conventional hysteresis control cannot maintain a constant switching frequency over a wide load range, and 2. interleaved CFH buck converters based on the phase frequency error lack an effective current-balancing technique. These problems highlight the significant gaps in the current research, particularly regarding current balancing and maintaining a constant switching frequency in interleaved CFH buck converters.

To realize current balancing and CFH for interleaved buck converters, this paper proposes a frequency phase loop based on the threshold width adjustment (TWA-FPL), and a current-balancing loop based on the threshold median adjustment (TMA-CBL), as shown in Figure 1. The threshold width of the CFH buck converter is regulated by the PFD to maintain a constant switching frequency, while the threshold median is adjusted to achieve current balancing. To realize the threshold median adjustment, in each phase, a current-sensing resistor $R_S$ and a capacitor $C_S$ convert the inductor current per phase $i_L$ into the sensing voltage $v_S$. Then, the sensing voltages of all the phases are averaged as the reference voltage $v_{CSB}$ by resistor $R_B$, which is proportional to the average inductor current for all the phases. Finally, the threshold median $v_{TM}$ of the hysteresis comparator is adjusted by the error between $v_S$ and $v_{CSB}$.

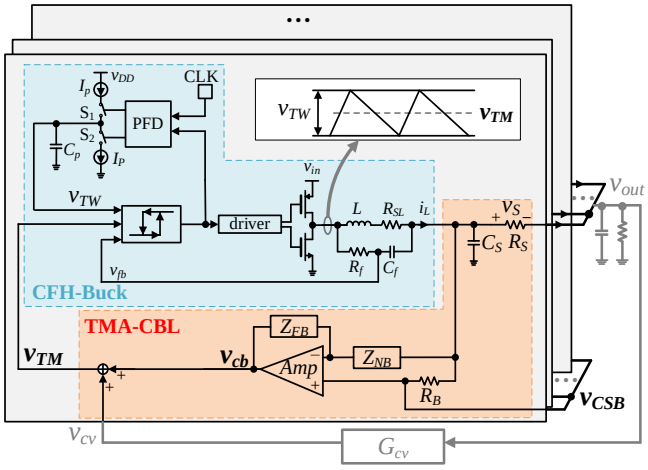


**Figure 1.** The proposed interleaved CFH buck converter with TMA-CBL.

The rest of this paper is organized as follows. In Section 2, the hysteresis comparator in the TWA-FPL is linearized so as to calculate the transfer function of the FPL. In Section 3, the TMA-CBL is proposed to realize current balancing for the interleaved CFH buck converter. Furthermore, the MPC-SSM is derived with a consideration of the coupling effect among the multiple phases. Section 4 presents the detailed circuit design of the control chip. Section 5 shows the layout and simulation results. Section 6 shows the prototype and experimental results. Section 7 concludes this paper. The abbreviations covered in this paper are listed at the last of the main text.

## 2. Linearization of Hysteresis Comparator in Threshold Width Adjustment-Based Frequency Phase Loop

To construct a model for the TWA-FPL, it is necessary to analyze the composition of the TWA-FPL, which is composed of a PFD, a charge pump (CP), and a hysteresis comparator, as shown in Figure 2. The PFD detects the phase error between the driving signal and the external clock, and the CP converts the phase error into the voltage $v_{TW}$. $v_{TW}$, as half of

the threshold width, is introduced into the hysteresis comparison. The RC network, at the output of the CP, is used to compensate the TWA-FPL.

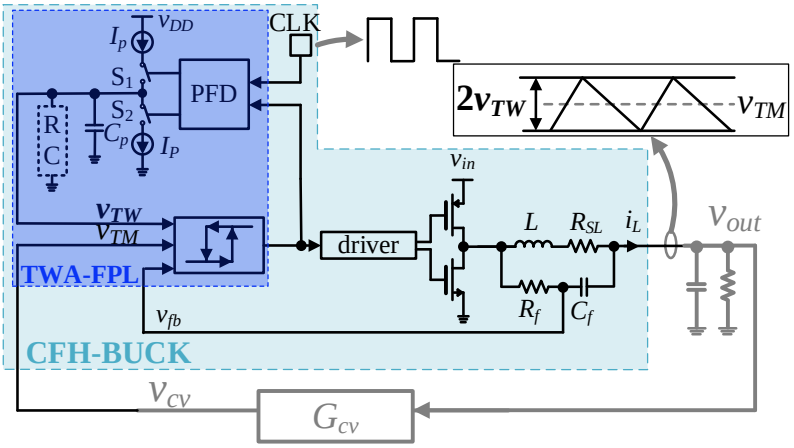


**Figure 2.** CFH buck converter based on the TWA-FPL.

According to Figure 2, the small-signal model of the TWA-FPL is shown in Figure 3. In Figure 3, $\varphi_{clk}$ and $\varphi_d$ are the clock phase and driving signal phase, respectively. $G_{cfp}$ is the transfer function of the RC compensator. $F_{\varphi v}$ is the transfer function of the hysteresis comparator, which is difficult to derive due to its non-linear behavior.

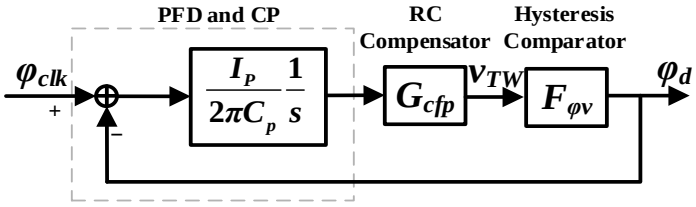


**Figure 3.** Small-signal model of the TWA-FPL.

For the transfer function of the hysteresis comparator, its calculation should consider the driving signal phase response when the threshold width steps, as shown in Figure 4. The threshold width is adjusted so that the driving signal is in the same frequency and phase as the external clock. The left part of Figure 4 shows the relationship between the variation in the threshold width and the phase variation, and the specific transfer function is derived below. After one switching cycle, the increment of the time delay is given by

$$T = \frac{2\Delta v_{TW} v_{in}}{(v_{in} - v_{out}) v_{out}} R_f C_f \tag{1}$$

where $\Delta v_{TW}$ is the step amplitude of the threshold width. $v_{in}$ and $v_{out}$ are the input voltage and the output voltage. $R_f$ and $C_f$ are the feedback resistor and the capacitor.

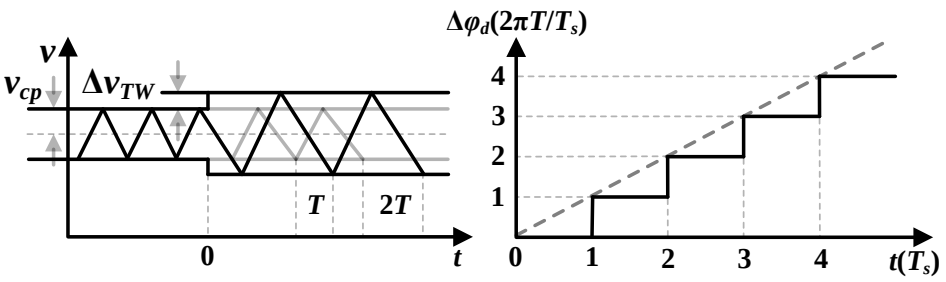


**Figure 4.** Phase response of the driving signal to changes in the threshold width.

Furthermore, according to (1), the linear approximation of the driving signal's phase variation is given by

$$\Delta\varphi_d(t) = 2\pi\frac{T}{T_s}t\frac{1}{T_s} = 2\pi\frac{2\Delta v_{TW}v_{in}}{(v_{in}-v_{out})v_{out}}\frac{R_fC_f}{T_s^2}t \tag{2}$$

where $T_s$ is the switching period.

Therefore, based on (2), the transfer function of the hysteresis comparison is given by

$$F_{\varphi v}(s) = \frac{\varphi_d(s)}{v_{TW}(s)} = 4\pi\frac{v_{in}}{(v_{in}-v_{out})v_{out}}\frac{R_fC_f}{T_s^2}\frac{1}{s} \tag{3}$$

According to Figure 3, the loop gain of the TWA-FPL is given by

$$T_{fp} = 2\frac{G_{cfp}I_pv_{in}R_fC_f}{C_p(v_{in}-v_{out})T_s^2s^2} \tag{4}$$

The bode plot of the TWA-FPL's loop gain is shown in Figure 5a. The system is unstable due to the loop gain having two poles at the origin. According to the compensation method of phase-locked loops, the loop needs to place a pole and a zero:

- As shown in Figure 5b, a zero is placed before the crossing frequency so that there is sufficient phase margin at the bandwidth and it is crossed with a slope of −20 dB/dec. When the phase margin is 60°, this pole is $\omega_z = \sqrt{\frac{4}{3}\frac{I_pv_{in}R_fC_f}{C_p(v_{in}-v_{out})v_{out}T_s^2}}$.
- As shown in Figure 5c, based on Figure 5b, a pole needs to be placed at $\omega_p = 2\pi f_s/10$ in order to suppress the switching frequency ripple.

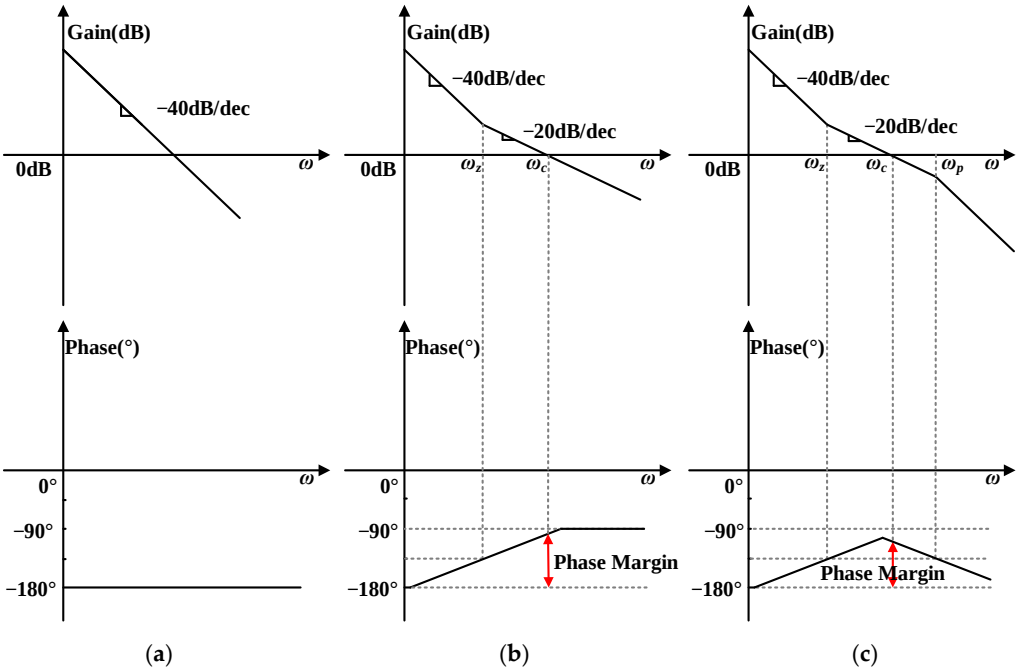


**Figure 5.** Bode plots of TWA-FPL's loop gain: (**a**) uncompensated, (**b**) with one zero compensation, and (**c**) with one pole and one zero compensation.

## 3. Multi-Phase Coupled Small Signal Model Analysis for Steady-State Accuracy and Loop Stability

To minimize steady-state error and ensure loop stability of the TMA-CBL, MPC-SSM and the loop gain of the TMA-CBL are derived. According to the loop gain, a compensator is designed to achieve a high DC loop gain and sufficient phase margin.

### *3.1. Multi-Phase Coupled Small Signal Model Analysis*

To analyze the stability of the current balancing loop, an MPC-SSM is derived considering the coupling effect among multiple phases, as shown in Figure 6. Each phase is constructed with a power stage (from the duty cycle to the inductor current), a hysteresis comparator (from the feedback voltage and the threshold median to the duty cycle), a feedback network (from the inductor current to the feedback voltage) and a TMA-CBL (from the error voltage to the threshold median). All phases are coupled by a shared voltage control loop. In order to analyze the dynamic response of a current imbalance step, a current imbalance disturbance $\hat{\imath}$ is introduced into the first phase. The Kth phase represents the phase that maintains the current balancing, i.e., K $\neq$ 1.

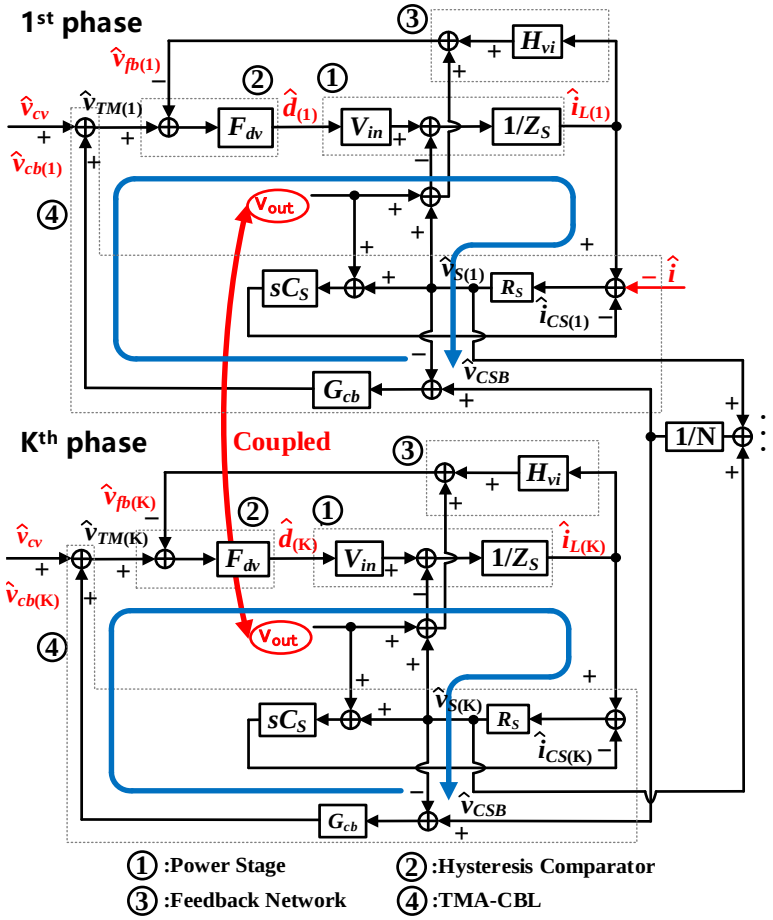


**Figure 6.** Multi-phase coupled small-signal model considering the coupling effect among multiple phases.

In Figure 6, $Z_S$ describes the impedance of the power stage. $H_{vi}$ describes the transfer function of the feedback network. $F_{dv}$ describes the transfer function of the hysteresis comparator. $Z_S$, $H_{vi}$ and $F_{dv}$ are given by

$$\begin{cases} Z_S = \frac{(sL+R_{SL})(R_f+1/sC_f)}{sL+R_{SL}+R_f+1/sC_f} \\ H_{vi} = \frac{sL+R_{SL}}{s^2LC_f+s(R_{SL}+R_f)C_f+1} \\ F_{dv} = \frac{2L}{v_{in}T_SH_{vi}} \end{cases} \tag{5}$$

where $L$ is the inductance value; $R_{SL}$ is the parasitic resistance of the inductor; $R_f$ is the feedback resistance value; $C_f$ is the feedback capacitance value. All these parameters are labeled in Figure 1. $v_{in}$ is the input voltage and $T_s$ is the switching period.

According to Figure 6, small signals of the inductor current $\hat{i}_L$, feedback voltage $\hat{v}_{fb}$, capacitor current $\hat{i}_{CS}$, and output of the TMA-CBL $\hat{v}_{cb}$ are the same expressions for the first and Kth phase, as given by $\hat{v}_S$

$$\begin{cases} \hat{i}_L = \left[\left(\hat{v}_{cv} + \hat{v}_{cb} - \hat{v}_{fb}\right)F_{dv}V_{in} - \left(\hat{v}_S + \hat{v}_{out}\right)\right]/Z_S \\ \hat{v}_{fb} = \hat{i}_L H_{vi} + \hat{v}_S + \hat{v}_{out} \\ \hat{i}_{CS} = sC_S(\hat{v}_S + \hat{v}_{out}) \\ \hat{v}_{cb} = G_{cb}(\hat{v}_{CSB} - \hat{v}_S) \end{cases} \tag{6}$$

where $\hat{v}_S$, $\hat{v}_{cb}$ and $\hat{v}_{out}$ are small signals for sensing the resistor voltage, the output of the voltage control loop and the output voltage. $G_{cb}$ is the compensator transfer function of the TMA-CBL.

The sensing resistor voltages are different expressions for the first and Kth phase. Small signals of the sensing resistor voltage and the reference voltage are given by

$$\begin{cases} \hat{v}_{S(1)} = \left(\hat{i}_{L(1)} - \hat{i}_{CS(1)} - \hat{i}\right)R_S, \hat{v}_{S(\mathrm{K})} = \left(\hat{i}_{L(\mathrm{K})} - \hat{i}_{CS(\mathrm{K})}\right)R_S \\ \hat{v}_{CSB} = \frac{\left(\sum_{\mathrm{K}=2}^{N}\hat{v}_{S(\mathrm{K})} + \hat{v}_{S(1)}\right)}{N} \end{cases} \tag{7}$$

where $N$ is the total phase number.

According to Figure 6, small signals of the output voltage and the output of the voltage control loop are expressed as

$$\begin{cases} \hat{v}_{out} = Z_O\left[\sum_{\mathrm{K}=2}^{N}\left(\hat{i}_{L(\mathrm{K})} - \hat{i}_{CS(\mathrm{K})}\right) + \hat{i}_{L(1)} - \hat{i}_{CS(1)} - \hat{i}\right] \\ \hat{v}_{cv} = -G_{cv}\hat{v}_{out} \\ Z_O = \dfrac{R_L}{sR_LC + 1} \end{cases} \tag{8}$$

where $R_L$ and $C$ are the output resistance and the capacitance value.

### *3.2. Loop Compensation of the TMA-CBL*

Furthermore, a compensator is designed based on the derived MPC-SSM. Combining (5)–(8), small signals for inductor currents of the first and Kth phases ($\hat{i}_{L(1)}$ and $\hat{i}_{L(\mathrm{K})}$) are derived as (9). In (9), $G_{iv}$ describes the transfer function from the output voltage to the inductor current, which depends on $G_{cv}$ and $G_{cb}$. $G_{il}$ describes the transfer function from the current disturbance to the inductor current, which depends on $G_{cb}$. $G_{vl}$ describes the transfer function from the current disturbance to the output voltage, which depends on $G_{cv}$.

$$\begin{cases} \hat{i}_{L(1)} = \hat{v}_{out}G_{iv} + \hat{i}G_{il}, \hat{i}_{L(\mathrm{K})} = \hat{v}_{out}G_{iv}, \hat{v}_{out} = \hat{i}G_{vl} \\ G_{iv} = \frac{G_{cb}\left(\frac{R_S}{NZ_O}F_{dv}V_{in} + sR_SC_SF_{dv}V_{in}\right) - G_{cv}F_{dv}V_{in} - F_{dv}V_{in} - 1}{G_{cb}R_SF_{dv}V_{in} + Z_S + R_SF_{dv}V_{in} + H_{vi}F_{dv}V_{in} + R_S} \\ G_{il} = \frac{G_{cb}R_SF_{dv}V_{in} + R_SF_{dv}V_{in} + R_S}{G_{cb}R_SF_{dv}V_{in} + Z_S + R_SF_{dv}V_{in} + H_{vi}F_{dv}V_{in} + R_S} \\ G_{vl} = \frac{-Z_O(Z_S + H_{vi}F_{dv}V_{in})}{Z_S + R_SF_{dv}V_{in} + H_{vi}F_{dv}V_{in} + R_S + NZ_O(G_{cv}F_{dv}V_{in} + F_{dv}V_{in} + 1 + sC_SZ_S + sH_{vi}C_SF_{dv}V_{in})} \end{cases} \tag{9}$$

Therefore, from (9), the closed-loop transfer function of the first phase is derived as

$$G_{cl_b(1)} = \frac{\hat{i}_{L(1)}}{i} = G_{iv}G_{vl} + G_{il} \tag{10}$$

According to the relationship between the closed-loop transfer function and the loop gain, the loop gain is derived from (10), as given in (11).

$$T_{b(1)} = \frac{G_{cl_b(1)}}{1 + G_{cl_b(1)}} = \frac{G_{iv}G_{vl} + G_{il}}{1 - G_{iv}G_{vl} - G_{il}} \tag{11}$$

Based on (5) and (9)–(11), loop gain $T_{b(1)}$ depends on the circuit parameters ($L$, $R_{SL}$, $R_f$, $C_f$, $R_L$, $C$, $R_S$, $C_S$, $N$), and transfer functions of the voltage control loop and the TMA-CBL compensators ($G_{cv}$, $G_{cb}$). $G_{cv}$ is designed according to the small-signal model of the voltage control loop. Therefore, loop gain $T_{b(1)}$ is only improved by $G_{cb}$.

Substituting the circuit parameters and the transfer function of the voltage control loop compensator into (5) and (9)–(11), bode plots of loop gain $T_{b(1)}$ without and with compensation ($G_{cb}$ = 1 and $G_{cb} = K_b/s$) are shown in Figure 7. Without the compensation ($G_{cb}$ = 1), the low DC gain of the $T_{b(1)}$ causes large steady-state error. To reduce the current balancing error, a type-I compensator ($G_{cb} = K_b/s$) is adapted, which places a pole at the origin as a dominant pole to improve the DC gain. Furthermore, to achieve a sufficient phase margin, parameter $K_b$ satisfies

$$\begin{cases} A_v K_b \frac{1}{BW} \frac{1}{\sqrt{1+\left(\frac{BW}{\omega_{p0}}\right)^2}} = 1 \\ 180^\circ - 90^\circ - \arctan\frac{BW}{\omega_{p0}} = PM \end{cases} \tag{12}$$

where $A_v$ and $\omega_{p0}$ are the DC gain and the domain pole of $T_{b(1)}$ without the compensation, respectively. BW and PM are bandwidth and phase margin of $T_{b(1)}$ with the compensation. Therefore, from (12), if PM = 60°, parameter $K_b$ is selected as

$$K_b = \frac{2}{3}\frac{\omega_{p0}}{A_v} \tag{13}$$

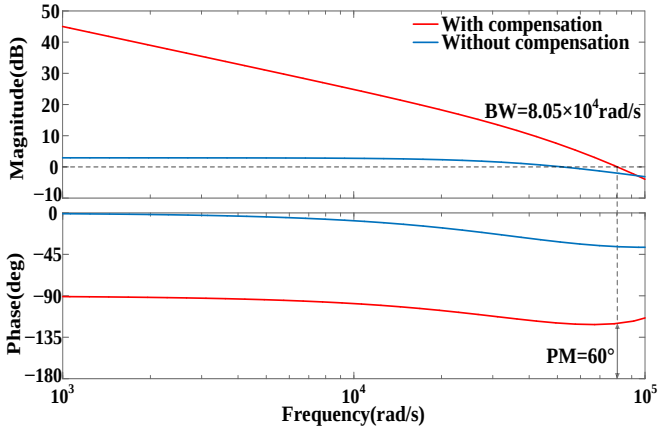


**Figure 7.** Bode plots of loop gain $T_{b(1)}$ without and with compensation.

## 4. Detailed Circuit Design

The proposed four-phase interleaved buck converter is shown in Figure 8. It consists of a bandgap and protect module, a soft-start module, a voltage control loop compensator and a four-single-phase buck converter, where a single-phase buck converter consists of a PFD, a CP, a deadtime generator, a driver, power switches, a threshold generator, a hysteresis comparator and a current balance loop. Input signals are $v_{ref}$, $v_{out}$, $v_{fb}$<1:4>,

CLK<1:4>, $V_{O_CS}$<1:4> and $V_{o_com}$, and output signals are $I_{out}$<1:4>, where $I_{out}$<1:4> are output currents of per phase, $V_{O_CS}$<1:4> are voltages converted by inductance current of per phase, and $V_{o_com}$ is voltage converted by average inductance current. To analyze the operating details, some critical module designs are discussed as follows.

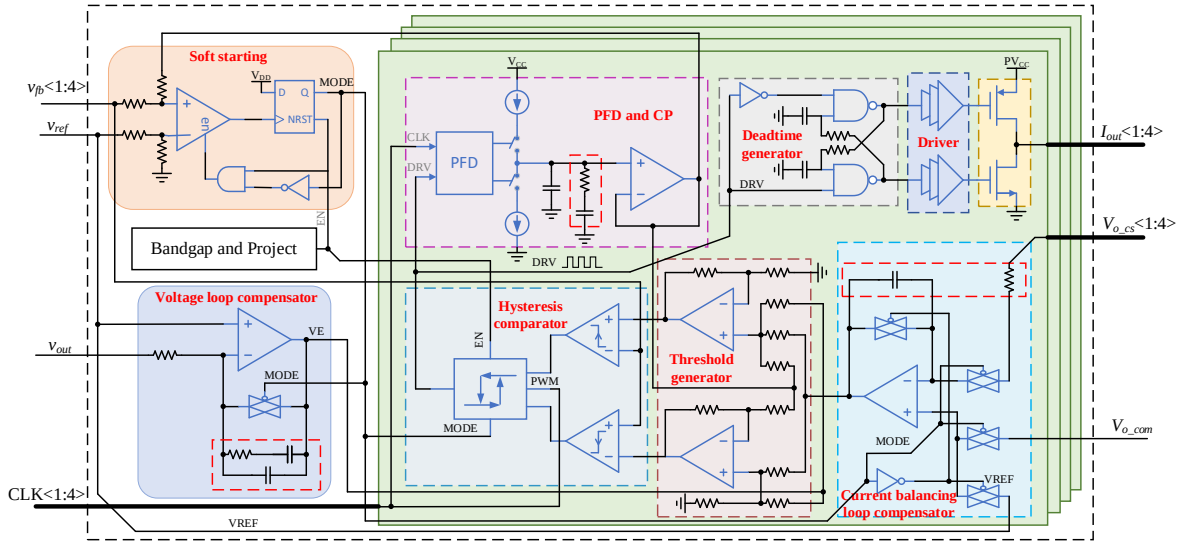


**Figure 8.** Schematic diagram of the four-phase interleaved CFH buck converter.

### *4.1. Soft-Starting Module*

The schematic diagram of the soft-starting module is shown in Figure 9. The input signals are $v_{fb}$, $v_{ref}$, $V_{CP}$, SYS_RDY and EN, and the output signal is MODE. When the feedback voltage $v_{fb}$ is larger than the low voltage threshold $v_{ref}$-$V_{CP}/5$, the output signal MODE flips to a high voltage level from a low voltage level. Afterward, the proposed converter starts to operate at the closed-loop control.

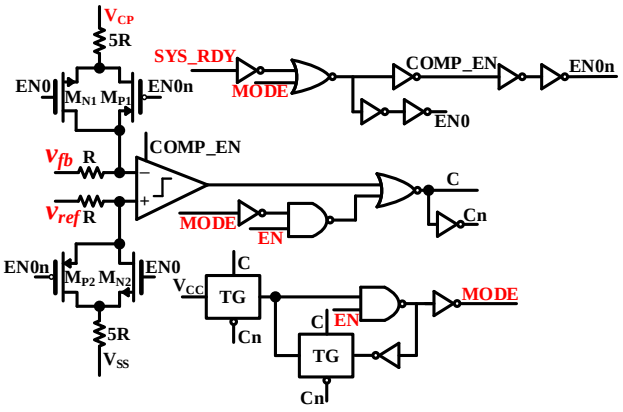


**Figure 9.** Schematic diagram of the soft-starting module.

EN is an active high enable signal for the converter starting. SYS_RDY is an active low enable signal for turning off the comparator and the resistor divider network to eliminate the bias current after soft-starting. The logic of the output signal MODE is in Figure 10. The soft-starting is classified into three stages:

- The converter is off (EN = 0): MODE and C are set to a low voltage level.
- The converter is on (EN = 1), and $v_{fb} < v_{ref}$-$V_{CP}/5$: MODE and C are set to a low voltage level.
- The converter is on (EN = 1), and $v_{fb} > v_{ref}$-$V_{CP}/5$: C flips to a high voltage level in a short time, and MODE flips to a high voltage level and latch, which indicates that the converter enters closed-loop control.

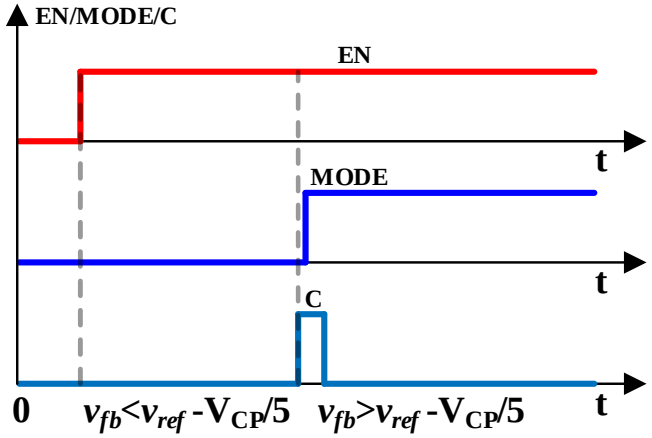


**Figure 10.** Main operating signal waveforms.

### *4.2. Phase Frequency Detector and Charge Pump*

The schematic diagram of the PFD is shown in Figure 11. Conventional PFD and CP are difficult to converge at the large frequency and phase errors. Therefore, the PFD and CP are improved:

- The proposed adjusting frequency circuit can reduce the frequency error quickly.
- The proposed CP can adjust the charge or discharge current to accelerate the regulating process.

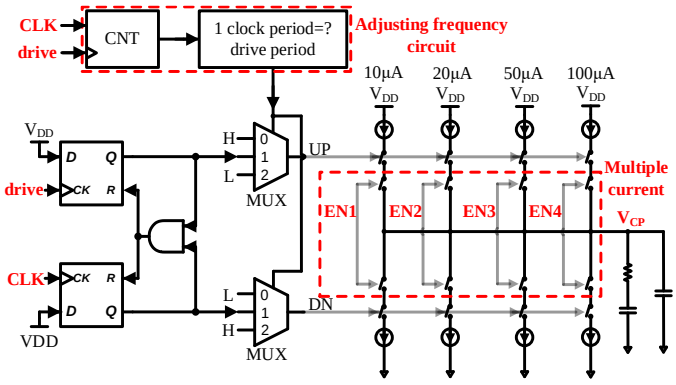


**Figure 11.** Schematic diagram of the improved PFD and CP.

According to Figure 11, the frequency error of the drive signal and the clock is reduced to 0.5$f_{CLK}$~$f_{CLK}$:

- $f_d > f_{CLK}$ (UP = 1, DN = 0): $V_{CP}$ rises to increase the switching frequency.
- $f_d < f_{CLK}$ (UP = 0, DN = 1): $V_{CP}$ falls to decrease the switching frequency. Then, the multiplexers select outputs of D flip-flops to reduce the phase error.

Finally, $V_{CP}$ is regulated to synchronize the driving signal with the clock.

### *4.3. Threshold Generator*

To generate the thresholds of the hysteresis comparator, the threshold generator should proportionally add or subtract outputs of the frequency phase loop, voltage loop and current balancing loop. Input signals are CSCMPI, CSCMPO, $v_{ref}$, $V_{o_com}$, $V_{o_cs}$, MODE, MODEN, $V_E$ and $V_{CP}$, and output signals are $V_{TH}$ and $V_{TL}$, where CSCMPI and CSCMPO are compensation networks of current balancing loop.

At the soft-starting period, outputs of the current balancing loop and the voltage control loop, follow the reference voltage by unit gain amplifiers, as shown in Figure 8.

According to Figure 12, when the proposed converter operates at the soft-starting period (MODE = 0 and MODEN = 1), $V_{TH}$ and $V_{TL}$ are given by

$$\begin{aligned} V_{TH} &= \frac{V_E}{2} + \frac{v_{ref}}{2} + \frac{V_{CP0}}{5} = v_{ref} + \frac{V_{CP0}}{5} \\ V_{TL} &= \frac{V_E}{2} + \frac{v_{ref}}{2} - \frac{V_{CP0}}{5} = v_{ref} - \frac{V_{CP0}}{5} \end{aligned} \tag{14}$$

where $V_{CP0}$ is the initial output voltage of the TWA-FPL.

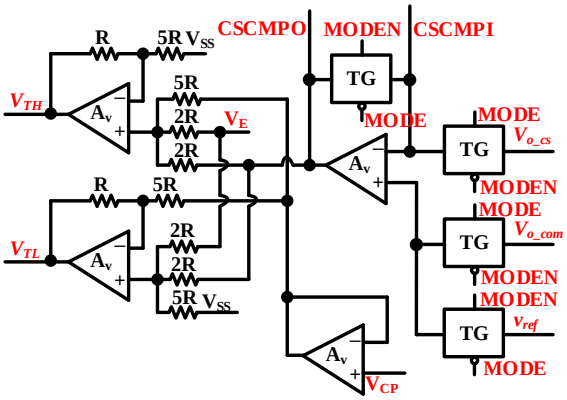


**Figure 12.** Schematic diagram of the threshold generator.

At the closed-loop control period, outputs of the current balancing loop and the voltage control loop are generated by the compensators. When the proposed converter operates at the closed-loop control period (MODE = 1 and MODEN = 0), $V_{TH}$ and $V_{TL}$ are given by

$$\begin{aligned} V_{TH} &= \underbrace{\tfrac{1}{2}G_{cv}(v_{ref} - v_{out})}_{V_E} + \tfrac{1}{2}G_{cb}(V_{o_com} - V_{o_cs}) + \underbrace{\tfrac{1}{5}G_{cfp}(\varphi_{clk} - \varphi_d)}_{V_{CP}} \\ V_{TL} &= \underbrace{\tfrac{1}{2}G_{cv}(v_{ref} - v_{out})}_{V_E} + \tfrac{1}{2}G_{cb}(V_{o_com} - V_{o_cs}) - \underbrace{\tfrac{1}{5}G_{cfp}(\varphi_{clk} - \varphi_d)}_{V_{CP}} \end{aligned} \tag{15}$$

Therefore, according to (15), the threshold median is determined by the voltage control loop and the current balancing loop, and the threshold width is determined by the frequency phase loop.

### *4.4. Hysteresis Comparator*

To reduce the comparing delay, two single-edge fast comparators and RS flip-flops are used. The hysteresis comparator is shown in Figure 13.

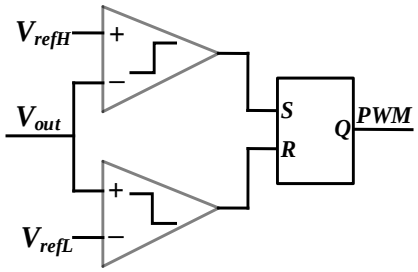


**Figure 13.** Hysteresis comparator implemented by two single-edge fast comparators.

The single-edge fast comparator is shown in Figure 14. $M_0$~$M_5$ constitute a dissymmetrical differential input structure. M1 regulates its current by the feedback voltage $v_{fb}$. $M_6$ copies the current of $M_1$, and $M_7$ copies $I_{bp}$. Furthermore, the current of $M_1$ is compared with $I_{bp}$ to obtain the output.

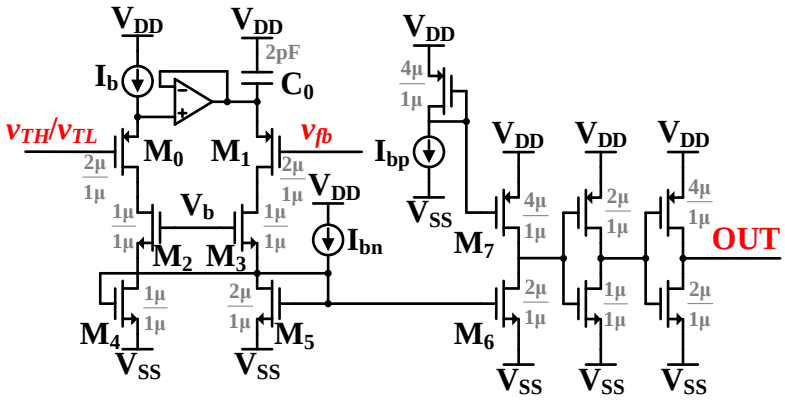


**Figure 14.** Schematic diagram of the single-edge fast comparator.

A high-speed single-edge comparator is the most important at the switching frequency above 10 MHz. The small comparing delay can improve the loop stability. The dominant pole is at the gate nodes of $M_5$ and $M_6$ due to the capacitor of the gate node. The capacitance of the gate node is enlarged because of the Miller effect of $M_6$. The dominant pole is approximated as

$$\omega_p \approx \frac{g_{m5}}{C_{GS5} + (1 - A_v)C_{GD6} + C_{GS6}} \tag{16}$$

where $A_V$ is the voltage gain generated by $M_6$. Obviously, reducing the amplitude of $A_v$ effectively increases the pole and reduces the comparing delay.

Although the single-edge comparator has the advantage of high speed, comparing accuracy is affected by the substrate bias effect, threshold voltages of transistors, temperature and so on. The compensating branch is constructed by $M_0$, $M_2$ and $M_4$, and the source voltage of $M_1$ follows $M_0$ by the unit gain amplifier. The compensating branch has a long signal path and larger delay due to the transmission delay of the unit gain amplifier, which causes the dissymmetrical comparing delay of the single-edge comparator. Therefore, the high-speed hysteresis comparator requires two single-edge comparators.

At the tt process corner, the rising rates of the input signal are 1000 V/µs and 100 V/µs, and the comparing delays are 878 ps and 2.4 ns, respectively. In addition, when the rising rate is 100 V/µs, the slew rate of the hysteresis comparator is 18,000 V/µs.

## 5. Layout and Simulation Results

A four-phase interleaved CFH buck converter is designed with HHGrace 180 nm BCD process, which occupies a 2.55 mm × 1.775 mm die area. The layout of the chip is shown in Figure 15. Cadence IC is used to perform transistor-level simulations using foundry-provided models. Current balancing error, soft-starting period, transient response and efficiency are evaluated in post-layout simulations.

Figure 16 shows current balancing errors at 1% and 5% sensing resistor deviations after TMA-CBL reaches a steady state. In Figure 16a, the sensing resistor deviation in the first phase is +1% and the sensing resistor deviations in the other phases are −1%. Its current balancing error is 0.48%. In Figure 16b, the sensing resistor deviation in the first phase is +5% and the sensing resistor deviations in the other phases are −5%. Its current balancing error is 0.68%.

The soft-starting is implemented by PWM with a gradually increasing duty cycle. The driving signals use external PWM signals from CLK<1:4>. When the feedback signal $v_{ref}$ rises to the low voltage threshold $v_{ref}$-$V_{CP}/5$, the soft-starting module changes the chip operating mode and closed-loop control starts operation, as shown in Figure 17. At the closed-loop control period, the current balancing loop and the voltage control loop compensate and generate the thresholds. Figure 17a shows the output voltage $v_{out}$, inductor currents $i_L$ and outputs of TMA-CBLs $v_{cb}$ in the transition period of TMA-CBL. After the output voltage achieves the steady state, TMA-CBL starts to work. Inductor currents are adjusted from

imbalance to balance. Figure 17b shows the output voltage $v_{out}$, the driving signal *DR* and the outputs $v_{TW}$ of TWA-FPLs in the transition period. After TWA-FPL starts to work, the frequency and phase of the driving signal are adjusted to synchronize with the external clock.

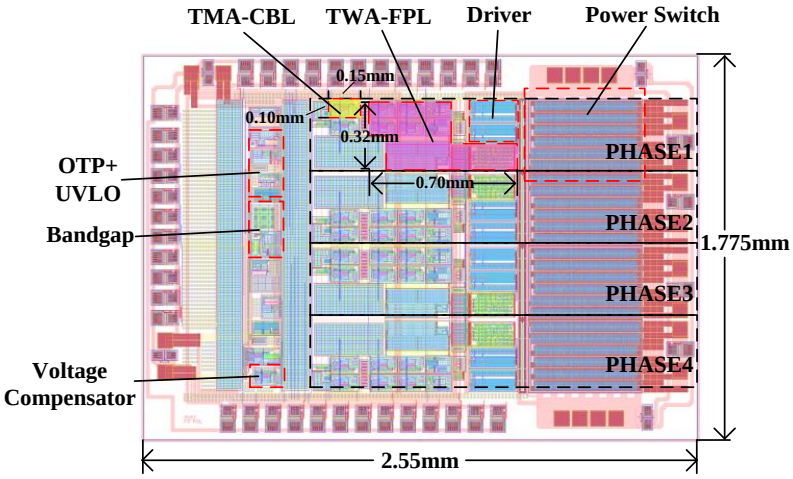


**Figure 15.** The layout of the four-phase interleaved CFH buck converter.

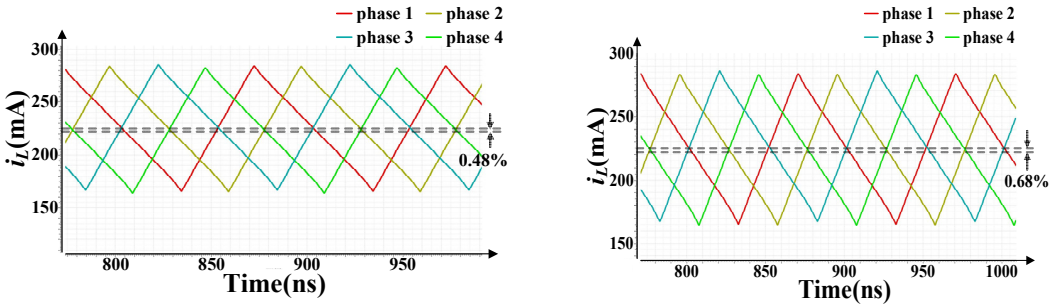


**Figure 16.** Current balancing errors at (**a**) 1% and (**b**) 5% sensing resistor deviations.

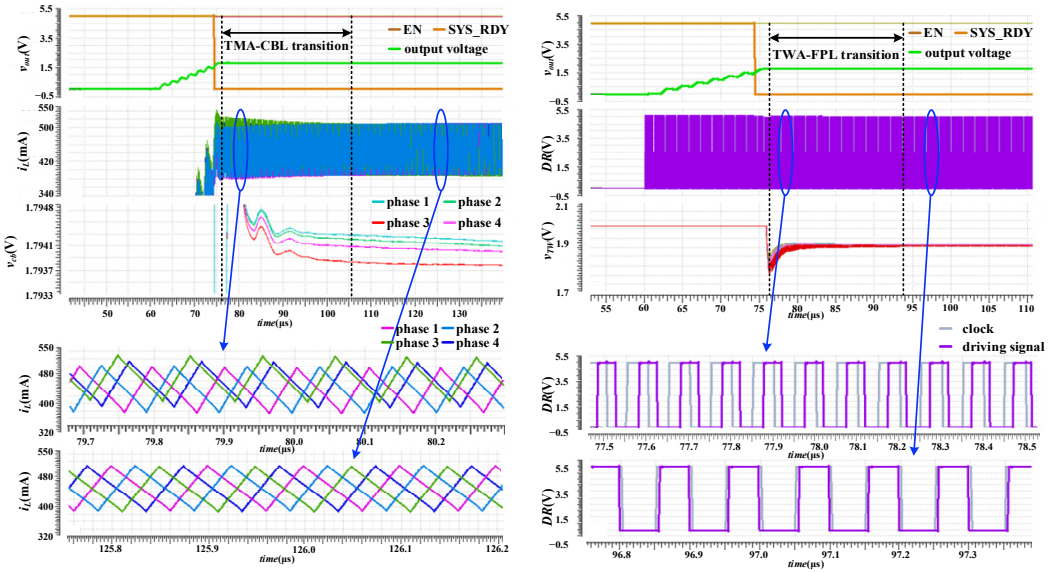


**Figure 17.** Regulating periods of (**a**) voltage and current balancing controls and (**b**) frequency phase loop.

## 6. Prototype and Experimental Results

Based on the above chip, the inductors and capacitors of each phase power stage, the resistors of the current balancing network, and the resistors and capacitors of each loop compensator are added to the peripheral circuits to design the test PCB of this chip; a photo of the prototype is shown in Figure 18.

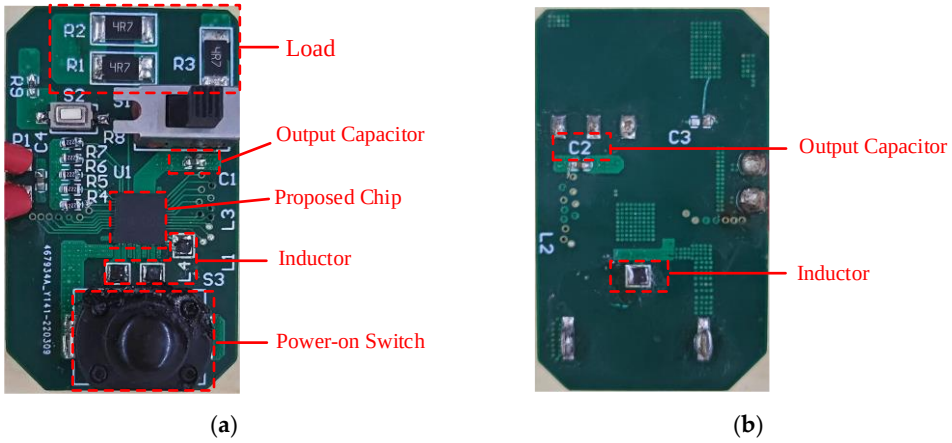


**Figure 18.** Prototype photo of the chip system (**a**) frontside (**b**) backside.

Figure 19 shows the bench setup for the prototype measurement, where the model number of the power supply is IT6720 (ITECH, Nanjing, China) and the model number of the oscilloscope is MDO3024 (TEKTRONIX, Shanghai, China).

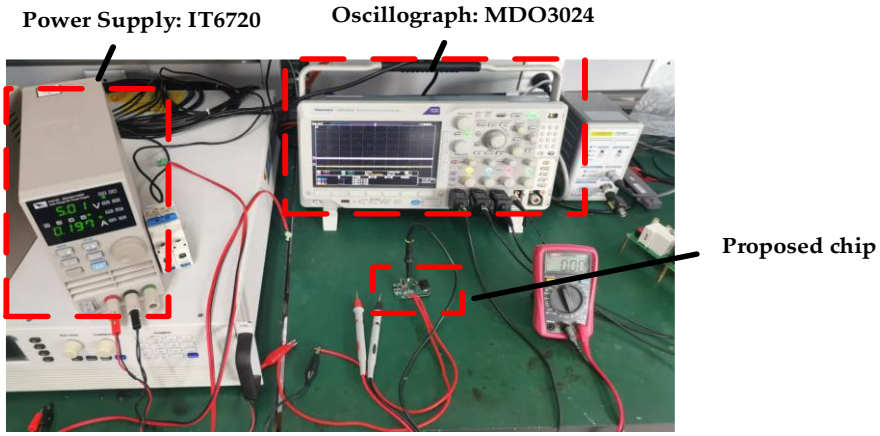


**Figure 19.** The bench setup for the prototype measurement.

Figure 20 shows the output voltage waveform when the output current steps. The output voltage overshoots are 374 mV and 370 mV when the output current steps from 0.89 A to 1.78 A and from 1.78 A to 0.89 A, respectively. Their response times are both 4.9 µs approximately.

Figure 21 shows efficiencies with output power at different switching frequencies and input voltages. The peak efficiency reaches 89.51% at 10 MHz switching frequency, 3.3 V input voltage and 1.8 V output voltage.

Table 1 shows a comparison of the proposed interleaved CFH buck converter with other CFH converters [15,16]. The power level of this work is twice that of [15]. The CFH buck proposed in this paper utilizes a multiphase interleaving technique and has a lower voltage ripple compared to [15,16]. In this paper, the parameter FOM is defined as

$$\text{FOM} = \frac{10^3}{8} \times \frac{(v_{in} - v_{out})(\text{V}) \times v_{out}(\text{V})}{L(\mu H) \times C(\mu F) \times \text{Voultage Ripple}(\text{mV}) \times f_{sw}^2(\text{MHz}^2) \times v_{in}(\text{V})} \quad (17)$$

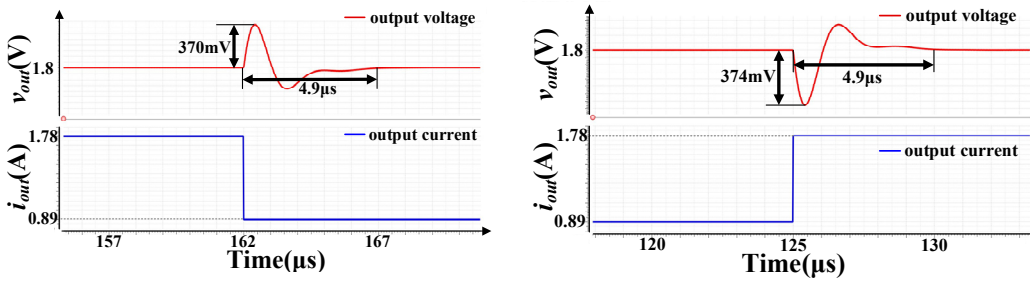


**Figure 20.** Output voltage waveform when the output current steps (**a**) from 0.89 A to 1.78 A and (**b**) from 1.78 A to 0.89 A.

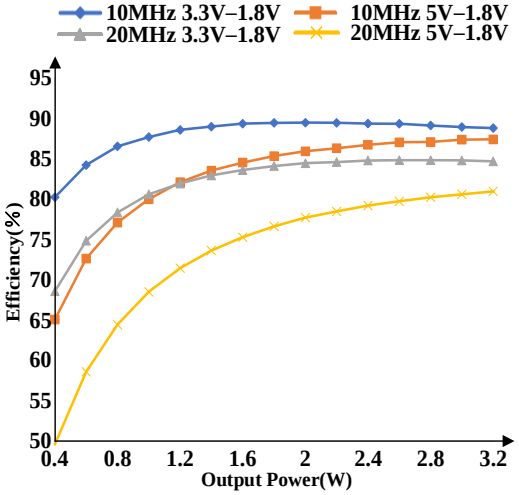


**Figure 21.** Efficiencies of the four-phase interleaved CFH buck converter.

**Table 1.** Performance comparison with the reported works.

| Publication | This Work | [15] | [16] | [22] | [26] |
|---|---|---|---|---|---|
| Technology | 180 nm BCD | 350 nm CMOS | 65 nm CMOS | 180 nm BCD | 130 nm BCD |
| Control Methods | Interleaved CFH | CFH | CFH | Current mode | Current mode |
| Balancing Method | Threshold Median Adjustment | × | × | Duty Cycle Adjustment | Single Threshold Adjustment |
| $f_{sw}$ × Phase | 10 MHz × 4 | 1 MHz | 1, 0.5, 0.25 MHz | 500 KHz × 4 | 2.25 MHz × 4 |
| Inductance ($L$) | 1 µH × 4 | 4.7 µH | 4.7 µH | × | 470 nH × 4 |
| Capacitance ($C$) | 100 nF × 5 | 10 µF | 10 µF | × | 88 µF |
| $v_{in}$ (V) | 3.3~5 | 3.3~3.6 | 2.7~3.3 | 12 | 2.8~5 |
| $v_{out}$ (V) | 1.6~2 | 0.9~2.5 | 1 | 1 | 0.68~1.92 |
| Load Range (W) | 0.4~3.2 | <1.5 | 0.02~0.15 | <12 | <7.68 |
| Peak Efficiency | 89.51% | 90% | 96.5% | × | 91.1% |
| Voltage Ripple (mV) | 0.2 | 59.289 | 32.5 | × | × |
| FOM | 3.6 | 0.0353 | 0.912 | × | × |
| Current Balancing Accuracy | <0.68% | × | × | 6.3% | <10.5% |

Voltage ripple is affected by switching frequency, input voltage, output voltage, inductance and capacitance values. FOM can exclude the influence of the above factors on the voltage ripple and can more fairly reflect the ability of the circuit itself to suppress

the voltage ripple. The FOM of this work is four times that of [16], which means better ripple suppression. Therefore, this work has significant advantages on the power level and voltage ripple. In addition, the circuit structure of TWA-FPL enables constant frequency control and solves the EMI problem.

In this paper, the current balancing among the phases is achieved by adjusting the median value of the threshold, which is named as TMA-CBL structure. Table 1 shows a comparison of TMA-CBL with other current balancing methods [22,26]. It can be seen that the accuracy of current balancing in this paper is much higher than theirs.

In summary, this work has significant advantages in voltage ripple, constant switching frequency and current balancing accuracy.

## 7. Conclusions

This paper proposes a TMA-CBL method for current balancing in interleaved CFH buck converters. An MPC-SSM model is established to ensure the loop stability of the converter, and the current balancing error is analyzed to verify the accuracy of the proposed TMA-CBL approach. With the implementation of the TMA-CBL, the current balancing error is reduced to below 0.68% even when the sensing resistors deviate by 5%. This effectively addresses the current balancing issue in interleaved buck converters in CFH controls, offering potential benefits in ripple reduction and power extension. However, this work primarily addresses steady-state performance, with limited analysis of transient response and dynamic behavior. Future research could focus on enhancing the method's effectiveness during transient conditions to ensure reliable performance in a wider range of operating scenarios.

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## Abbreviations

| | |
|---|---|
| CFH | constant frequency hysteresis |
| CP | charge pump |
| EMI | electromagnetic interference |
| MPC-SSM | multi-phase coupled small-signal model |
| PFD | phase frequency detector |
| TMA-CBL | current balancing loop that is obtained using the threshold median adjustment |
| TWA-FPL | frequency phase loop based on threshold width adjustment |

## References

1. Burton, E.A.; Schrom, G.; Paillet, F.; Douglas, J.; Lambert, W.J.; Radhakrishnan, K.; Hill, M.J. FIVR—Fully integrated voltage regulators on 4th generation Intel® Core™ SoCs. In Proceedings of the 2014 IEEE Applied Power Electronics Conference and Exposition—APEC 2014, Fort Worth, TX, USA, 16–20 March 2014; pp. 432–439.
2. Bharath, K.; Venkataraman, S. Power Delivery Design and Analysis of 14nm Multicore Server CPUs with Integrated Voltage Regulators. In Proceedings of the 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, USA, 31 May–3 June 2016; pp. 368–373.

3. Fukuoka, T.; Karasawa, Y.; Akiyama, T.; Oka, R.; Ishida, S.; Shirasawa, T.; Sonehara, M.; Sato, T.; Miyaji, K. An 86% Efficiency, 20MHz, 3D-Integrated Buck Converter with Magnetic Core Inductor Embedded in Interposer Fabricated by Epoxy/Magnetic-Filler Composite Build-Up Sheet. In Proceedings of the 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 17–21 March 2019; pp. 1561–1566.
4. Ain, Q.u.; Basim, M.; Shah, S.A.A.; Lee, K.Y. A Design of high-efficiency Constant On-Time Control DC-DC Buck Converter for Power Management integrated circuits. In Proceedings of the 2022 19th International SoC Design Conference (ISOCC), Gangneung-si, Republic of Korea, 19–22 October 2022; pp. 13–14.
5. Li, P.; Bashirullah, R.; Hazucha, P.; Karnik, T. A Delay Locked Loop Synchronization Scheme for High Frequency Multiphase Hysteretic DC-DC Converters. In Proceedings of the 2007 IEEE Symposium on VLSI Circuits, Kyoto, Japan, 14–16 June 2007; pp. 26–27.
6. Li, P.; Xue, L.; Hazucha, P.; Karnik, T.; Bashirullah, R. A Delay-Locked Loop Synchronization Scheme for High-Frequency Multiphase Hysteretic DC-DC Converters. *IEEE J. Solid-State Circuits* **2009**, *44*, 3131–3145. [CrossRef]
7. Song, M.K.; Dehghanpour, M.F.; Sankman, J.; Ma, D. A VHF-level fully integrated multi-phase switching converter using bond-wire inductors, on-chip decoupling capacitors and DLL phase synchronization. In Proceedings of the 2014 IEEE Applied Power Electronics Conference and Exposition—APEC 2014, Fort Worth, TX, USA, 16–20 March 2014; pp. 1422–1425.
8. Himmelstoss, F.A.; Votzi, H.L. Simple Chargers for a Small DC Micro-Grid for a Home Emergency Power System. *Electricity* **2023**, *4*, 216–234. [CrossRef]
9. Sturcken, N.; Petracca, M.; Warren, S.; Mantovani, P.; Carloni, L.P.; Peterchev, A.V.; Shepard, K.L. A Switched-Inductor Integrated Voltage Regulator with Nonlinear Feedback and Network-on-Chip Load in 45 nm SOI. *IEEE J. Solid-State Circuits* **2012**, *47*, 1935–1945. [CrossRef]
10. Lu, W.; Li, S.; Yang, Y.; Zhao, Z.; Iu, H.H.C. Constant-Frequency Capacitor Current Hysteresis Control of Buck Converter Using Reconstructed Ideal-Capacitor Voltage. *IEEE Trans. Ind. Electron.* **2019**, *66*, 7916–7926. [CrossRef]
11. Lu, W.; Wu, X.; Zhao, M.; Chen, M. Self-adaptive window control technique for hysteretic buck converter with constant frequency. In Proceedings of the 2012 IEEE International Conference on Electron Devices and Solid State Circuit (EDSSC), Bangkok, Thailand, 3–5 December 2012; pp. 1–2.
12. Kathiresan, A.C.; PandiaRajan, J.; Sivaprakash, A.; Sudhakar Babu, T.; Islam, M.R. An Adaptive Feed-Forward Phase Locked Loop for Grid Synchronization of Renewable Energy Systems under Wide Frequency Deviations. *Sustainability* **2020**, *12*, 7048. [CrossRef]
13. Huerta, S.C.C.; Alou, P.; Oliver, J.Á.; Garcia, O.; Cobos, J.A.; Abou-Alfotouh, A.M. Nonlinear Control for DC–DC Converters Based on Hysteresis of the $C_{OUT}$ Current with a Frequency Loop to Operate at Constant Frequency. *IEEE Trans. Ind. Electron.* **2011**, *58*, 1036–1043. [CrossRef]
14. Zheng, Y.; Chen, H.; Leung, K.N. A Fast-Response Pseudo-PWM Buck Converter With PLL-Based Hysteresis Control. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2012**, *20*, 1167–1174. [CrossRef]
15. Chen, J.J.; Hwang, Y.S.; Ku, Y.; Li, Y.H.; Chen, J.A. A Current-Mode-Hysteretic Buck Converter with Constant-Frequency-Controlled and New Active-Current-Sensing Techniques. *IEEE Trans. Power Electron.* **2021**, *36*, 3126–3134. [CrossRef]
16. Seo, J.I.; Lim, B.M.; Lee, S.G. A 96.5% Efficiency Current Mode Hysteretic Buck Converter With 1.2% Error Auto-Selectable Frequency Locking. *IEEE Trans. Power Electron.* **2018**, *33*, 7733–7743. [CrossRef]
17. Yang, H.-H.; Wu, H.; Zhang, A.-A.; Cao, X.-G. A high efficiency buck converter based on PLL for frequency stabilization. *Microelectron. J.* **2023**, *142*, 105987. [CrossRef]
18. Utz, S.; Pforr, J. Current-balancing controller requirements of automotive multi-phase converters with coupled inductors. In Proceedings of the 2012 IEEE Energy Conversion Congress and Exposition (ECCE), Raleigh, NC, USA, 15–20 September 2012; pp. 372–379.
19. Tran, M.T.; Thekkan, S.; Polat, H.; Tran, D.-D.; El Baghdadi, M.; Hegazy, O. Inductive Wireless Power Transfer Systems for Low-Voltage and High-Current Electric Mobility Applications: Review and Design Example. *Energies* **2023**, *16*, 2953. [CrossRef]
20. Bogdanovs, A.; Krievs, O.; Ribickis, L.; Pforr, J. Fuzzy Logic Current Balancing Controller Implementation in an Automotive Multi-Phase DC Converter with Coupled Inductors. In Proceedings of the 2020 IEEE 61th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON), Riga, Latvia, 5–7 November 2020; pp. 1–10.
21. Dou, Y.; Ouyang, Z.; Andersen, M.A.E. Integrated Coupled Inductors with Functionality of Current Balancing Transformer for Two-Phase Synchronous DC–DC Converters. *IEEE Trans. Power Electron.* **2020**, *35*, 4472–4476. [CrossRef]
22. Hu, K.Y.; Chen, Y.S.; Tsai, C.H. A Digital Multiphase Converter with Sensor-less Current and Thermal Balance Mechanism. In Proceedings of the 2018 IEEE Asian Solid-State Circuits Conference (A-SSCC), Tainan, Taiwan, 5–7 November 2018; pp. 175–178.
23. Jahanbakhshi, M.H.; Etezadinejad, M. Modeling and Current Balancing of Interleaved Buck Converter Using Single Current Sensor. In Proceedings of the 2019 27th Iranian Conference on Electrical Engineering (ICEE), Yazd, Iran, 30 April–2 May 2019; pp. 662–667.
24. Su, Y.P.; Chen, W.C.; Huang, Y.P.; Lee, Y.H.; Chen, K.H.; Luo, H.Y. Pseudo-Ramp Current Balance (PRCB) Technique With Offset Cancellation Control (OCC) in Dual-Phase DC-DC Buck Converter. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2014**, *22*, 2192–2205. [CrossRef]

25. Huang, W.; Qahouq, J.A.A. Input Voltage Ripple-Based Sensorless Current Sharing Autotuning Controller for Multiphase DC–DC Converters. *IEEE Trans. Ind. Appl.* **2016**, *52*, 4117–4125. [CrossRef]
26. Roh, Y.S.; Moon, Y.J.; Park, J.; Jeong, M.G.; Yoo, C. A Multiphase Synchronous Buck Converter with a Fully Integrated Current Balancing Scheme. *IEEE Trans. Power Electron.* **2015**, *30*, 5159–5169. [CrossRef]

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