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Study on Novel Schottky Contact Super Barrier Rectifier with Deep Isolated MOS Trench in Epitaxial N-Drift Layer

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Abstract: In this paper, a novel 120 V-class silicon Schottky contact super barrier rectifier with a deep isolated MOS trench in an epitaxial n-drift layer (DOT-SSBR) is studied through experiments, featuring the deep isolated MOS trenches (DOTs) in an epitaxial layer compared with conventional SSBR. The combination of SSBR and DOT obviously increase the breakdown voltage while preserving the significant advantages of SSBR. The pinching-off electric field effect by the DOTs in the epitaxial n-drift layer increases the average of electric field inside the drift layer and decreases the electric field on the mesa surface when the proposed DOT-SSBR is reversely biased. After the further optimization of the Schottky contact super barrier (SSB) parameters on mesa, the proposed DOT-SSBR maintains almost the same forward voltage, reduces the reverse leakage current at the reverse voltage of 50 V by approximately 10.0%, and greatly increases the breakdown voltage by approximately 38.6%, when compared with the conventional SSBR. The fabrication process, the measured high-temperature characteristics of forward I-V curves and reverse leakage current, and the measured reverse recovery current of the new device are also presented. An auxiliary simulation analysis to provide insight about the physics of the device is also presented.

Keywords: Schottky contact super barrier rectifier (SSBR); low forward voltage; high temperature; MOS trench; breakdown voltage; pinching-off electric field effect

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1. Introduction

Medium- and low-voltage silicon power semiconductor diodes are widely used in power conversion and power supply. A planar Schottky barrier diode (SBD) is commonly used as a rectifying device because of its low forward voltage and fast reverse recovery. However, its specific on-resistance and forward voltage increase sharply as the breakdown voltage increases. Similar to the concept of a pinching-off electric field by PN junction in junction barrier Schottky (JBS) [1], the trench MOS barrier Schottky (TMBS) [2] uses deep MOS trenches to pinch off the electric field, which not only reduces the mesa surface electric field, but also changes the electric field distribution in n-drift layer, and reduces the transverse depletion of PN junction in JBS. Therefore, it has a lower reverse leakage current, a higher breakdown voltage, and a smaller forward voltage. The TMBS technology has been widely developed due to its simple fabrication process and high performance; however, the high reverse leakage current, when operating at elevated temperatures, still remains due to the image force barrier lowering effect [3–6].

Recently, the concept of a silicon Schottky contact super barrier rectifier (SSBR) has been proposed and verified through simulation and experiments by our group [7], which shows good performances in simple manufacturing processes, low forward voltages, high-temperature stability and reasonable reverse leakage currents. With the coupling mechanism of Schottky contact barrier and super barrier, compared with conventional SBD, SSBR has two significant advantages in terms of electrical performance; one is the

low forward voltage, especially the ultra-low forward voltage under low current density, and the other is the high-temperature stability, especially the low leakage characteristic at high temperature. A comparison of the experimental results between the new SSBR and conventional SBD is given in detail.

However, all the presented SSBRs have a breakdown voltage of tens of volts. As the breakdown voltage increases, the forward voltage also increases sharply, because of the SSBR being a majority carrier device. Although the SSBR structure equipped with a p-injector plug has a bipolar conduction operation mechanism, this bipolar conduction only occurs under very high current density conditions. Under the condition of the conventional current density (near and below the rated condition), there is no bipolar conduction mechanism, and it is still a unipolar conduction.

As a solution to the above problems, by combining the concept of planar SSBR and the effect of the pinching-off electric field by deep MOS trenches [6], the aim of this paper is to demonstrate the experimental results of a novel 120 V-class silicon Schottky contact super barrier rectifier with a deep isolated MOS trench in an epitaxial n-drift layer (DOT-SSBR). An auxiliary simulation analysis will also be detailed. There are two considerations for using deep isolated MOS trench (DOT) instead of conventional deep MOS trench in the proposed DOT-SSBR. On the one hand, DOT can bring faster reverse recovery characteristics while maintaining the pinching-off electric field effect after replacing the conventional deep MOS trench, and on the other hand, the fabrication process is simple and compatible, which will be discussed in next section.

2. Device Structures, Fabrication Process and Operation Mechanism

The Scanning Electron Microscope (SEM) cross-section of the fabricated DOT-SSBR is illustrated in Figure 1. Compared with the conventional SSBR, the deep isolated MOS trenches (DOTs) are formed in the epitaxial n-drift layer for DOT-SSBR, and there are two cells of Schottky contact super barrier (SSB) are formed on the mesa between two adjacent DOTs. The key design parameters used in manufacturing are shown in Table 1.

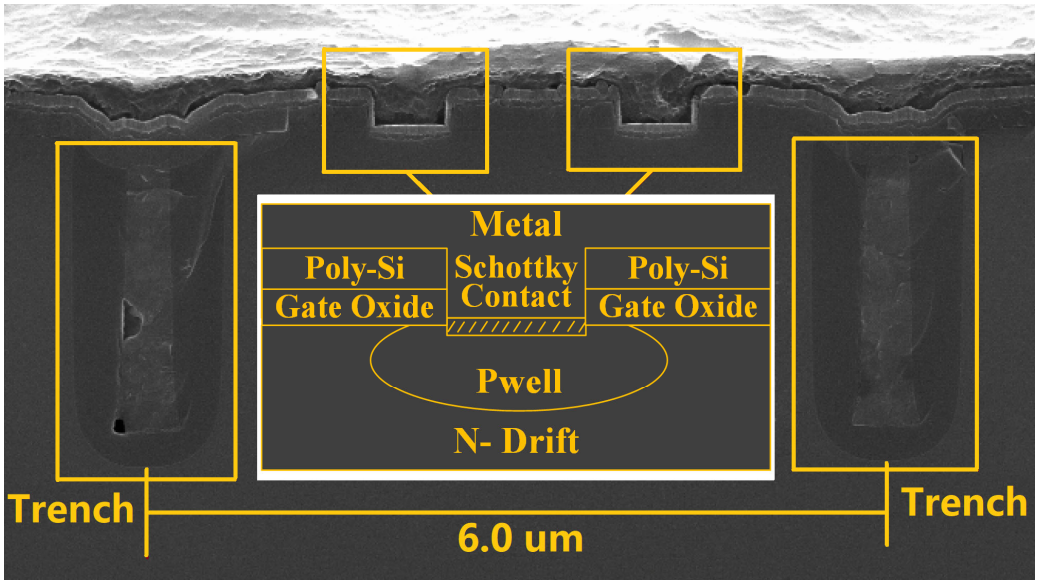

Figure 1. SEM cross-section of the fabricated DOT-SSBR.

The key steps of the fabrication process are shown in Figure 2. The process began with a silicon epitaxial wafer, which is a phosphorus-doped epitaxial layer on the arsenic-doped N^+ substrate. Both the DOT-SSBR and SSBR have the same epitaxial layer parameters (thickness, Td, and resistance of epitaxial layer, Rd) as illustrated in Table 1.

Table 1. Key design parameters for DOT-SSBR and SSBR.

Symbol	Parameter	DOT-SSBR	SSBR
Td	Thickness of epitaxial layer	9 μm	9 μm
Rd	Resistance of epitaxial layer	1.7 Ω·cm	1.7 Ω·cm
Dt	Depth of deep trench	2.6 μm	---
Wt	Width of deep trench	1.2 μm	---
Tg	Gate oxide thickness of SSB	9 nm	9 nm
Tp	Pwell implantation depth	0.25 μm	0.25 μm
Dp	Pwell implantation dose	10^{13}–10^{15} cm^{-2}	10^{13}–10^{15} cm^{-2}
Lc	Width of contact in SSB	0.6 μm	0.6 μm
Lo	Width of gate in SSB	1.4 μm	1.4 μm
A	Area of fabricated device	4.3 mm^2	4.3 mm^2

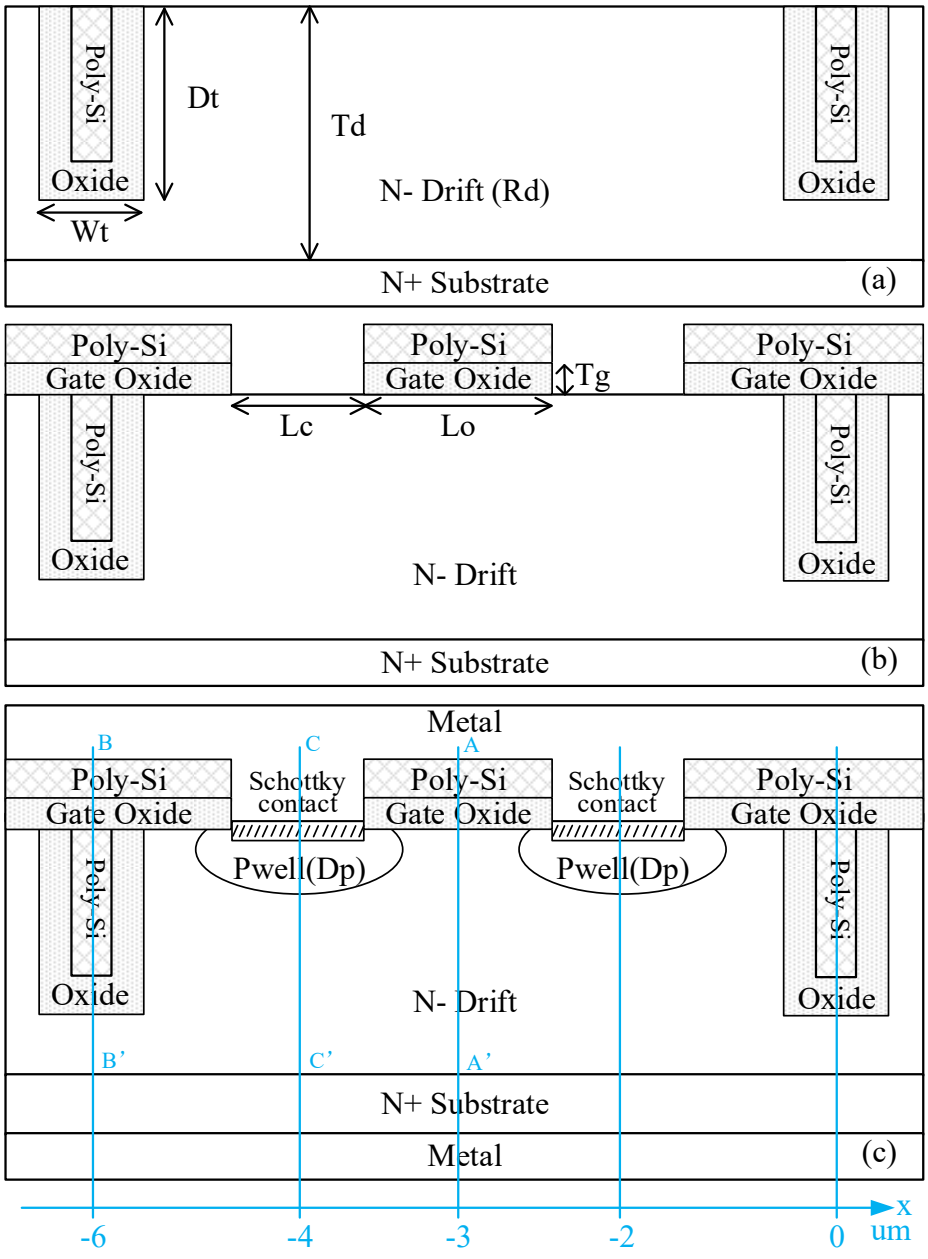

Figure 2. Key steps of the fabrication process for DOT-SSBR; (**a**) deep MOS trench formed, (**b**) polysilicon gate of SSB cell formed, (**c**) SSB cell formed.

As shown in Figure 2a, the deep silicon trench (depth Dt and width Wt, as listed in Table 1) is etched using a trench mask, the oxide in silicon trench with a thickness of approximately 0.4 μm is thermally grown (thermal oxidation), and the poly-silicon is deposited and heavily doped, followed by back etching. The junction terminal regions are also formed for both devices.

As shown in Figure 2b, the gate oxide with a thickness (Tg) of approximately 9 nm for the SSB cells is thermally grown (thermal oxidation), and the doped poly-silicon (Poly-Si) with a thickness of approximately 0.25 μm is formed by deposition, followed by back etching using a contact mask. The deep MOS trenches are floating and isolated from the anode contact by the gate oxide of the SSB cell, which is why it is called a deep isolated MOS trench (DOT). Compared with a conventional deep MOS trench, the DOT structure is equivalent to two capacitors in series, so its equivalent capacitance is reduced, which helps to improve reverse recovery performance. In addition, in DOT-SSBR, the width of Schottky contact shown in Figure 1 and Table 1 is the minimum size of the structure, which is approximately 0.6 μm. The Poly-Si width in the deep MOS trench is approximately 0.4 μm. For the 6-inch foundry with a minimum linewidth of 0.5 μm used in the experiment, it is difficult to lead the thin Poly-Si to the anode contact metal by the contact mask. Therefore, the thin gate oxide structure covering the deep MOS trench (thus forming the deep isolated MOS trench, DOT) also simplifies the process complexity, such as having smaller line width requirements.

As shown in Figure 2c, the P-well (Pwell) regions are achieved after one deep boron implantation and a Rapid Thermal Processing (RTP) at 1000 °C for sixty seconds [7]. The energy of this deep boron implantation is 80 keV; the dose (Dp) is from the order of 10^{13} cm^{-2} to 10^{15} cm^{-2} as shown in Table 1. The Pwell implantation dose (Dp) was selected as the process variable to optimize the trade-off between forward voltage and reverse leakage [7]. The titanium silicide (TiSix), which is formed by titanium/titanium nitride sputtering and another RTP, acts as the Schottky contact [7–9], followed by aluminum sputtering and the alloy process.

Both the depth of the deep trench (Dt) and the distance between two adjacent deep trenches (W) affect the electric field distribution in the drift layer. The larger the Dt or/and the smaller the W, the stronger the electric field pinching-off effect, and the smaller the mesa surface electric field, and vice versa. Different from TMBS, due to the p-well on the mesa surface, DOT-SSBR chooses a weak electric field pinching-off effect by DOTs, that is, the mesa surface electric field can remain large when the peak electric field is shifted to the inside of the drift layer. Therefore, the DOT-SSBR obtains a larger average electric field in the drift layer, resulting in a larger breakdown voltage. The width of deep trench (Wt) is a process-limited design parameter that should allow for the formation of a thick oxide layer inside and the filling of deep poly-silicon; the smaller the better for device performance.

Compared to conventional SSBR, the proposed DOT-SSBR features the deep isolated MOS trenches (DOTs) in an epitaxial n-drift layer. As the floating heavily doped Poly-Si is an equipotential body wrapped by the oxide layer, similar to the mechanism of pinching-off electric field in TMBS [6], the role of DOTs in DOT-SSBR is also to introduce the effect of pinching-off electric field, which introduces the peak electric field inside the n-drift layer under reverse bias. It will not only change the mesa surface electric field, but also change the average of electric field in n-drift layer.

Figure 3a,b show the simulated electric field at breakdown point of the cells of SSBR and DOT-SSBR, respectively. Compared to conventional SSBR, DOT-SSBR has the deep isolated MOS trenches (DOTs) in an epitaxial n-drift layer. In other words, DOT-SSBR without DOTs degenerates into a SSBR structure. As shown in both Figures 2c and 3a, the cell width of SSBR is 2 μm, ranging from X = −4 μm to X = −2 μm in simulation, and, as shown in Figures 2c and 3b, the cell width of DOT-SSBR is 6 μm, ranging from X = −6 μm to X = 0 μm.

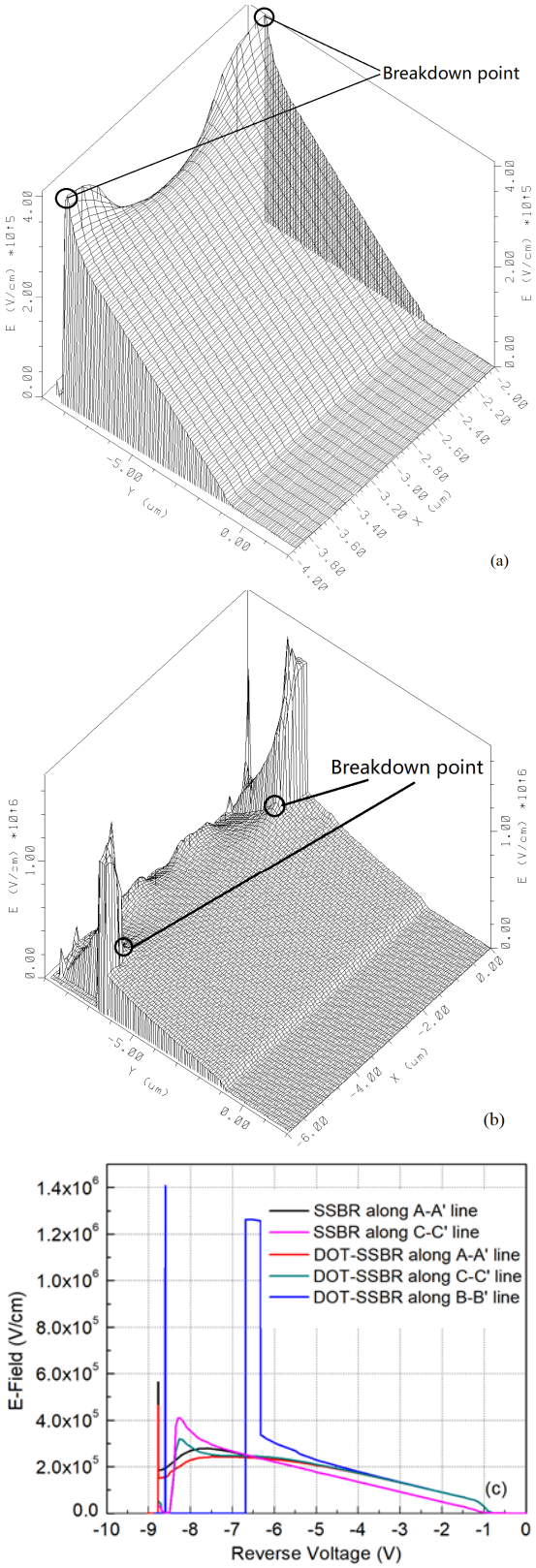

Figure 3. Simulated electric field at breakdown point of (**a**) SSBR, (**b**) DOT-SSBR, (**c**) SSBR along A-A′ line and C-C′ line (along X = −3 μm line and X = −4 μm line, shown in both Figures 2c and 3a), and DOT-SSBR along A-A′ line, C-C′ line and B-B′ line (along X = −3 μm line and X = −4 μm line and X = −6 μm line, shown in both Figures 2c and 3b).

It can be seen from Figure 3 that, compared with conventional SSBR, the DOTs in DOT-SSBR change the electric field distribution inside the n-drift layer under reverse bias, which not only reduces the mesa surface electric field but also increases the average electric field in the drift layer.

3. Experimental Results and Discussion

Figure 4 shows the measured forward and reverse I-V curves of the DOT-SSBR and SSBR. Each curve is formed by connecting several typical data points that are sufficient to describe the IV characteristics of the devices, and the value of each typical data point is the average of the samples on a 6-inch wafer. In addition to the deep isolated MOS trenches, the difference between DOT-SSBR and SSBR in the process conditions is the value of the Pwell implantation dose (Dp), and the value of Dp of SSBR is twice that of DOT-SSBR. A smaller value of Dp corresponds to a smaller super barrier and a smaller forward voltage to offset the increase in on-resistance caused by the decrease in effective active area after the introduction of DOTs. Therefore, as shown in Figure 4a, DOT-SSBR has almost the same forward I-V curve as that of SSBR. Thanks to the reduction in the mesa surface electric field caused by the pinching-off electric field effect of DOTs, DOT-SSBR has a smaller leakage current even though it has a smaller Dp (in the case of SSBR, small Dp leads to large leakage [7]), as shown in Figure 4b.

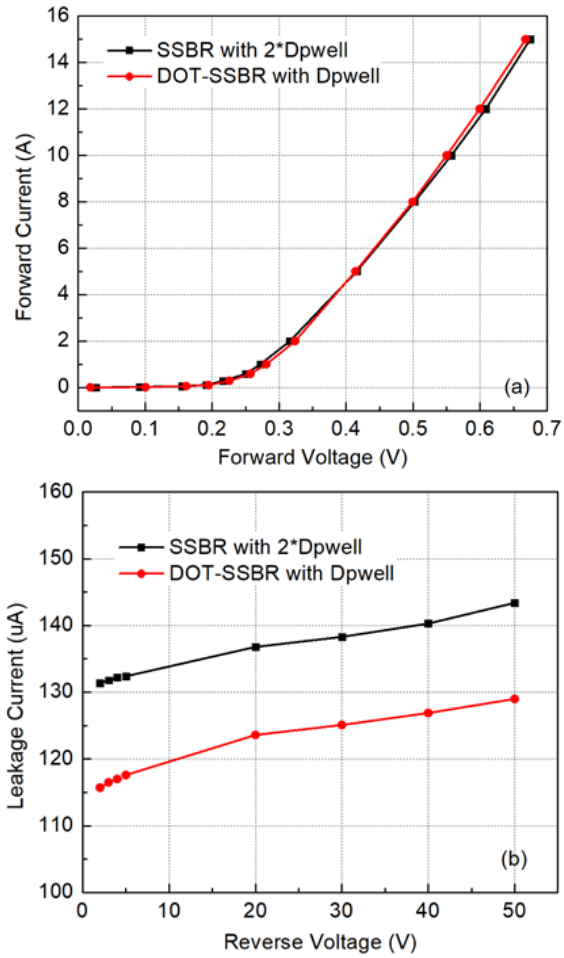

Figure 4. Measured (**a**) forward and (**b**) reverse characteristics of DOT-SSBR and SSBR. Each data point is the average of the sample points on a 6-inch wafer.

The statistical typical parameters are listed in Table 2. The distribution of the scattered data points for forward voltage, breakdown voltage and reverse leakage current from the 6-inch wafer samples for DOT-SSBR and SSBR are shown in Figure 5.

Table 2. Statistical typical parameters of DOT-SSBR and SSBR.

Devices	V_F (V) at I_F = 10 A	V_B (V) at I_R = 0.5 mA	I_R (μA) at V_R = 50 V
SSBR	0.557 ± 0.031	91.1 ± 1.34	143.4 ± 7.94
DOT-SSBR	0.550 ± 0.024	126.3 ± 2.15	129.0 ± 14.99

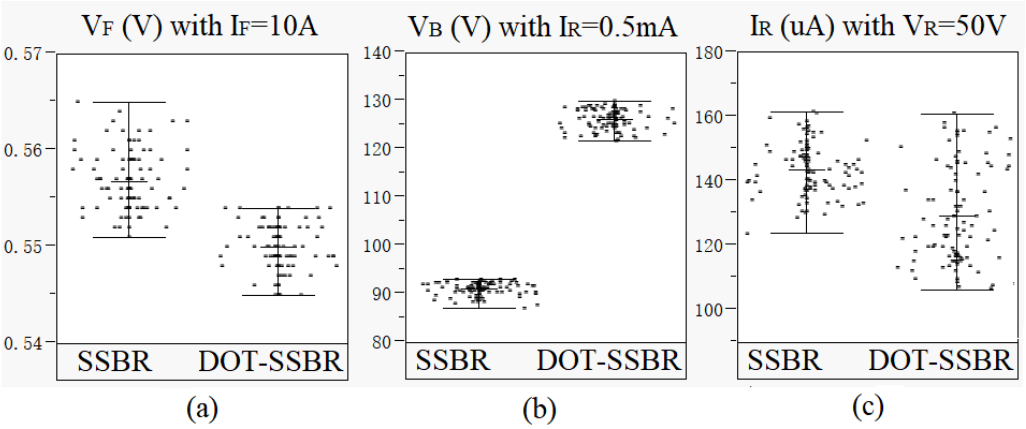

Figure 5. Distribution of scattered data points for (**a**) forward voltage, (**b**) breakdown voltage and (**c**) reverse leakage current from 6-inch wafer samples for DOT-SSBR and SSBR.

As listed in Table 2, at the reverse voltage of 50 V, the average reverse leakage current of DOT-SSBR (129.0 μA) is reduced by approximately 10.0% compared to that (143.4 μA) of the SSBR, and, at the reverse current of 0.5 mA, the average breakdown voltage of DOT-SSBR (126.3 V) is greatly increased by approximately 38.6% compared to that (91.1 V) of the SSBR.

As shown in Table 2 and Figure 5, the breakdown voltage and reverse leakage current data points of DOT-SSBR are more scattered than SSBR because of the different depths of DOT located in the middle and edge of the 6-in wafer in the manufacturing process. At present, the deep MOS trench technology of the six-inch foundry with a minimum linewidth of 0.5 μm used in the experiment is not mature enough. In the future, better parameter consistency will be obtained by improving the deep MOS trench process, especially the deep MOS trench process consistency of the whole 6-inch wafer distribution.

Figure 6 shows the external appearance of the packaged SSBR and DOT-SSBR; the two rectifiers are in exactly the same package, with each package consisting of two chips. The package type is TO-220. The middle pin is a common cathode, and the other two pins are two independent anodes. Since the chip area and package of SSBR and DOT-SSBR are the same, the following comparative measured results can accurately reflect the electrical parameter differences caused by the different structures of the two devices.

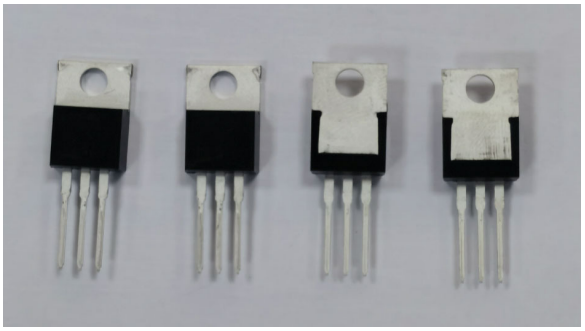

Figure 6. External appearance of the packaged SSBR and DOT-SSBR. The kind of package is TO-220. The middle pin is a common cathode, and the other two pins are two independent anodes.

Figure 7 shows the measured forward, reverse and C-V characteristics of the packaged DOT-SSBR and SSBR. As seen from Figure 7c, DOT-SSBR has a slightly larger capacitance as that of SSBR. Figure 8 shows the measured reverse recovery current of the packaged DOT-SSBR and SSBR. It is obvious that the proposed DOT-SSBR shows a slightly larger reverse current amplitude and could show higher reverse recovery charges than that of the conventional SSBR, which shows a trend consistent with the results in the C-V curves in Figure 7c (i.e., higher parasitic capacitances and hence higher charges). However, as unipolar conduction devices, both of the SSBR and DOT-SSBR have fast reverse recovery characteristics. The measured reverse recovery times are both approximately 37 ns.

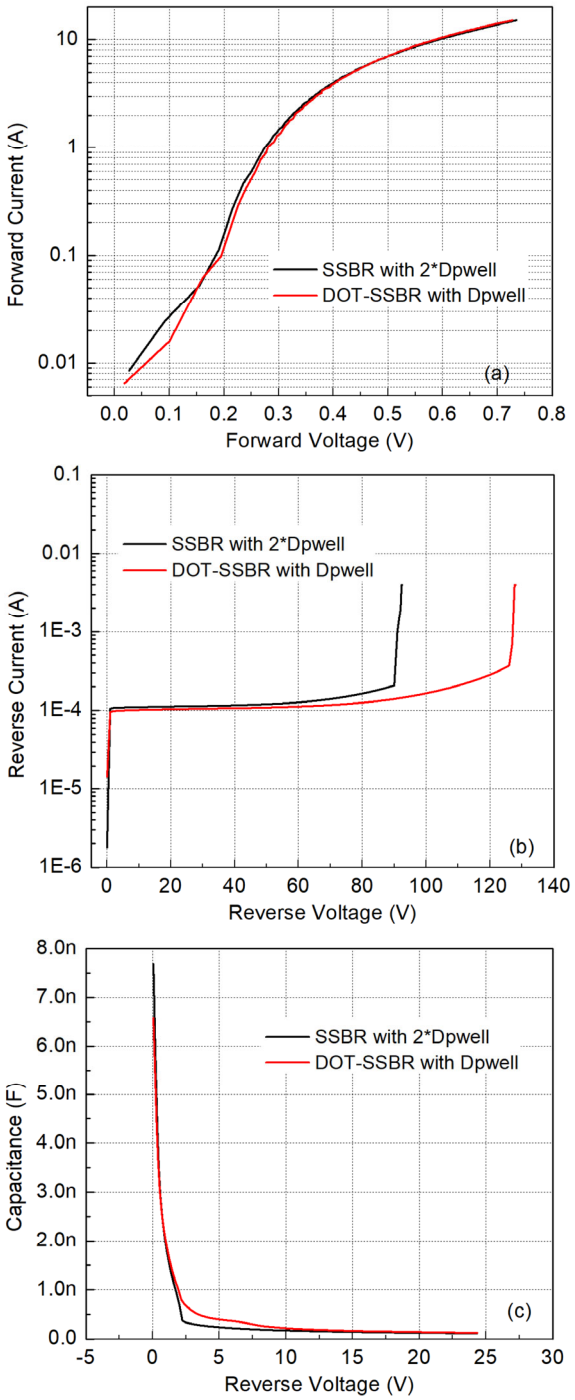

Figure 7. Measured (**a**) forward, (**b**) reverse and (**c**) C-V characteristics of packaged DOT-SSBR and SSBR.

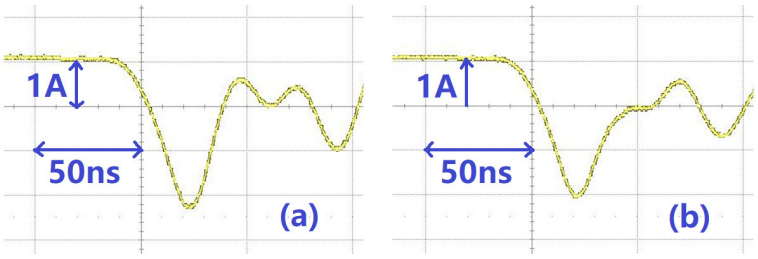

Figure 8. Measured reverse recovery current of packaged (**a**) DOT-SSBR and (**b**) SSBR.

Figure 9 shows the measured high-temperature characteristics of forward I-V curves and reverse leakage current for packaged DOT-SSBR and SSBR. As shown, both the DOT-SSBR and SSBR show almost the same high-temperature characteristics. However, for the high-temperature forward I-V curve of DOT-SSBR, as seen from Figure 9a,b, the point at which the temperature coefficient is zero is about V_F = 0.43 V, at which point the corresponding forward current is about 5 A. This feature is slightly better than SSBR. When the deep isolated MOS trench is introduced into SSBR-like devices, that is, DOT-SSBR, the high-temperature stability of SSBR, especially the low leakage characteristic at high temperature, is not damaged. It can be seen from Figure 9c.

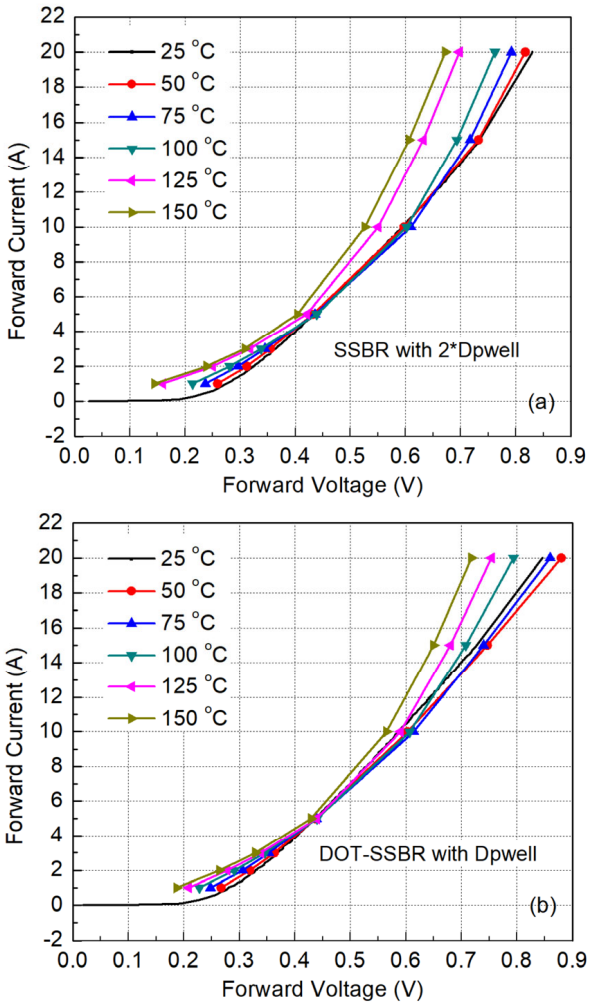

Figure 9. *Cont.*

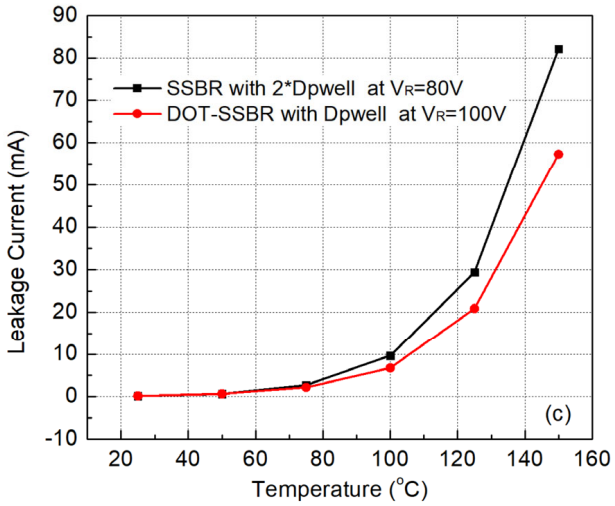

Figure 9. Measured high-temperature characteristics of (**a**) forward I-V curves for packaged SSBR, (**b**) forward I-V curves for packaged DOT-SSBR and (**c**) reverse leakage current for packaged DOT-SSBR and SSBR.

4. Conclusions

In conclusion, by combining the concept of planar SSBR and the effect of pinching-off electric field by deep isolated MOS trenches, a novel 120 V-class Schottky contact super barrier rectifier with a deep isolated MOS trench in an epitaxial n-drift layer (DOT-SSBR) is studied through experiments. An auxiliary simulation analysis, to provide insight about the physics of the device, is also presented. The breakdown voltage of the proposed DOT-SSBR was greatly increased without sacrificing the forward voltage or reverse leakage current when compared with the conventional SSBR. The fabrication process, the measured high-temperature characteristics of forward I-V curves and reverse leakage current, and the measured C-V characteristics and reverse recovery current of the new device are also demonstrated and discussed. In order to greatly increase the breakdown voltage of SSBR, when deep isolated MOS trenches are introduced into SSBR-like devices, that is, the proposed DOT-SSBR in this paper, the significant advantages in terms of electrical performance of SSBR are preserved, such as the low forward voltage, especially the ultra-low forward voltage under low current density, and the high-temperature stability, especially the low leakage characteristic at high temperature. At the same time, the proposed DOT-SSBR does not sacrifice the reverse leakage characteristics of SSBR or the fast-switching characteristics as a unipolar device of SSBR.

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