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Analysis of the Second-Order NS SAR ADC Performance Enhancement Based on Active Gain

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Abstract: This paper presents a novel second-order passive noise shaping (NS) successive approximation register (SAR) analog-to-digital converter (ADC) based on active gain. The proposed scheme achieves a further improvement in the signal-to-noise ratio (SNR) of the proposed NS SAR ADC by reducing the kT/C noise and the conversion rate. After having presented the conversion principle, the theoretical analysis of the performance enhancement based on noise and other considerations is presented.

Keywords: noise shaping; successive approximation register; analog-to-digital converter; signal-to-noise ratio

1. Introduction

The successive approximation register (SAR) analog-to-digital converter (ADC) is one of the most widely used ADC architectures. It offers medium resolution and is simple to design [1–4]. However, for high-resolution applications, its power efficiency degrades due to stringent requirements on the comparator noise and the exponentially growing capacitor digital-to-analog converter (DAC) array. The noise shaping (NS) SAR ADC is an emerging hybrid ADC architecture that combines the advantages of SAR and Sigma–Delta ADCs [5–8]. The NS SAR ADC significantly reduces in-band comparator noise and quantization noise without degrading power efficiency [9,10]. Comparator noise is a critical factor in signal-to-noise ratio (SNR). Due to the simple structure and lower power consumption of dynamic comparators, they are more widely used in SAR ADCs than the static comparator. However, the input referred noise of dynamic comparators is larger than static comparators because of its low gain. Although the comparator noise is shaped in NS SAR ADC, it remains too large for high-resolution systems. Several methods have been proposed to minimize it. The SNR and spurious free dynamic range (SFDR) enhancement technique is proposed [11–13], repeating comparison of least significant bit (LSB) by using redundant DAC to average comparator noise. To effectively reduce the comparator noise and increase its lower-bits decision accuracy, the majority voting (MV) technique is proposed [14,15], and a tri-level voting technique is employed [16]. However, these techniques come at the expense of a lower sampling rate.

Although NS SAR ADCs can also reduce the number of quantizer bits, the kT/C noise decreases as the capacitance increases. Therefore, increasing the capacitor array is essential for high-resolution applications. There are three drawbacks associated with a large capacitance. The first, a large capacitance means a large area, which burdens the whole chip. Second, a larger capacitance consumes more dynamic power. Third, a large sampling capacitance also increases the power consumption of the input buffer. Therefore, increasing the capacitance may not be an effective way to reduce the kT/C noise. To overcome the limitations of the large capacitance and the input-referred noise of the dynamic comparator, this paper proposes a second-order NS SAR ADC based on active gain. The proposed method achieves a further improvement in the SNR of NS SAR ADC and sampling speed

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while using the smaller capacitance. This paper provides a mathematical analysis of the noise and non-ideal factors demonstrating the effectiveness of the proposed scheme.

This paper is organized as follows. Section 2 presents a mathematical analysis of previous second-order fully-passive NS SAR ADC architecture. Section 3 discusses the two schemes of proposed second-order NS SAR ADC based on active gain. Section 4 compares the advantages and disadvantages of the proposed schemes. Section 5 concludes this paper.

2. Mathematical Analysis of Previous Second-Order Fully-Passive NS SAR ADC

Some prior works utilized operational transconductance amplifiers (OTA) to construct active filters, which can achieve good NS effect [9]. However, OTA consumes high power and is scaling-unfriendly. In recent years, methods utilizing switches and capacitors to implement fully passive filters have been proposed [17,18]. These passive switched capacitor filters are simple, low power, robust, and scaling-friendly. The previous second-order fully-passive NS SAR ADC work is shown in Figure 1 [16]. According to the signal flow diagram shown in Figure 1, V_{int1} and V_{int2} can be obtained:

$$V_{int1}(z) = (1-a)\frac{a}{1-(1-a)z^{-1}}V_{res}(z) \quad (1)$$

and

$$V_{int2}(z) = \frac{a}{1-(1-a)z^{-1}}V_{int1}(z) = (1-a)\frac{a^2}{[1-(1-a)z^{-1}]^2}V_{res}(z) \quad (2)$$

where the residual voltage is $V_{res}(z) = V_{in}(z) - D_{OUT}(z)$.

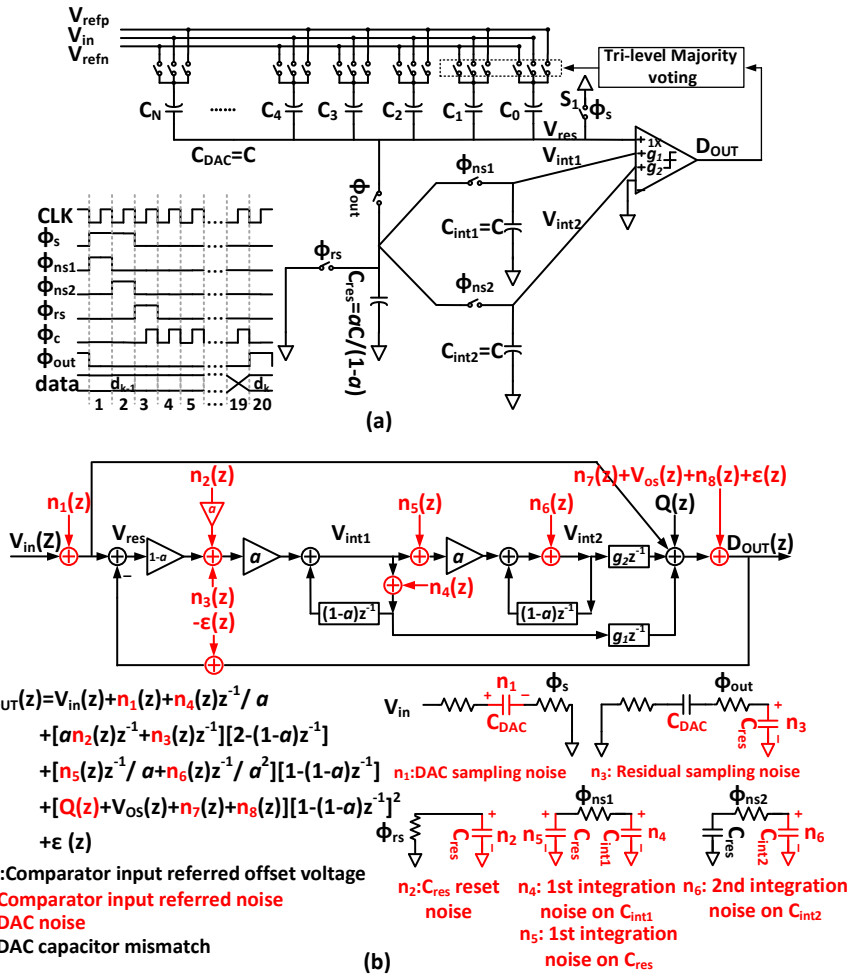

Figure 1. Previous NS SAR ADC work. (**a**) Second-order fully-passive NS SAR ADC architecture. (**b**) Signal flow diagram.

The relationship between input and output can be expressed as:

$$D_{OUT}(z) = V_{in}(z) + g_1 z^{-1} V_{int1}(z) + g_2 z^{-1} V_{int2}(z) + Q(z) \quad (3)$$

where Q(z) is quantization noise. By substituting (1) and (2) into (3), the z-domain transfer function with only quantization noise of the previous NS SAR ADC can be calculated as follows:

$$D_{OUT}(z) = V_{in}(z) + \frac{\left[1-(1-a)z^{-1}\right]^2}{1+(1-a)(g_2a^2+g_1a-2)z^{-1}+(1-a)^2(1-g_1a)z^{-2}} Q(z) \quad (4)$$

The typical values of a, g_1, g_2, and oversampling ratio (OSR) in Figure 1 are 1/4, 4, 16, 16, respectively. The parameter a is robust against process–voltage–temperature (PVT) variations and mismatches because it depends on the ratio of the capacitance. The parameters g_1 and g_2 represent the strengths of different input pairs of the comparator, and they are insensitive to PVT variations and mismatches. However, the variations of g_1 and g_2 with PVT do not affect the stability of the structure, which has been analyzed in detail [16].

The parameters a, g_1, and g_2 may be affected by PVT variations and mismatches during the manufacturing process. However, a, g_1, and g_2 are regarded as constant in the following analysis because PVT variations and mismatches are ignored. Therefore, the z-domain transfer function including only quantization noise can be simplified as follows:

$$D_{OUT}(z) = V_{in}(z) + \left[1-\frac{3}{4}z^{-1}\right]^2 Q(z) \quad (5)$$

The z-domain transfer function including quantization noise and other noise is shown in Figure 1b. The signal transfer function (STF) is given by STF = 1, indicating that there is no energy loss in the signal power. For different noise sources, the noise transfer functions (NTFs) are different. The quantization noise transfer function is given by $(1 - 0.75\, z^{-1})^2$. The noise power $n_1^2 - n_6^2$ are kT/C, $(1 - a)$kT/aC = 3 kT/C, $(1 - a)^2$kT/aC = 2.25 kT/C, akT/C = 0.25 kT/C, $(1 - a)^2$kT/aC = 2.25 kT/C, and akT/C = 0.25 kT/C, where k is the Boltzmann constant. Their in-band noise power will be calculated separately. In order to estimate the in-band power of the quantization noise, it is useful to find the magnitude of the quantization noise transfer function in the frequency domain by setting $z = e^{j2\pi f}$. For frequencies that satisfy $f \ll 1$, $|NTF(e^{j2\pi f})| \approx 1/16 + 3(\pi f)^2$. The in-band power of the quantization noise, P_{Q_ib}, can be calculated as:

$$\begin{aligned} P_{Q\_ib} &= 2\int_0^{\frac{1}{2OSR}} \left|\left(1-\tfrac{3}{4}z^{-1}\right)^2\right|^2 P_Q df \\ &\approx 2\int_0^{\frac{1}{2OSR}} \left(\tfrac{1}{16}+3(\pi f)^2\right)^2 P_Q df \\ &\approx \left(\tfrac{1}{256}+\tfrac{\pi^2}{32}\tfrac{1}{OSR^2}+\tfrac{3.6\pi^4}{32}\tfrac{1}{OSR^4}\right)\tfrac{P_Q}{OSR} \end{aligned} \quad (6)$$

where P_Q is the quantization noise power of the SAR ADC without NS. Ignoring considering other noises, the improved ideal effective number of bits (ENOBs), denoted as $ENOB_{imp}$, can be expressed as the following expression.

$$ENOB_{imp} = \frac{-10\log\left(\frac{1}{256}\frac{1}{OSR}+\frac{\pi^2}{32}\frac{1}{OSR^3}+\frac{3.6\pi^4}{32}\frac{1}{OSR^5}\right)}{6.02} \quad (7)$$

When the OSR is set to 16, $ENOB_{imp} \approx 5.76$ can be obtained. Oversampling can reduce the in-band noise power by OSR times. By observing (6), it can be found that NS suppresses the low-frequency quantization noise power by approximately a factor of 256. Similar to quantization noise, comparator input-referred noise and DAC noise are also affected by the passive second-order NS.

Using similar calculations, the in-band noise powers of different noise sources can be obtained separately. The in-band noise power $n_{1\_ib}^2 - n_{6\_ib}^2$ are approximately n_1^2/OSR, $[0.1 + \pi^2/(32OSR^2)]n_2^2/OSR$, $[1.56 + \pi^2/(2OSR^2)]n_3^2/OSR$, $16n_4^2/OSR$, $[1 + 4\pi^2/OSR^2]$ n_5^2/OSR, $[16 + 64\pi^2/OSR^2]n_6^2/OSR$. It is obvious that the structure's NS ability for different noises is not the same. If the noise is unaffected by NS, the noise power becomes 1/OSR times the original after oversampling. Since $n_{2\_ib}^2$ is smaller than n_2^2/OSR, the noise n_2 is shaped to contribute less noise. By examining $n_{1\_ib}^2 - n_{6\_ib}^2$, it is clear that only the in-band noise powers of C_{res} reset noise n_2, comparator input referred noise n_7 and DAC noise n_8 are suppressed by NS, and DAC sampling noise n_1 is not affected by NS. However, the in-band noise powers of $n_3 - n_6$ are enlarged by NS. Since $n_1 - n_6$ and n_8 are all kT/C noise and only n_8 is second-order shaped, $n_1 - n_6$ are the primary contributors of the kT/C noise.

The kT/C noise and comparator input-referred noise n_7 are the main two noise sources by mathematical analysis of previous second-order fully-passive NS SAR ADC. NS effectively suppresses the low-frequency comparator input-referred noise power, reducing it by approximately a factor of 256. In this structure, the comparator input-referred noise is suppressed by the second-order NS. However, NS achieves limited suppression of low-frequency C_{res} reset noise power, reducing it by about a factor of 10, while the in-band noise powers of $n_3 - n_6$ are enlarged by NS. In order to effectively reduce the kT/C noise, the capacitance must be large enough for high-resolution applications. To address this issue, the second-order NS SAR ADC based on active gain is proposed.

3. The Proposed Second-Order NS SAR ADC

In order to reduce the kT/C noise, an open-loop amplifier is used in the proposed second-order NS SAR ADC based on active gain. However, it can decrease the kT/C noise, except the DAC sampling noise. On the basis of second-order NS SAR ADC based on active gain, the improved second-order NS SAR ADC based on active gain is proposed to suppress the DAC sampling noise. Key parameters related to the amplifier need to be designed and selected reasonably for optimum noise performance. Finally, the speed issue and kickback noise issue of the proposed structures are analyzed.

3.1. The Second-Order NS SAR ADC Based on Active Gain

The schematic and signal flow diagram of SAR ADC are shown in Figure 2a [19]. Based on the signal flow diagram, the z-domain transfer function including only quantization noise is $D_{out}(z) = V_{in}(z) + Q(z)$. The quantization noise Q(z) can be obtained.

$$Q(z) = D_{out}(z) - V_{in}(z) \tag{8}$$

The schematic and equivalent signal flow diagram of SAR ADC based on active gain are shown in Figure 2b. An open-loop amplifier is integrated between the DAC capacitor array and the comparator. The DC gain of the open-loop amplifier is A. Based on the equivalent signal flow diagram, the quantization noise $Q_A(z)$ can be obtained.

$$Q_A(z) = A(D_{out}(z) - V_{in}(z)) = AQ(z) \tag{9}$$

Therefore, the z-domain transfer function including only quantization noise of SAR ADC based on active gain is:

$$D_{out}(z) = V_{in}(z) + Q(z) \tag{10}$$

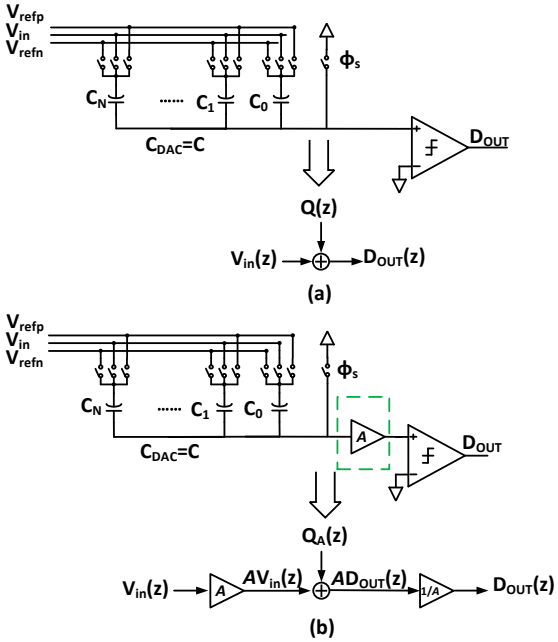

Figure 2. (**a**) Schematic and signal flow diagram of SAR ADC. (**b**) Schematic and equivalent signal flow diagram of SAR ADC based on active gain.

This result is the same as the transfer function of the SAR ADC, indicating that the addition of the amplifier does nothing to quantization noise. To assess the impact on other noises, the DAC sampling noise and the comparator input referred noise are added to the signal flow diagram shown in Figure 3. Since the DAC capacitor array and comparators in Figure 2a,b are identical, the DAC sampling noise $n_1(z)$ and the comparator input referred noises $n_7(z)$ remain consistent in both Figure 3a,b.

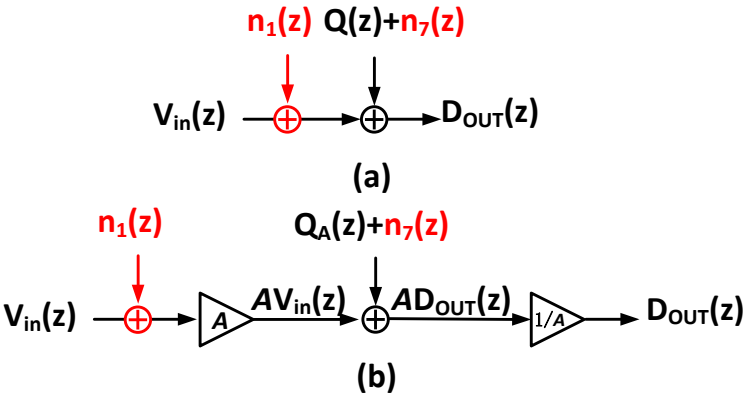

Figure 3. (**a**) Signal flow diagram with the DAC sampling noise and comparator input referred noise of SAR ADC. (**b**) Equivalent signal flow diagram with the DAC sampling noise and comparator input referred noise of SAR ADC based on active gain.

According to the signal flow diagram shown in Figure 3a, the z-domain transfer function with the DAC sampling noise and comparator input referred noise of SAR ADC is:

$$D_{out}(z) = V_{in}(z) + Q(z) + n_1(z) + n_7(z) \tag{11}$$

However, the z-domain transfer function with the DAC sampling noise and comparator input referred noise of SAR ADC based on active gain can be obtained based on the signal flow diagram shown in Figure 3b.

$$D_{out}(z) = V_{in}(z) + Q(z) + n_1(z) + \frac{n_7(z)}{A} \quad (12)$$

By comparing (11) and (12), It can be found that the amplifier suppresses the comparator input referred noise but not DAC sampling noise. Therefore, using the amplifier can suppress a portion of the noises, such as comparator input-referred noise, but has no influence on quantization noise and DAC sampling noise.

To mitigate the disadvantages of large capacitors, the scheme of the second-order NS SAR ADC based on active gain is proposed, as illustrated in Figure 4a. Compared to the second-order fully-passive NS SAR ADC, this scheme incorporates three additional components, which include an open-loop amplifier, a cancellation capacitor C_{nc}, and a sampling switch S_2. C_{nc} must satisfy C_{nc}:C_{res}:C_{int1}:C_{int2} = 3:1:3:3. A represents the DC gain of the open-loop amplifier. At the end of the sampling phase, the sampling switches S_1 and S_2 are switched off simultaneously. Hence, the offset voltage V_{osamp} of the amplifier can be stored on the cancellation capacitor C_{nc}. During the conversion phase, the final residual voltage of the DAC array is amplified by a factor of A, which decreases the effect of noise $n_2 - n_7$ and n_9 on circuit performance.

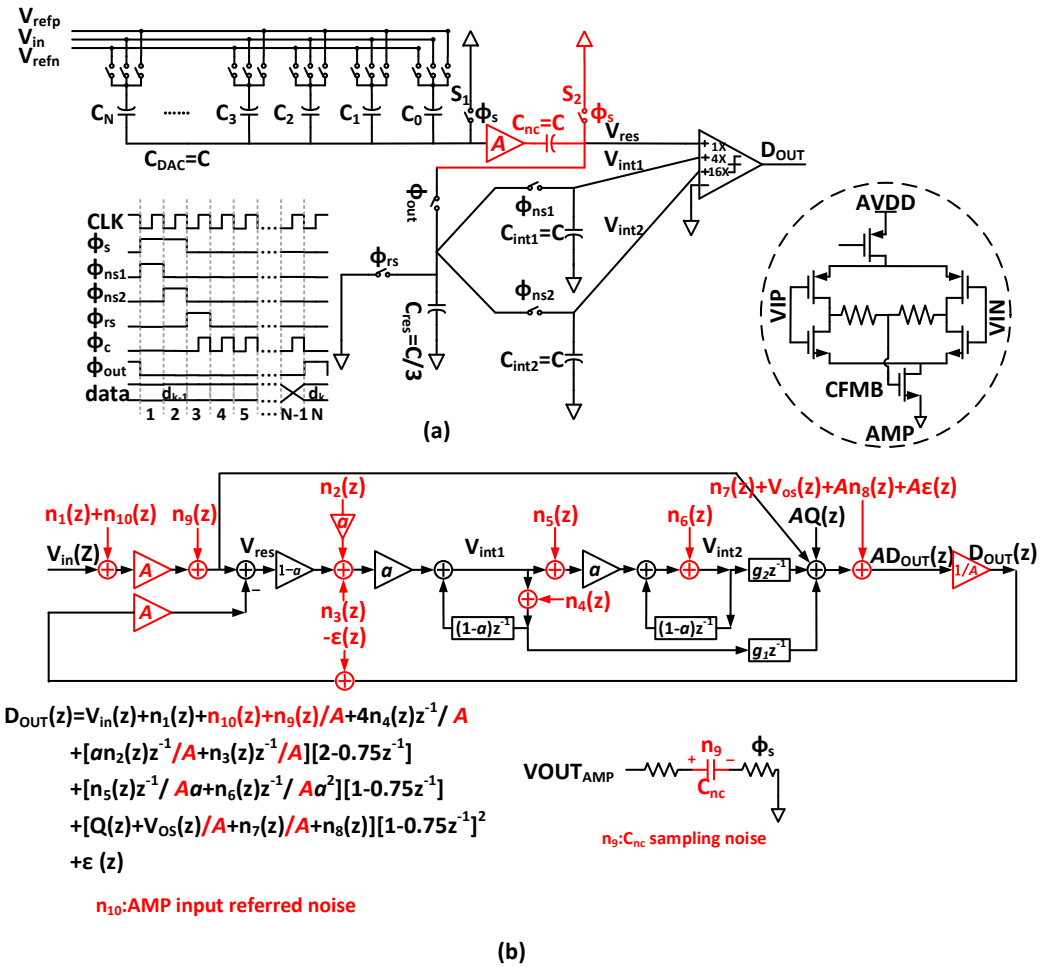

Figure 4. Proposed second-order NS SAR ADC scheme. (**a**) Second-order NS SAR ADC based on active gain. (**b**) Signal flow diagram.

In Figure 4, the residual voltage is $V_{res}(z) = A\,(V_{in}(z) - D_{OUT}(z))$. The output voltage of the amplifier can be thought of as V_{res} because the voltage stored on C_{nc} does not change during the SAR conversion. When φ_{out} becomes high, V_{res} is sampled by C_{res}, and the voltage on C_{res} is $(1 - a)\,V_{res}(z)$. When φ_{ns1} and φ_{ns2} go high, the same expressions for V_{int1} and V_{int2} are obtained as those in the second-order fully-passive NS SAR. Therefore, (1) and (2) can be also obtained.

Using the signal flow diagram in Figure 4b, (13) can be obtained.

$$AD_{OUT}(z) = AV_{in}(z) + g_1 z^{-1} V_{int1}(z) + +g_2 z^{-1} V_{int2}(z) + AQ(z) \tag{13}$$

(1) and (2) are substituted into (13), and the z-domain transfer function with only quantization noise of the proposed NS SAR ADC can be calculated without considering the PVT variations and mismatches of a, g_1, and g_2.

$$D_{OUT}(z) = V_{in}(z) + \left(1 - 0.75z^{-1}\right)^2 Q(z) \tag{14}$$

The comparison of (14) and (5) demonstrates that using the amplifier has no effect on quantization noise. In order to accurately describe the noise suppression advantages of the proposed scheme for other noises, the signal flow diagram and complete z-domain transfer function with all noises of the proposed NS SAR ADC are shown in Figure 4b. The STF is still 1, and the noise transfer function has been changed. The magnitude of the noise $n_2 - n_7$ and n_9 is attenuated by the open-loop amplifier gain A, and the power of the noise $n_2 - n_7$ and n_9 is attenuated by A^2. The noise $n_2 - n_7$ and n_9 is related to the capacitors C_{nc}, C_{res}, C_{int1}, and C_{int2}. Therefore, the active amplifier can be used to greatly reduce the capacitance of the capacitors C_{nc}, C_{res}, C_{int1}, and C_{int2}. Both n_9 and AMP input-referred noise n_{10} are new noise sources. The power of C_{nc} sampling noise n_9 is kT/C. The structure of the amplifier [20] shown in Figure 4a can be employed in the proposed NS SAR ADC. The single-end input-referred noise power spectrum density (PSD) of a CMOS-input preamp is:

$$\frac{\overline{n_{10}^2}}{\Delta f} = \frac{4kT\gamma}{G_m} \tag{15}$$

where the theoretical value of γ is 2/3 for long-channel devices and G_m is the transconductance of the open-loop amplifier. The noise bandwidth of the open-loop amplifier during the sampling phase is about $1/4R_{out}C_{nc}$. $R_{out} = A/G_m$ is the output resistance of the open-loop amplifier. Thus, the power of AMP input referred noise n_{10} can be calculated as:

$$\overline{n_{10}^2} = \frac{4kT\gamma}{G_m} \times \frac{1}{4R_{out}C_{nc}} = \frac{kT\gamma}{AC} \tag{16}$$

It can be seen that the AMP input-referred noise power is inversely proportional to the amplifier gain A from (16). Only the noises n_1 and n_8 are not suppressed by A. The noise n_1 directly affects the output signal and is not second-order-shaped like n_8. Therefore, n_1 becomes the main kT/C noise source.

3.2. Improved Second-Order NS SAR ADC Based on Active Gain

To alleviate the deterioration of the output signal by noise n_1, the improved second-order NS SAR ADC based on active gain is proposed, shown in Figure 5. The kT/C noise cancellation principle proposed by [21,22] is employed. There is a change in the timings compared to Figure 4a. φ_s is split into φ_{sDAC} and φ_{snc}, controlling switches S_1 and S_2, respectively.

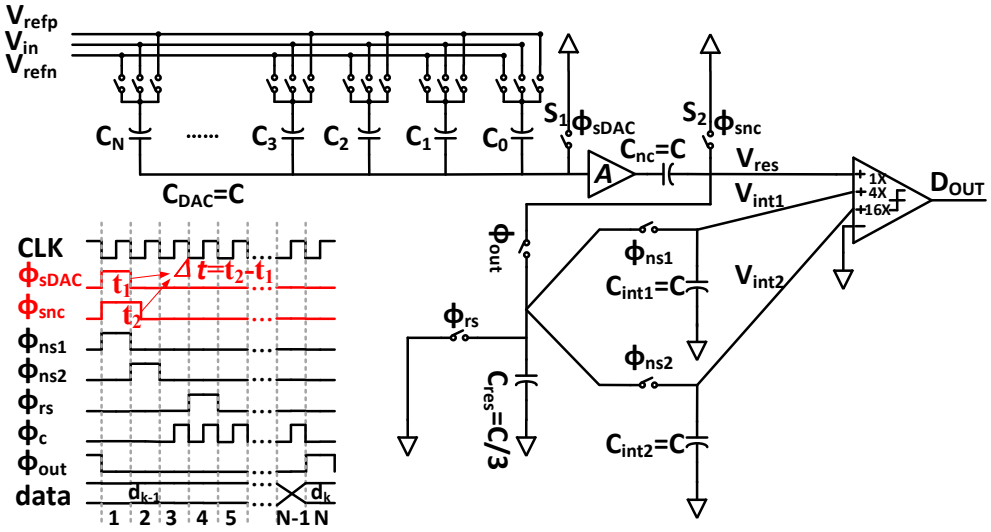

Figure 5. Improved second-order NS SAR ADC scheme.

The kT/C noise cancellation principle is shown in Figure 6. The sampling phase is divided into the C_{DAC} sampling phase and the C_{nc} sampling phase. The C_{DAC} sampling phase lasts from t_0 to t_1 controlled by φ_{sDAC}. At the moment t_1, the sampled input signal $V_{in}(t_1)$ and kT/C noise n_1 are stored on C_{DAC}. The offset voltage V_{osamp} of the amplifier is stored on the C_{nc}, as in Figure 4a. The C_{nc} sampling phase operates from t_1 to t_2 controlled by φ_{snc}. At t_2, the input signal is $V_{in}(t_2)$, and the input voltage of the amplifier is $V_{in}(t_2) - V_{in}(t_1) - n_1 - V_{osamp}$. Assuming the amplifier has infinite bandwidth, it fully settles during the C_{nc} sampling phase. The voltage stored on C_{nc} is:

$$V_{C_{nc}} = A\left[V_{in}(t_2) - V_{in}(t_1) - n_1 - V_{osamp}\right] \quad (17)$$

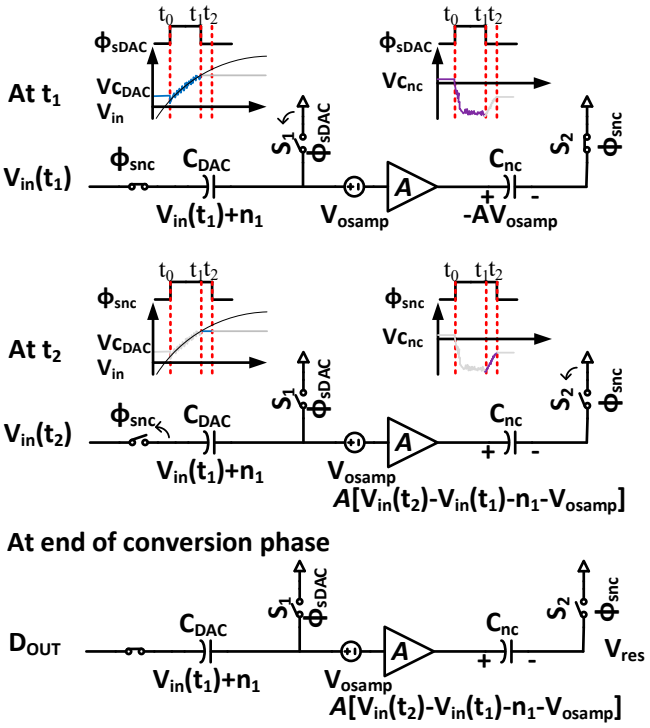

Figure 6. The kT/C noise cancellation principle.

Neglecting capacitances C_{int1}, C_{int2}, and C_{res}, the input–output relation can be computed as (18) at the end of the conversion phase.

$$D_{OUT} = V_{in}(t_2) + V_{res}/A \approx V_{in}(t_2) \tag{18}$$

By observing (18), it can be seen that the sampling noise n_1 can be completely canceled if the amplifier has an infinite bandwidth. In fact, the bandwidth of the amplifier is limited. Therefore, the sampling noise voltage stored on C_{nc} is:

$$n_1\_C_{nc} = -An_1\left(1 - e^{-\Delta t/\tau}\right) \tag{19}$$

where τ is the settling time constant of the amplifier [23] and the time interval satisfies $\Delta t = t_2 - t_1$. The voltage stored on C_{nc} is $A[V_{in}(t_2) - V_{in}(t_1) - n_1(1 - e^{-\Delta t/\tau}) - V_{osamp}]$. The new input–output relationship can be computed as:

$$D_{OUT} = V_{in}(t_2) + n_1 e^{-\Delta t/\tau} \tag{20}$$

From the above analysis, it can be concluded that kT/C noise cancellation allows the sampling noise power to be attenuated by $e^{2\Delta t/\tau}$. As a result, the z-domain transfer function of the improved second-order NS SAR ADC scheme can be expressed as follows:

$$\begin{aligned} D_{OUT} = {} & V_{in}(z) + n_1 e^{-\frac{\Delta t}{\tau}}(z) + n_{10}(z) + \tfrac{n_9(z)}{A} + \tfrac{n_4(z)z^{-1}}{Aa} \\ & + \left(\tfrac{an_2(z)z^{-1}}{A} + \tfrac{n_3(z)z^{-1}}{A}\right)\left(2 - 0.75z^{-1}\right) \\ & + \left(\tfrac{n_5(z)z^{-1}}{Aa} + \tfrac{n_6(z)z^{-1}}{Aa^2}\right)\left(1 - 0.75z^{-1}\right) \\ & + \left(Q(z) + \tfrac{V_{OS}}{A} + \tfrac{n_7(z)}{A} + n_8(z)\right)\left(1 - 0.75z^{-1}\right)^2 \\ & + \varepsilon(z) \end{aligned} \tag{21}$$

It is possible to achieve a reduction in the overall capacitance in the improved second-order NS SAR ADC by designing the values of A and $\Delta t/\tau$ in a rational way. This makes it possible to use the structure in high-resolution applications where large-area capacitors are not applicable.

3.3. The Values of A and $\Delta t/\tau$

The selection of A and $\Delta t/\tau$ is crucial for the attenuation of kT/C noise and the performance of the proposed scheme. If the gain A is too large, it can easily lead to saturation of the open-loop amplifier. On the contrary, if the gain A is too small, noises $n_2 - n_7$ and $n_9 - n_{10}$ cannot be sufficiently suppressed, resulting in little performance improvement. Therefore, the value of A must be reasonable. To ensure that the open-loop amplifier accurately amplifies the residual voltage of the DAC array generating V_{res}, it is necessary to ensure that (22) is satisfied.

$$A\left[V_{in}(t_2) - V_{in}(t_1) - n_1 - V_{osamp}\right] + AV_{res\_DAC} < \frac{AVDD}{2} - V_{dsat} \tag{22}$$

where V_{res_DAC} is the residual voltage of the DAC array, AVDD is the power supply voltage, and V_{dsat} is the saturation drain voltage. In order for the amplifier to quickly remain stable in the amplification region at the end of the conversion, V_{res_DAC} is taken to be at least 4LSB instead of LSB (LSB = $(V_{refp} - V_{refn})/2^N$). The maximum amount of change in the input signal during the time interval Δt is:

$$|V_{in}(t_2) - V_{in}(t_1)|_{max} \approx \left|\sin'(2\pi f_{inmax}t)\right|_{max} \times \Delta t = 2\pi f_{inmax} \times \Delta t = \pi f_{sam} \times \Delta t/OSR \tag{23}$$

where f_{inmax} is the maximum frequency of the input signal, f_{sam} is the sampling frequency, and $f_{inmax} = f_{sam}/2OSR$. n_1 is the DAC sampling noise voltage with a noise

power of kT/C_{DAC}. Thus, the distribution of n_1 is N (0, $\sqrt{kT/C_{DAC}}$). The maximum value of n_1 can be considered:

$$|n_1|_{max} = 5\sqrt{kT/C_{DAC}} \tag{24}$$

The maximum gain can be calculated as follows:

$$A_{max} = \frac{\frac{AVDD}{2} - V_{dsat}}{\frac{\pi f_{sam}}{OSR} \times \Delta t + 5\sqrt{\frac{kT}{C_{DAC}}} + |V_{osamp}|_{max} + 4LSB} \tag{25}$$

In order to minimize sampling noise without increasing the array of sampling capacitors C_{DAC}, the value of $\Delta t/\tau$ needs to be as large as possible. However, it is clear that an increase in Δt leads to a decrease in A and sampling speed. Reducing τ will increase power consumption and improve sampling speed. Therefore, the value of $\Delta t/\tau$ cannot be too large. This requires a compromise between noise performance, power consumption, and speed.

3.4. Improved Sampling Speed

The structure of the three-path dynamic strong-arm comparator can be used in the proposed improved second-order NS SAR ADC scheme shown in Figure 7. The widths of the three input pairs are W, 4 W, and 16 W. Compared to a classic one-path comparator, which has the same total input pair width of 21 W, the noise referred to the 1× path of the three-path comparator is 21 times larger but it is attenuated by 16 times due to NS. As a result, the in-band noise of the three-path comparator is 21/16 times larger than that of the one-path comparator. Therefore, the noise of the three-path comparator is still relatively large for high-resolution applications. In a word, the second-order fully-passive NS SAR ADC, which mainly reduces the quantization noise from (5), does not bring any benefits to the comparator noise. To improve the SNR, reducing the comparator noise is necessary. For example, the NS SAR [14] performs a single comparison for the first 9 bits (including 1 redundant bit) and only performs repeated comparisons for the LSB bit, which reduces the sampling rate by almost half. However, the technique proposed in this paper not only reduces the kT/C noise but also reduces the comparator noise n_7 from (21). The proposed technique has no extra cycles to average the comparator noise but increases the power consumption of an amplifier. A compromise between power consumption and speed is needed for the designer.

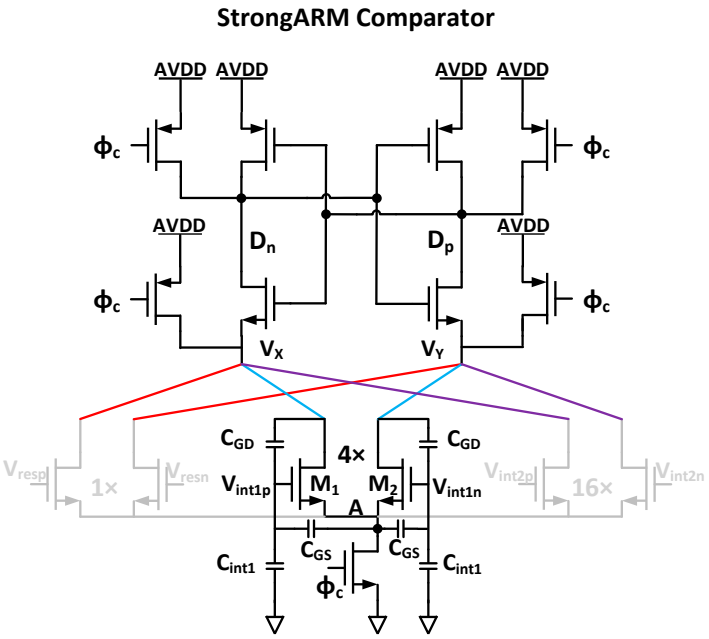

Figure 7. Three-path dynamic strong-arm comparator.

3.5. Kickback Noise

A three-path dynamic strong-arm comparator is shown in Figure 7. This is a strong-arm latch with three input pairs. The summation of the input voltage is realized by merging the currents of input pairs, which are controlled by the input voltage. The summation is controlled by the clock and does not require a static analog adder. However, V_{res}, V_{int1}, and V_{int2} need a fixed voltage gain ratio of 1:4:16. Because passive integrators do not provide voltage gain, it is best that the comparator provides the voltage gain ratio. Therefore, it is optimal for this comparator to have three input pairs. As a result, the relative gains can be realized by sizing the input pairs of the comparator into specific ratios. Setting the voltage gain ratio by sizing the input pairs is beneficial for PVT variation and mismatch. This does not require the involvement of amplifiers, which reduces the circuit complexity and saves power consumption.

The comparator is reset when φ_c is low. D_n, D_p, V_x, and V_Y are AVDD. When φ_c is high, V_x and V_Y begin to vary, resulting in one of D_n and D_p becoming low. The large voltage variations of V_x and V_Y are coupled through the parasitic capacitances of the input transistors to the input of the comparator. The input voltage will be disturbed, which will worsen the accuracy of the comparator. This disturbance is usually called kickback noise [24]. The kickback noise includes common noise and differential noise. The common kickback noise is coupled through C_{GS} (assume $C_{GS1} = C_{GS2} = C_{GS}$). The common kickback noise can usually be ignored since it has a common coupling point. The differential kickback noise is related to the difference V_{X-Y} between V_X and V_Y, as well as the ratio of C_{GD} to C_{int1} using the 4× path as an example. The detailed analysis of V_{X-Y} is shown in [25]. Assume $C_{GD1} = C_{GD2} = C_{GD}$; the differential kickback noise ε_k can be approximately expressed as:

$$\varepsilon_k \approx \frac{C_{GD}}{C_{int1} + C_{GD}} V_{X-Y} \approx \frac{C_{GD}}{C_{int1}} V_{X-Y} \tag{26}$$

Thus, the reduction in capacitance leads to a degradation of the kickback noise. If C_{int1} shrinks by a factor of A^2, the new kickback noise ε_k' will be approximately $A^2\varepsilon_k$. The input referred to as kickback noise is about $A\varepsilon_k$. If the capacitance is too small, the kickback noise will be the dominant noise. The kickback noise needs to be optimized when the capacitance becomes smaller. On the one hand, the size of the input transistors is optimized to reduce the parasitic capacitance C_{GD}. On the other hand, there is a trade-off between capacitance and kickback noise.

4. Performance Comparison

For the purpose of facilitating comparison, the single-ended second-order fully-passive NS SAR ADC, NS SAR ADC based on gain, and improved NS SAR ADC based on gain are equipped with three-path dynamic strong-arm comparators and only the effect of kT/C thermal noise on SNR is considered. In order to achieve the same SNR, the three different structures require different capacitance sizes. Therefore, N-bit binary weighted DACs (unit capacitance may vary) are used [26]. For the second-order fully-passive NS SAR ADC, the input capacitance is the total capacitance of N-bit binary weighted DAC. Thus, the input capacitance of the second-order fully-passive NS SAR ADC, named C_{it}, is:

$$C_{it} = 2^N C_0 \tag{27}$$

where C_0 is the unit capacitance of the second-order fully-passive NS SAR ADC.

The ratio between the input capacitance and the integrating capacitance is C_{it}:C_{res}:C_{int1}:C_{int2} = 3:1:3:3, shown in Figure 1a. Hence, the total capacitance of the second-order fully-passive NS SAR ADC, named C_{tt}, can be obtained.

$$C_{tt} = \frac{10 \times 2^N C_0}{3} \tag{28}$$

An open-loop amplifier is introduced in the structure of NS SAR ADC based on active gain. Meanwhile, a cancellation capacitor C_{nc} is introduced. The structure of NS SAR ADC based on active gain does not adopt the kT/C noise cancellation technique. In order to obtain the same SNR, the minimal input capacitance, named C_{ig_m}, is:

$$C_{ig\_m} = 2^N C_0 \tag{29}$$

Observing the z-domain transfer function of NS SAR ADC based on active gain, it can be known that the noise powers of $n_2 - n_6$ and n_9 associated with C_{nc}, C_{res}, C_{int1}, and C_{int2} are suppressed by the gain A^2. Therefore, C_{res}, C_{int1}, and C_{int2} can all be approximately scaled down by a factor of A^2 compared to that of the second-order fully-passive NS SAR ADC. The ratio of the integrating capacitances is C_{nc}:C_{res}:C_{int1}:C_{int2} = 3:1:3:3. Therefore, the minimal total capacitance of NS SAR ADC based on active gain, named C_{tg_m}, can be approximately expressed.

$$C_{tg\_m} \approx 2^N C_0 + \frac{10 \times 2^N C_0}{3} \times \frac{1}{A^2} \approx 2^N C_0 \left(\frac{10}{3A^2} + 1 \right) \tag{30}$$

On the basis of the structure of NS SAR ADC based on active gain, the kT/C noise cancellation technique is introduced into the structure of improved NS SAR ADC based on active gain. It can be found that the DAC sampling noise is suppressed by a factor of $e^{\Delta t/\tau}$ from (21). In other words, the DAC sampling noise power is suppressed by a factor of $e^{2\Delta t/\tau}$. The input capacitance of the structure of improved NS SAR ADC based on active gain can be reduced by a factor of $e^{2\Delta t/\tau}$ compared to that of the second-order fully-passive NS SAR in order to obtain the same SNR. Therefore, the minimal input capacitance of the structure of improved NS SAR ADC, named C_{iig_m}, is:

$$C_{iig\_m} \approx \frac{2^N C_0}{e^{2\Delta t/\tau}} \tag{31}$$

Therefore, the minimal total capacitance of improved NS SAR ADC based on active gain, named C_{tig_m}, can be approximately expressed as follows:

$$C_{tig\_m} \approx 2^N C_0 \left(\frac{10}{3A^2} + \frac{1}{e^{2\Delta t/\tau}} \right) \tag{32}$$

In order to compare (27) and (28) and (29)–(32), the expressions all contain C_0, which is the unit capacitance of the second-order fully-passive NS SAR ADC. However, this does not mean that the unit capacitance of NS SAR ADC based on active gain and improved NS SAR ADC based on gain is C_0, and the unit capacitance of NS SAR ADC based on active gain and improved NS SAR ADC based on gain can be reasonably assigned based on the total capacitance and input capacitance.

The minimal C_{total} and input cap are shown by (27)–(32). However, non-ideal factors will limit the C_{total} and input cap in the process of circuit implementation, especially the C_{total}. Taking the kickback noise as an example, if C_{int1} is reduced by A^2 times, the input-referred kickback noise associated with C_{int1} will be increased by about A times from (26). If C_{int1}, C_{int2}, C_{res}, and C_{nc} are all reduced by A^2 times, the input-referred kickback noise will be increased by about A times. Worsened kickback noise may lead to the deterioration of the SNR. This will limit C_{int1} from shrinking by a factor of A^2, which results in C_{total} not reaching the minimal C_{total}. Moreover, the influence of non-ideal factors such as clock feedthrough and charge injection will gradually increase with the decrease in C_{total}. Therefore, the selection of C_{total} also needs to consider the influence of non-ideal factors in the circuit implementation. However, even considering non-ideal factors, the C_{total} of second-order fully-passive NS SAR is large, and the C_{total} of improved NS SAR ADC base is small when the same SNR is achieved. Compared to the other two structures' C_{total}, the C_{total} of NS SAR based on active gain is medium. The capacitance

value reflects the circuit's ability to suppress kT/C noise. The smaller the capacitance used to achieve the same performance, the better the circuit performance of suppressing kT/C noise. Therefore, capacitance is also an important parameter for SAR ADCs. Only the architecture of improved NS SAR ADC based on gain adopts the kT/C noise cancellation technique, so the input capacitance of this structure is minimal. This alleviates the difficulty of designing the input buffer. Active gain is introduced in the structures of NS SAR ADC based on gain and improved NS SAR ADC based on gain to decrease the comparator noise and the kT/C noise excluding kT/C sampling noise. The comparator noise is suppressed by the open-loop amplifier, which makes it unnecessary to use extra clock cycles to reduce the comparator noise. This improves the sample rate, which is a parameter characterizing the speed of the ADC. However, the open-loop amplifier used in the proposed architectures also consumes static power, which is not friendly to the overall power consumption and Schreier Figure of Merit (FoM) or Walden FoM. Therefore, power consumption is also an important parameter to compare. Performance comparison and summary of the single-ended second-order fully-passive NS SAR ADC, NS SAR ADC based on gain and improved NS SAR ADC based on gain is shown in Table 1.

Table 1. Performance comparison and summary.

Architecture	Second-Order Fully-Passive NS SAR	NS SAR Based on Active Gain	Improved NS SAR Based on Activegain
C_{total}	large	medium	small
ADC Input Cap	$2^N C_0$	$2^N C_0$	$\frac{2^N C_0}{e^{2\Delta t/\tau}}$
kT/C Suppressed?	×	√	√
Comparator Noise Suppressed?	√	√	√
Extra Cycles?	√	×	×
Static Power	×	√	√

5. Conclusions

This paper proposes a novel second-order passive NS SAR ADC based on active gain, which effectively suppresses the negative effect of kT/C on SNR. Compared to the second-order fully-passive NS SAR ADC, an open-loop amplifier, a cancellation capacitor C_{nc}, and C_{nc} sampling switch S_2 are added to the proposed scheme. The open-loop amplifier mitigates both kT/C noise and comparator noise, improving sampling speed while significantly reducing capacitance. Although smaller capacitance leads to reduced dynamic power consumption, the introduction of the open-loop amplifier results in static power consumption. This necessitates a trade-off between performance and power consumption. However, this scheme is still a good choice for high-speed and high-resolution applications.

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References

1. Elzakker, M.v.; Tuijl, E.v.; Geraedts, P.; Schinkel, D.; Klumperink, E.A.M.; Nauta, B. A 10-bit Charge-Redistribution ADC Consuming 1.9 μW at 1 MS/s. *IEEE J. Solid-State Circuits* **2010**, *45*, 1007–1015. [CrossRef]
2. Liu, C.C.; Chang, S.J.; Huang, G.Y.; Lin, Y.Z.; Huang, C.M. A 1V 11fJ/conversion-step 10bit 10MS/s asynchronous SAR ADC in 0.18μm CMOS. In Proceedings of the 2010 Symposium on VLSI Circuits, Honolulu, HI, USA, 16–18 June 2010; pp. 241–242.
3. Shen, Y.; Tang, X.; Shen, L.; Zhao, W.; Xin, X.; Liu, S.; Zhu, Z.; Sathe, V.S.; Sun, N. A 10-bit 120-MS/s SAR ADC With Reference Ripple Cancellation Technique. *IEEE J. Solid-State Circuits* **2020**, *55*, 680–692. [CrossRef]

4. Xu, D.G.; Xu, K.K.; Xu, S.L.; Liu, L.; Liu, T. A System-Level Correction SAR ADC with Noise-Tolerant Technique. *J. Circuits Syst. Comput.* **2018**, *27*, 1850202. [CrossRef]
5. Obata, K.; Matsukawa, K.; Miki, T.; Tsukamoto, Y.; Sushihara, K. A 97.99 dB SNDR, 2 kHz BW, 37.1 µW noise-shaping SAR ADC with dynamic element matching and modulation dither effect. In Proceedings of the 2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits), Honolulu, HI, USA, 15–17 June 2016; pp. 1–2.
6. Shu, Y.S.; Kuo, L.T.; Lo, T.Y. An Oversampling SAR ADC With DAC Mismatch Error Shaping Achieving 105 dB SFDR and 101 dB SNDR Over 1 kHz BW in 55 nm CMOS. *IEEE J. Solid-State Circuits* **2016**, *51*, 2928–2940. [CrossRef]
7. Chen, Z.; Miyahara, M.; Matsuzawa, A. A 2nd order fully-passive noise-shaping SAR ADC with embedded passive gain. In Proceedings of the 2016 IEEE Asian Solid-State Circuits Conference (A-SSCC), Toyama, Japan, 7–9 November 2016; pp. 309–312.
8. Li, S.; Qiao, B.; Gandara, M.; Pan, D.Z.; Sun, N. A 13-ENOB Second-Order Noise-Shaping SAR ADC Realizing Optimized NTF Zeros Using the Error-Feedback Structure. *IEEE J. Solid-State Circuits* **2018**, *53*, 3484–3496. [CrossRef]
9. Fredenburg, J.A.; Flynn, M.P. A 90-MS/s 11-MHz-Bandwidth 62-dB SNDR Noise-Shaping SAR ADC. *IEEE J. Solid-State Circuits* **2012**, *47*, 2898–2904. [CrossRef]
10. Guo, W.; Zhuang, H.; Sun, N. A 13b-ENOB 173dB-FoM 2nd-order NS SAR ADC with passive integrators. In Proceedings of the 2017 Symposium on VLSI Circuits, Kyoto, Japan, 5–8 June 2017; pp. C236–C237.
11. Miki, T.; Morie, T.; Matsukawa, K.; Bando, Y.; Okumoto, T.; Obata, K.; Sakiyama, S.; Dosho, S. A 4.2 mW 50 MS/s 13 bit CMOS SAR ADC With SNR and SFDR Enhancement Techniques. *IEEE J. Solid-State Circuits* **2015**, *50*, 1372–1381. [CrossRef]
12. Kuo, H.L.; Lu, C.W.; Chen, P. An 18.39 fJ/Conversion-Step 1-MS/s 12-bit SAR ADC With Non-Binary Multiple-LSB-Redundant and Non-Integer-and-Split-Capacitor DAC. *IEEE Access* **2021**, *9*, 5651–5669. [CrossRef]
13. Jiao, Z.; Luo, H.; Zhang, J.; Wang, X.; Chen, L.; Zhang, H. An 84dB-SNDR 1-0 Quasi-MASH NS SAR with LSB Repeating and 12-bit Bridge-Crossing Segmented CDAC. In Proceedings of the 2023 IEEE Custom Integrated Circuits Conference (CICC), San Antonio, TX, USA, 23–26 April 2023; pp. 1–2.
14. Harpe, P.; Cantatore, E.; Roermund, A.v. A 10b/12b 40 kS/s SAR ADC with Data-Driven Noise Reduction Achieving up to 10.1b ENOB at 2.2 fJ/Conversion-Step. *IEEE J. Solid-State Circuits* **2013**, *48*, 3011–3018. [CrossRef]
15. Hwang, Y.H.; Song, Y.; Park, J.E.; Jeong, D.K. A Fully Passive Noise-Shaping SAR ADC Utilizing Last-Bit Majority Voting and Cyclic Dynamic Element Matching Techniques. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2022**, *30*, 1381–1390. [CrossRef]
16. Zhuang, H.; Guo, W.; Liu, J.; Tang, H.; Zhu, Z.; Chen, L.; Sun, N. A Second-Order Noise-Shaping SAR ADC with Passive Integrator and Tri-Level Voting. *IEEE J. Solid-State Circuits* **2019**, *54*, 1636–1647. [CrossRef]
17. Chen, Z.; Miyahara, M.; Matsuzawa, A. A 9.35-ENOB, 14.8 fJ/conv.-step fully-passive noise-shaping SAR ADC. In Proceedings of the 2015 Symposium on VLSI Circuits (VLSI Circuits), Kyoto, Japan, 17–19 June 2015; pp. C64–C65.
18. Guo, W.; Sun, N. A 12b-ENOB 61µW noise-shaping SAR ADC with a passive integrator. In Proceedings of the ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference, Lausanne, Switzerland, 12–15 September 2016; pp. 405–408.
19. Kandala, M.; Sekar, R.; Chenglong, Z.; Haibo, W. A low power charge-redistribution ADC with reduced capacitor array. In Proceedings of the 2010 11th International Symposium on Quality Electronic Design (ISQED), San Jose, CA, USA, 22–24 March 2010; pp. 44–48.
20. Zhan, M.; Jie, L.; Tang, X.; Sun, N. A 0.004mm^2 200MS/S Pipelined SAR ADC with kT/C Noise Cancellation and Robust Ring-Amp. In Proceedings of the 2022 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 20–26 February 2022; pp. 164–166.
21. Liu, J.; Tang, X.; Zhao, W.; Shen, L.; Sun, N. A 13-bit 0.005-mm^2 40-MS/s SAR ADC With kT/C Noise Cancellation. *IEEE J. Solid-State Circuits* **2020**, *55*, 3260–3270. [CrossRef]
22. Li, H.; Youssef, M.; Shen, Y.; Cantatore, E.; Harpe, P. Analysis of the Sampling Noise Cancellation Technique in a Track-and-Hold Amplifier. In Proceedings of the 2021 28th IEEE International Conference on Electronics, Circuits, and Systems (ICECS), Dubai, United Arab Emirates, 28 November–1 December 2021; pp. 1–5.
23. Xu, K. Silicon electro-optic micro-modulator fabricated in standard CMOS technology as components for all silicon monolithic integrated optoelectronic systems*. *J. Micromech. Microeng.* **2021**, *31*, 054001. [CrossRef]
24. Figueiredo, P.M.; Vital, J.C. Kickback noise reduction techniques for CMOS latched comparators. *IEEE Trans. Circuits Syst. II Express Briefs* **2006**, *53*, 541–545. [CrossRef]
25. Razavi, B. The StrongARM Latch [A Circuit for All Seasons]. *IEEE Solid-State Circuits Mag.* **2015**, *7*, 12–17. [CrossRef]
26. Wu, K.J.; Li, J.; Wang, X.Z.; Ning, N.; Xu, K.K.; Yu, Q. Switching sequence optimization for gradient errors compensation in the current-steering DAC design. *Microelectron. J.* **2020**, *95*, 104662. [CrossRef]