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Isolated Gate Driver for Medium Voltage Applications Using a Single Structure

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Abstract: According to the International Electrotechnical Commission, medium voltage ranges from 1 kV to 36 kV. In this voltage range, the field of power electronics has been focusing on developing power converters with high efficiency. Converters for such applications include solid-state transformers, energy storage systems for vehicle charging, electric aircraft, etc. Power ranges could reach tens to hundreds of kilowatts at relatively high frequency (10–50 kHz). Currently, there are no high-frequency power semiconductors capable of switching these voltage levels. Instead of using a single power switch, a string of power switches is used. The upper switches in the string require special attention because they need the highest isolation capabilities and a floating control signal and power supply for the gate driver. Many techniques have been proposed to accomplish this, but they commonly use separate circuits for the control signal and the power supply, increasing the cost, size, and complexity of the gate driver. This paper presents a gate driver for medium voltage with high-voltage isolation capabilities in a single structure for the control signal and the power supply. The proposed gate driver uses a resonant converter that transmits power within the gate driver information. A demodulator separates the gate driver information from the power signal, obtaining the power supply and the control signal for the switch. The paper includes simulation and experimental results that demonstrate the viability of the proposal. The experimental results show the principal features of the gate driver, achieving improvements in complexity, isolation capabilities, and both rise and fall times for large input capacitances of power semiconductor switches. The proposed gate driver presents a rise time of 44 ns and a fall time of 46 ns for the gate input capacitance of currently available SiC MOSFETs. The isolation barrier uses a 25 mm air gap, achieving an isolation capability of approximately 68.2 kV, which exceeds the requirements for MV applications.

Keywords: medium voltage gate driver; resonant circuits

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1. Introduction

The need to manage high-power applications with acceptable efficiency levels has encouraged the development of medium voltage power electronic converters. One of the most significant challenges for these converters is the voltage insulation capability, which must be guaranteed to operate at medium voltage levels. Traditionally, galvanic isolation is achieved with dry transformers. These transformers have small air leaks, such as cavities and delamination, that could lead to partial discharge and damage the insulation over time.

Medium Voltage (MV) Silicon Carbide (SiC) devices with high blocking voltages (10–15 kV) have been developed in recent years [1–4], allowing for a reduction in the number of power switches and gate drivers connected in medium voltage applications compared to devices with lower blocking voltages. These devices are still in the initial stages of development but, with advancements in power electronics, they are expected to meet such applications at lower costs. Nevertheless, even with the prospect of new developments in power semiconductors, the need to place devices in series connection maintains the requirement for isolated gate drivers, which is the primary focus of this work.

Some applications where MV SiC MOSFETs or IGBTs are used include high-power electric vehicle battery charging facilities [5,6], Solid-State Transformers (SSTs) for medium voltage distribution systems [7,8], traction systems [9,10], future all-electric aircraft [11,12], or naval distribution electric systems [13]. All these applications handle large amounts of power at medium or high voltage, which implies that both the semiconductors used and the elements of the circuit need to have special characteristics, one of the most significant being the high blocking voltage. The current technological limitations in terms of blocking voltage are an actual problem for semiconductors. All these semiconductors are connected in special arrangements to distribute the controlled voltage.

Using semiconductors in medium voltage networks also brings a series of additional challenges for the gate driver circuit, such as ensuring sufficient isolation between the control and power stages, feeding the semiconductors with floating signals, and ensuring correct synchronization between them. In medium voltage systems, standard methods of isolation still face some challenges. New gate driver topologies for medium voltage have been developed to meet the aforementioned insulation requirements [14,15], focusing on reliability in transmitting gating signal and power supply for the floating gate driver, as well as providing an attractive solution in terms of cost and complexity [16].

The transmission of control signals and power supply through an insulation barrier poses a technical challenge in many applications [17]. Various solutions for controlling semiconductors in high voltage applications have been proposed, for example, a combination of optocouplers and galvanic insulation acting as an isolation barrier for controlling power semiconductors in a solid-state transformer [18]. The optocoupler circuit transmits control signals to command the MV semiconductor, while power supply is transmitted using a specialized insulation transformer that provides the required energy supply of the gate driver on the medium voltage side. Another solution proposed in [19] employs galvanic isolation for both power supply and control signals, allowing independent data and power transfer using a specialized isolation transformer. This driver concept utilizes a single E-core to transfer the required power and control signals between the primary and secondary sides, sharing the same core. In [20], a fiber optic is proposed to transmit the control signal, whereas the power supply is through galvanic isolation. The isolated power supply is transmitted through a dielectric barrier; on the primary side, a DC voltage-to-current converter is used whereas, on the secondary side, a DC current-to-voltage converter is employed.

Wireless gate driver solutions are becoming increasingly attractive for medium voltage applications [21,22]. These gate drivers use air as a dielectric barrier, which offers significant advantages over other dielectrics, such as the absence of partial discharges, a common cause of insulation breakdown. Another advantage of using air as a dielectric is its practically zero cost. In wireless gate drivers, both control signal and power supply are transmitted through the air using antennas or magnetic couplings. The primary side transmits power and gate signals using a specialized circuit, while the receiving side obtains both signals (control and power) to control the power switching devices.

It is important to note that all reported solutions transmit control signals and power supply separately. They utilize one circuit for transmitting the control signal and another for power transmission (see Figure 1). Each power switch in the string must have its own gate driver.

This article introduces a high-isolation capability gate driver for floating power switches (SiCs, IGBTs, or MOSFETs) connected in a string configuration used in MV applications. The isolation is based on air, which fulfills the requirements in the MV range. The proposed gate driver transmits both the gate signal and the power needed by the floating power switch in a single structure (isolated resonant converter), unlike previous proposals that use separate structures or isolation techniques. The novel gate driver modulates the duty cycle (gate signal) into the control signal of an air-isolated resonant converter (power). On the secondary side, a demodulator circuit separates the gate signal. Then, the isolated power and the gate signal trigger the floating power switches. Figure 2 shows the general

structure of the proposed gate driver. Each power switch in the string requires a similar gate signal block.

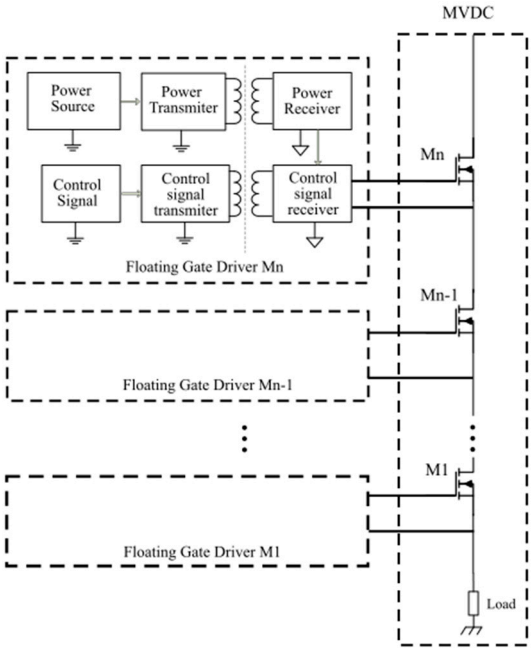


Figure 1. MV simplified gate driver scheme, with independent power and gate signal circuits [17].

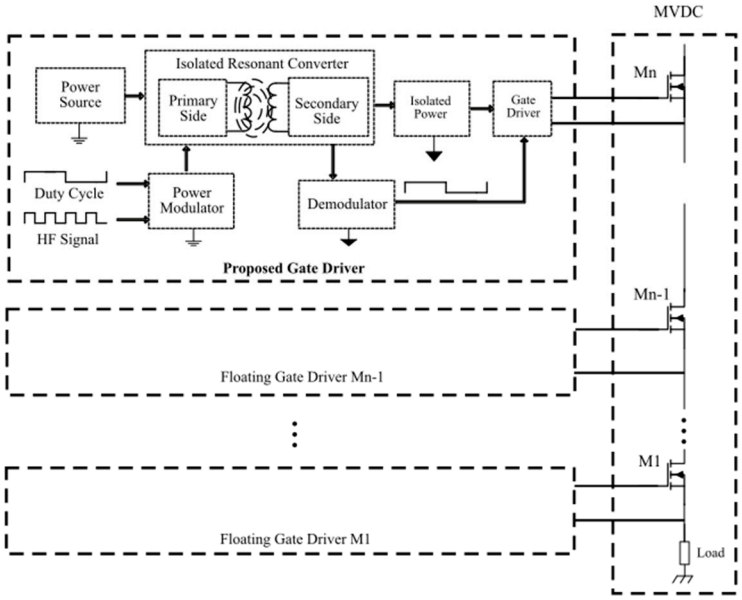


Figure 2. Simplified proposed gate driver scheme with single insulating structure.

Section 2 will discuss the gate driver in detail. In Section 3, the design process of the power stage is described. Section 4 presents a design example whereas, in Section 5, the experimental results and discussion are presented. Finally, Section 6 highlights the conclusions, advantages and limitations of the proposed gate driver.

2. Proposed Gate Driver

The proposed control strategy will be implemented in the power stage as shown in Figure 3 [23]. The resonant converter maintains resonance regardless of the input voltage amplitude. Resonance conditions are determined by the reactance ratio of circuit elements and the switching frequency.

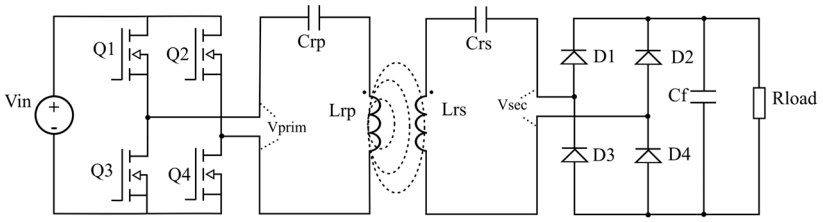


Figure 3. Resonant converter employed as the transmission stage.

The control strategy is based on modulation of the power signal with the desired duty cycle, then transmission to the secondary side. Essentially, the strategy combines the required duty cycle (Figure 4a) with a high-frequency signal (Figure 4b) to generate gate signals for the Q1–Q4 power MOSFETs (Figure 4c). This switching pattern causes the amplitude of the supply voltage for the resonant tank to change between unipolar and bipolar signals (Figure 4d), transmitting the power signal information within the duty cycle, as shown in Figure 4e. The power signal has lower amplitude during the ON-time of the original duty cycle and higher amplitude during the OFF-time, depending on whether the resonant tank input voltage is unipolar or bipolar.

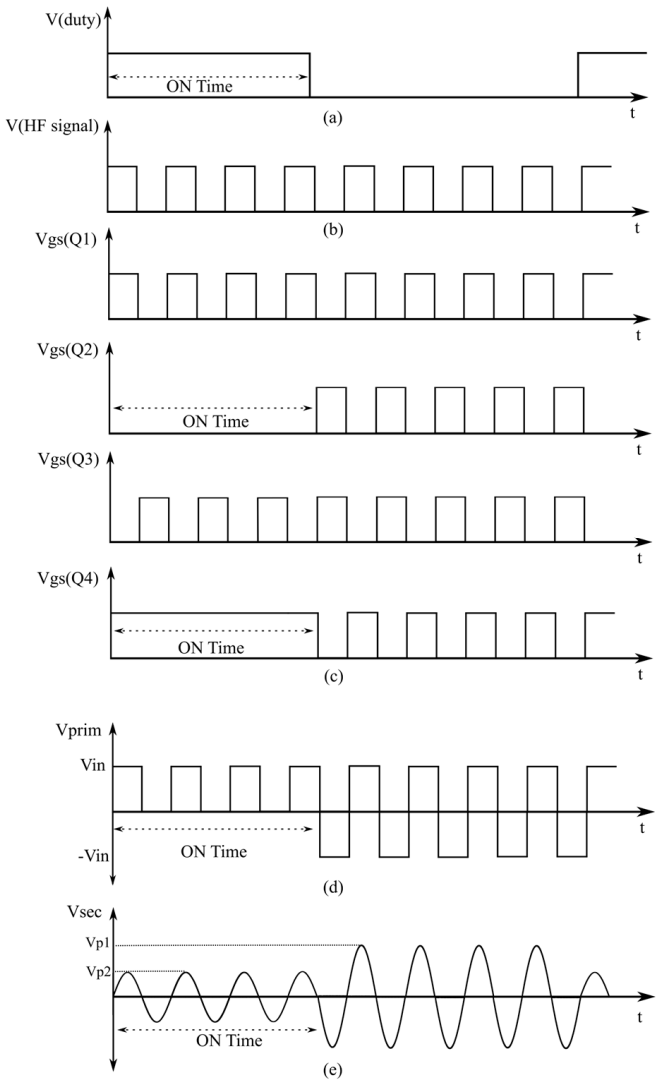


Figure 4. Theoretical waveforms, (**a**) original duty cycle, (**b**) high-frequency signal, (**c**) control signal for Q1–Q4 MOSFETs, (**d**) input voltage for resonant converter, (**e**) output voltage in resonant converter.

A demodulator circuit samples the transmitted power signal to recover the duty cycle information. The demodulator circuit retrieves the duty cycle information from the output voltage of the resonant tank. Figure 5 depicts a possible implementation of the demodulator circuit. It subtracts the rectified lower-amplitude signal from a sample of the transmitted power signal. Then, a near-zero comparator generates a high-frequency square waveform, which is then filtered to produce the inverted original duty cycle. This circuit could be improved for higher precision on the duty cycle recovery.

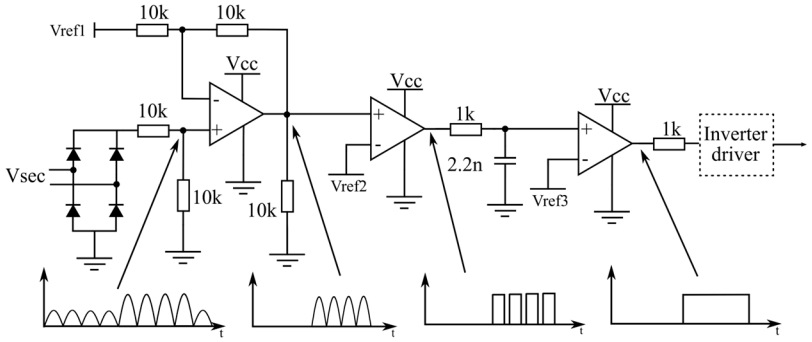


Figure 5. Implementation of the demodulator circuit.

3. Power Stage Driver Description

Considering both a resonant tank with a high-quality factor and operation close to the resonance frequency, the circuit behaves as a filter. Under these conditions, the power source and the full-bridge bridge power semiconductors can be treated like a pure sinusoidal AC source, as shown Figure 6.

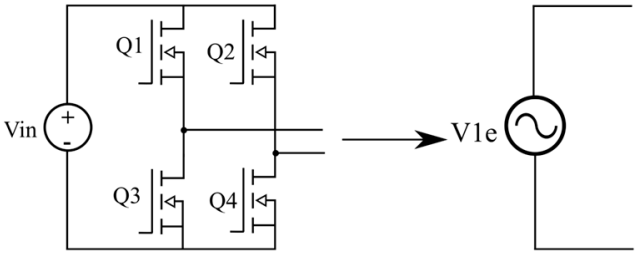


Figure 6. Simplified DC power source and inverter power stage of the resonant converter.

The amplitude is the first harmonic at the switching frequency. During the on-time of the original duty cycle, a unipolar switching pattern is applied, so the equivalent sinusoidal power source is:

$$V_{1e_on_time} = \frac{2V_{in}}{\pi} sin(2\pi f_{s,res_conv} t) \quad (1)$$

During the off-time of the original duty cycle, the equivalent sinusoidal power source is:

$$V_{1e_off_time} = \frac{4V_{in}}{\pi} sin(2\pi f_{s,res_conv} t) \quad (2)$$

where:

$V_{1e_on_time}$ is the equivalent sinusoidal power source during the on-time

$V_{1e_off_time}$ is the equivalent sinusoidal power source during the off-timeV_{in} is the DC voltage source

f_{s,res_conv} is the switching frequency of the resonant converter

The transmitting coil, drawn out as a transformer in the resonant converter in Figure 3, could be simplified to the equivalent inductive coupling circuit using the mutual inductance and self-inductance concepts. The transmitting-coils equivalent circuit is shown in Figure 7.

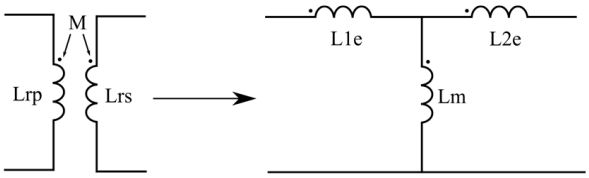


Figure 7. Equivalent inductive coupling. Lrp is the transmitting coil, Lrs is the receiving coil, L1e is the primary auto-inductance coil, L2e is the secondary auto-inductance coil, Lm is the mutual inductance.

The self-inductances L1e, L2e and the mutual inductance Lm values are obtained by measuring a built-in transmitting structure. Considering the above simplifications, an equivalent circuit for the resonant converter of Figure 3 is shown in Figure 8.

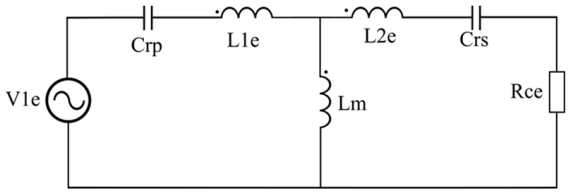


Figure 8. Resonant circuit partially reduced. R_{ce} is the equivalent load resistor.

As mentioned above, the resonance frequency of the tank is selected as equal to the switching frequency of the converter. Through the following simplifications, the equivalent resonant circuit shown in Figure 8 can be reduced to the equivalent circuit shown in Figure 9.

$$Z_1 = R_{ce} + j(X_{L2e} - X_{Crs}) \tag{3}$$

$$Z_2 = jX_{Lm} \tag{4}$$

$$Z_3 = \frac{Z_1 Z_2}{Z_1 + Z_2} \tag{5}$$

$$R_{equiv} = \mathrm{Re}(Z_3) \tag{6}$$

$$X_{equiv} = \mathrm{Im}(Z_3) + X_{L1e} \tag{7}$$

$$\mathrm{R}_{equiv} = \frac{R_{ce}(X_{Lm} + X_{L1e})(X_{Lm} - X_{Crs} + X_{L2e}) - R_{ce}[X_{L1e}(X_{Lm} - X_{Crs} + X_{L2e}) - X_{Lm}(X_{Crs} - X_{L2e})]}{R_{ce}^2 + (X_{Lm} - X_{Crs} + X_{L2e})^2} \tag{8}$$

$$X_{equiv} = \frac{R_{ce}^2(X_{Lm} + X_{L1e}) + [X_{L1e}(X_{Lm} - X_{Crs} + X_{L2e}) - X_{Lm}(X_{Crs} - X_{L2e})](X_{Lm} - X_{Crs} + X_{L2e})}{R_{ce}^2 + (X_{Lm} - X_{Crs} + X_{L2e})^2} \tag{9}$$

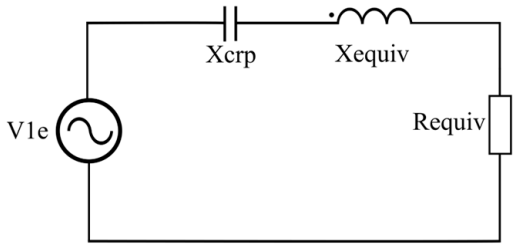


Figure 9. Equivalent circuit of the resonant tank of Figure 3.

The design procedure begins with the input parameters: input voltage, maximum power (which implies the input capacitance of the power switches to be triggered and additional power due to components in the secondary circuit), target gate driver voltage, and parameters of the transmitting and receiving coils (according to the required isolation). These parameters are then applied to the design equations shown in Table 1.

Table 1. Design equations of the resonant converter.

Parameter	Description	Equation
V_{p2}	Fundamental voltage (max)	$\frac{2V_{in}}{\pi}$
V_o	Output voltage of the resonant converter (max)	V_{ocd}
R_{ce}	Equivalent load resistor	$\frac{{V_{ocd}}^2}{2P_{o\max}}$
X_{Lm}	Mutual reactance	$2\pi f_{s,res_conv} L_m$
X_{L1e}	Reactance of self-inductance 1	$2\pi f_{s,res_conv} L_{1e}$
X_{L1e}	Dispersion reactance on secondary	$2\pi f_{s,res_conv} L_{2e}$
R_{equiv}	Equivalent serial resistance	Equation (8)
X_{equiv}	Equivalent serial reactance	Equation (9)
${R_{equiv}}^*$	Resistance serial equivalent value	$\frac{{V_{p2}}^2}{2P_{o\max}}$
X_{Crs}	Secondary capacitor reactance	$R_{equiv} - {R_{equiv}}^* = 0$
C_{rs}	Secondary capacitor	$\frac{1}{2\pi f_s X_{Crs}}$
X_{Crp}	Primary capacitor reactance	$X_{Crp} = X_{equiv}$
C_{rp}	Primary capacitor	$\frac{1}{2\pi f_s X_{equiv}}$
Q	Quality factor	$\frac{X_{equiv}}{R_{equiv}}$

4. Gate Driver Design Example

High-frequency power semiconductors with high blocking voltage are still under development (10–15 kV), and not all their technical characteristics are available. One of the commercially available MOSFETs in SiC technology is the CPM2-1700-0045B MOSFET (1700 V—72 Amp—$R_{DS(on)}$ 45 mΩ), commercialized by CREE™, Durham, NC, USA. From the viewpoint of the gate driver, the most important parameter is the gate input capacitance C_{iss}; for the CPM2-1700-0045B, 3672 pF is a typical value.

To calculate the approximate gate driver power, let us assume V_{GS} = 12 volts, a maximum load capacitance of 33 nF (much greater than the typical value of the CPM2-1700-0045B CREE™ SiC MOSFET), and a maximum switching frequency of 30 kHz. The approximate gate driver power can be evaluated using Equation (10).

$$P_{Qc} \approx \frac{{V_{driver}}^2}{X_{Ciss}} = \frac{{V_{driver}}^2}{\frac{1}{2\pi f_{s\max} C_{iss}}} = {V_{driver}}^2 2\pi f_{s\max} C_{iss} \quad (10)$$

$$P_{Qc} = 12^2 \times 2 \times \pi \times 30 \times 10^3 \times 33 \times 10^{-9} \approx 0.9 \text{ W} \quad (11)$$

Additionally, the power consumption of the secondary circuits must be considered; let us assume a maximum power of 2 watts.

Equation (12) calculates the distance between the transmitting and receiving coils based on the required isolation and the dielectric strength between the coils.

$$d_{dist} = \frac{V_{isol_req}}{D_{diel_rig}} \quad (12)$$

where:

d_{dist} is the distance between transmitting and receiving coil

V_{isol_req} is the voltage isolation required

D_{diel_rig} is the dielectric rigidity.

In medium voltage applications, the voltage to be isolated can reach 36 kV. Let us consider a voltage to be isolated as 1.5 times the MV, which is 54 kV. In the proposed gate

driver, air is used as the insulating barrier, which has a dielectric rigidity of 27.28 kV per cm when plane–plane electrodes are used [24]. Therefore, the distance between coils is:

$$d_{dist} = \frac{54\text{ kV}}{27.28\text{ kV/cm}} \approx 2.0\text{ cm} \quad (13)$$

An insulation distance of 25 mm is used, which provides at least 68 kV of insulation. For the transmitting and receiving coils, a commercially available coil will be used (760308141 plain coil from Wurth Electronics™, Waldenburg, Germany). Under a distance between coils of 25 mm, the transmitting structure was tested, giving a magnetizing inductance of 10.3 µH and self-inductances of 9.2 µH. Table 2 shows the parameters for the design of an example of the proposed MV wireless gate driver.

Table 2. Parameters used to design an example of the proposed floating gate driver.

Parameter	Description	Value
P_o	Output power	2 W
V_{in}	Input voltage	12 V
V_{ocd}	Output voltage	12 V
f_{s,res_conv}	Switching frequency of the resonant converter	800 kHz
L_m	Magnetizing inductance	10.3 µH
V_{isol_req}	Isolation target with air as barrier	72 kV
L_{1e}	Self-inductance 1	9.2 µH
L_{2e}	Self-inductance 2	9.2 µH

Within the design parameters in Table 2, and following the design procedure of Table 1, the resulting values are shown in Table 3.

Table 3. Resulting values of the design procedure.

Parameter	Description	Equation
V_{p2}	Fundamental voltage (max)	7.64 V
V_o	Output voltage of the resonant converter (max)	12 V
R_{ce}	Equivalent load resistor	36 Ω
X_{Lm}	Mutual reactance	5.52 Ω
X_{L1e}	Reactance of self-inductance 1	46.22 Ω
X_{L2e}	Dispersion reactance on secondary	46.22 Ω
$R_{equiv}{}^*$	Resistance serial equivalent value	14.6 Ω
X_{Crs}	Secondary capacitor reactance	51.9 Ω
C_{rs}	Secondary capacitor	3.83 nF
X_{Crp}	Primary capacitor reactance	51.7 Ω
C_{rp}	Primary capacitor	3.84 nF
Q	Quality factor	61

Figure 10 shows the gate driver used for simulation purposes, indicating the values resulting from the design procedure. To verify the operation of the gate driver, a simulation was carried out using the software SIMetrix/SIMPLIS™ V7.1 with the values shown in Figure 10.

Figure 11 shows the input current and voltage waveforms of the resonant converter under a condition of a 50% duty cycle. During the on-time of the duty cycle, the transmitted voltage is unipolar whereas, during the off-time, the transmitted voltage is bipolar. This signal is transmitted from the primary coil to the secondary. The demodulator circuit differentiates the unipolar from the bipolar waveform, recovering the power switch gate driver information.

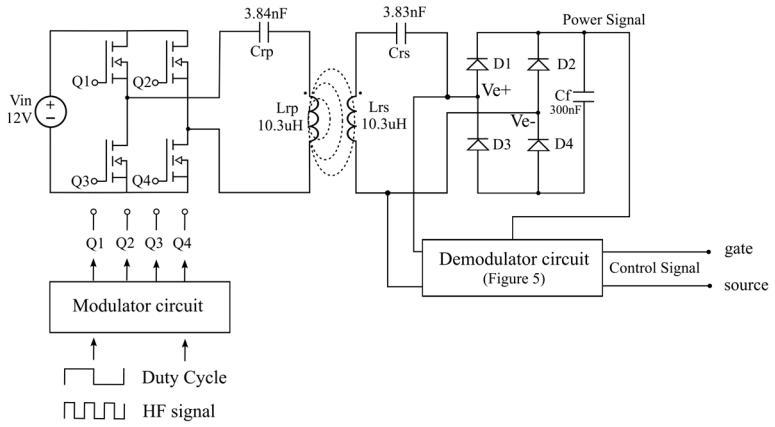


Figure 10. Gate driver design example.

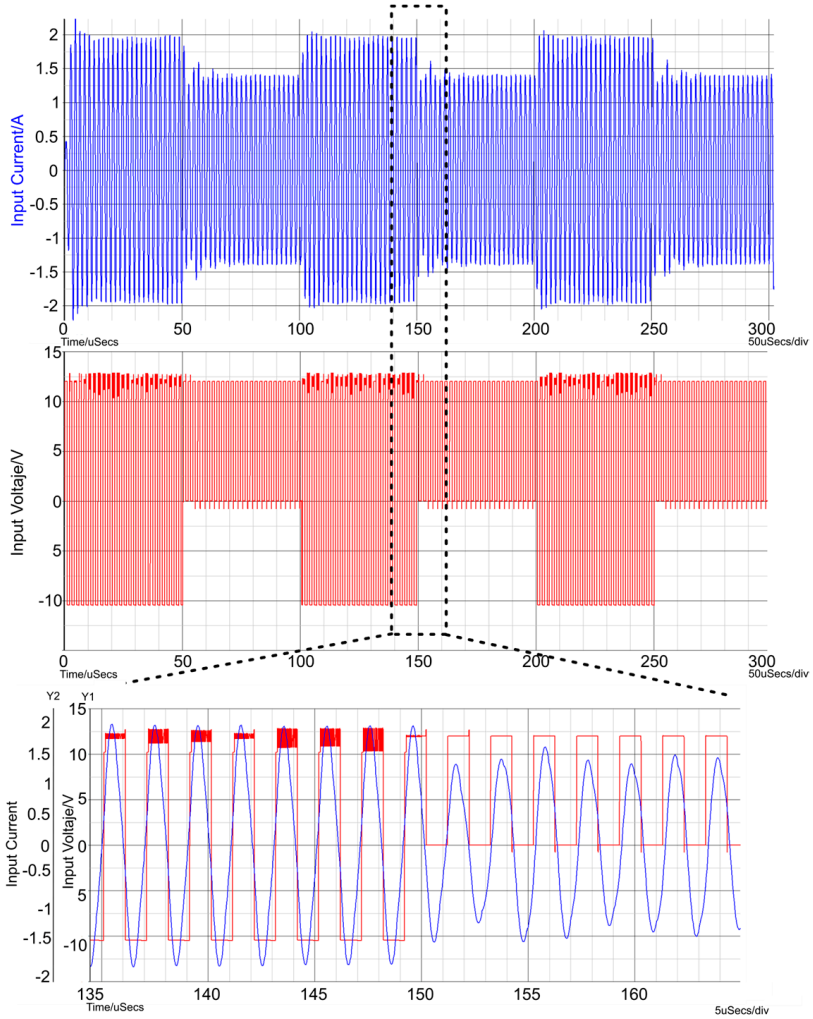


Figure 11. Input current and voltage waveforms in the resonant converter under 50% duty cycle.

5. Experimental Results and Discussion

This section presents the experimental results under different operating conditions and discusses the performance of the proposed gate driver. Parameters, such as duty cycle transmission, rise time, fall time, and duty cycle delay, typically provided in data sheets, will be shown.

Table 4 shows the main test conditions used to validate the operation of the proposed gate driver. The switching frequency of the power switch is 10 kHz, while the resonant

converter switching frequency is 800 kHz. A higher resonant converter switching frequency relative to the power switch results in higher precision of the transmitted duty cycle, but faster devices in the demodulator circuit must be used.

Table 4. Test condition of the gate driver.

Parameter	Value
Switching frequency of the power switch under test	10 kHz
Switching frequency of the resonant converter	800 kHz
Gate driver voltage	12 V
Air gap	25 mm (68 kV of isolation)
Maximum load capacitance	33 nF

Figure 12 shows the experimental prototype. The lower part is the transmitting circuit, while the upper part is the receptor, which includes the demodulator, power conditioning, and driver circuits.

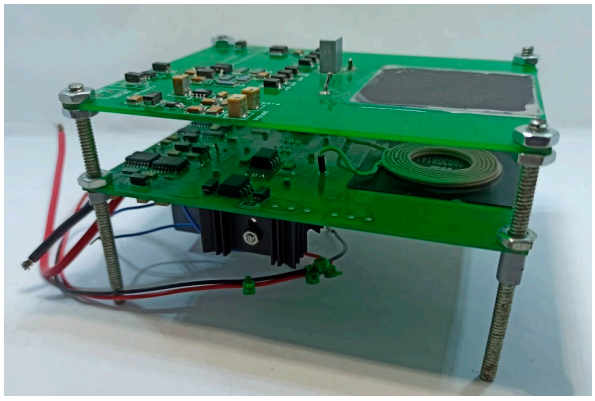


Figure 12. Proposed gate driver.

Figure 13 shows the test circuit used for obtaining the gate driver performance. The load capacitor emulates the MOSFET gate input capacitance C_{iss}.

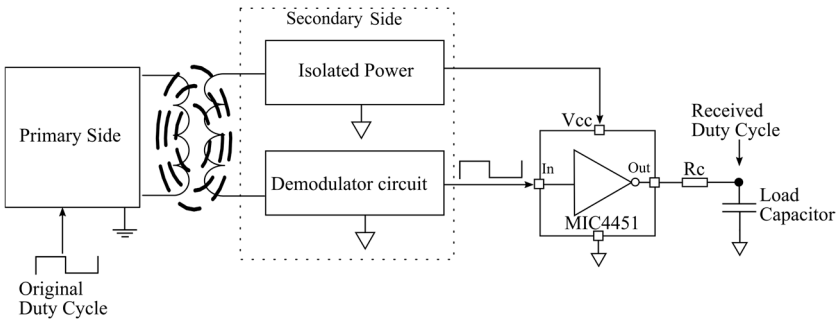


Figure 13. Gate driver test circuit.

5.1. Duty Cycle Transmission

The duty cycle transmission test determines the differences between the duty cycle sent from the gate driver primary side (original duty cycle) and the received duty cycle on the secondary side. Figure 14 shows the original and received duty cycles emulating the MOSFET gate input capacitance C_{iss} with a 3.3 nF capacitor (close to the input capacitance of the CPM2-1700-0045B SiC MOSFET by CREE™). Under these conditions, the original duty cycle is 10.51%, whereas the received duty cycle is 10.70%.

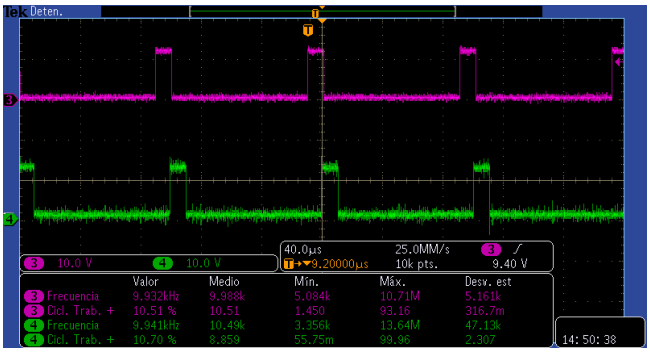


Figure 14. Duty cycle test (original signal at channel 3 and received one at channel 4).

Figure 15 shows the receiving duty cycles vs. original duty cycle using a 3.3 nF capacitance.

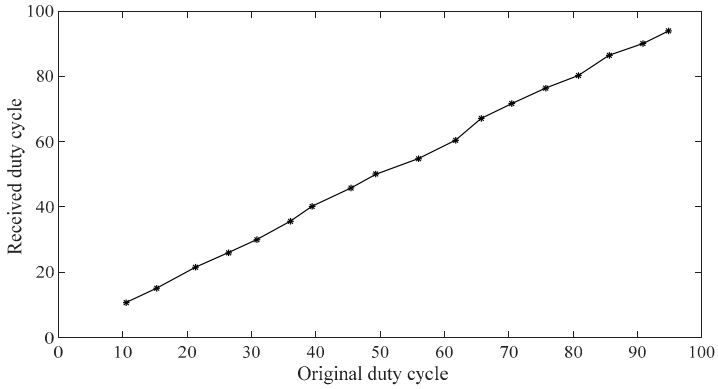
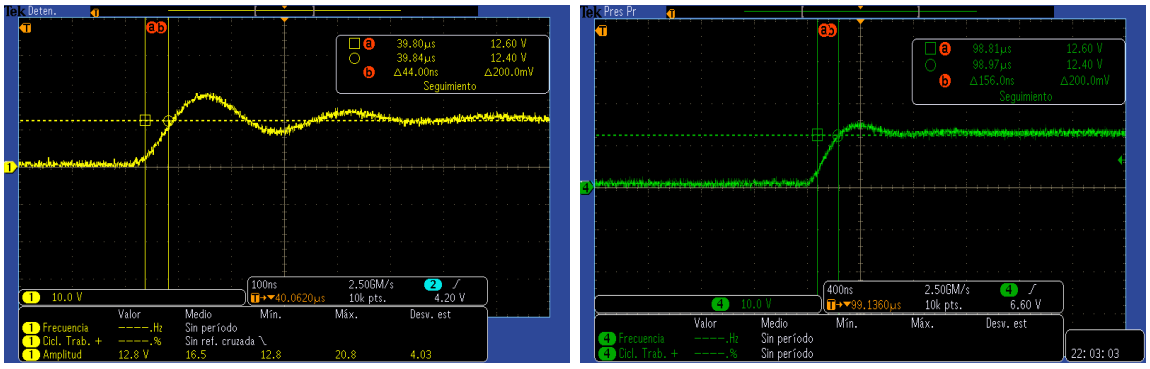


Figure 15. Original duty cycle vs. received duty cycle with 3.3 nF load capacitance.

5.2. Rise Time and Fall Time

In gate drivers, parameters such as rise time and fall time are related to switching losses. To minimize the switching losses, the rise time and fall time should be as low as possible, although this means that the gate driver must carry higher gate current. The rise time and fall time depend on both the MOSFET gate capacitance and the gate resistor. Figure 16 shows the measured rise time with load capacitances of 1 nF and 33 nF (Figures 16a and 16b, respectively) using a gate resistor of 2.3 Ω.



(**a**) (**b**)

Figure 16. Rise time for load capacitance, (**a**) 1 nF, (**b**) 33 nF, with 2.3 Ω gate resistor.

Figure 17 shows the rise time measurements using different gate resistances for different load capacitances.

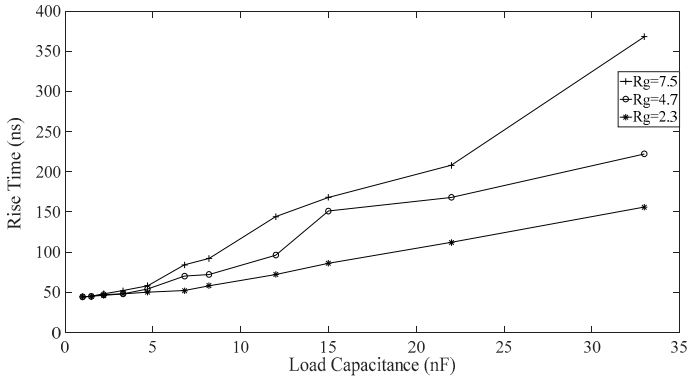
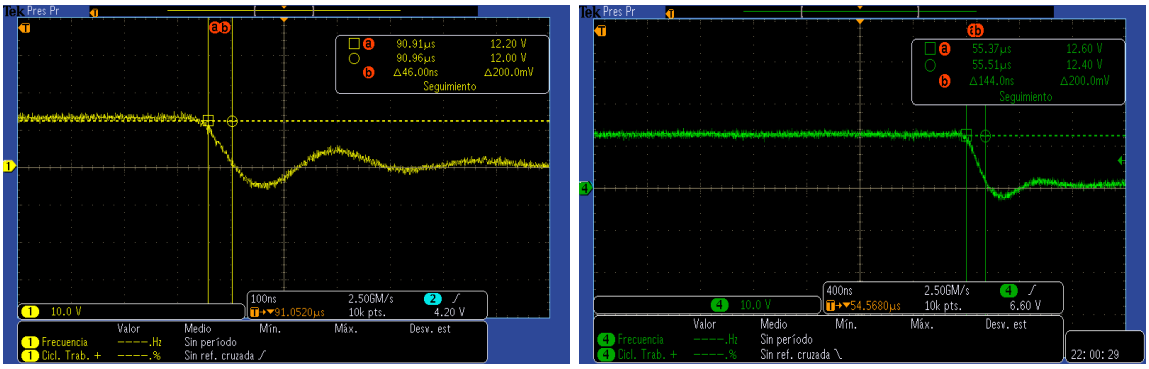


Figure 17. Rise time vs. load capacitances for different gate resistances (Rg = 2.3 Ω to 7.5 Ω).

Figure 18 shows the fall time for load capacitances of 1 nF and 33 nF using 2.3 Ω gate resistance. The fall time using different gate resistors for different load capacitances is shown in Figure 19.



(**a**) (**b**)

Figure 18. Fall time for load capacitance, (**a**) 1 nF, (**b**) 33 nF, with 2.3 Ω gate resistor.

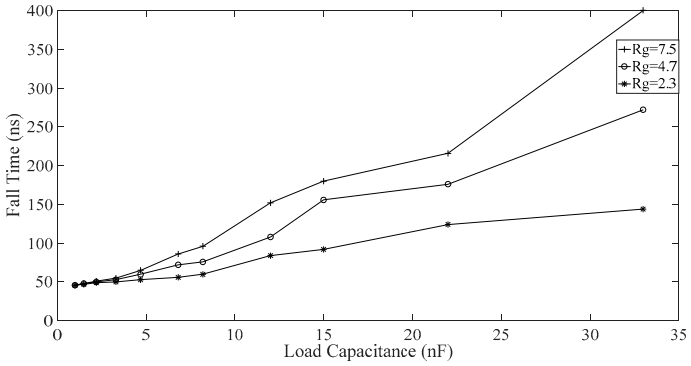


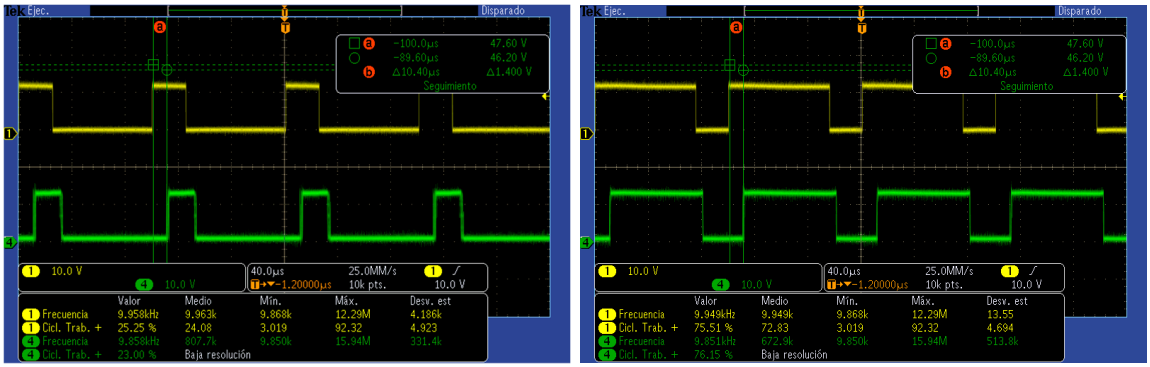
Figure 19. Fall time vs. load capacitances for different gate resistances (Rg = 2.3 Ω to 7.5 Ω).

In practical implementation, the fall time is faster than the rise time because of the dynamic input and reverse transfer capacitance of the MOSFET gate.

5.3. Duty Cycle Delay

The duty cycle delay test determines the delay between the original duty cycle and the duty cycle received on the secondary side. During these tests, a 3.3 nF capacitor was used as a load to emulate the MOSFET input capacitance. The tests were conducted with duty cycles between 10% and 95%. The results show that the delay is 10.4 µs and remains practically constant for different duty cycles and for capacitances from 1 nF to 33 nF. The

results were obtained by measuring the delay between the rising edge of the sent and received duty cycle (see Figure 20).



(**a**) (**b**)

Figure 20. Measurements of the delay between the original and received duty cycle (Channel 1, send duty cycle, Channel, 4 received duty cycle), (**a**) D = 25%, (**b**) D = 75%.

5.4. Discussion

The carried-out tests demonstrate the viability of the proposed gate driver. Experimental results emulating MOSFET gate input capacitance with load capacitances from 1 nF to 33 nF and different gate resistances were tested. The emulated maximum load capacitance is up to nine times the typical input capacitance of available commercial devices.

Table 5 summarizes the most relevant results of the developed gate driver for medium voltage application.

Table 5. Overall performance of the proposed gate driver.

Parameter	Results
Minimum duty cycle	10%
Maximum duty cycle	95%
Maximum deviation in transmission	±1.03 D sent
Rise time	44–156 ns
Fall time	46–144 ns
Delay between original and received duty cycle	10.4 µs
Insulation barrier	68.2 kV (theoretical)

Table 6 shows a comparative with previous power supplies and/or gate drivers for MV applications. The table shows the information given by the articles.

Table 6. Comparative with previous power supplies and/or gates for MV.

Reference	Topology	Power Transmission	Gate signal Transmission	Capacitance Load	Rise Time	Fall Time	Insulation Barrier	Power Insolation	Gate Signal Insolation
[18]	Half-Bridge	Yes	Yes	1.3 nF	No information	No information	16 kV	Magnetic Core	Ligh
[19]	Half-Bridge	Yes	Yes	6.7 nF	No information	No information	No information	Magnetic Core	Magnetic core
[21]	Full-Bridge	No	Yes	300 pF	233.7 ns	140 ns	No information	–	PCB
				1 nF	489.3 ns	356 ns			
				2 nF	984 ns	763 ns			
[22]	Full-Bridge	Yes	Yes	No information	No information	No information	20 kV	Magnetic Core	Ligh
[25]	Class E	Yes	No	–	–	–	35 kV	Air	–
[26]	Half-Bridge	Yes	No	–	–	–	18 kV	PCB	–
Proposed gate driver	Full-Bridge	Yes	Yes	1 nF	44 ns	156 ns	68.2 kV	Air	Air
				33 nF	46 ns	144 ns			

6. Conclusions

This paper presents a wireless gate driver for MV applications that transmits both power supply and gate driver signals using a single isolated structure. The proposed gate driver basically consists of a modulator, a transmitting circuit based on a single-magnetic structure resonant converter, and a receiving circuit that includes the secondary-side power supply and the control signal demodulator.

The proposed design procedure uses the parameters according to the characteristics and power demanded by the switching power semiconductor to be controlled. The experimental design uses 25 mm of air separation between magnetic structures, guaranteeing a voltage isolation of 68.2 kV. The transmission strategy employs two signals: the switching frequency of the devices to be driven (10 kHz in the experimental results) as the modulating signal and 800 kHz as the carrier signal. The resonant tank was designed at the carrier frequency.

Increasing the resonant tank frequency leads to more high-frequency pulses within the transmitted duty cycle, resulting in a lower deviation in the received duty cycle; however, it also increases the switching losses of the resonant converter. The designed demodulator can obtain the duty cycle information from the transmitted power signal with no more than 1.03% duty cycle deviation. The deviation between the sent and received duty cycles should be corrected by the closed-loop system. In the proposed gate driver, the delay between input and output was 10.4 µs. This is mainly due to the available laboratory components used in the demodulator circuit. A faster slew rate of the op-amp will reduce the delay between input and output signals.

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