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An Improved SPWM Strategy for Effectively Reducing Total Harmonic Distortion

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Abstract: In the inverter circuit, the speed at which the MOSFET is impacted by the presence of a parasitic inductor within the printed circuit board (PCB) leads to a delay in the switching process. Furthermore, the parasitic inductor within the circuit can easily form an LC oscillation with the parasitic capacitor of the MOSFET. These two issues result in an inconsistency between the actual output of the MOSFET and the driving signal waveform, leading to distortion in the sinusoidal pulse width modulation (SPWM) waveform and an increase in total harmonic distortion (THD). It is a common practice to mitigate gate oscillation by introducing a resistor at the gate of the MOSFET. However, elevating the resistance leads to deceleration in the charging process of the MOSFET's parasitic capacitor, consequently causing an increase in the switching delay, and thereby increasing THD. Therefore, an effective strategy to reduce THD is proposed in this paper, while augmenting the gate resistance, computing the MOSFET switching delay, and applying corrective compensation. In this way, the inherent issues of the switch are addressed, resulting in inverter output waveforms that closely resemble sine waves and reduced THD. Through a combination of simulation and empirical experimentation, the efficacy of the proposed approach in significantly reducing THD in the inverter's output waveform has been empirically substantiated.

Keywords: MOSFET; THD; SPWM; inverter; delay; signal correction

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1. Introduction

Nowadays, inverter technology has become an indispensable part of power electronics [1], with its applications broadly spanning various fields, from motor drives [2,3] and flexible AC Transmission Systems (FACTS) [4,5] to renewable energy systems [6,7]. As technology advances and application demands continue to grow, researchers' focus progressively shifts towards achieving high-efficiency gains, low-stress operation modes, and minimal total harmonic distortion (THD) levels in inverters, aiming to enhance overall system performance and energy utilization efficiency. In conventional inverter designs, increasing the operating frequency of switching elements is a common strategy employed to reduce harmonic content in the output waveform, thereby lowering THD [8]. The implementation of high-frequency switching significantly accelerates the inverter's responsiveness to load variations, imparting superior dynamic performance characteristics. Concurrently, the adoption of multilevel inverter topologies represents an alternative approach to mitigate the total harmonic distortion (THD) in inverter outputs, thereby enhancing the overall power quality [9,10]. These inverters, by stacking multiple voltage levels, are capable of producing output waveforms that closely resemble ideal sine waves,

markedly enhancing waveform quality and reducing THD. This innovation paves the way for new approaches in high-precision and high-quality power conversion applications, thereby broadening their scope in industries demanding exacting power standards. While the multilevel inverter architecture presents numerous advantages, it also encounters several design and maintenance challenges, particularly those pertaining to capacitors, which are notably prominent. In multilevel inverters, capacitors, serving as vital energy storage components, experience value mismatches or performance degradation over time, which directly leads to uneven energy distribution among capacitor branches, a phenomenon referred to as capacitor imbalance. Capacitor imbalance not only deteriorates the integrity of the output waveform, increasing THD, but also potentially renders the system unstable, thereby decreasing overall efficiency and reliability.

In the 1970s, a groundbreaking work introduced a novel harmonic suppression technique tailored for two-level voltage source inverters, marking a significant milestone in power electronic control strategies [11]. At its core, this technology boasts a unique and innovative approach. It relies on meticulously designed pulse waveforms decomposed through Fourier transforms into a series of frequency components, allowing for careful adjustment of these components through mathematical means to ensure specific low-order harmonics are precisely eliminated. This process entails constructing and solving a set of complex nonlinear equations, each directly tied to the phase configuration of the pulse sequence, demonstrating a sophisticated manipulation of wave dynamics for harmonic mitigation. The primary hurdle lies in the solution of the nonlinear equation set, a process that is not only computationally intensive and demanding with high computational resources and time requirements, but also arduous, severely hindering the real-time application potential of the technology under the technological constraints of the era. Owing to the inherent demand for rapid response and dynamic adjustment capabilities in power electronic conversion systems, this computational complexity essentially curtails the widespread adoption and practical deployment of the harmonic mitigation strategy in real-world industrial settings.

With the evolution of software control techniques, a multitude of advanced modulation strategies have emerged to effectively suppress the THD in inverter outputs. These encompass but are not limited to, sinusoidal pulse width modulation (SPWM) [12–15], space vector modulation (SVM) [16,17], and specific harmonic elimination pulse width modulation (SHEPWM) [18]. These methodologies, by ingeniously adjusting switch states and optimizing the output waveform, significantly enhance power quality, providing a potent toolkit for realizing cleaner and more efficient power conversion. While the aforementioned modulation techniques have demonstrated remarkable efficacy in reducing THD, they also commonly encounter several design and implementation challenges. Take SVPWM and SHEPWM as examples, the implementation of these algorithms typically entails higher computational complexity, requiring more substantial computational resources and intricate algorithmic designs, which undeniably escalate the integration complexity and hardware costs of the system. Especially for cost-sensitive or computationally constrained applications, this may pose a bottleneck to their widespread deployment. In contrast to SPWM, a more intuitive and less computationally burdensome modulation strategy approach like SVPWM employs more intricate switching patterns. While offering advantages in modulation precision and harmonic suppression, they can also lead to increased switching losses. This not only impacts the inverter's efficiency performance but may also shorten the lifespan of critical electronic components, thereby introducing a new trade-off between efficiency and economy. Thus, future research avenues must not only persistently seek out more efficient and streamlined modulation algorithms but also emphasize the co-optimization of algorithms with hardware, ensuring both effective THD reduction and the economic viability and practicality of systems, thereby advancing the green development of power electronics technology.

Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) boast significantly swifter switching capabilities in comparison to traditional bipolar transistors, such as

BJTs and IGBTs, with this attribute proving especially vital in high-frequency inverter applications. By efficaciously curtailing switching losses, it augments system efficiency and curbs the necessity for auxiliary filtering components, thereby enhancing overall system performance and compactness. Furthermore, MOSFETs feature exceptionally low on-state resistance, which further diminishes energy loss during conduction, thereby making a substantial contribution to enhancing overall efficiency. Its superior thermal management, evidenced by efficient cooling and stable performance at elevated temperatures, renders MOSFETs the preferred option for high-power density and challenging inverter designs operating under harsh conditions. In inverter design, the utilization of MOSFETs has led not only to substantial leaps in efficiency and reductions in both volume and weight but also to a comprehensive enhancement of system performance and reliability. Consequently, this paper selects MOSFETs as the subject for analysis and computation. Regarding the selection of MOSFETs, the decision hinges upon the specific demands of the application scenario. Silicon Carbide (SiC) emerges as a frontrunner in environments characterized by high voltages, substantial power requirements, and elevated temperatures, where its robust performance is indispensable. Conversely, Gallium Nitride (GaN) distinguishes itself through its exceptional capabilities in medium to low-voltage settings, where it facilitates high-frequency operation with remarkably low losses, thus proving to be an unparalleled choice for applications requiring swift and efficient switching dynamics.

This paper presents an innovative strategy aimed at thoroughly analyzing and effectively addressing the core challenge of THD in inverter outputs, delving into the fundamental mechanisms behind its generation to suppress harmonic formation at the root. The crux of the THD issue lies in the latency effects inherent in switching operations and the resultant oscillatory phenomena, which, in tandem, significantly distort the output waveform. Traditionally, oscillation issues have been mitigated by introducing resistive elements into circuits, which, while dampening waveform fluctuations to a certain extent, inevitably exacerbate switching delays, presenting a solution that sacrifices one benefit for another. To address this dilemma, this paper's strategy innovatively employs refined circuit designs, skillfully integrating the principle of equivalent area to achieve precise compensation for switch delay signals. This design not only effectively mitigates switch delays but also targets the oscillation issue specifically, thereby significantly reducing THD without compromising the system's response speed. Moreover, the strategy focuses on enhancing waveform quality, and through the synergistic application of these techniques, the inverter's output waveform is significantly approximated to an ideal sinusoidal shape, resulting in a substantial reduction in THD. The efficacy of the proposed modulation strategy in curtailing the THD of the inverter has been rigorously attested through a dual-pronged approach encompassing both simulation exercises and empirical trials. This not only elevates power quality but also bolsters the overall efficiency and compatibility of the system. This groundbreaking endeavor not only charts new directions in harmonic mitigation techniques within the realm of power electronics but also furnishes a scientific foundation and practical roadmap for achieving more efficient and environmentally friendly power conversion and transmission systems, thereby possessing profound theoretical significance and vast application potential.

The organization of this paper proceeds as follows. Section 2 delves into the origins of inverter harmonics, elucidating the impact of non-linear loads, switch characteristics, and control strategies on waveforms through a combination of theory and illustrative examples. Section 3 introduces the innovative methods for reducing THD, detailing the technical principles, design concepts, algorithm implementations, and circuit optimization measures, showcasing how to strike a balance between efficiency and waveform integrity. Section 4 delves into an exhaustive analysis of the outcomes derived from both simulation models and real-world experimental data, thereby bridging the theoretical underpinnings with practical applications. Section 5 summarizes the research findings, highlighting the contributions and innovations made, and looks forward to the future, outlining research

directions and impending challenges, thereby providing guidance for further studies in the field.

2. Main Sources of Inverter Harmonics

In this section, taking the conventional inverter as an example, the main sources of inverter harmonics are analyzed: turn-ON and turn-OFF delay caused by intrinsic limitations of the switches, and oscillations raised by resonances between the circuit components. As illustrated in Figure 1, the conventional inverter encompasses a DC input source denoted as Vin, four MOSFETs marked as S1, S2, S3, and S4, an inductor represented by L, a capacitor indicated by C, and a load resistor denoted by R.

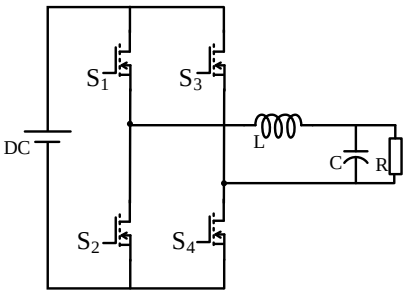


Figure 1. The conventional inverter.

2.1. Delay in Switching Processes

For the purpose of this paper, the MOSFET has been chosen, characterized by its tri-terminal structure comprising the gate (G), source (S), and drain (D). Referencing Figure 2, the capacitive components intrinsic to the MOSFET are explicitly labeled. C_{GS} signifies the capacitor existing between the gate and source terminals, C_{GD} epitomizes the capacitor spanning the gate and drain, while C_{DS} embodies the capacitor linking the drain and source terminals. These parasitic capacitors play a significant role in determining the dynamic behavior of the MOSFET, especially at higher frequencies. These parasitic capacitances between terminals are represented by

$$\begin{cases} C_{iss} = C_{GD} + C_{GS} \\ C_{oss} = C_{DS} + C_{GD} \\ C_{rss} = C_{GD} \end{cases} \tag{1}$$

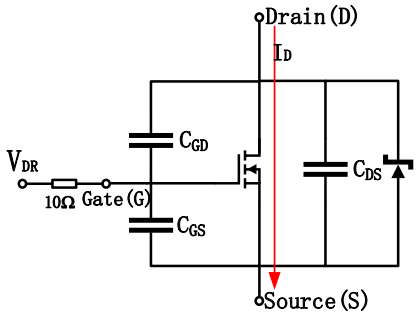


Figure 2. Equivalent model of MOSFET. The red arrows indicate the direction of the current flow.

Based on the aforementioned formula and the datasheet for this particular MOSFET model, the value of the input capacitance C_{iss} is determined to be 350 pF. The output capacitance C_{oss} is found to be 45 pF. The reverse transfer capacitance C_{rss} is calculated to be 30 pF. Then, the value of C_{GS} is the difference between C_{iss} and C_{rss}, which amounts to 320 pF.

For analytical purposes, it is beneficial to dissect the turn-ON process of the MOSFET into a series of distinct phases. This breakdown facilitates a deeper understanding of

the underlying dynamics and transient behaviors during the activation of the device. As depicted in Figure 3a, the turn-ON process can be segmented into multiple temporal intervals, each characterized by unique electrical phenomena and device response.

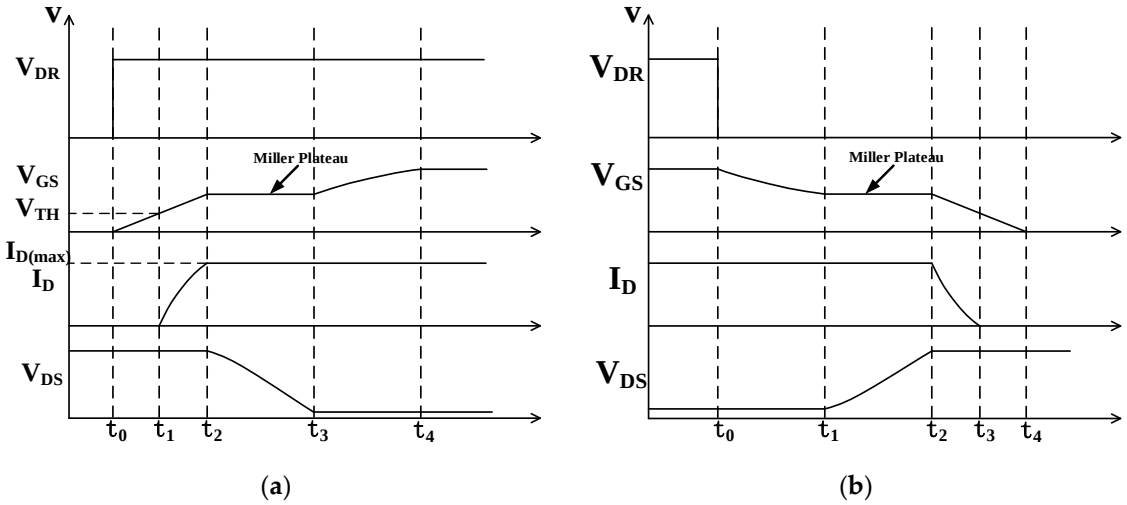


Figure 3. Waveforms of MOSFET: (**a**) When MOSFET is being turned ON. (**b**) When MOSFET is being turned OFF.

Prior to t_0: In this interval before t_0, the MOSFET is OFF. At t_0, the MOSFET begins to enter the turn-ON process.

Interval [t_0–t_1]: During this interval, the input capacitor C_{iss} is charged by the driving voltage V_{DR}, causing the voltage across G and S (represented by V_{GS}) to rise. At t_1, V_{GS} reaches the threshold value V_{TH}, and the MOSFET starts conducting. Before V_{GS} reaches V_{TH}, the drain current I_D is approximately zero.

Interval [t_1–t_2]: During this interval, the drain-source current I_D increases. When V_{GS} reaches the Miller plateau voltage (i.e., V_{GS} remains stagnant at a stable value, inhibiting rapid charging), I_D also reaches its maximum value $I_{D(max)}$, and V_{DS} starts to decrease gradually.

Interval [t_2–t_3]: During this interval, starting from t_2, the MOSFET operates in the saturation region with a constant V_{GS}, and C_{GS} is no longer charged, indicating unhindered conduction of current.

Interval [t_3–t_4]: During this interval, the drain–source voltage V_{DS} drops to the saturation voltage at t_3, where it fully conducts, $V_{DS} = I_{D(max)} \times R_{DS(on)}$, where $R_{DS(on)}$ is the ON-resistance of the MOSFET. The voltage of capacitor C_{GD} is decreased, while C_{GS} gets charged, they are charged by V_{DD}. The voltage across C_{GS} gradually rises until t_4 when V_{GS} reaches V_{DD}. V_{GS} reaches the steady state at t_4, the turn-ON process is completed.

The turn-OFF process of the MOSFET is the inverse of its turn-ON process, as shown in Figure 3b. It is unnecessary to reiterate it here.

Due to the aforementioned steps involved in the intervals t_0–t_3, the actual output voltage deviates from the driving signal waveform, leading to waveform distortion and increased THD.

2.2. Oscillation Issues

In printed circuit board (PCB) design, a parasitic inductor is inevitable, primarily originating from signal traces, vias, discontinuities in plane layers, and the power distribution network. The magnitude of the parasitic inductor depends on a variety of factors, including but not limited to the length, width, shape, number of layers, and the spacing between layers of the trace. For the driving circuit of the MOSFET modeled in Figure 4, R denotes the driving resistor, and L is the parasitic inductor of the PCB wiring.

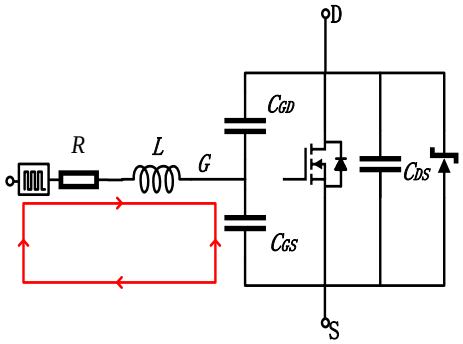


Figure 4. The driving circuit of MOSFET. The red arrows indicate the direction of the current flow.

Designating the MOSFET's gate drive voltage as the input, denoted by u_i, and taking the voltage across the parasitic capacitor C_{GS} as the output signal, the model can be described by the following equation:

$$LC_{GS}\frac{d^2u_{GS}}{dt^2} + RC_{GS}\frac{du_{GS}}{dt} + u_{GS} = u_i \tag{2}$$

R, L, and C_{GS} form a second-order circuit.

$$\frac{d^2u_{GS}}{dt^2} + \frac{R}{L}\frac{du_{GS}}{dt} + \frac{1}{LC_{GS}}u_{GS} = \frac{1}{LC_{GS}}u_i \tag{3}$$

After rearranging the equation and performing a Laplace transformation on it,

$$s^2 + 2\xi\omega_n s + \omega_n^2 = 0 \tag{4}$$

Damping factor = $(R/2)\sqrt{C_{GS}/L}$ reflects the value of the damping and the angular frequency; $\omega_n = 1/\sqrt{LC_{GS}}$ corresponds to the intrinsic angular frequency. Let s_1 and s_2 denote the roots of the characteristic equation. According to the relationship between R, L, and C_{GS}, the following situations can be distinguished:

1. $R > 2\sqrt{L/C_{GS}}$, s_1 and s_2 are two distinct real roots, indicating an overdamped state. The system's output does not exhibit oscillation.
2. $R = 2\sqrt{L/C_{GS}}$, s_1 and s_2 are two equal real roots, indicating a critically damped state. The system's output also does not display oscillation.
3. $R < 2\sqrt{L/C_{GS}}$, s_1 and s_2 are complex conjugate roots, indicating an underdamped state. The system's output exhibits severe oscillation, which leads to harmonics in the inverter.

The ubiquitous presence of parasitic inductance significantly impacts the overall performance of circuit systems, particularly under high-frequency operating conditions. With regard to signal traces, based on a widely accepted industry consensus, every extension of one thousand mils (approximately equivalent to 25.4 mm) in trace length corresponds to an incremental parasitic inductance of around 5.076 nanohenries. For the quantified estimation via parasitic inductance, the empirical formula adopted by the industry is as follows:

$$\mathrm{L_{via}} = 5.08\mathrm{h} \cdot [\ \ln(4\mathrm{h}/\mathrm{d}) + 1\ ] \tag{5}$$

where $\mathrm{L_{via}}$ represents the inductance of the via, h is the length of the via, and d is the diameter of the central drill hole.

Based on the aforementioned information, through calculations, the parasitic inductance of the PCB can be determined to be 8.75 nH. Based on the third criterion of the aforementioned judgment conditions, it can be concluded that the circuit system is in an underdamped state, with oscillations in the output leading to the presence of harmonics.

Theoretically and commonly, there are three measures for avoiding circuit oscillation:

1. Increasing the resistance R to meet the criteria will help to eliminate oscillations. However, it should be noted that increasing R reduces efficiency and also increases the switching delay time. Therefore, it is common practice to select a resistance value close to, but not exceeding, critical damping to address this issue effectively while minimizing adverse effects.
2. Properly design the PCB wiring to minimize parasitic inductance within the circuit; however, parasitic inductance cannot be entirely eliminated, only reduced as much as possible.
3. Choosing a switching device with a greater capacitance between the gate and source electrodes appears beneficial at first glance; however, upon examining the dynamics of the switch's conduction phase, it becomes evident that this choice induces a deceleration in switching velocity, thereby exacerbating harmonic distortion.

According to the switching process revealed in Figure 4, it can be concluded that increasing R will decelerate the charging process of parasitic capacitors, resulting in further increases in harmonics.

3. Proposed Modulation Method for Effectively Reducing THD

Based on the analysis in Section 2, increasing R can mitigate oscillations, but it also leads to an increase in the switching device's delay time. Thus, the trade-off between the switching delay and oscillation presents a fundamental contradiction; eliminating both delay and oscillation-induced harmonics simultaneously is unachievable. Instead, harmonics caused by delay and oscillation can only be minimized through judicious circuit design and parameter selection, but they cannot be completely eradicated. Consequently, this paper proposes an algorithm designed to effectively reduce the total harmonic distortion. Therefore, upon comprehensive consideration of these two factors, the proposed method aims to reduce the harmonics by compensating for the switching delay time caused by increasing driving resistance. It is an improved SPWM modulation method that makes the output waveform of the inverter closer to a sine wave, thereby reducing THD.

3.1. Area-Equivalence Principle

The area-equivalence principle encapsulates a fundamental concept, particularly concerning the interaction between narrow pulses and dynamic systems. According to this principle, when narrow pulses, despite their varying shapes, possess the same impulse defined as the integral of the pulse amplitude over its duration, which geometrically corresponds to the area enclosed by the pulse waveform-exert nearly identical influences upon an inertial element. This principle is illustrated vividly through Figure 5a–d, which depicts distinct pulse configurations, each characterized by a unique waveform but sharing an equal impulse. Based on this principle, the SPWM method can be utilized to effectively simulate sinusoidal waveform by inputting pulse sequences with equal amplitudes and duty cycles varying with the sine wave amplitude.

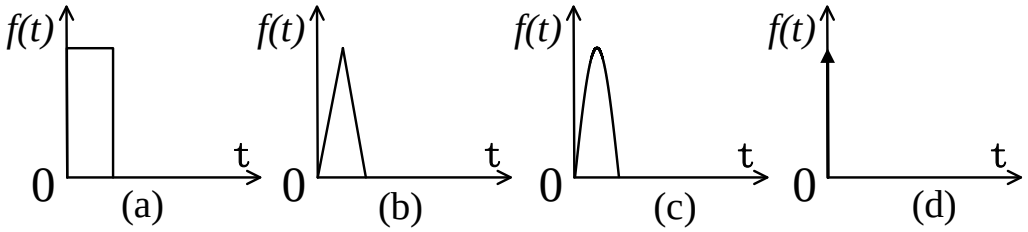


Figure 5. Narrow pulses with different shapes but the same impulse: (**a**) Rectangular pulse. (**b**) Triangle pulse. (**c**) Sinusoidal half-wave pulse. (**d**) Unit pulse.

3.2. Proposed Modulation Method

The symmetric rule sampling method for unipolar SPWM waves, as portrayed in Figure 6, represents a strategic approach to generating control signals for power electronic

converters, specifically targeting the enhancement of efficiency and a reduction in harmonic distortions. This method is distinguished by its precision in timing, achieved through a meticulous sampling technique that adheres to the principle of symmetry around the peak points of the triangular carrier wave. In this methodology, sampling occurs exclusively at the apex of the triangular carrier wave, ensuring that the sampling intervals (T_1 and T_2) are equal, thus preserving the inherent symmetry of the modulation process.

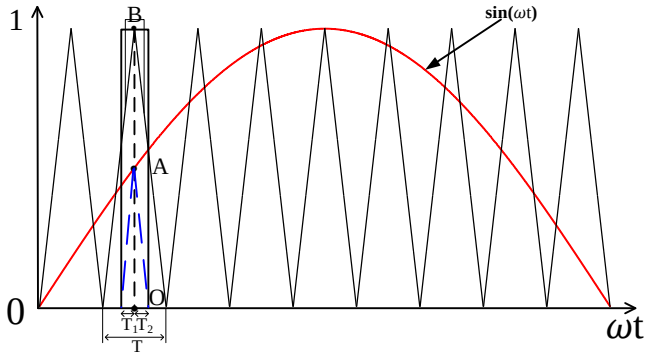


Figure 6. Principle of symmetric regular sampling method for unipolar SPWM wave. A represents the sampling points of the sinusoidal wave, and B represents the peak points of the triangular carrier wave.

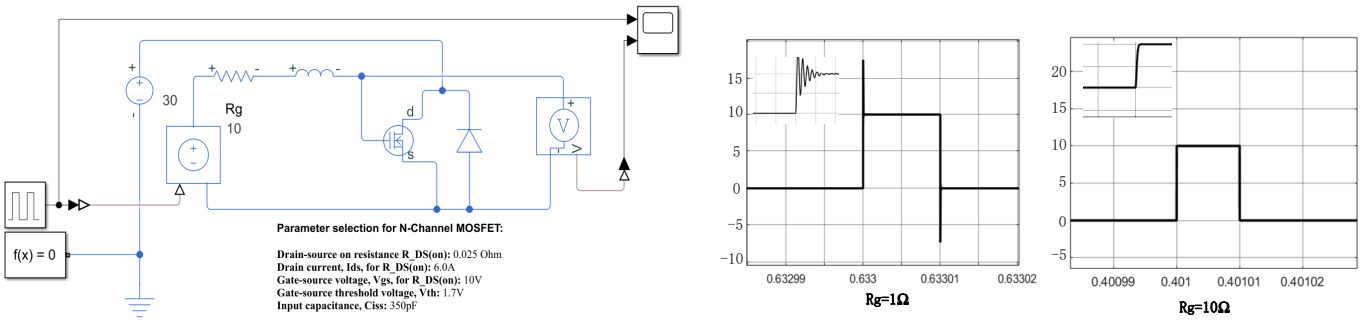
This equalization of sampling times is pivotal in maintaining the integrity of the SPWM signal, as it directly influences the accuracy of the pulse widths generated for controlling the switching devices within the power converter. The calculation of the switch's turn-ON time, a critical parameter in determining the efficiency and performance of the power conversion, is facilitated by the application of the triangle-similarity principle. This principle leverages the geometric properties of similar triangles formed during the modulation process to accurately determine the durations during which the switch is in the conducting state. By establishing a direct relationship between the modulating signal (the reference sine wave) and the carrier wave, the method allows for the computation of the precise instant at which the switch should transition from the OFF state to the ON state, optimizing the power delivery and minimizing losses. Utilizing the triangle similarity principle, the switch's turn-ON time can be calculated.

$$\begin{cases} \mathrm{T_{on}} = \mathrm{T_1} + \mathrm{T_2} \\ T_1 = T_2 \\ \frac{\mathrm{OB}}{\mathrm{OA}} = \frac{T}{T_1 + T_2} \\ \mathrm{OA} = \sin(\omega \mathrm{t_o}) \\ OB = 1 \end{cases} \tag{6}$$

Finally, the switch's turn-ON time is expressed as

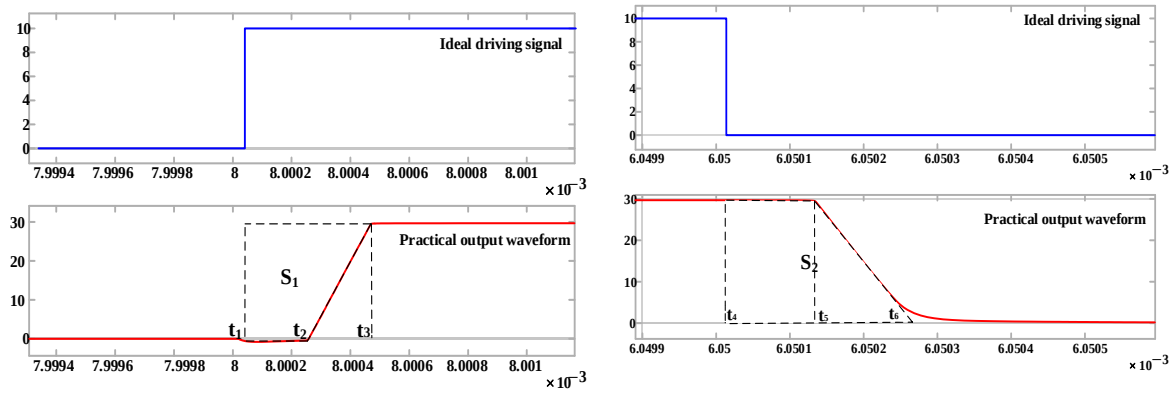
$$\mathrm{T_{on}} = \mathrm{T}\sin(\omega \mathrm{t_0}) \tag{7}$$

To explain how the proposed method is applied, an equivalent MOSFET model considering the switch's delay and oscillation issues, along with the circuit's parasitic parameters are built in MATLAB/Simscape, as shown in Figure 7a, where $f(x) = 0$ indicates ground. When the gate resistance R_g changes from 1 Ω to 10 Ω, as presented in Figure 7b, the oscillation is diminished; however, it results in a switching delay. To facilitate explanation, the phenomena of switch oscillation and delay shown in Figure 7b have been exaggerated. Further analysis of the phenomenon and principles of switch delay is provided in the following text and in Figure 8.



(**a**) (**b**)

Figure 7. Equivalent MOSFET simulation model considering delay and oscillation issues: (**a**) Equivalent MOSFET model. (**b**) Elevating the driving resistance to diminish oscillation.



(**a**) (**b**)

Figure 8. The waveforms of the MOSFET under non-ideal conditions: (**a**) MOSFET ON-delay. (**b**) MOSFET OFF-delay.

Figure 8a depicts the delay during turn-ON and Figure 8b illustrates the turn-OFF delay. During switching-ON, the output waveform's amplitude changes at instants t_1, t_2, and t_3. Similarly, during switching-OFF, the output waveform's amplitude changes at instants t_4, t_5, and t_6.

The area of S_1, implying that the practical output energy is smaller than that under ideal conditions due to the delay in the MOSFET turn-ON process, is expressed as

$$S_1 = \frac{(t_2 - t_1) + (t_3 - t_1)}{2} V_o \tag{8}$$

The area of S_2 represents the excess energy due to delays in the turn-OFF process of the MOSFET,

$$S_2 = \frac{(t_5 - t_4) + (t_6 - t_4)}{2} V_o \tag{9}$$

To mitigate switching delay-induced THD, the adjustment of the area difference between S_1 and S_2 is crucial. S_1 and S_2 depend on specific parameters of the circuit design. For example, a high current-limiting resistance in the driving signal leads to an increase in the turn-on time and consequently enlarges S_1. Conversely, reducing the current-limiting resistance reduces the size of S_1. Additionally, the capacitance, inductance, and design of fast turn-ON and turn-OFF circuits within the circuit also influence the sizes of S_1 and

S_2. Typically, the area of S_2 is larger than that of S_1, resulting in the actual output energy exceeding the theoretical output energy. This specific value is expressed by

$$S_2 - S_1 = \frac{(t_5 + t_6 + 2t_1 - t_2 - t_3 - 2t_4)V_o}{2} \tag{10}$$

Based on the principle of area equivalence, it is crucial to actively reduce the area difference of the turn-ON process and turn-OFF process, in order to align the output results with expectations. Convert the area difference into turn-ON time,

$$\Delta t = \frac{(t_5 + t_6 + 2t_1 - t_2 - t_3 - 2t_4)}{2} \tag{11}$$

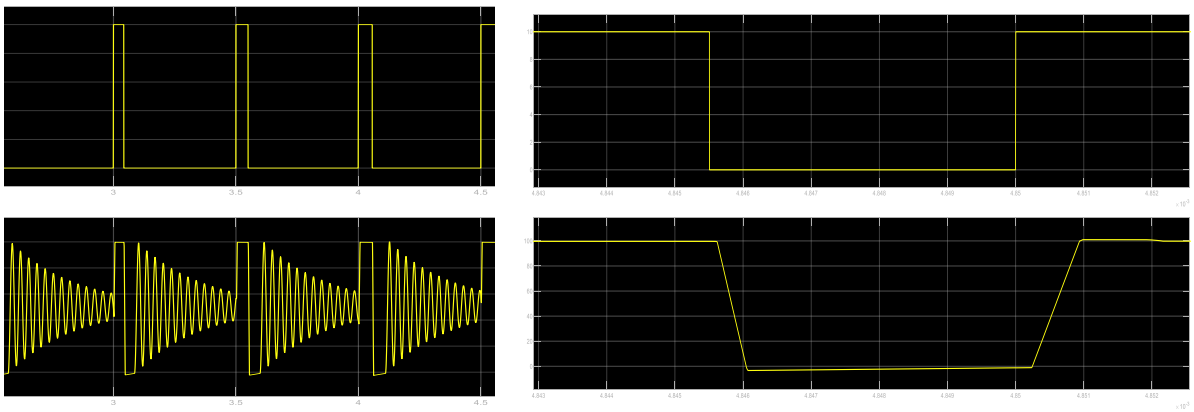
Hence, the required turn-ON time for the switch is

$$T'_{on} = T_{on} + \Delta t = T\sin(\omega t_0) + \frac{(t_5 + t_6 + 2t_1 - t_2 - t_3 - 2t_4)}{2} \tag{12}$$

In this way, the output energy matches the desired value, and the output waveform becomes closer to a sine waveform, resulting in a reduction in THD.

3.3. Application in the Conventional Inverter

The output waveform of the conventional inverter is shown in Figure 9. Figures 9a and 9b, respectively, present enlarged views of the output waveforms near the zero-crossing and peak values. Due to the narrow driving signal pulse, the switches do not have enough time to fully turn on before entering the OFF state, resulting in energy attenuation oscillations between the upper and lower switches on the same side, as shown in Figure 9a. Increasing the resistance level can effectively resolve the oscillation problem but results in a switching delay. Figure 9b shows the output near the peak value, where the pulse width is relatively wide and the waveform tends to stabilize, with oscillations weakening or even ceasing. The observed issues are solely associated with the switching delay. With the proposed modulation strategy, T_{on}' is utilized as the conduction time for the aforementioned switching delays near the zero-crossing point and near the peak value, respectively. This is equivalent to applying corrective compensation to a portion of the control signal, which still effectively reduces THD. Simulation results are presented in the following section.



(**a**) (**b**)

Figure 9. Output waveforms of the inverter: (**a**) Near the zero crossing point. (**b**) Near the peak value.

4. Analysis of Simulation and Experimental Results

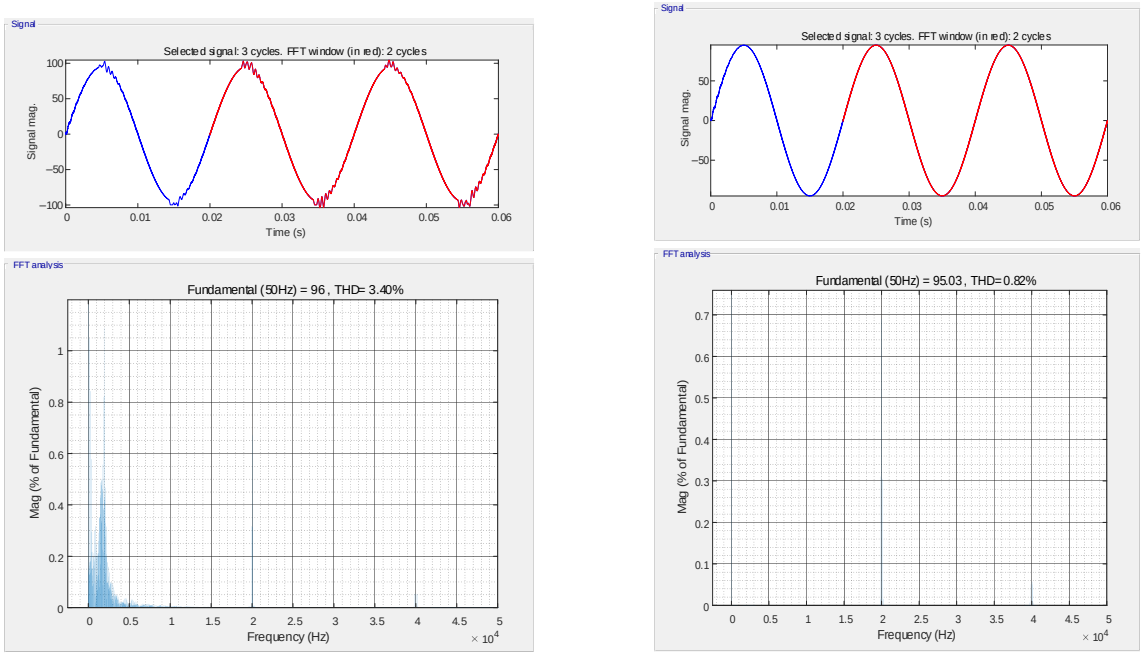
In this section, the SPWM and the proposed method are, respectively, employed to control the conventional inverter. The THD results before and after filtering are obtained

and analyzed, aiming to effectively reduce total harmonic distortion. The simulation parameters for the conventional inverter are listed in Table 1.

Table 1. Simulation Parameters.

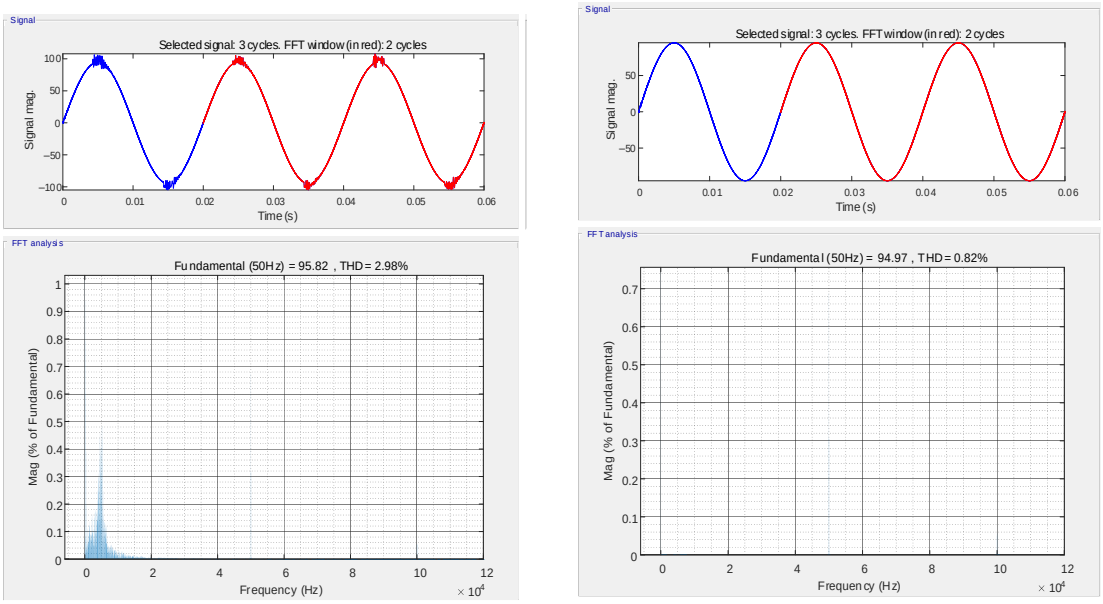
Parameters	Values
Input voltage V_i	100 V
Switching Frequency (f_s)	20 kHz, 50 kHz, 100 kHz
Filter Inductor L	0.8 mH, 0.32 mH
Filter Capacitor C	8 µF, 3.2 µF
Load (Resistive)	100 Ω

For a conventional inverter with a switching frequency of 20 kHz, a filter inductance of 0.8 mH, and a filter capacitance of 8 µF, the comparative simulation results for SPWM and the proposed modulation strategy are shown in Figure 10. Using the SPWM and the proposed effective total harmonic distortion reduction strategy, the filtered output waveforms using the two methods are displayed in Figure 10a,b, resulting in THD values of 0.82% and 3.40%, respectively. For the cases where the switching frequency is 50 kHz and 100 kHz, a filter inductance of 0.32 mH, and a filter capacitance of 3.2 µF, the comparative results of the filtering effects between the two methods are depicted in Figures 11 and 12, respectively. At a frequency of 50 kHz, the filtered output waveforms using these two methods are shown in Figure 11a,b, respectively, with THD values being 2.98% and 0.82%, respectively. At a frequency of 100 kHz, the filtered output waveforms are shown in Figure 12a,b, with THD values being 4.3% and 0.2%, respectively. From Figures 10–12, it is clear that the proposed method can effectively reduce the total harmonic distortion of the inverter output waveform before and after filtering, thereby validating its feasibility.



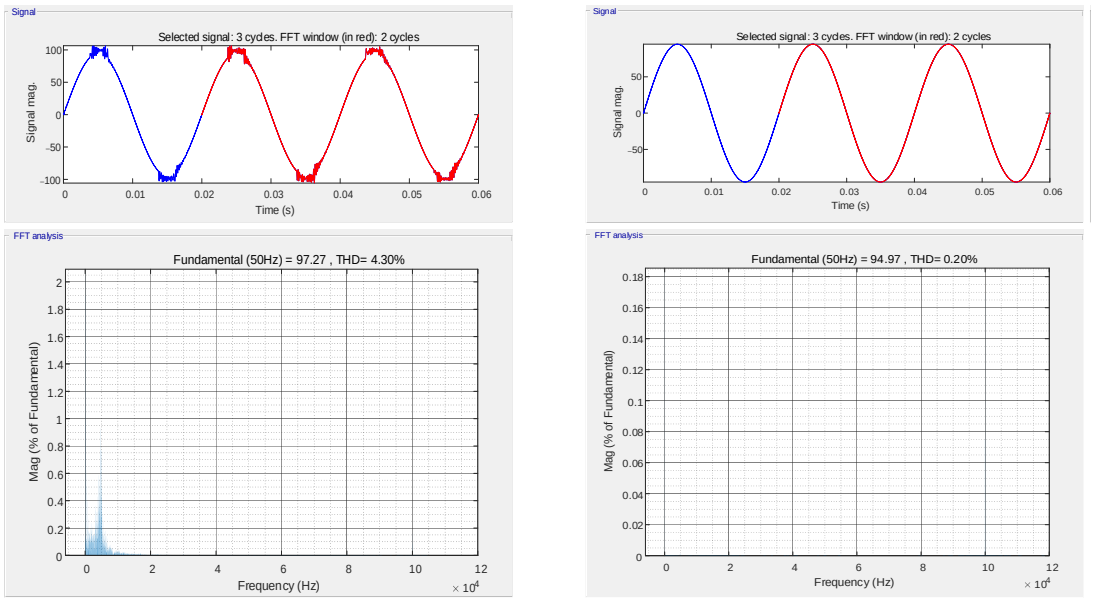
(**a**) (**b**)

Figure 10. THD of filtered output waveform at a frequency of 20 kHz: (**a**) SPWM. (**b**) The proposed method.



(**a**) (**b**)

Figure 11. THD of filtered output waveform at a frequency of 50 kHz: (**a**) SPWM. (**b**) The proposed method.



(**a**) (**b**)

Figure 12. THD of filtered output waveform at a frequency of 100 kHz: (**a**) SPWM. (**b**) The proposed method.

In order to validate the effectiveness of the proposed modulation algorithm, a test rig was assembled, as depicted in Figure 13. For this experiment, a switching frequency of 20 kHz and a load resistance of 100 Ω were selected for testing. The experimental conditions were aligned with the simulation parameters, and a 10x voltage divider was employed for the measurement of the output voltage to guarantee precise data acquisition. The modulation waveform, denoted as S, was configured with an amplitude of 1.95. The filtered output voltage waveform presented in Figure 14 illustrates a notable decrease in THD, evidencing the algorithm's success in markedly improving the waveform quality.

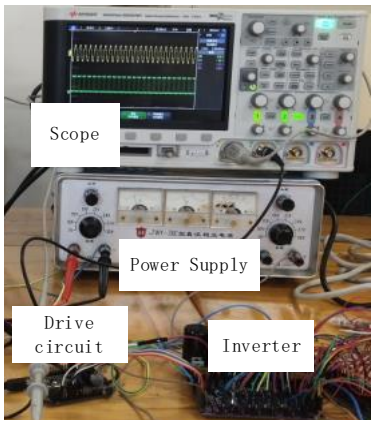


Figure 13. Experimental prototype of the proposed converter.

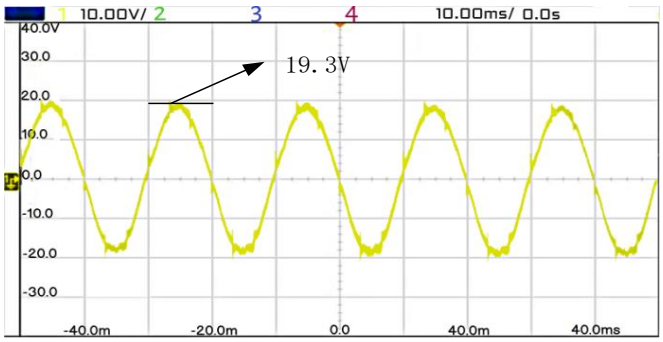


Figure 14. The filtered output waveform.

5. Conclusions

A comprehensive strategy is proposed to effectively reduce THD starting from two main factors: switching delay and oscillation. Addressing oscillation, the strategy advocates for the judicious selection of resistances within the driving circuit, ensuring that these components are finely tuned to dampen any potential oscillatory behavior. This not only stabilizes the circuit's operation but also plays a pivotal role in minimizing the distortion of the output waveform. Simultaneously, the strategy confronts the challenge of switching delay head-on. By leveraging the principles of area equivalence and similarity, the methodology calculates the precise compensation needed to rectify delays encountered during the switching process. This compensation is then applied through signal correction, allowing for the adjustment of switching event timing to counteract the inherent delays. This innovative approach ensures that the output waveform closely emulates a perfect sinusoid, thereby significantly reducing THD. By applying corrective compensation to the switching processes, the proposed strategy aims to solve the waveform distortion comprehensively, enabling output waveforms that closely resemble sinusoidal waves and ultimately reducing THD. The proposed method helped overcome the inherent issue of the hardware itself via algorithmic solutions, significantly suppressing THD. A systematic comparison of simulation outcomes with empirical results from practical implementation has rigorously confirmed the method's validity and applicability.

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Conflicts of Interest: Author Jielu Zhang was employed by the company Jiangsu Tailong Reducer Co. Ltd. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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