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State Space Average Modeling, Small Signal Analysis, and Control Implementation of an Efficient Single-Switch High-Gain Multicell Boost DC-DC Converter with Low Voltage Stress

Said A. Deraz [1,2], Mohamed S. Zaky [3,*], Kotb B. Tawfiq [2,4,5,*] and Arafa S. Mansour [6]

[1] Electrical Engineering Department, Faculty of Engineering-Rabigh, King Abdulaziz University, Jeddah 21589, Saudi Arabia; sderaz@kau.edu.sa
[2] Electrical Engineering Department, Faculty of Engineering, Menoufia University, Shebin El-Kom 32511, Egypt
[3] Department of Electrical Engineering, College of Engineering, Northern Border University, Arar 1321, Saudi Arabia
[4] Department of Electrical Engineering and Computer Science, Khalifa University, Abu Dhabi 127788, United Arab Emirates
[5] Department of Electromechanical, Systems and Metal Engineering, Ghent University, 9000 Ghent, Belgium
[6] Electrical Engineering Department, Faculty of Engineering, Beni-Suef University, Beni-Suef 62511, Egypt; arafa.sayed@eng.bsu.edu.eg
* Correspondence: mohamed.zaky@nbu.edu.sa (M.S.Z.); kotb.basem@ugent.be (K.B.T.)

Abstract: This paper presents the closed-loop control of a single-switch high-gain multicell boost DC-DC converter working in a continuous conduction mode (CCM). This converter is particularly designed for applications in photovoltaic systems. One of the main advantages of the proposed converter is that it only employs one active semiconductor switch, which decreases the converter losses and cost, increases the efficiency, and simplifies the control circuit. Moreover, the multicell nature of the proposed converter offers the possibility of obtaining the required voltage gain by selecting the number of cells. State space average (SSA) modeling and small-signal analysis are used to model the switching converter power stages of the proposed converter. The parasitic series resistances of the passive elements of the converter circuit are considered to improve the accuracy of the modeling. Small-signal analysis is used to derive the open-loop transfer functions, input-to-output and control-to-output transfer functions of the proposed converter to examine its dynamic performance. The stability of the converter is analyzed to design the parameters of the voltage controller using the proposed modeling method. The experimental prototype of the proposed single-switch two-cell boost DC-DC converter was implemented. The simulation and experimental results proved the effectiveness of the proposed boost DC-DC converter under different working conditions. It has a fast dynamic response without overshoots. A comprehensive comparison between the proposed converter and previous boost converters is provided. It guarantees a required variable and constant high voltage gain with a wider duty ratio range. It compromises between the required performance, the low number of components, low voltage stress on the components, and cost-effectiveness. The experimental efficiency of the proposed converter is about 96% at a 100 W load.

Keywords: state space average modeling; small signal analysis; multicell boost DC-DC converter; high gain; control-to-output transfer function; parasitic resistances; PI voltage controller design

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1. Introduction

The global need for electricity is increasing all the time. Because of the poor supply and high cost of traditional energy sources, there is a growing need to use renewable energy sources (RESs). Among these renewable energy sources, photovoltaics (PVs), wind turbines (WTs), and fuel cells (FCs) have developed rapidly in recent decades. To tie these sources with the utility grid, the low DC output voltage levels produced by them must be boosted to high DC voltage levels. High-voltage gain DC-DC converters are widely utilized in a

diversity of applications, such as RESs, uninterruptible power supplies (UPSs), new-energy electric vehicles (NEEVs), aircraft power supply systems, railway energy storage systems, etc. [1–3]. High-boosting DC-DC converters are often employed to increase voltage and efficiency in diverse ways, each with its own set of advantages and disadvantages [4].

Non-isolated standard DC-DC converters are characterized by their simple installation, ease of control circuit use, and low cost. But despite these features, they are not suitable for applications that require high voltage gain due to the need to work at large duty cycle values. This, in turn, leads to more switching and conduction losses at constant input voltage, increasing input current ripples and decreasing system effectiveness [5].

Several innovative DC-DC topologies have been developed to accomplish significant extreme voltage gain. Isolated and non-isolated are the types of high-gain DC-DC topologies. Isolated topologies have significant issues, such as heat effects, voltage ripples on the power switches, core saturation, and leakage inductance, and their enormous volume makes them more costly. Non-isolated types are used instead for their better voltage gain; they are more compact and less expensive because no galvanic isolation is required [6–25]. A non-isolated step-up interleaved converter was introduced in [6]. High voltage gain with a minimal switch voltage stress was satisfied, but it has more components and is not suitable for applications that require smaller gain or lighter loads. In [7], a conventional DC-DC boost converter was linked to a switched capacitor and coupled inductor to raise the voltage gain and efficacy. Nevertheless, inductor core losses continue to be affected by excessive input current ripples. To obtain high voltage gain with a moderate duty cycle and increase efficiency, the interleaved boost converter was introduced in [8,9]. However, they have difficulty separating gate signals, raising costs. Furthermore, the voltage gain was like that of a traditional boost converter. Reference [10] proposed a variety of switched capacitor-based DC-DC boost converters, while [11] employed a switched capacitor/inductor. Although high voltage gain was achieved, they had significant conduction losses, severe switching stresses, and complicated circuits. A cascaded boost converter that provides high voltage gain with minimal switching losses and current ripples was employed in [12]. However, drawbacks, such as increased costs, decreased efficiency, and the complexity of the control system, were identified. A single-cell DC-DC topology based on a hybrid switched inductor was introduced in [13]. High voltage gain, low power switching stresses, and high efficiency were satisfied. However, the number of components in this converter diminished efficiency while increasing the circuit's cost and size. Reference [14] proposed a single-switch DC-DC-boosting topology based on a traditional boost converter, voltage lift method, and a switched capacitor. Also, a single-switch DC-DC converter based on a traditional boost converter and a switched capacitor was suggested in [15]. High efficiency and small voltage stresses through the main switch and diodes were attained, but the voltage gain was still small compared with other topologies, and the number of converter components was large. A non-isolated DC-DC boost converter achieved by merging a dual step-up converter with a switching inductor topology was provided in [16]. High voltage gain, low switching losses, and small voltage stresses across the switches were accomplished, but the large number of components increased the size of the converter. In [17], a DC-DC converter with a voltage multiplier cell (VMC) was described. High voltage gain, minimal voltage stress across the switches, and great efficiency were noted. On the other hand, the large component count increased the topology dimensions and costs. A single-switch DC-DC topology was introduced in [18]. The design of this converter featured a double voltage lift approach, and it comprised a VMC, a super lift Luo converter, and a cascaded step-up topology. Issues relating to high-voltage gain and minimum input current ripples were addressed, but the large number of components reduced the converter efficiency. Reference [19] offered a new SEPIC boost DC-DC topology. The semiconductor switches operated with soft switching, which reduced the converter losses and enhanced the efficiency. Nevertheless, the voltage gain was not very high, and the number of components was large. Other topologies such as quasi-Z-source, quasi-Y-source, or a combination between them were found in [20–23]. Even though these topologies

provide substantial voltage gain with low duty cycles and constant input current, they have restricted duty cycles, severe stresses on the main switch, and complicated driving circuits. Reference [24] developed a DC-DC converter that employed VMC with a voltage extend circuit to increase the voltage gain. It was possible to achieve extreme voltage gain and minimal voltage stresses on the active components. However, the input current was discontinuous since the primary switch was connected directly with the input DC source, and the number of components was large. In addition, as the number of cells increased, converter efficiency fell. The topologies found in [25–30] introduced variety of designs based on quad-switched inductors, a combination of boost and SEPIC, switched inductors, or active-passive inductor cells. Although the voltage gain derived from these converters was greater than that from the conventional, some of them had a large number of components [25,27,29,30], and others had a large number of switches [26,28,29], which, in turn, made the control circuit problematic, increased the losses, and raised costs. To address the aforementioned issues, a modified DC-DC step-up converter was developed and presented in [31]. Its characteristics included continuous input current, easy control, extreme voltage gain, and low voltage stress on the active switches. Likewise, cascading extra cells with ultra-high voltage gain can be provided. To model, analyze, and design such converters, developed tools such as state space average (SSA) modeling and small signal analysis were introduced [32–36]. Solving the state space equations of such DC-DC converters is more challenging because the duty cycle serves as the converters' control input. The behavior of the DC-DC converters is nonlinear and time-varying. However, in order to design the controller, the system must be linear and time-invariant. Therefore, the state space average model (SSAM) and the small signal model (SSM) are used for this purpose. In [32], the SSAM of a boost DC-DC converter considering all the parasitic elements was presented. The transfer functions of a proposed AC-AC converter were derived in [33] using the SSM and the gains of proportional-integral (PI) voltage controller based on the stability analysis using the frequency response method. In [34], small signal analysis and PI controller implementation of a boost converter-fed permanent magnet DC (PMDC) motor for electric vehicle (EV) applications were introduced. In [35], the various principles of SSAM of DC-DC boost converters operating in CCM were presented. The effects of parasitic elements were also included. In [36], a two-loop control strategy for a current-fed half-bridge (CFHB) DC-DC converter was presented. Both the current control loop and the voltage control loop are designed at a phase margin of 60°. The stability of the control system was validated using PSIM software. In [37,38], electrothermal average models of a diode–IGBT switch and a diode-MOSFET switch for modeling the DC-DC converters were introduced, respectively. The equations used in the introduced models allow modeling the converter operation in both CCM and discontinuous conduction mode (DCM). In [39], an average SSM of a conventional boost DC-DC converter in CCM considering the switching power loss was presented. In [40], a reduced average model of a high-voltage gain DC-DC converter with multicell diode-capacitor network considering ideal components was presented to overcome the complexity of the multicell converter modeling. The reduced model was used to simplify the closed-loop controller design.

In this paper, an SSAM and an SSM of a novel single switch high gain multicell boost DC-DC converter are developed considering the series parasitic resistances of the passive elements. With the help of the developed models, an extensive analysis is conducted to investigate the steady state and dynamic characteristics of the proposed converter. A small signal model and the corresponding control-to-output and input-to-output open-loop transfer functions of the proposed topology are presented. The stability analysis of the proposed topology is presented to design the voltage controller of the proposed converter. The validity of the developed SSAM of the proposed converter is emphasized through experimental verification of the proposed single switch two-cell boost DC-DC converter. Different results are presented under different operating conditions.

The advantages of the single switch two-cell boost DC-DC converter are as follows:

- Low voltage stress on the main switch and diodes.
- Simplicity of control due to single-switch topology.
- The structure of the converter can be extended to n cells for high voltage gain.
- Compact size and minimum number of components guarantee a cost-effective converter.
- Good robustness of the closed-loop control under different working conditions.

2. Proposed Converter Topology

Figure 1 displays a new topology for a single-switch multicell step-up DC-DC converter [31]. The proposed converter topology consists of only one semiconductor switch (SW) that controls the power flow from the input side (supply) to the output side (load) through switching on and off, n cells, output diode, and an output capacitor. Each cell of the proposed converter circuit consists of one inductor, one capacitor, and two diodes. In [31], the circuit description and its modes of operation were explained in detail. The steady-state behavior of the proposed converter was analyzed. Also, the voltage gain in continuous conduction mode (CCM) was evaluated. According to this, the voltage gain of n cells is given by the following formula:

$$g = \frac{2-d}{1-d} + 2(n-1) \tag{1}$$

where g is the voltage gain and d is the main switch duty ratio.

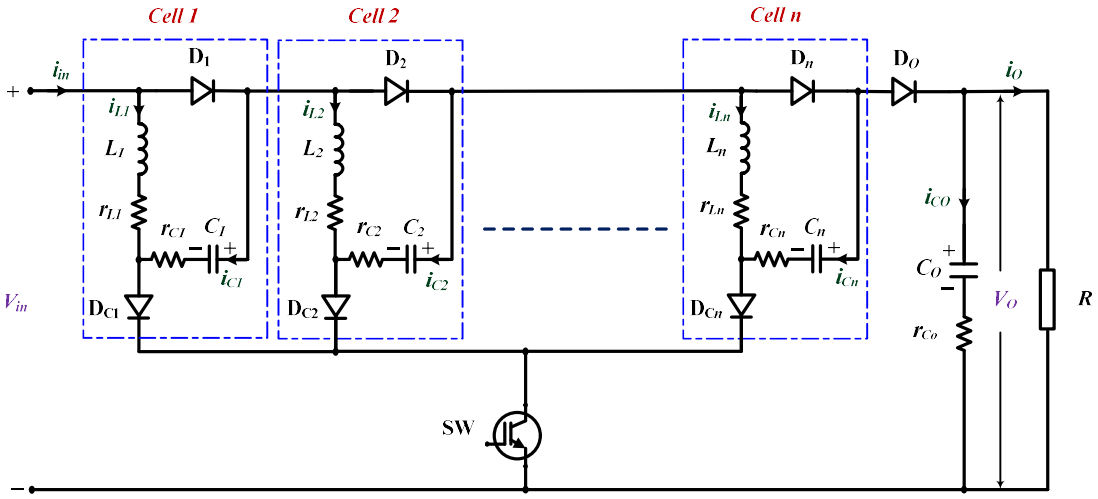


Figure 1. Single-stage multicell boost DC-DC converter with parasitic series resistances of the passive elements.

3. State Space Average Modeling

The following assumptions are considered when deriving the SSAM of the proposed topology:

- The semiconductor switch is on (i.e., closed) for a time dT_s and is off (i.e., open) for a time $(1-d)T_s$ during a switching period time T_s.
- The duty ratio (d) is expressed as the ratio of the time the switch is on (on time) over the switching period time T_s. The switching frequency (F_s) is given as $F_s = 1/T_s$.
- The converter works in the CCM, considering the design considerations of inductors and capacitors as follows:

$$\left.\begin{aligned} L_n &= \frac{d(n+1-d)}{\Delta_i\, g^2} R T_s \\ C_n &= \frac{g^2 T_s}{\Delta_v R} \frac{(1-d)}{(n+1-d)} \\ C_o &= \frac{(1-d)T_s}{\Delta_v R}\left(\frac{g}{(n+1-d)} - 1\right) \end{aligned}\right\} \tag{2}$$

where L_n is the inductance of cell n, C_n is the capacitance of cell n, Co is the output capacitance, R is the load resistance, Δ_i is the allowable percentage of the inductor current ripple, and Δ_v is the allowable percentage of the capacitor voltage ripple.

- The semiconductor switch and all diodes are modeled as ideal semiconductor devices.
- The parasitic series resistances of the passive elements (i.e., inductors and capacitors) are taken into consideration.

3.1. On State ($0 < t < dT_s$)

Figure 2 illustrates the on-state equivalent circuit of the proposed multicell converter. The active and inactive semiconductor devices are shown in Figure 2a, while the analogous circuit diagram of the converter is displayed in Figure 2b. In the on state, the semiconductor switch and all diodes except the output diode (D_o) are closed.

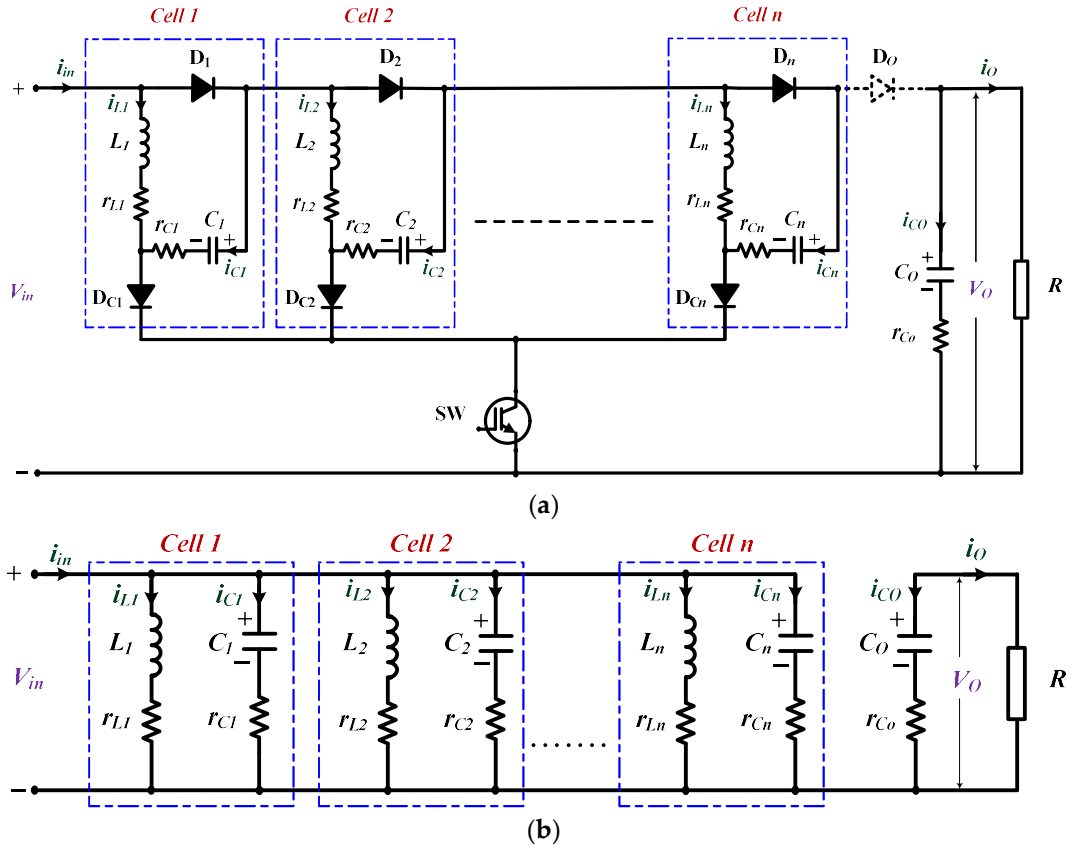


Figure 2. On state equivalent circuit of the proposed multicell converter: (**a**) active and inactive components, and (**b**) analogous electrical circuit.

Using Kirchhoff's voltage law (KVL), the differential equations of each converter cell are derived as

$$v_{in} = i_{Li}\, r_{Li} + L_i \frac{di_{Li}}{dt} \tag{3}$$

$$v_{in} = i_{Ci}\, r_{Ci} + v_{Ci} = r_{Ci}\, C_i \frac{dv_{Ci}}{dt} + v_{Ci} \tag{4}$$

where v_{in} refers to the input voltage, and L_i and r_{Li} are the inductance and the equivalent series resistances (ESR) of the inductor of cell i, respectively. C_i and r_{Ci} are the capacitance and the ESR of the capacitor of cell i, respectively, while i_{Li} and v_{Ci} are the inductor current and the capacitor voltage of the cell i, respectively.

Using KVL/KCL (Kirchhoff's current law), the differential equations of the output circuit are derived as

$$i_o = -i_{Co} \tag{5}$$

where i_o and i_{Co} are the output current and the current via the output capacitor, respectively. These currents are given as

$$i_o = \frac{v_o}{R} = \frac{i_{Co} r_{Co} + v_{Co}}{R} \tag{6}$$

$$i_{Co} = C_o \frac{dv_{Co}}{dt} \tag{7}$$

where C_o and r_{Co} are capacitance and ESR of the output capacitor, respectively. v_o and v_{Co} are the output voltage and the output capacitor voltage, respectively, and R is the output (load) resistance.

For SSAM, the inductor current for the converter cell i_{Li}, the capacitor voltage for the converter cell v_{Ci}, and the voltage across the output capacitor v_{Co} are considered as state variables. Therefore, for an n cell converter, there are $2n + 1$ state variables. Using Equations (3)–(7), the differentiation of the state variables is given as

$$\frac{di_{Li}}{dt} = \frac{1}{L_i} V_{in} - \frac{r_{Li}}{L_i} i_{Li} \tag{8}$$

$$\frac{dv_{Ci}}{dt} = \frac{1}{r_{Ci}\, C_i} V_{in} - \frac{1}{r_{Ci}\, C_i} v_{Ci} \tag{9}$$

$$\frac{dv_{Co}}{dt} = \frac{-1}{C_o\, (r_{Co} + R)} v_{Co} \tag{10}$$

Since the state space equations in the on state can be given as

$$\dot{x} = A_1 x + B_1 u \tag{11}$$

$$y = C_1 x + E_1 u \tag{12}$$

Therefore:

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{dv_{C1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dv_{C2}}{dt} \\ \vdots \\ \frac{di_{Ln}}{dt} \\ \frac{dv_{Cn}}{dt} \\ \frac{dv_{Co}}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-r_{L1}}{L_1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{-1}{r_{C1}C_1} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-r_{L2}}{L_2} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{r_{C2}C_2} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \ddots & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-r_{Ln}}{L_n} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{r_{Cn}C_n} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{C_o(r_{Co}+R)} \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{C1} \\ i_{L2} \\ v_{C2} \\ \vdots \\ i_{Ln} \\ v_{Cn} \\ v_{Co} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{r_{C1}C_1} \\ \frac{1}{L_2} \\ \frac{1}{r_{C2}C_2} \\ \vdots \\ \frac{1}{L_n} \\ \frac{1}{r_{Cn}C_n} \\ 0 \end{bmatrix} v_{in} \tag{13}$$

The output voltage in the on state is given as

$$v_o = \begin{bmatrix} 0 & 0 & 0 & 0 & \cdots & 0 & 0 & \frac{R}{r_{Co}+R} \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{C1} \\ i_{L2} \\ v_{C2} \\ \vdots \\ i_{Ln} \\ v_{Cn} \\ v_{Co} \end{bmatrix} + [0] v_{in} \tag{14}$$

3.2. Off State ($dT_s < t < T_s$)

Figure 3 illustrates the off-state equivalent circuit of the proposed multicell converter. The active and inactive semiconductor devices are shown in Figure 3a, while the analogous circuit diagram is illustrated in Figure 3b. In the off state, the semiconductor switch and all

diodes except the output diode (D_o) are open. Using KVL/KCL, the general differential equation of the multicell converter in the off state is derived as

$$v_{in} = \sum_{i=1}^{n} \left(i_{Li}\, r_{Li} + L_i \frac{di_{Li}}{dt} - i_{Ci}\, r_{Ci} - v_{Ci} \right) + v_o \tag{15}$$

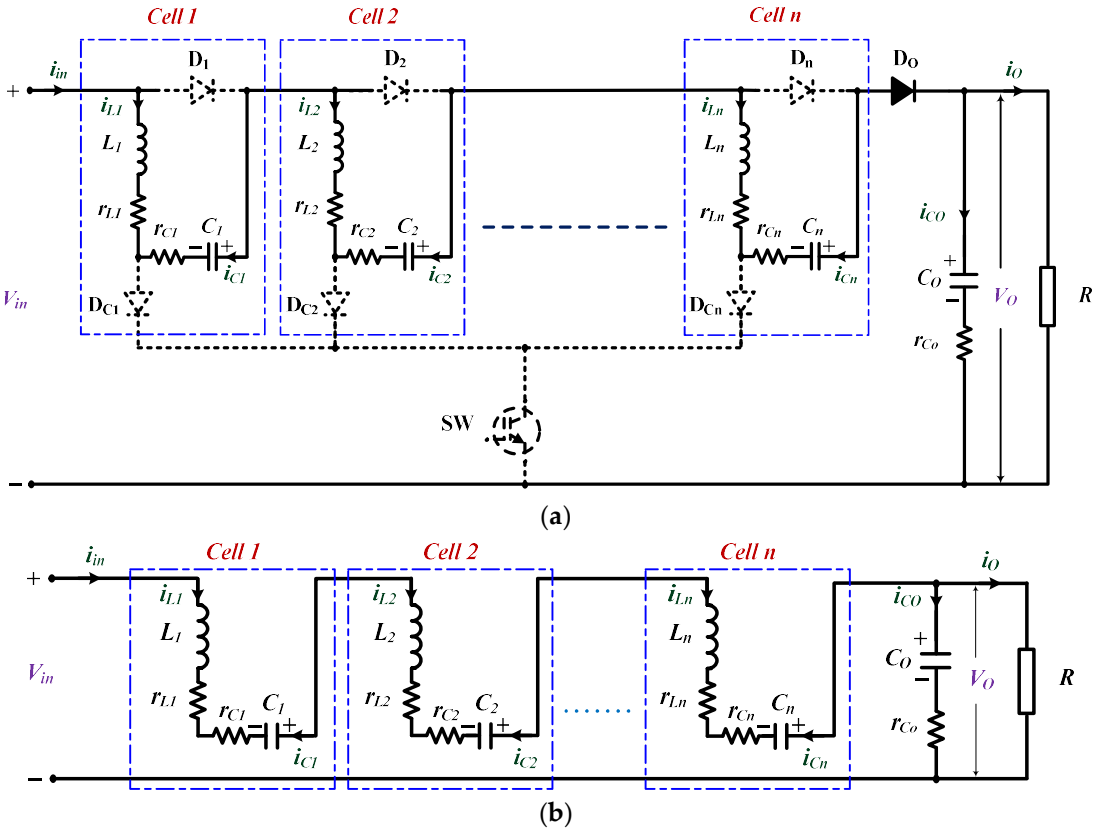


Figure 3. Off-state equivalent circuit of the proposed multicell converter: (**a**) active and inactive components, and (**b**) analogous electrical circuit.

Since

$$i_{Ci} = -i_{Li} \tag{16}$$

Therefore,

$$v_{in} = \sum_{i=1}^{n} \left(i_{Li}(r_{Li} + r_{Ci}) + L_i \frac{di_{Li}}{dt} - v_{Ci} \right) + v_o \tag{17}$$

Since

$$i_{L1} = i_{L2} = i_{Ln} \tag{18}$$

Therefore,

$$i_o = i_{L1} - i_{Co} \tag{19}$$

Using Equations (17)–(19), the differentiation of the state variables is given as

$$\frac{di_{Li}}{dt} = \frac{1}{nL_i} v_{in} + \alpha_i i_{Li} + \frac{1}{L_i} v_{Ci} - \frac{1}{nL_i} \left(\frac{R}{r_{Co} + R} \right) v_{Co} \tag{20}$$

where

$$\alpha_i = \frac{-1}{L_i} \left(r_{Li} + r_{Ci} + \frac{r_{Co}\, R}{n\,(r_{Co} + R)} \right) \tag{21}$$

$$\frac{dv_{Ci}}{dt} = \frac{-1}{C_i} i_{Li} \tag{22}$$

$$\frac{dv_{Co}}{dt} = \frac{R}{C_o\,(r_{Co}+R)} i_{L1} + \frac{-1}{C_o\,(r_{Co}+R)} v_{Co} \tag{23}$$

where i_{L1} is the inductor current of cell 1. Since the state space equations in the off state can be given as

$$\dot{x} = A_2 x + B_2 u \tag{24}$$

$$y = C_2 x + E_2 u \tag{25}$$

Therefore:

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{dv_{C1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{dv_{C2}}{dt} \\ \vdots \\ \frac{di_{Ln}}{dt} \\ \frac{dv_{Cn}}{dt} \\ \frac{dv_{Co}}{dt} \end{bmatrix} = \begin{bmatrix} \alpha_1 & \frac{1}{L_1} & 0 & 0 & 0 & 0 & 0 & \frac{-1}{nL_1}\left(\frac{R}{r_{Co}+R}\right) \\ \frac{-1}{C_1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \alpha_2 & \frac{1}{L_2} & 0 & 0 & 0 & \frac{-1}{nL_2}\left(\frac{R}{r_{Co}+R}\right) \\ 0 & 0 & \frac{-1}{C_2} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \ddots & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \alpha_n & \frac{1}{L_n} & \frac{-1}{nL_n}\left(\frac{R}{r_{Co}+R}\right) \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{C_n} & 0 & 0 \\ \frac{R}{C_o(r_{Co}+R)} & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{C_o(r_{Co}+R)} \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{C1} \\ i_{L2} \\ v_{C2} \\ \vdots \\ i_{Ln} \\ v_{Cn} \\ v_{Co} \end{bmatrix} + \begin{bmatrix} \frac{1}{nL_1} \\ 0 \\ \frac{1}{nL_2} \\ 0 \\ \vdots \\ \frac{1}{nL_n} \\ 0 \\ 0 \end{bmatrix} v_{in} \tag{26}$$

where α_1, α_2 and α_n are

$$\alpha_1 = \frac{-1}{L_1}\left(r_{L1} + r_{C1} + \frac{r_{Co}R}{n(r_{Co}+R)}\right) \tag{27}$$

$$\alpha_2 = \frac{-1}{L_2}\left(r_{L2} + r_{C2} + \frac{r_{Co}R}{n(r_{Co}+R)}\right) \tag{28}$$

$$\alpha_n = \frac{-1}{L_n}\left(r_{Ln} + r_{Cn} + \frac{r_{Co}R}{n(r_{Co}+R)}\right) \tag{29}$$

The output voltage in the off state is given as

$$v_o = \begin{bmatrix} \frac{r_{Co}R}{r_{Co}+R} & 0 & 0 & 0 & \cdots & 0 & 0 & \frac{R}{r_{Co}+R} \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_{C1} \\ i_{L2} \\ v_{C2} \\ \vdots \\ i_{Ln} \\ v_{Cn} \\ v_{Co} \end{bmatrix} + [0] v_{in} \tag{30}$$

3.3. Average Model

Since the SSAM expresses the average behavior of the state variables over a switching period, the state space averaged description is given as

$$\dot{x} = Ax + Bu \tag{31}$$

$$y = Cx + Eu \tag{32}$$

where the A, B, C, and E matrices are given as

$$A = dA_1 + \grave{d}A_2 \tag{33}$$

$$B = dB_1 + \acute{d}B_2 \tag{34}$$

$$C = dC_1 + \acute{d}C_2 \tag{35}$$

$$E = dE_2 + \acute{d}E_2 \tag{36}$$

where

$$\acute{d} = (1 - d) \tag{37}$$

Hence

$$A = \begin{bmatrix} \frac{-r_{L1}}{L_1}d + \alpha_1\acute{d} & \frac{1}{L_1}\acute{d} & 0 & 0 & 0 & 0 & 0 & \frac{-1}{nL_1}\left(\frac{R}{r_{Co}+R}\right)\acute{d} \\ \frac{-1}{C_1}\acute{d} & \frac{-1}{r_{C1}C_1}d & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-r_{L2}}{L_2}d + \alpha_2\acute{d} & \frac{1}{L_2}\acute{d} & 0 & 0 & 0 & \frac{-1}{nL_2}\left(\frac{R}{r_{Co}+R}\right)\acute{d} \\ 0 & 0 & \frac{-1}{C_2}\acute{d} & \frac{-1}{r_{C2}C_2}d & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \ddots & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-r_{Ln}}{L_n}d + \alpha_n\acute{d} & \frac{1}{L_n}\acute{d} & \frac{-1}{nL_n}\left(\frac{R}{r_{Co}+R}\right)\acute{d} \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{C_n}\acute{d} & \frac{-1}{r_{Cn}C_n}d & 0 \\ \frac{R}{C_o(r_{Co}+R)}\acute{d} & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{C_o(r_{Co}+R)} \end{bmatrix} \tag{38}$$

$$B = \begin{bmatrix} \frac{d}{L_1} + \frac{\acute{d}}{nL_1} \\ \frac{d}{r_{C1}C_1} \\ \frac{d}{L_2} + \frac{\acute{d}}{nL_2} \\ \frac{d}{r_{C2}C_2} \\ \vdots \\ \frac{d}{L_n} + \frac{\acute{d}}{nL_n} \\ \frac{d}{r_{Cn}C_n} \\ 0 \end{bmatrix} \tag{39}$$

$$C = \begin{bmatrix} \frac{r_{Co}R\acute{d}}{r_{Co}+R} & 0 & 0 & 0 & \cdots & 0 & 0 & \frac{R}{r_{Co}+R} \end{bmatrix} \tag{40}$$

$$E = [0] \tag{41}$$

At steady state,

$$\dot{x} = 0 \tag{42}$$

Therefore, the average values of the state variables of the proposed multicell step-up converter are calculated as

$$x = -A^{-1}Bu \tag{43}$$

4. Small Signal Analysis

Small signal analysis is a useful technique for examining the dynamic performance and stability of power electronics converters. It can be used to determine the transfer functions to examine the output performance of the power electronics converters against disturbances or variations in the input. To obtain the SSM of the proposed single-switch multicell step-up

DC-DC converter, a perturbation in all variables of the SSAM is introduced around the steady-state operating point such that

$$x = X + \widetilde{x} \tag{44}$$

$$u = U + \widetilde{u} \tag{45}$$

$$y = Y + \widetilde{y} \tag{46}$$

$$d = D + \widetilde{d} \tag{47}$$

$$\acute{d} = \acute{D} - \widetilde{d} \tag{48}$$

$$\acute{D} = 1 - D \tag{49}$$

$$v_{in} = V_{in} + \widetilde{v}_{in} \tag{50}$$

$$v_o = V_o + \widetilde{v}_o \tag{51}$$

where the capitalized quantities (X, Y, D, V_{in}, ...) are the steady state values (DC values) and the dashed quantities ($\widetilde{x}$, $\widetilde{y}$, $\widetilde{d}$, $\widetilde{v}_{in}$, ...) are small perturbations (AC values). Since the SSAM can be given as

$$\frac{dx}{dt} = (dA_1 + \acute{d}A_2)x + (dB_1 + \acute{d}B_2)u \tag{52}$$

Therefore,

$$\frac{d\left(X + \widetilde{x}\right)}{dt} = ((D + \widetilde{d})A_1 + (\acute{D} - \widetilde{d})A_2)\left(X + \widetilde{x}\right) + ((D + \widetilde{d})B_1 + (\acute{D} - \widetilde{d})B_2)(U + \widetilde{u}) \tag{53}$$

Hence,

$$\begin{aligned}\tfrac{d\widetilde{x}}{dt} = &\underbrace{(DA_1 + \acute{D}A_2)X + (DB_1 + \acute{D}B_2)U}_{} + \underbrace{(DA_1 + \acute{D}A_2)\widetilde{x}}_{} + \underbrace{(DB_1 + \acute{D}B_2)\widetilde{u}}_{} \\ &+ \underbrace{((A_1 - A_2)X + (B_1 - B_2)U)\widetilde{d}}_{} + \underbrace{((A_1 - A_2) + (B_1 - B_2))\widetilde{d}\widetilde{x}}_{}\end{aligned} \tag{54}$$

The previous equation consists of five terms. The first term is neglected because it is DC (steady state). The fifth term is a second-order term. It is also neglected because the value obtained from multiplication of the two incremental terms (around the equilibrium point) would be very small compared to the first-order terms, while the other three terms are first-order linear terms. Therefore, the state space equations of SSM can be given as

$$\frac{d\widetilde{x}}{dt} = (DA_1 + \acute{D}A_2)\widetilde{x} + (DB_1 + \acute{D}B_2)\widetilde{u} + ((A_1 - A_2)X + (B_1 - B_2)U)\widetilde{d} \tag{55}$$

Using the same previous procedure:

$$\widetilde{y} = (DC_1 + \acute{D}C_2)\widetilde{x} + (DE_1 + \acute{D}E_2)\widetilde{u} + ((C_1 - C_2)X + (E_1 - E_2)U)\widetilde{d} \tag{56}$$

Therefore, the duty cycle to the output voltage (control-to-output) transfer function $G_{vd}(s)$ of the proposed multicell converter can be given as

$$\begin{aligned}G_{vd}(s) = \left.\frac{\widetilde{v}_o(s)}{\widetilde{d}(s)}\right|_{\widetilde{v}_{in}(s)=0} &= (DC_1 + \acute{D}C_2)(sI - (DA_1 + \acute{D}A_2))^{-1}((A_1 - A_2)X \\ &+ (B_1 - B_2)U) + ((C_1 - C_2)X + (E_1 - E_2)U)\end{aligned} \tag{57}$$

where I is the identity matrix, while the input voltage to the output voltage (input-to-output) transfer function $G_{vg}(s)$ of the proposed multicell converter can be given as

$$\begin{aligned} G_{vg}(s) = \left.\frac{\widetilde{v}_o(s)}{\widetilde{v}_{in}(s)}\right|_{\widetilde{d}(s)=0} \\ = (DC_1 + \acute{D}C_2)(sI - (DA_1 + \acute{D}A_2))^{-1}(DB_1 + \acute{D}B_2) \\ +(DE_1 + \acute{D}E_2) \end{aligned} \tag{58}$$

Table 1 displays the parameters of the proposed single-switch two-cell boost DC-DC converter that are used for the simulation and experimental purposes.

Table 1. Parameters of the proposed single-switch two-cell boost converter.

Parameter	Value
V_{in}	24 V
V_o	132 V
r_{Li}	0.64 Ω
L_i	1.7 mH
r_{Ci}	0.12 Ω
C_i	47 µF
r_{Co}	0.12 Ω
C_o	47 µF
F_s	5 kHz
R	130 Ω
Diodes	MUR1560
Main switch (SW)	FGH40N60UFD

Using Equation (57), the open-loop control-to-output transfer function $G_{vd}(s)$ of the proposed two-cell boost converter is determined as

$$G_{vd}(s) = \frac{-0.2113\,s^5 - 7.348 \times 10^4 s^4 - 7.793 \times 10^9 s^3 - 2.379 \times 10^{14} s^2 + 2.022 \times 10^{18} s + 9.906 \times 10^{20}}{s^5 + 1.783 \times 10^5 s^4 + 8.049 \times 10^9 s^3 + 8.928 \times 10^{12} s^2 + 1.529 \times 10^{16} s + 5.981 \times 10^{18}} \tag{59}$$

Using Equation (58), the open-loop input-to-output transfer function $G_{vg}(s)$ of the proposed two-cell boost converter is determined as

$$G_{vg}(s) = \frac{26.45\,s^4 + 1.095 \times 10^7 s^3 + 1.46 \times 10^{12} s^2 + 6.207 \times 10^{16} s + 2.854 \times 10^{19}}{s^5 + 1.783 \times 10^5 s^4 + 8.049 \times 10^9 s^3 + 8.928 \times 10^{12} s^2 + 1.529 \times 10^{16} s + 5.981 \times 10^{18}} \tag{60}$$

5. Stability Analysis

As important measures of the converter stability, Figure 4 illustrates the bode plot diagram of the open-loop control-to-output transfer function $G_{vd}(s)$ of the suggested two-cell boost converter, while the root locus diagram is shown in Figure 5. It is found that the gain margin $G_m = -35.2$ dB at phase crossover frequency $F_{cp} = 403$ Hz and phase margin $P_m = -66.2^\circ$ at gain crossover frequency $F_{cg} = 6220$ Hz, which refers to the instability. Also, as shown in Figure 5, there is a zero on the right half side of the s-plane.

Figure 6 illustrates the bode plot diagram of the open-loop input-to-output transfer function $G_{vg}(s)$ of the proposed two-cell boost converter, while the root locus diagram is displayed in Figure 7. It is found that the phase margin $P_m = 14.3^\circ$ at gain crossover frequency $F_{cg} = 483$ Hz, which refers to the stability.

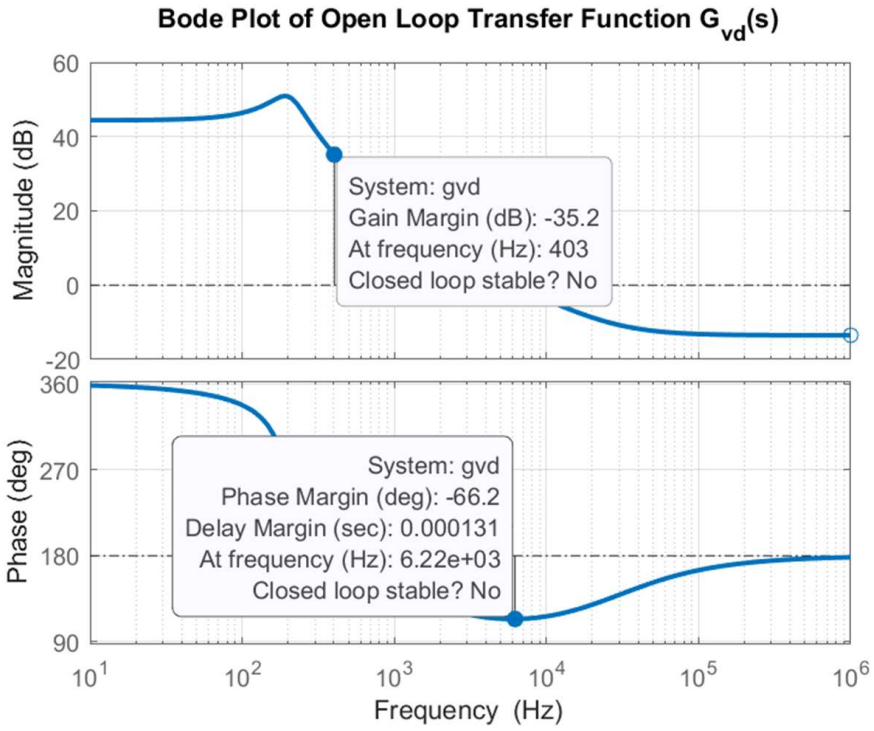


Figure 4. Bode plot diagram of the open-loop control-to-output transfer function of the proposed multicell converter (n = 2).

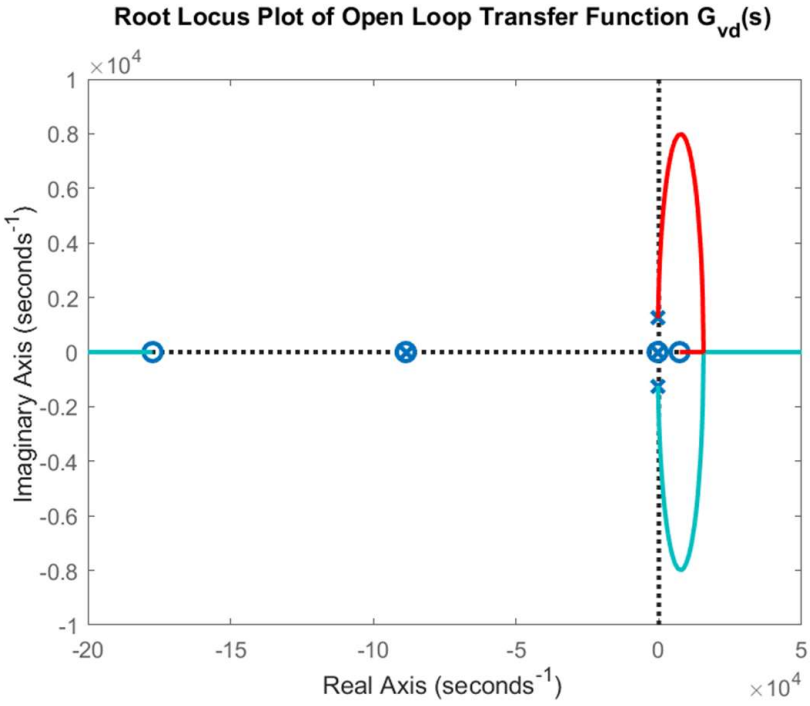


Figure 5. Root locus diagram of the open-loop control-to-output transfer function of the proposed multicell converter (n = 2).

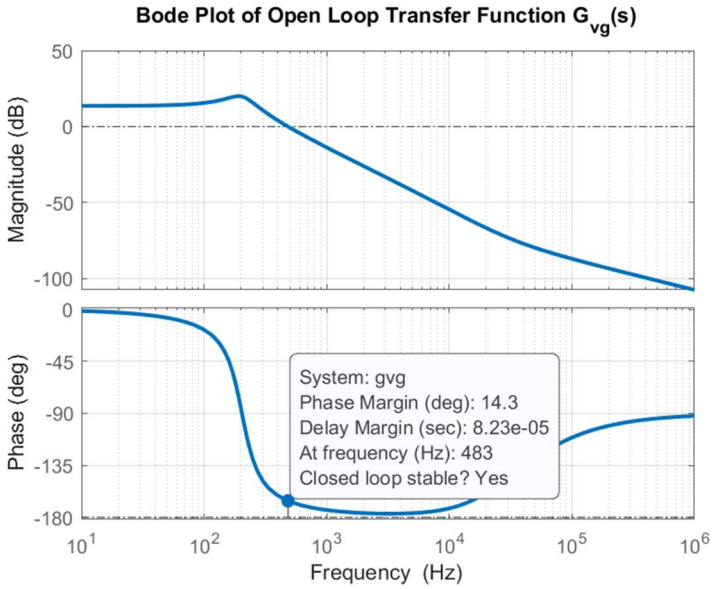


Figure 6. Bode plot diagram of the open-loop input-to-output transfer function of the proposed multicell converter (n = 2).

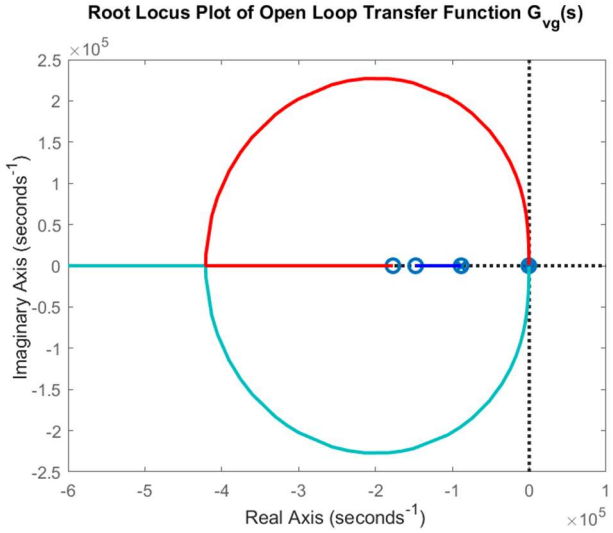


Figure 7. Root locus diagram of the open-loop input-to-output transfer function of the proposed multicell converter (n = 2).

6. Experimental System Setup

To prove the validity of the developed SSAM of the proposed multicell converter, an experimental setup of the presented topology with two cells (n = 2) has been built and its performance has been compared with the simulated performance based on the SSAM of the suggested converter.

Figure 8 shows a photo of the actual experimental setup of the proposed single-switch two-cell boost DC-DC converter. It consists of a DC power supply (24 V, 20 A), a single-switch two-cell proposed boost DC-DC converter, a resistive load, a function generator (AFG-3051, 50 MHz, GW Instek, Taipei, Taiwan), a digital storage oscilloscope (TDS8204, 200 MHz, 2 GSa/s, Owon, Zhangzhou, China), a digital signal processor (DS1104, dSPACE, Paderborn, Germany), a voltage transducer (LV 25-p, LEM, Meyrin, Switzerland), and a drive circuit. The proposed converter is supplied from a DC source 24 V to supply a resistive load of 130 Ω by controlling the power switch pulses that come from the function generator with a switching frequency of 5 KHz. The oscilloscope is used to capture the

voltage and current waveforms. The proposed converter circuit is examined in both open-loop and closed-loop operations. The schematic diagram for the experimental setup system is shown in Figure 9. This system shows the system structure for open-loop and closed-loop operations.

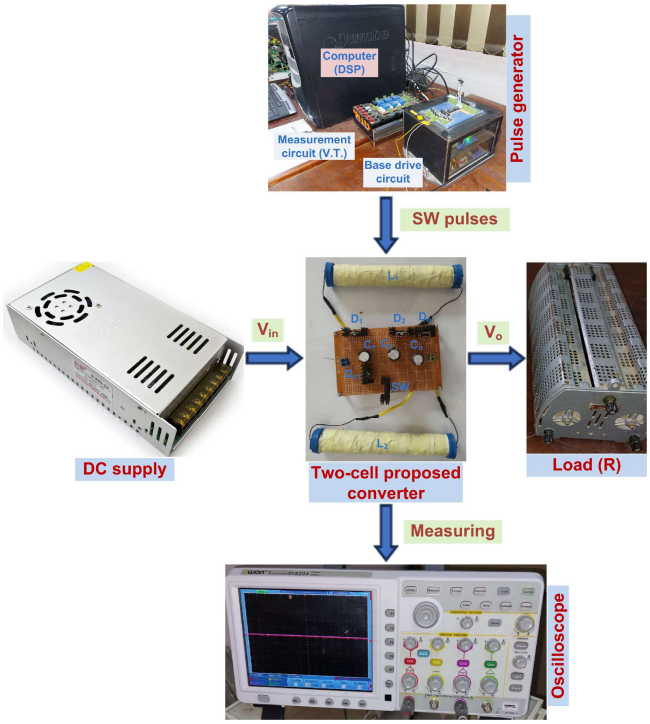


Figure 8. Actual photos of the experimental setup system components for open-loop and closed-loop operations.

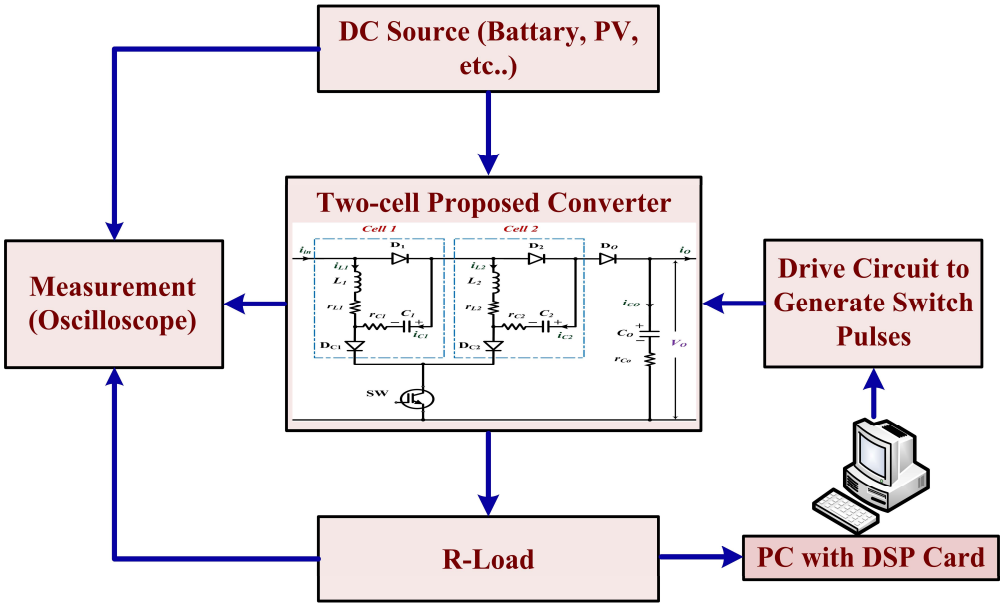
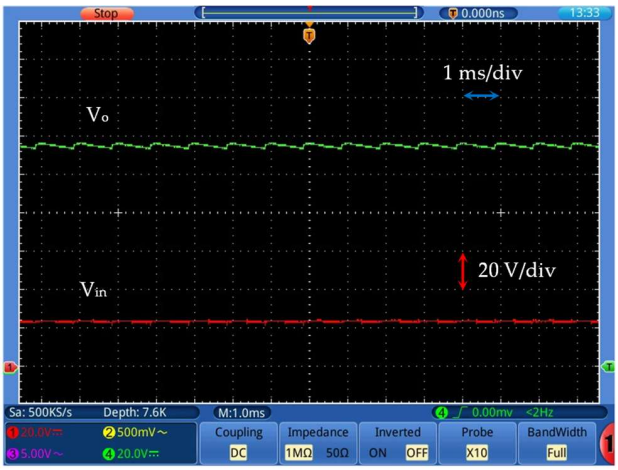


Figure 9. The schematic diagram for the experimental setup system for open-loop and closed-loop operations.

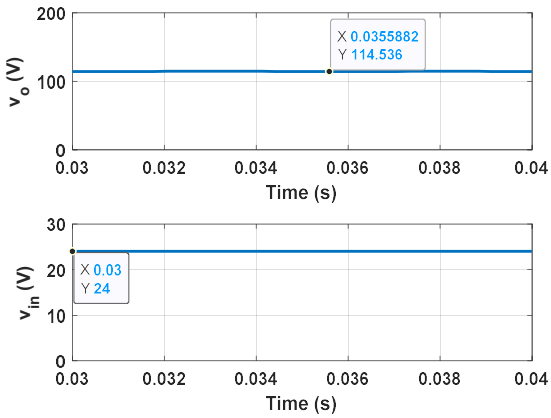
7. Open-Loop Performance

The proposed single-switch two-cell boost DC-DC converter is first examined in the open-loop operation. Figures 10 and 11 show the comparison between the experimental and

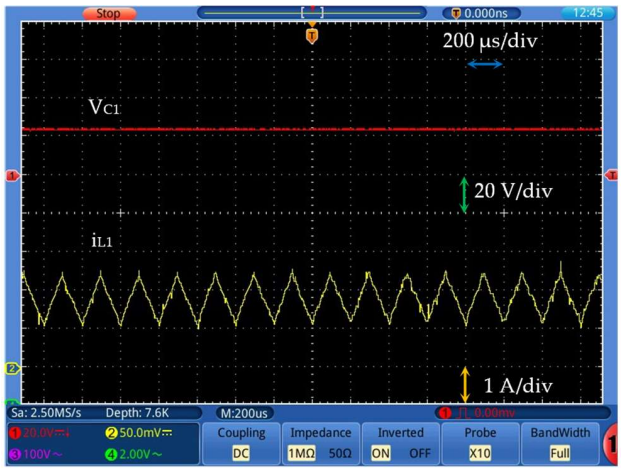
simulated SSAM open-loop performance of the proposed single-switch two-cell boost DC-DC converter at duty cycles $D = 0.5$ and $D = 0.6$, respectively. The simulation results are obtained using Matlab R2023b software. The steady-state average values of the variables (V_o, V_{C1}, i_{L1}, V_{C2}, and i_{L2}) of the SSAM of the suggested topology are compared to the corresponding experimental switching waveforms captured from the actual laboratory setup at steady state at the same input voltage V_{in} = 24 V. As shown in Figure 10, the SSAM simulation gives a theoretical average output voltage (V_o) of 114.54 V, while the output voltage of the experimental converter oscillates between 113 V and 117 V due to switching (experimental average of (113 + 117)/2 = 115 V). Therefore, the theoretical average (114.54 V) and the experimental average (115 V) of the output voltage are very close, which proves the SSAM validation. Also, the inductor currents (i_{L1} and i_{L2}) are similar in experimental and simulation tests. The steady-state value of the simulated inductor current-based SSAM of the converter has a value of 1.76 A, while the steady-state experimental inductor current (i_{L1} or i_{L2}) oscillates between 1.1 A and 2.6 A (experimental average of (1.1 + 2.6)/2 = 1.85 A). Moreover, the capacitors' voltages (v_{C1} and v_{C2}) are similar in experimental and simulation tests.



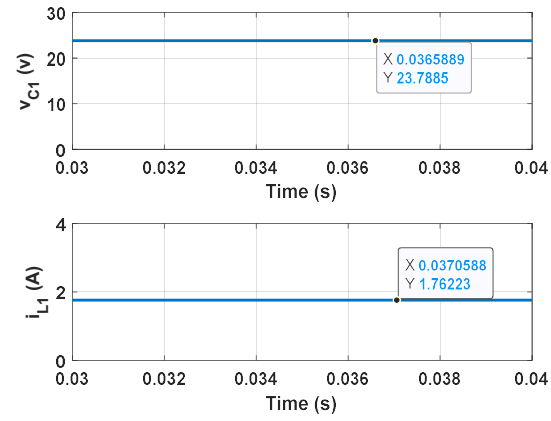
(**a**) experimental V_o and V_i



(**b**) simulated V_o and V_i

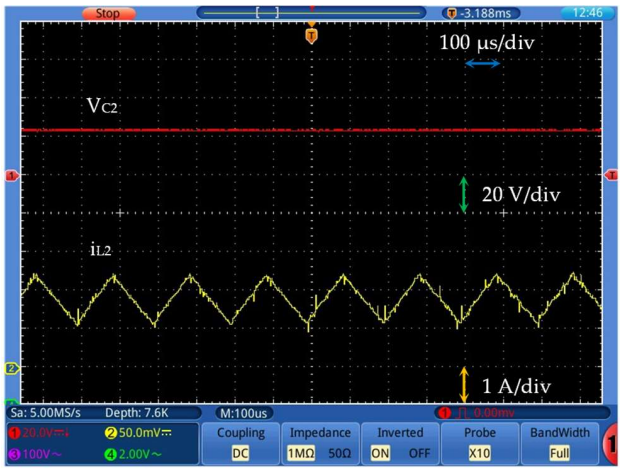


(**c**) experimental V_{c1} and i_{L1}

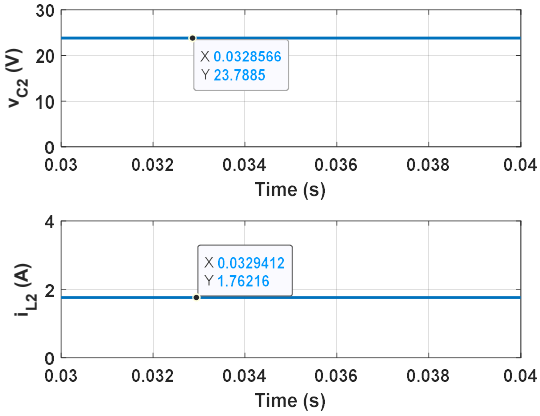


(**d**) simulated V_{c1} and i_{L1}

Figure 10. *Cont.*

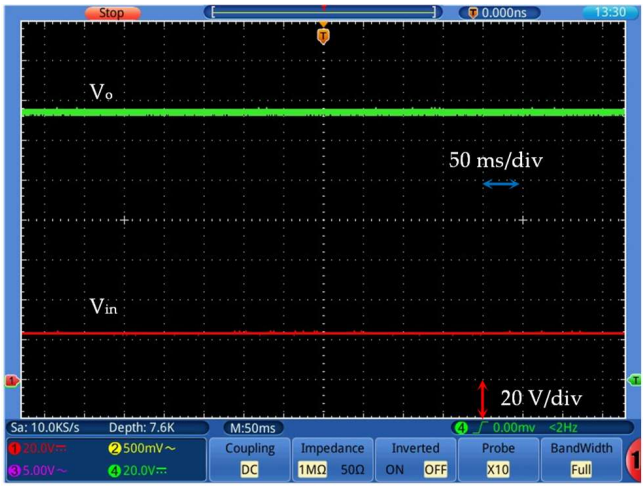


(**e**) experimental V_{C2} and i_{L2}

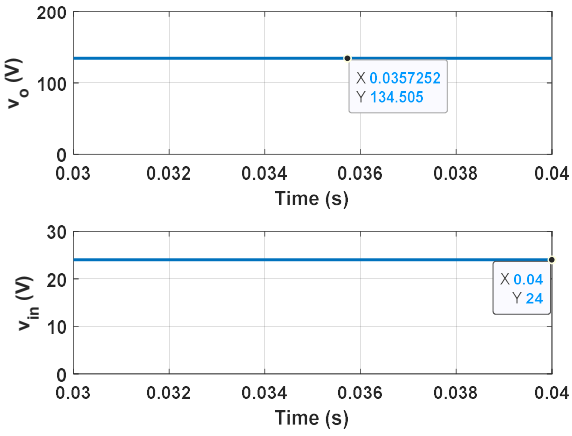


(**f**) simulated V_{C2} and i_{L2}

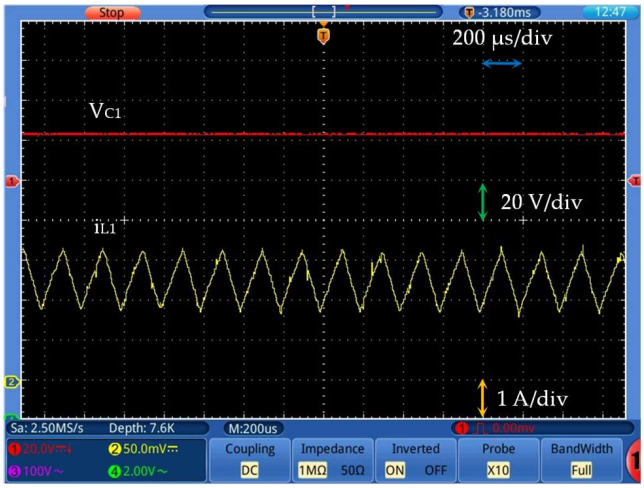
Figure 10. Open-loop performance of the proposed multicell converter (n = 2) when the input voltage V_{in} = 24 V, D = 0.5, and F_s = 5 kHz: (**a**,**c**,**e**) experimental and (**b**,**d**,**f**) simulation results based on the SSAM.



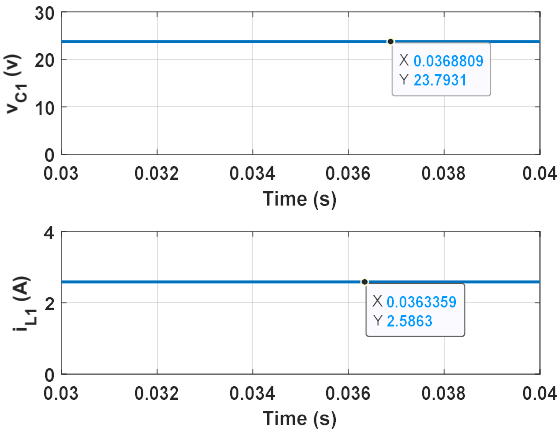
(**a**) experimental V_o and V_i



(**b**) simulated V_o and V_i

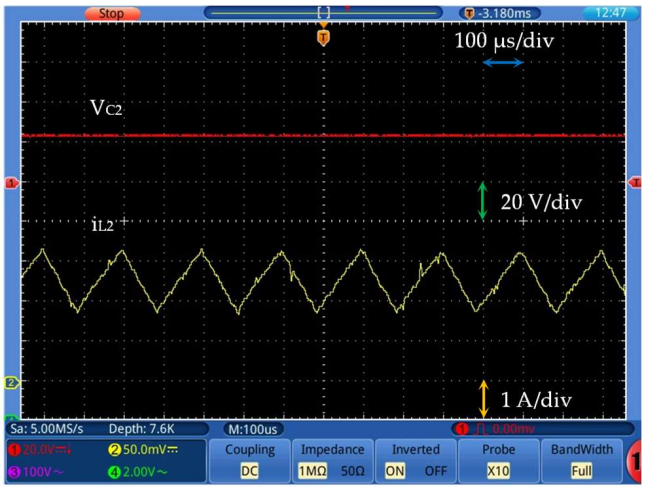


(**c**) experimental V_{C1} and i_{L1}

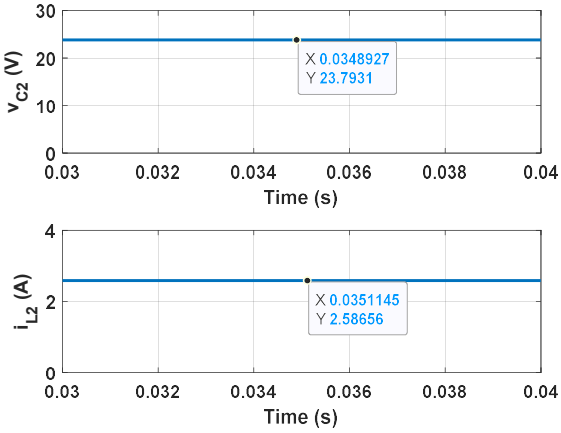


(**d**) simulated V_{C1} and i_{L1}

Figure 11. *Cont.*



(**e**) experimental V_{C2} and i_{L2}



(**f**) simulated V_{C2} and i_{L2}

Figure 11. Open-loop performance of the proposed multicell converter (n = 2) when the input voltage V_{in} = 24 V, D = 0.6, and F_s = 5 kHz: (**a**,**c**,**e**) experimental and (**b**,**d**,**f**) simulation results based on the SSAM.

The steady-state simulated capacitor voltage has a value of 23.79 V, while the corresponding steady-state experimental capacitor voltage (v_{C1} or v_{C2}) oscillates between 23.5 V and 24 V. Similar performances are obtained when the converter is operated at duty cycle D = 0.6, as shown in Figure 11. The SSAM smooths out the switching ripple inherent in the state variables of the experimental converter. Moreover, the comparison between the obtained simulation and experimental results validates the developed SSAM of the proposed converter.

8. Closed-Loop Performance

The experimental prototype of the proposed multicell converter (n = 2) is also examined during a closed-loop control. Converter stability and dynamic performance need to be improved by designing the PI controller. Consequently, the phase and gain margins by designing a robust feedback (closed-loop) controller are properly selected. A schematic diagram of the circuit that is utilized to control the output voltage of the proposed converter is shown in Figure 12.

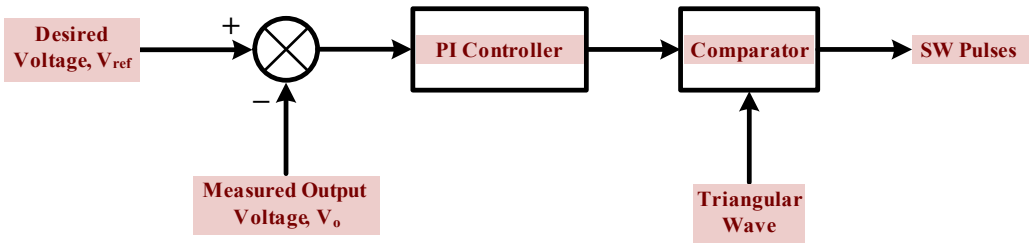


Figure 12. A schematic graph of a closed-loop control circuit with PI controller.

8.1. PI Controller

The transfer function of the PI controller is given as

$$G_{PI}(s) = \frac{K_P\, s + K_I}{s} \tag{61}$$

where K_P and K_I are the parameters of the PI controller. To obtain a stable and well-regulated DC-DC converter, the phase margin of the controlled converter should be greater than 45° [41]. A higher phase margin enhances the transient performance of the

converter. A PI controller is designed to regulate the output voltage of the multi-cell DC-DC boost converter against load, input voltage, and reference voltage variations. The PI controller parameters are selected based on the stability analysis using the frequency response technique. The proportional (K_P) and integral (K_I) gains of the PI controller are selected to be $K_P = 0.001$ and $K_I = 0.4$ based on the required phase margin of 96.8° and gain margin of 15.3 dB. Figure 13 displays a bode plot of the closed-loop system with the designed PI controller. It is clear from the figure that the designed closed-loop control system is stable.

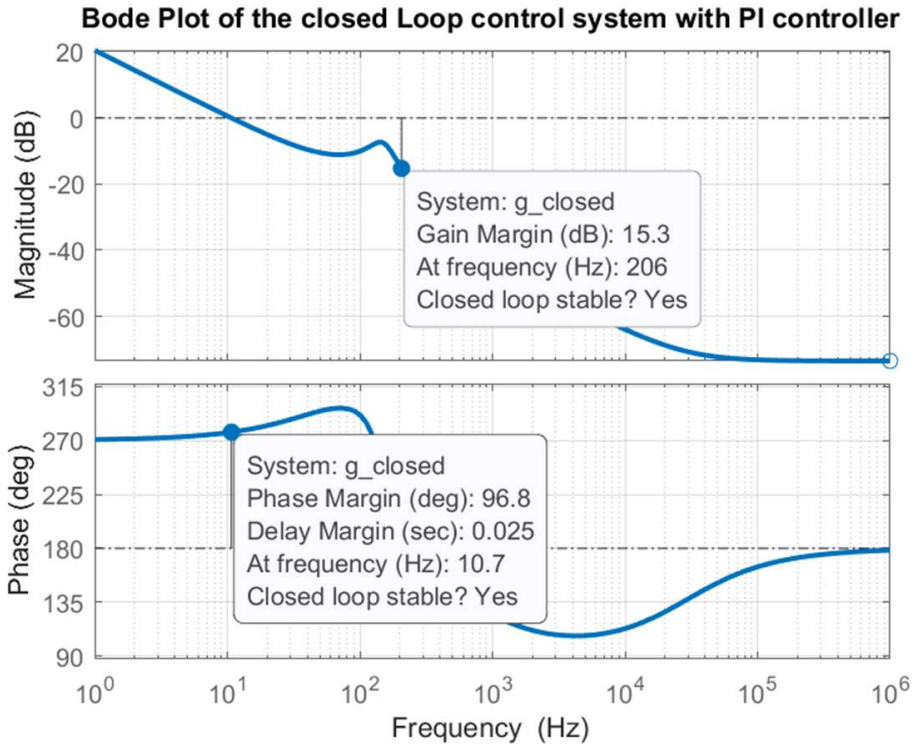


Figure 13. Bode plot diagram of the closed-loop control system of the proposed multicell converter ($n = 2$) with the designed PI controller based on stability analysis.

8.2. Closed-Loop Results

The experimental responses of the proposed multicell converter ($n = 2$) during closed-loop control are captured. Figure 14 shows the output voltage response starting with changing the reference voltage (V_{ref}) to 150 V at $V_{in} = 24$ V. It is observed that the output voltage signal has a good dynamic response and tracks the reference voltage smoothly without overshoots and undershoots. To examine the robustness of the closed-loop control of the proposed multicell converter ($n = 2$), Figure 15 demonstrates the output voltage and current responses by changing the resistive value of the load at $V_{ref} = 140$ V. Figure 16 presents the output voltage response at $V_{ref} = 145$ V by changing the input voltage (V_{in}) from 31 V → 24 V → 31 V. As obvious, the output voltage signal has a good dynamic response. Also, Figure 17 shows the output voltage response at $V_{in} = 24$ V by changing the reference voltage (V_{ref}) from 125 V → 115 V. The output voltage response tracks the reference voltage smoothly.

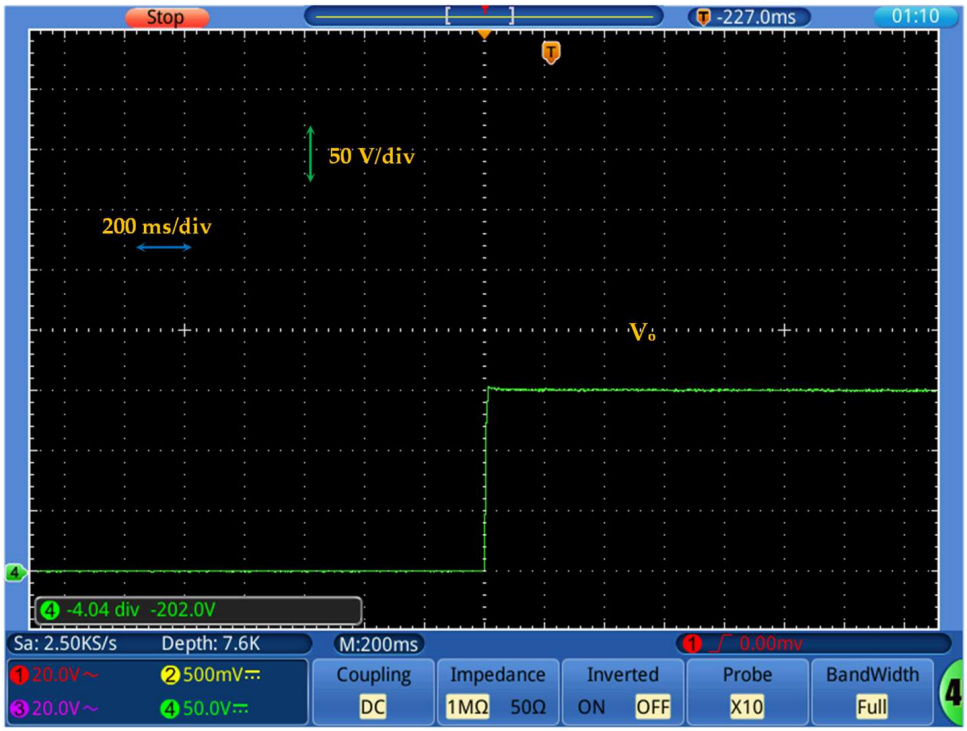


Figure 14. Output voltage response starting with changing the reference voltage (V_{ref}) to 150 V at V_{in} = 24 V.

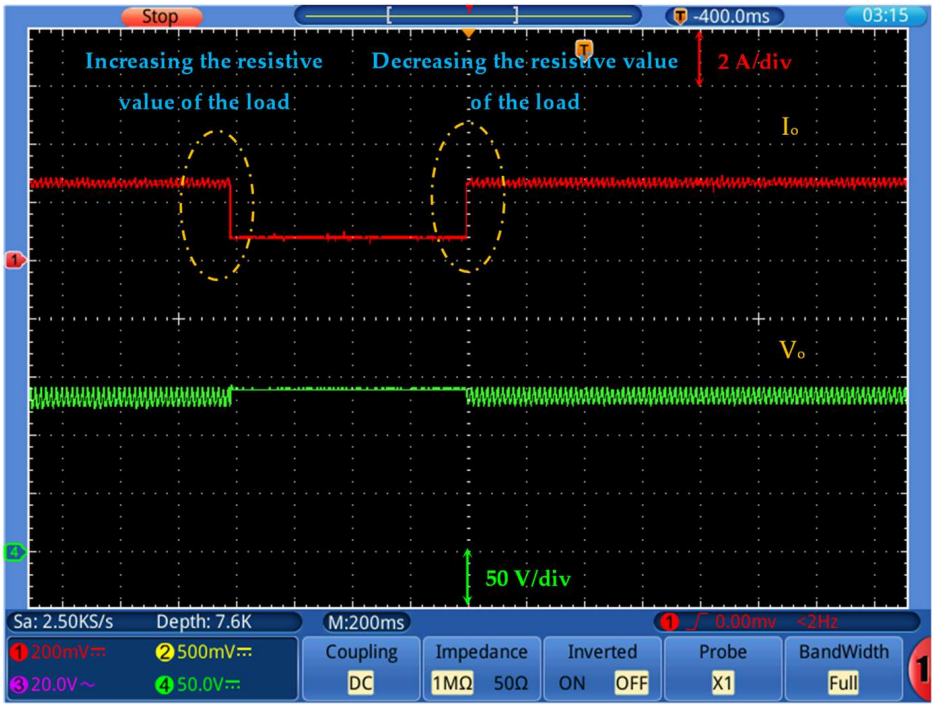


Figure 15. Output voltage and current responses with the load variation at V_{ref} = 140 V.

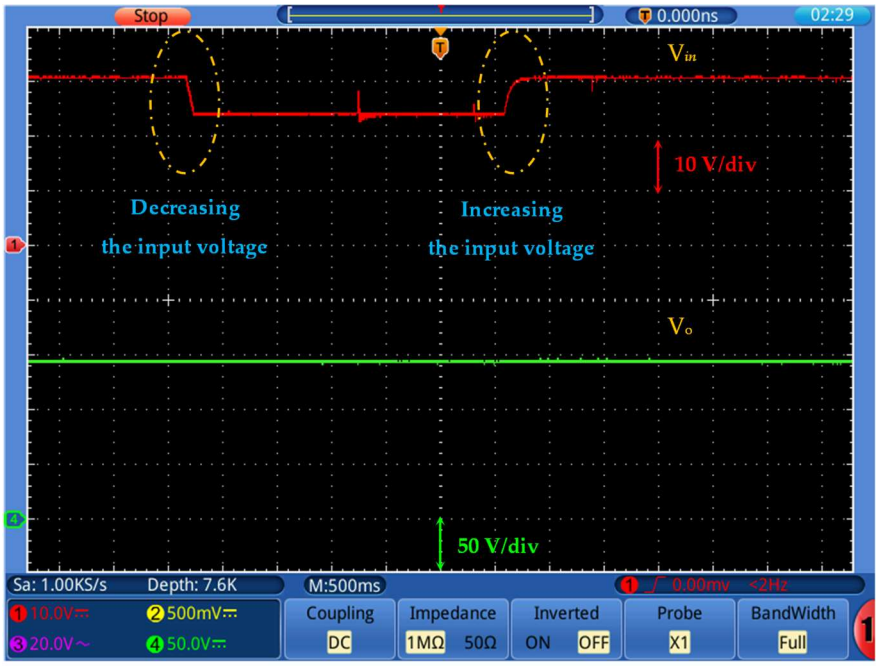


Figure 16. Output voltage response at V_{ref} = 145 V by changing the input voltage (V_{in}) from 31 V → 24 V → 31 V.

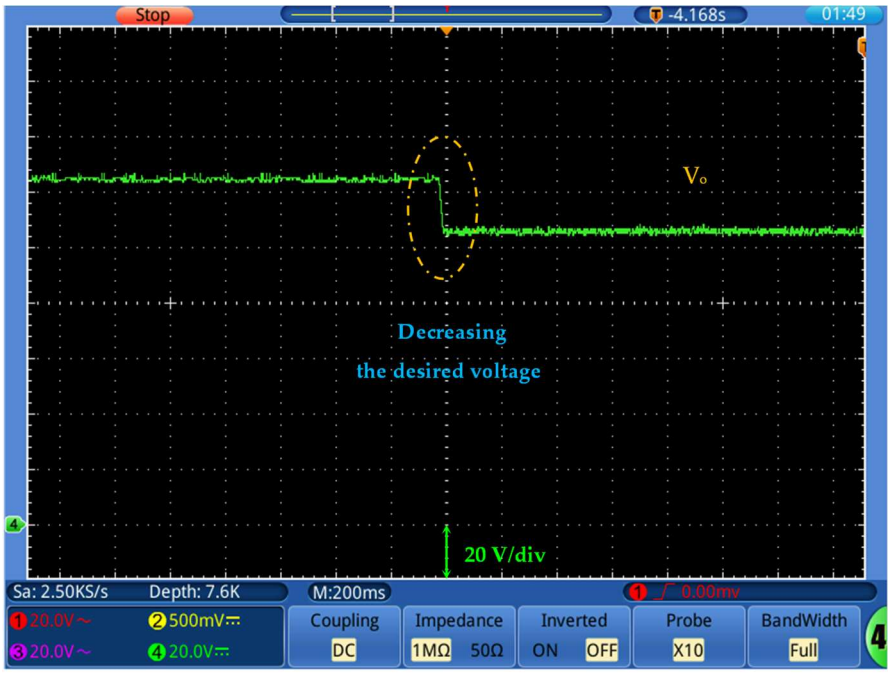


Figure 17. Output voltage response at V_{in} = 24 V by changing the desired voltage (V_{ref}) from 125 V → 115 V.

9. Comparison with Recent Converters

To evaluate the effectiveness of the single-switch high-gain multicell boost DC-DC converter, a comprehensive comparison between the proposed converter and previous boost converters is provided, as shown in Table 2. The number of components, which include switches, inductors, diodes, and capacitors, are presented for the proposed and other converters. It is obvious that the proposed converter has a smaller number of components compared to previous converters [25,27,29,30] and has an identical number of components as that reported in [26], and more than that in [28], which has the smaller

count. Therefore, this converter topology structure contributes to a cost-effective system that is compact and lightweight compared to other topologies.

Table 2. Comparison between the two-cell proposed converter and recent topologies.

Item	Ref. [25]	Ref. [26]	Ref. [27]	Ref. [28]	Ref. [29]	Ref. [30]	The Proposed $n = 2$
Switch, SW	2	2	1	2	3	1	1
Inductor, L	4	3	4	2	6	3	2
Capacitor, C	1	3	6	2	1	7	3
Diode, D	9	2	3	2	11	5	4
Total Component Count	16	10	14	8	21	16	10
Gain, G	$\frac{(1+3\,D)}{(1-D)}$	$\frac{D}{(1-D)^2}$	$\frac{3\,D}{(1-D)}$	$\frac{2}{(1-D)}$	$\frac{(1+5\,D)}{(1-D)}$	$\frac{(2+2\,D)}{(1-D)}$	$\frac{(4-3\,D)}{(1-D)}$
Normalized Voltage Stress on the SW (V_{SW}/V_{in})	$\frac{(G+1)}{2\,G}$	$\frac{G}{D}$	$\frac{(G+3)}{3}$	$\frac{G}{2}$	$\frac{(G+2)}{3}$	$\frac{(G+2)}{4}$	$(G-1)$
Normalized Voltage Stress on the D_o (V_{Do}/V_{in})	G	$\frac{G}{D}$	$\frac{(G+3)}{3}$	G	$(G+1)$	$\frac{(G+2)}{4}$	$(G-1)$
F_s (KHz)	50	60	33	100	20	100	5
Open/Closed Loop	Open-loop	Open-loop	Open-loop	Open-loop	Open/Closed-loop	Open/Closed-loop	Open/Closed-loop
Control Method	n/a	n/a	n/a	n/a	PI Controller	Type III voltage controller	PI Controller
Exp. Efficiency (%) P_{out} = 100 W	n/a	n/a	93	92	95.6	92.1	96
Type of Load	Grounded	Grounded	Grounded	Grounded	Floating	Floating	Grounded
G at D = 0.4	3.67	1.11	2	3.33	5	4.67	4.67

The table below also shows the relationships between the duty ratio (D) and voltage gain (G), normalized voltage stress on the SW (V_{SW}/V_{in}), normalized voltage stress on the D_o (V_{Do}/V_{in}), F_s (KHz), open/closed loop, control method, experimental efficiency at 100 W, and G at D = 0.4 for the proposed and other converter topologies. It can be seen that the voltage gain (G) at D = 0.4 gives a higher gain compared to previous works and is identical to that of the converter in [30]. However, the converter in [30] has a larger number of components compared to the proposed converter.

To provide deeper insight into, and analysis of, the proposed converter and previous converter works, Figures 18–25 show plots based on the data in Table 2. In Figure 18, the voltage gain (G) under duty ratio changes (D) for the proposed converter and the prior converter topologies are plotted. As obvious, the proposed converter boasts a higher voltage gain compared to previous boosting converters for $D \leq 0.4$. Additionally, the proposed converter demonstrates superior voltage gain even at very low duty cycles. This indicates that the suggested boost converter experiences lower switching and conduction losses, resulting in higher efficiency.

Figure 19 shows the normalized voltage stress on the SW (V_{SW}/V_{in}) versus the voltage gain. It is observed that the SW in the proposed converter experiences good voltage stress at high voltage gain compared to the power switches in previous converters. It can be seen that the previous converter topologies with low voltage stress have a large number of components, as in [25,27,29,30]. Additionally, the proposed converter topology has a reasonable voltage stress compared to the converters in [26,28], which have nearly the same number of components. In Figure 20, the voltage stress on the diode in the proposed converter has a moderate value compared to the diodes in the previous converters. This comparison proves the improved performance of the proposed converter and stress reduction.

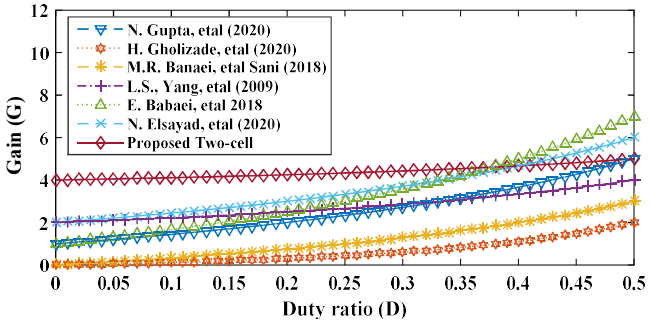


Figure 18. Voltage gain versus duty ratio.

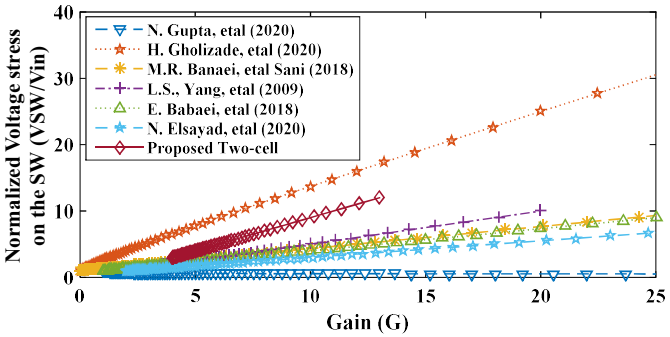


Figure 19. Normalized voltage stress on the *SW* (V_{SW}/V_{in}) versus gain.

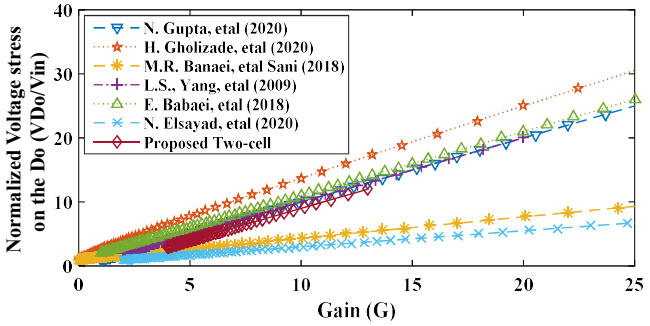


Figure 20. Normalized voltage stress on the D_o (V_{Do}/V_{in}) versus gain.

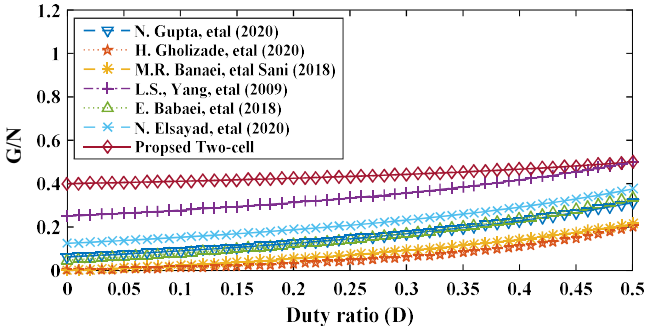


Figure 21. Gain to total component count ratio (G/N) versus duty cycle.

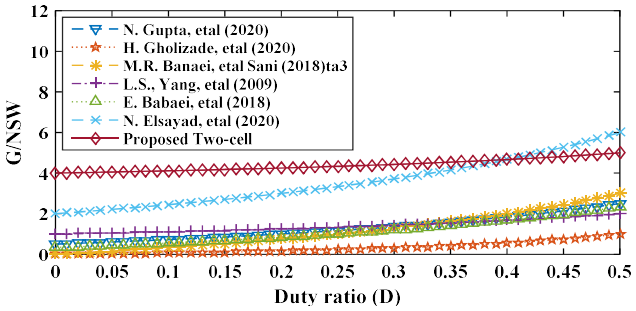


Figure 22. Gain to switch count ratio (G/N_{SW}) versus duty cycle.

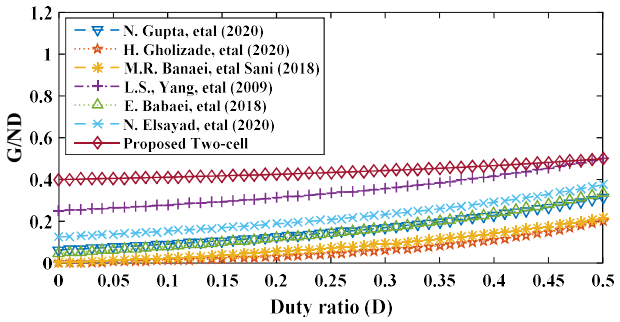


Figure 23. Gain to diode count ratio (G/N_D) versus duty cycle.

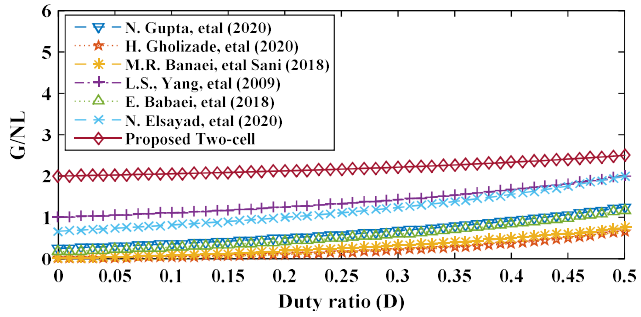


Figure 24. Gain to inductor count ratio (G/N_L) versus duty cycle.

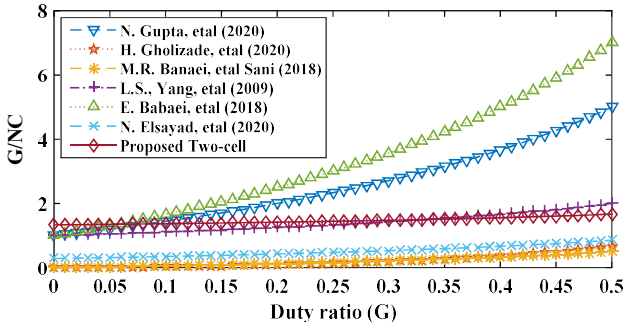


Figure 25. Gain to capacitor count ratio (G/N_C) versus duty cycle.

In Figures 21–25, the duty ratio is plotted versus gain to total component count ratio (G/N), gain to switch count ratio (G/N_{SW}), gain to diode count ratio (G/N_D), gain to diode count ratio (G/N_D), gain to inductor count ratio (G/N_L), and gain to capacitor count ratio (G/N_C) for the proposed converter and the prior converter works. As is obvious, the proposed converter exhibits higher gain compared to previous converters concerning the number of components. The proposed converter shows a higher gain compared to previous converter works, particularly for $D \leq 0.5$.

Therefore, the proposed converter is appropriate for renewable energy applications that require variable and constant high output voltage with a wider range of duty ratios. This converter topology structure contributes to a cost-effective system that is compact and lightweight compared with other topologies. It compromises between the required performance, the low number of components, low voltage stress on the components, high efficiency, and cost-effectiveness.

10. Conclusions

This paper presented the state space average model of a new single-switch multicell high-gain boost DC-DC converter considering the series parasitic resistances of the passive elements operating in CCM. Based on the state space average model, a small signal model of the proposed converter was introduced. The control-to-input and input-to-output open-loop transfer functions of the offered converter have been derived and presented. The behavior of the proposed topology based on the state space average model was obtained using Matlab R2023b software. The stability analysis of the suggested topology using a bode plot and root locus diagrams was investigated. The PI controller parameters for closed-loop control of the proposed converter were designed. Simulation results of the converter state space average model have been verified by comparing with the corresponding experimental results for actual hardware of the proposed converter with two cells for open-loop and closed-loop operations. It was found that the derived state space average and small signal models of the proposed multicell boost converter are convenient and accurate. These developed models can be considered as effective tools for studying dynamic performance, investigating stability, and designing control of the proposed converter. Based on the experimental results, the proposed converter has a fast dynamic response during starting, load change, input voltage, and reference voltage variations. A comprehensive comparison between the proposed converter and previous converters found that the proposed converter exhibits higher gain compared to previous converters with respect to the number of components. This converter's topology contributes to a cost-effective system that is compact and lightweight compared with other topologies. It compromises between the required performance, the low number of components, low voltage stress on the components, and cost-effectiveness.

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