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Variable-Frequency Control for Totem-Pole Bridgeless Power Factor Correction Converter to Achieve Zero-Voltage Switching Without Zero-Crossing Detection Circuits

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Abstract: The totem-pole bridgeless power factor correction (PFC) converter, known for its advantages including simple topology, capability for zero-voltage switching (ZVS), and low common mode interference, presents an opportunity to enhance the efficiency and environmental friendliness of power systems. However, these converters have issues such as ZVS, requiring zero-crossing detection (ZCD) under circuits' critical continuous mode (CRM) or additional auxiliary resonant circuits, resulting in increased circuit costs and control complexity. Therefore, this paper proposes a variable switching frequency digital control method to achieve ZVS under a wide operating range without ZCD circuits. At the same time, under the premise of ZVS, an interleaved parallel scheme is adopted to further minimize the current ripple and enhance the quality of the current waveform. Finally, an experimental 2 kW two-phase interleaved totem-pole bridgeless PFC converter prototype is designed to verify that the proposed method is correct and effective. The experimental prototype can reach an efficiency of 97.78%.

Keywords: critical continuous mode; totem pole; variable switching frequency; zero-voltage switching

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1. Introduction

A high power factor (PF) and low total harmonic distortion (THD) can save energy and reduce interference with other electronic devices [1–3]. Consequently, power factor correction (PFC) converters are beneficial in power supplies to meet the required power quality standards [4,5]. Figure 1 shows the topology of the bridge boost PFC [6,7], where the rectifier bridge shapes the input voltage into a forward full wave while passing through a classic boost converter to obtain the DC voltage. To achieve power factor correction, sinusoidal pulse width modulation (PWM) is used to synchronize the inductance current with the input voltage. Regardless of whether the power transistor is turned on or off, the current will flow through two slow recovery diodes, so the conduction loss of the bridge PFC is higher, especially at low-voltage input applications [8–10].

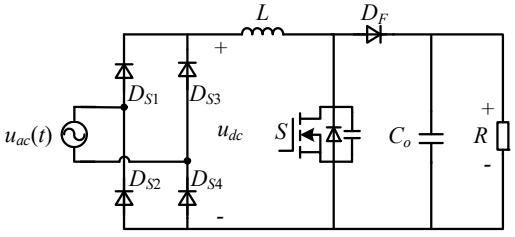


Figure 1. The traditional bridge boost PFC AC-DC topology [6,7].

A great deal of research has been conducted on various bridgeless PFC converters to reduce the conduction losses of bridge diodes [11,12]. The totem-pole bridgeless PFC has a

simple structure [13], as shown in Figure 2. It has the advantages of low common mode interference, low conduction loss, and the ability to achieve zero-voltage switching (ZVS) of switches in critical continuous mode (CRM). Therefore, it has been widely applied in power supplies, energy storage systems, telecom infrastructure, electric vehicle battery chargers, etc. [14,15]. Meanwhile, with the development and application of wide-bandgap devices, the totem-pole bridgeless PFC has received significant attention due to the possibility of achieving ZVS for switches operated at high switching frequencies.

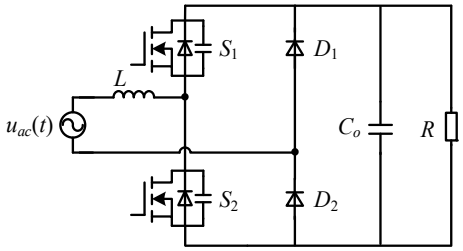


Figure 2. The totem-pole bridgeless PFC AC-DC topology [6].

To further reduce the conduction loss of the totem-pole bridgeless PFC converter, the two diodes in Figure 2 can be replaced with active switches, as shown in Figure 3. Meanwhile, by adopting proper PWM logic, it can also achieve bidirectional power transfer, which is a solution suited to applications that require battery charging/discharging.

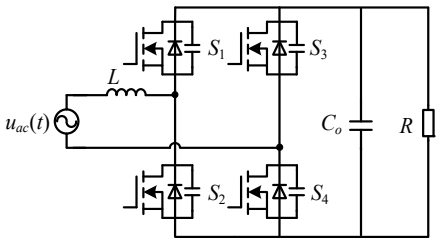


Figure 3. The modified totem-pole bridgeless PFC AC-DC topology [6].

As shown in Figure 3, the totem-pole bridgeless PFC converters feature a simple structure, low component counts, and bidirectional power flow capability, attracting widespread attention [15]. With the development of switches, especially wide-bandgap switches, increasing the switching frequency can help to increase the power density of the system and reduce the size of passive components. However, increasing the switching frequency can lead to dominant switching loss due to the influence of various parasitic parameters of the switches. Likewise, research has been conducted on achieving soft switching in totem-pole bridgeless PFC circuits. The application of this technology can reduce the switching loss generated by the switches during high-frequency operation [16]. It is common to achieve ZVS by operating in CRM [16–19] or by adding additional auxiliary circuits [20–23]. Compared to adding auxiliary circuits, operating in CRM requires less auxiliary hardware and does not modify the main electrical circuit. In the CRM operation of totem-pole boost converters, zero-current detection (ZCD) circuits are typically incorporated to detect inductor current zero crossings and minimize switching loss [16–19]. In [16], optimal switching frequency variation range control is employed to optimize the switching frequency range, where the generation of the ZCD signal involves comparing the current sensing signal with a zero reference point. In [17], auxiliary winding is added to assist in obtaining a ZCD signal, and a simple analog-based accurate variable on-time control is proposed to achieve full-load ZVS and power factor correction. In [18], the body diode conduction of the active switch is detected to adjust the synchronous rectification turn-off time to achieve ZVS with minimum turn-on current and reduce the circulating current. However, several challenges arise for these methods relying on ZCD circuits, particularly at high switch frequencies. These include the inaccurate detection of zero-crossing points due to susceptibility to noise

from high dv/dt and di/dt operations and the need for additional detecting circuits and PWM logic generation units [18,19].

On the other hand, auxiliary circuits can be added to achieve ZVS without using ZCD circuits. The authors in [20] propose the use of surge-current-limiting circuits to achieve soft switching of a totem-pole bridgeless PFC converter. Additionally, the authors in [21] combine interleaved totem-pole bridgeless PFC with a post-stage dual-active-bridge converter to form a single-stage structure, achieving partial ZVS. In [22], another switch bridge leg and an auxiliary inductor are used in a totem-pole bridgeless PFC rectifier to achieve ZVS of the main switches. In [23], an auxiliary soft-switching cell composed of two inductors, a capacitor, and an FET is added to achieve ZVS. Nevertheless, for these approaches without ZCD circuits, an additional circuit is added to the main circuit, which can increase the converter components and even complicate the working modes, thereby increasing the control complexity.

Consequently, aiming at ZVS over a wide range without the need for ZCD circuits or other additional components, this paper introduces a digital control strategy with variable-frequency control. This strategy incorporates an additional conduction time compensation mechanism that, by dynamically adjusting the switching frequency, allows the current to build up sufficiently before the corresponding switch is turned on. This effectively discharges the switch junction capacitor and allows ZVS to be implemented. This approach not only eliminates the complexity of ZCD circuits but also enhances the performance and reliability of the converter. In addition, the proposed control strategy is adopted in a two-phase interleaved parallel structure to further reduce the current ripple.

This paper is organized as follows: In Section 2, the ZVS models are analyzed with the consideration of switch junction capacitors. The derivation of the conditions and range are of ZVS given in detail. The variable-frequency control method without ZCD circuits and the increased conduction time are analyzed in Section 3. Subsequently, the totem-pole bridgeless PFC converter with two-phase interleaved connections with the proposed control method is analyzed in Section 4. Section 5 presents the experimental results from a 2000 W prototype that verifies the theoretical analysis and proposed modulation schemes. Finally, Section 6 presents the conclusion.

2. ZVS Analysis Considering Switch Junction Capacitors

Achieving ZVS not only reduces switching loss but also EMI noise. This section establishes ZVS models considering switch junction capacitances, derives the necessary ZVS conditions, and defines the ZVS range. This fundamental analysis is employed for the development of a control method to achieve efficient ZVS.

2.1. ZVS Model Analysis with Junction Capacitors

The diodes in the totem-pole bridgeless PFC, as illustrated in Figure 2, are replaced with two Si MOSFETs (S_3 and S_4), as shown in Figure 4. Combined with corresponding PWM logic, the converter operates in CRM to achieve soft switching. To further reduce switching losses at high frequency, SiC MOSFETs can be used for S_1 and S_2.

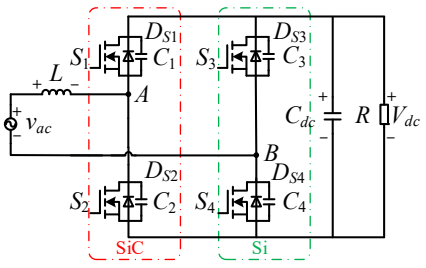


Figure 4. SiC totem-pole soft-switching bridgeless PFC AC-DC topology.

Due to the similar working mode of the SiC totem-pole bridgeless PFC converter in the positive and negative half cycles of AC voltage input, the analysis conducted here is

based only on the input voltage in the positive half cycle. The main waveforms of the totem-pole bridgeless PFC rectifier operating in CRM are shown in Figure 5 and can be divided into six stages. v_{gs1} and v_{gs2} are the drive signals of S_2 and S_1, respectively. v_{S2} is the drain–source voltage of S_2. i_{S1} and i_{S2} are the currents of S_1 and S_2, respectively. During the positive half cycle, S_4 stays on, S_3 stays off, and S_2 and S_1 are the main switches operating with high switching frequency.

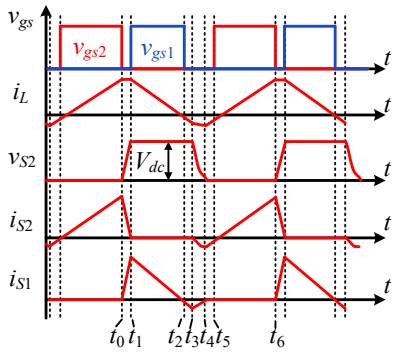


Figure 5. Main waveform operating in CRM.

Stage 1 [t_0–t_1] is shown in Figure 6a. At t_0, S_2 is turned off, and the inductor current i_L charges the junction capacitor C_2 of S_2 while discharging the junction capacitor C_1 of S_1. The duration of stage l is relatively short since i_L is at its peak at t_0 and thus the charging process will be over in a short time. At t_1, S_1 is turned on. After this stage, the current that previously flowed through S_2 continues to flow through S_1. The voltage v_{c2} of C_2 can be expressed as

$$v_{c2}(t) = i_L(t_0)t/(2C_{oss}) \tag{1}$$

where C_{oss} is the junction capacitor of S_1 and S_2, with $C_{oss} = C_1 = C_2$.

Stage 2 [t_1–t_2] is shown in Figure 6b. In this stage, at t_1, the voltage v_{ds2} of S_2 increases to the bus voltage V_{dc}. Meanwhile, the voltage v_{ds1} of S_1 decreases to 0, and the diode D_{S1} of S_1 conducts. S_1 achieves ZVS, and the voltage of L is equal to $V_{dc} - v_{ac}(t)$. The inductor current i_L linearly decreases, and i_L decreases to 0 at t_2. In this stage, the inductor current i_L can be expressed as

$$i_L(t) = i_L(t_1) - (V_{dc} - v_{ac}(t))t/L \tag{2}$$

Stage 3 [t_2–t_3] is shown in Figure 6c. At t_2, S_1 is turned off, and the diode D_{S1} of S_1 continues to conduct due to reverse recovery. Moreover, i_L is reversed and continues to decrease, and can be expressed as

$$i_L(t) = -(V_{dc} - v_{ac}(t))t/L \tag{3}$$

Stage 4 [t_3–t_4] is shown in Figure 6d. At t_3, the diode D_{S1} of S_1 is cut off, and C_1, C_2, and L begin to resonate. The voltage v_{ds2} of S_2 begins to decrease, and the drain–source voltage v_{ds1} of S_1 begins to rise. v_{ds2} decreases to the minimum value at t_4, and this stage ends. During this stage, the relationship can be shown as

$$i_L(t) = -(V_{dc} - v_{ac}(t))\sin\omega_0 t/Z + i_L(t_3)\cos\omega_0 t \tag{4}$$

And the drain–source voltage of S_2 can be expressed as

$$v_{ds2}(t) = v_{ac}(t) + (V_{dc} - v_{ac}(t))\cos\omega_0 t + i_L(t_3)Z\sin\omega_0 t \tag{5}$$

Here, $Z = \sqrt{L/2C_{oss}}$, $\omega_0 = 1/\sqrt{2C_{oss}L}$.

Stage 5 [t_4–t_5] is shown in Figure 6e. At $t = t_4$, the drain–source voltage of S_2 decreases to zero, and the diode D_{S2} of S_2 conducts. During this stage, i_L rises from a negative state to 0, which can be expressed as

$$i_L(t) = -i_L(t_4) + v_{ac}(t)t/L \tag{6}$$

Stage 6 [t_5–t_6] is shown in Figure 6f. At t_5, S_2 is turned on by the gate drive signal. If V_{ds2} is zero, the turn-on of ZVS will be achieved. Subsequently, i_L increases linearly until $t = t_6$, and S_2 turns off and repeatedly enters the next cycle. The expression for i_L is

$$i_L(t) = v_{ac}(t)(t - t_5)/L \tag{7}$$

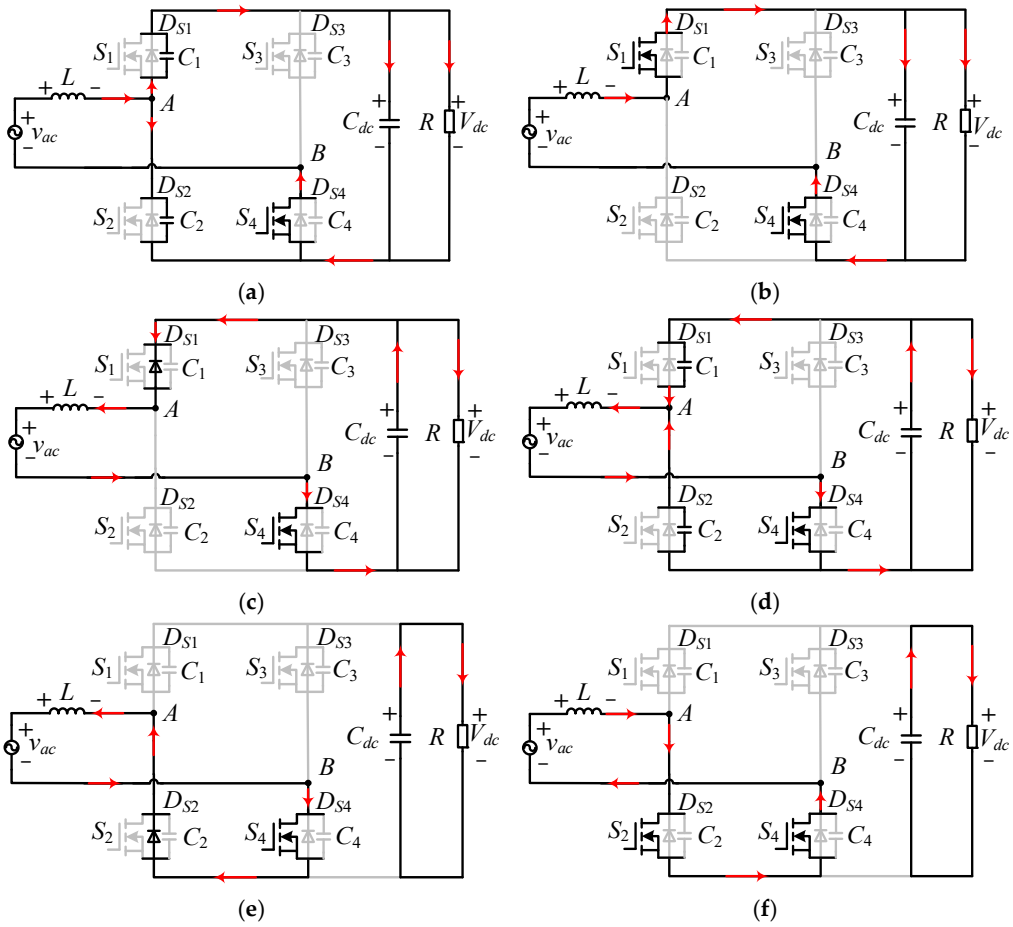


Figure 6. Operating stages in the positive half cycle. (**a**) Stage 1 [t_0–t_1]. (**b**) Stage 2 [t_1–t_2]. (**c**) Stage 3 [t_2–t_3]. (**d**) Stage 4 [t_3–t_4]. (**e**) Stage 5 [t_4–t_5]. (**f**) Stage 6 [t_5–t_6].

2.2. ZVS Condition and Region

In stage 4, the totem-pole bridgeless PFC achieves turn-on of the ZVS or valley through the resonance between the inductor current and the junction capacitor of the high-frequency switch. In the traditional CRM, from (5), if $I_L(t_3) = 0$, the valley value of the voltage v_{c2} of C_2 is deduced as $v_{c2} = 2v_{ac}(t) - V_{dc}$ and the voltage v_{c1} of C_1 is $v_{c1} = v_{dc} - v_{c2}(t) = 2v_{dc} - 2v_{ac}(t)$. Therefore, the condition for achieving ZVS in S_2 is

$$v_{c2}(t) = 2v_{ac}(t) - V_{dc} \leq 0 \Rightarrow v_{ac}(t) \leq V_{dc}/2 \tag{8}$$

Thus, when the input voltage $v_{ac} \leq v_{dc}/2$ during its positive half cycle, S_2 can achieve ZVS turn-on. However, it cannot when $v_{ac} > v_{dc}/2$. Under this condition, C_2 needs to be

discharged with an additional charge current or energy. The additional charge Q_e needs to meet the following:

$$Q_e \geq C_{s2}(2v_{ac}(t) - V_{dc}) + C_{s1}(V_{dc} - (2V_{dc} - 2v_{ac}(t))) = 2C_{oss}(2v_{ac}(t) - V_{dc}) \quad (9)$$

After normalization, Q_e^* can be obtained:

$$Q_e^* \triangleq Q_e/(2C_{oss}V_o) \geq 2v_{in}(t)/V_o - 1 = 2k - 1 \quad (10)$$

where $k = v_{ac}(t)/V_{dc}$ and Q_e^* is proportional to k.

Equations (9) and (10) yield the ZVS region, which is also shown in Figure 7, illustrating the Q_e^* charge required to achieve ZVS across different instant input voltages, where k is the voltage conversion gain. The graph reveals two regions: the "A-Natural ZVS" region, where ZVS can be achieved without extra charge energy under the case $k \leq 0.5$, and the "B-ZVS Expansion" region, denoting ZVS performance under $k > 0.5$. Notably, for $k > 0.5$, the inductor current must cross zero to provide an extra charge Q_e* to achieve ZVS. Consequently, in CRM, the charge energy becomes ineffective under $k > 0.5$ when the inductor current stays at zero, resulting in the absence of soft switching, as observed in traditional CRM.

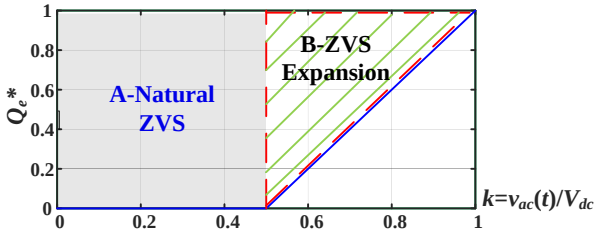


Figure 7. The ZVS region of the totem-pole bridgeless PFC converter.

In real applications, Q_e^* can be generated by adding extended conduction time for the active power switches. However, this extension must be implemented after the zero-crossing point of the inductor current. In conventional control strategies dependent on ZCD, it is insufficient to merely detect the zero-crossing point. The system needs to compensate for the delay and guarantee adequate negative current for the achievement of ZVS. This requires complex calculations and compensations based on the power conditions and the precise timing of the zero-crossing event.

3. Variable-Frequency Control without ZCD Circuits to Achieve ZVS Considering Switch Junction Capacitors

In this section, an eliminating ZCD circuit control method with variable frequency is proposed to achieve the full-range ZVS of totem-pole bridgeless PFC. The circuit model is established with consideration of the switch junction capacitors. Based on this model, the minimum charging current of the inductor is derived, and thus, the additional compensated turn-on time for the switches is obtained. Further, the control to extend the turn-on time is combined with the variable-frequency control in the DSP implementation.

3.1. Conventional Method with ZCD and the Concept Diagram without ZCD

The conventional methods for achieving ZVS typically rely on ZCD circuits, as exemplified in [24]. The corresponding control block diagram is illustrated in Figure 8. As shown, a double loop control is adopted to generate the peak current reference for the hysteresis comparator to compare with the inductor current i_L to control the peak value of the inductor. Meanwhile, a ZCD unit is adopted to control the valley point of i_L. It should be noted that the energy is not sufficienct to discharge the junction capacitor of the switches if the turn-off current is strictly equal to zero, as discussed in Section 2.2. Thus, an adaptive SR time controller is needed to slightly adjust the turn-off time instant. This involves

intricate calculations and compensations based on the power conditions and the precise timing of the zero-crossing event. Consequently, the control strategies with ZCD circuits still involve complexity, especially at high switching frequencies utilizing SiC MOSFETs, where accurate timing is critical and delay or noises can affect performance.

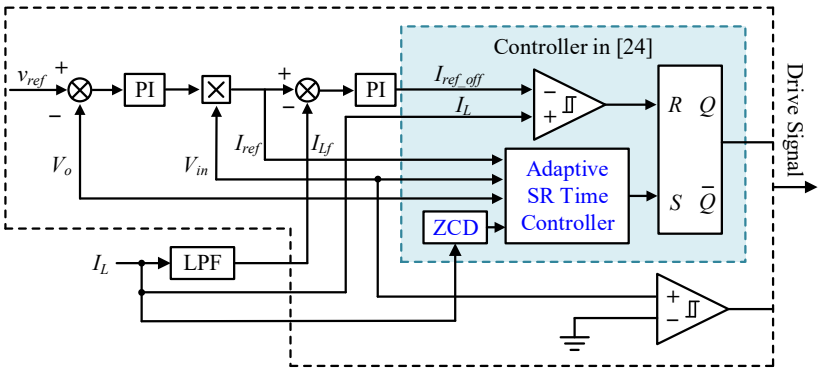


Figure 8. Control diagram of the control method relaying on ZCD circuits in [24].

Actually, to achieve ZVS for the switches of totem-pole bridgeless PFC converters, the key concept is to ensure that the switch turn-off current stays near zero (the energy is not sufficient to discharge the junction capacitor of the switches if the turn-off current is strictly equal to zero). Essentially, the inductor current value is related to the switching frequency, duty cycle, input voltage, output voltage, etc. So, the desired switch turn-off instant current can be controlled by controlling the switching frequency. Consequently, a concept diagram of the proposed control is shown in Figure 9. As can be seen, a variable frequency control unit is adopted rather than using a ZCD and adaptive SR time controller in Figure 8. Similar to conventional digital control of PFC, the voltage and current loops generate the signal for the PWM unit, and the modulation frequency is controlled through a variable frequency unit (the detailed derivation for the variable frequency will be analyzed in Section 3.2). This direct variable frequency control can respond more precisely, avoiding the possible delay and complexity brought by the ZCD circuit.

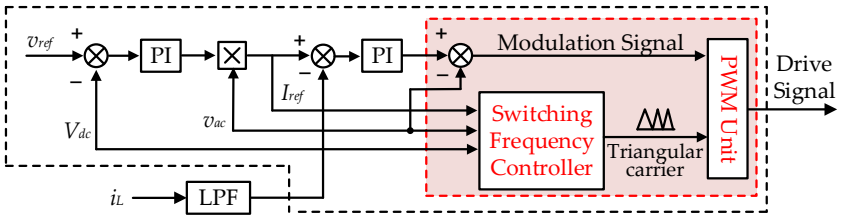


Figure 9. Control diagram of the proposed digital control method without the need for ZCD.

3.2. Working Principal Analysis and Variable Frequency Derivation without ZCD to Achieve ZVS

As in a previous discussion, the variable frequency unit is the key controller for the proposed concept. Thus, based on the working principal analysis, illustrating the relationship between the switch turn-off current and the switching frequency and then deriving the frequency control law to achieve ZVS are important. It is also important to investigate how real-time adjustments to the switching frequency function and ensure ZVS without relying on ZCD for zero-crossing detection.

Figure 10 illustrates the operational waveforms of the converter in CRM during the positive half cycle of the AC voltage. During the period in which S_2 is turned on and S_1 is turned off, the voltage across the inductor L is fixed, causing a linear rise in i_L. Concurrently, the input voltage $v_{ac}(t)$ during this interval is expressed as

$$v_{ac}(t) = V_m \sin(\omega t) = L i_{pk}(t) / T_{on}(t) \tag{11}$$

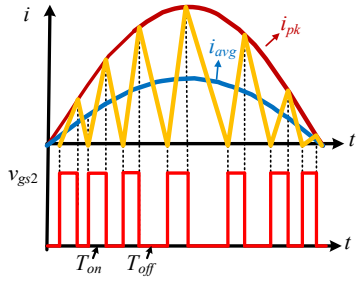


Figure 10. Operating waveform in CRM during the positive half cycle.

Here, for S_1, T_{on} is the turn-on time. Subsequently, i_L linearly decreases when S_1 is turned on, and $v_{ac}(t)$ is calculated as

$$v_{ac}(t) = V_m \sin(\omega t) = -Li_{pk}(t)/T_{off}(t) + V_{dc} \tag{12}$$

Here, T_{off} denotes the turn-off time.

With CRM, the envelope of the peak value of $i_L(t)$ is denoted as $i_{pk}(t) = 2i_{avg}(t)$. Moreover, throughout a half cycle, $i_{avg}(t)$ equals the AC current. Therefore, the expression for the peak value of $i_L(t)$ is obtained as

$$i_{pk}(t) = 2I_m \sin(\omega t) \tag{13}$$

Furthermore, the T_{on} and T_{off} of the SiC switches can be determined by applying the volt-second area balance principle of the inductor.

$$T_{on}(t) = Li_{pk}(t)/v_{ac}(t) = 2Li_{avg}(t)/v_{ac}(t) \tag{14}$$

$$T_{off}(t) = Li_{pk}(t)/(V_{dc} - v_{ac}(t)) = 2Li_{avg}(t)/(V_{dc} - v_{ac}(t)) \tag{15}$$

Combining (13)–(15), the frequency condition to achieve CRM operation can be derived.

$$f_s(t) = 1/(T_{on}(t) + T_{off}(t)) = v_{ac}(t)(V_{dc} - v_{ac}(t))/(2Li_{avg}(t)V_{dc}) \tag{16}$$

Equation (16) represents the frequency expression in CRM. In digital control, the frequency can be used to update the cycle count value in DSP. Based on (16), the variation trend of f_s within half a cycle is plotted as an example case in Figure 11. As shown, f_s is the lowest at $\pi/2$, which is the peak/valley value of the input sine voltage. When $v_{ac}(t)$ approaches zero, the switching frequency is the highest.

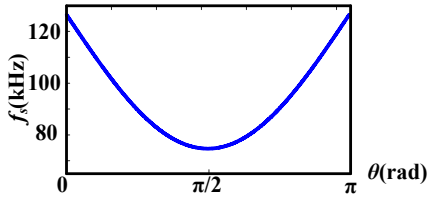


Figure 11. The switching frequency trend during half a cycle of a period.

The previous analysis in Section 2.2 shows that in the CRM operation, the totem-pole bridgeless PFC can only naturally achieve ZVS when the input AC voltage is less than half of the output DC voltage.

Figure 12 illustrates the waveform when adding the additional conduction time within the descending phase of the inductor current, where $t_e = t_3 - t_2$ represents the additional conduction time. Because the two stages of [t_0–t_1] and [t_1–t_2] are the same as the traditional CRM control, which has been analyzed in Section 2.1, they will not be discussed here. Compared to the mode analysis in Section 2.1, an additional mode has been added, which

is the additional conduction mode from t_2 to t_3, as shown in Figure 13. The specific analysis for modes from t_2–t_6 is discussed as follows.

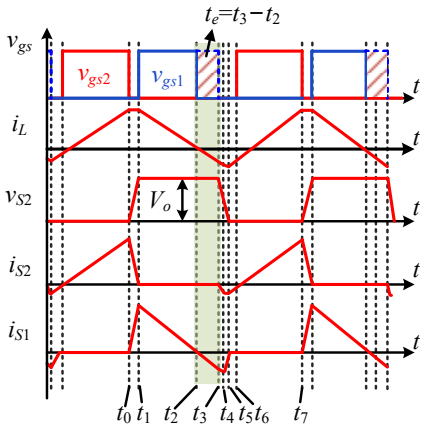


Figure 12. Waveform of the additional conduction time (positive half cycle).

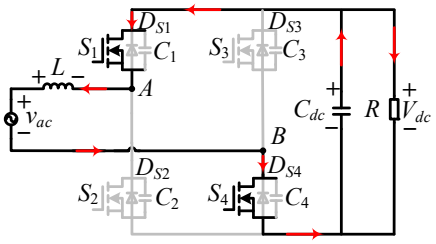


Figure 13. The equivalent circuit of the additional conduction time from t_2 to t_3.

Stage 1 [t_2–t_3]: At t_2, the inductor current i_L crosses 0, and the driving signal for S_1 continues to conduct instead of turning off, causing i_L to reverse and continue to decrease. The expression of i_L in this mode is the same as (3). At t_3, i_L decreases to the bias current (or valley point) $i_L$zvs to provide energy to charge the switch junction capacitors. The bias current is used to charge and discharge the junction capacitor of the high-frequency switches, which can be expressed as

$$i_{Lzvs}(t) = -(V_{dc} - v_{ac}(t))(t_3 - t_2)/L \tag{17}$$

Stage 2 [t_3–t_4]: At t_3, S_1 is turned off, and the body diode of S_1 undergoes reverse recovery. i_L continues to decrease in reverse, and the duration of this stage is very short.

Stage 3 [t_4–t_5]: At t_4, the body diode of S_1 is cut off, and L, C_1, and C_2 begin to oscillate. At t_5, the voltage of S_2 drops to 0.

Stage 4 [t_5–t_6]: During this mode, the body diode of S_2 is on, and L is charged through S_2. When $t = t_5$, i_L is reversed. At this stage, the drain–source voltage of S_2 continues to be 0, which means S_2 can achieve ZVS.

Based on the above analysis, the additional conduction time of S_3 and S_4 can be controlled to reverse the charge and store energy for the inductor current, which can be used for the energy charging of the junction capacitor of the switches in the high-frequency bridge arm to achieve ZVS. The analysis of the negative bias current required for the inductor current to achieve ZVS is as follows:

In the resonance stage of inductor L and capacitors C_1 and C_2 (refer to Figure 6 d for the circuit stage), the following formula can be obtained based on the relationship between capacitor current and inductor voltage:

$$C_1 \frac{dv_{c1}}{dt} = i_L + C_2 \frac{dv_{c2}}{dt} \tag{18}$$

$$L\frac{di_L}{dt} + v_{ac} - V_{dc} + v_{c1} = 0 \tag{19}$$

$$v_{c1} = V_{dc} - v_{c2} \tag{20}$$

Taking $C_1 = C_2 = C_{oss}$ and substituting (20) into (18), the following is deduced:

$$C_{oss}\frac{dv_{c1}}{dt} = i_L + C_{oss}\frac{d(V_{dc} - v_{c1})}{dt} = i_L - C_{oss}\frac{dv_{c1}}{dt} \Rightarrow 2C_{oss}\frac{dv_{c1}}{dt} = i_L \tag{21}$$

Based on (1) and (21), the equivalent circuit displayed in Figure 14 can be illustrated.

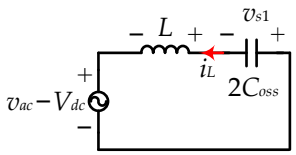


Figure 14. Equivalent circuit.

From the above equivalent circuit, based on energy conservation, (22) can be obtained, where i_{Lzvs} is the bias current to achieve the turn-on of ZVS in the main switch.

$$0.5Li_{Lzvs}^2 \geq \int (v_{ac} - V_{dc})i_L dt + 0.5 \cdot 2C_1 v_{c1}^2 \tag{22}$$

Substituting (21) into (22) yields the i_{Lzvs} conditions that need to be met to achieve the main switch ZVS.

$$i_{Lzvs}(t) \geq \sqrt{2[2C_{oss}V_{dc}(v_{ac}(t) - V)(v_{ac}(t) - V_{dc})]/L + C_{oss}V_{dc}^2} \tag{23}$$

Therefore, by substituting the relevant circuit parameters into (23), the bias current required for the main switch to achieve ZVS can be plotted as an example to show the inductor current required to achieve ZVS under different instant input voltages, as shown in Figure 15. As shown, when the grid voltage is relatively low, ZVS can be achieved without the need for additional negative current. When the grid voltage is higher, the switches need an additional negative bias current to achieve ZVS.

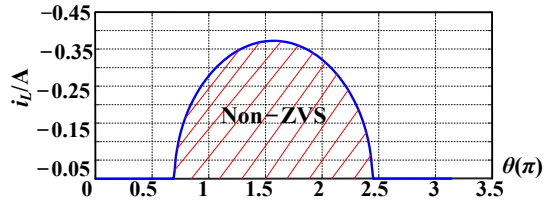


Figure 15. Inductor current required to achieve ZVS.

Consequently, through substitution of the required inductor current into (16), the frequency condition to achieve full-working-range ZVS can be calculated as

$$f_{s_full}(t) = v_{ac}(t)(V_{dc} - v_{ac}(t))/[2L(i_{avg}(t) + i_{Lzvs}(t))V_{dc}] \tag{24}$$

4. Current Ripple Reduction and Digital Implementation of the Proposed Control Method

As previously mentioned, achieving ZVS in CRM reduces switching turn-on losses, but the peak-to-peak inductor current, nearly double the average current, can increase high-frequency ripple at the AC input. To mitigate this issue, the proposed control method can be applied to a totem-pole bridgeless PFC converter with two-phase interleaved connections [25]. This section provides current ripple models to demonstrate the effectiveness

of the interleaved structure and analyzes how the proposed control method is implemented in this configuration.

4.1. Current Ripple Reduction with Two-Phase Interleaving for Totem-Pole Bridgeless PFC Converter

Two-phase interleaving refers to adding a set of high-frequency bridge arms and inductors to the original single-phase totem-pole bridgeless PFC topology and multiplexing the power frequency bridge arms for parallel connection. It is worth noting that each phase in an interleaved structure can be regarded as operating independently. The interleaving structure does not alter the fundamental working principle of each phase. The topology is shown in Figure 16. High-frequency switches S_1 and S_2 and inductor L_1 form the main phase; high-frequency switches S_5 and S_6 and inductor L_2 form the secondary phase; and S_3 and S_4 are multiplexed as the main and secondary phases.

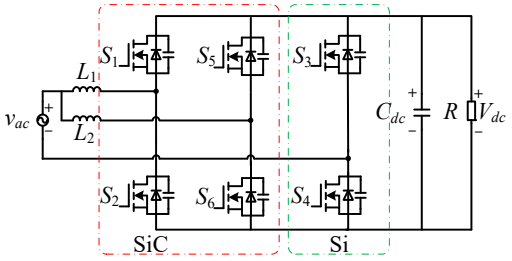


Figure 16. A schematic of the two-phase interleaved totem-pole bridgeless PFC converter.

4.2. Analysis of Current Ripple Reduction with Two-Phase Interleaving

The duty cycles d of the two main switches S_2 and S_6 are the same, while the driving phase for them is 180° phase-shifted, causing the inductor current of the main and secondary phases to differ in phase by 180°. The synchronous rectifiers S_1 and S_5 complement the main switches S_2 and S_6 in conduction. Due to the on-and-off states of S_2 and S_6, the converter consists of four different stages based on the analysis of the input voltage during the positive half cycle. When the interleaved converter operates in CRM, they have different current waveforms at duty cycles $d \leq 0.5$ and $d > 0.5$. Figure 17a shows the main waveform of the inductor current with $d \leq 0.5$, and Figure 17b shows the main waveform of the inductor current with $d > 0.5$. The following is an analysis of the current ripple under these two cases.

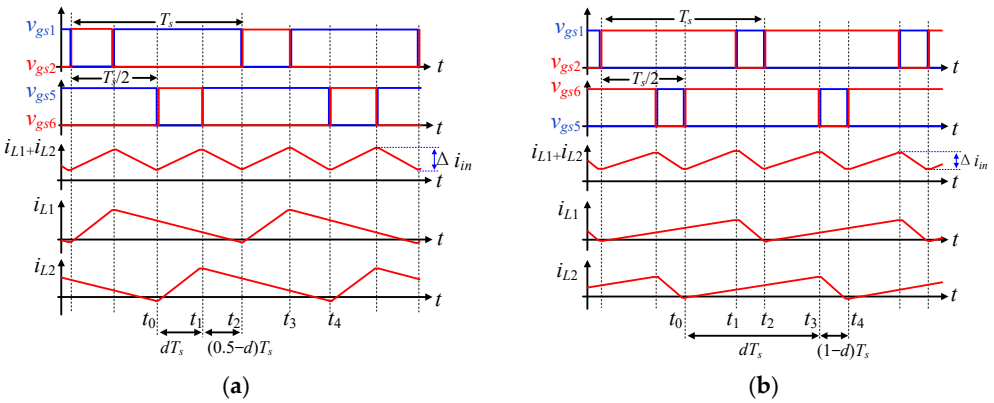


Figure 17. Two current waveforms of the two-phase interleaved totem-pole bridgeless PFC in CRM. (**a**) $d \leq 0.5$. (**b**) $d > 0.5$.

(1) $d \leq 0.5$

From Figure 17a, the inductor currents i_{L1} and i_{L2} of the two phases both linearly decrease in the [t_1–t_2] and [t_3–t_4] stages, indicating that the above converter operates in Mode 4. Based on the equivalent circuit of Mode 4, it can be concluded that

$$\begin{cases} L_1 \Delta i_{L1}/\Delta t = V_{dc} - v_{ac} \\ L_2 \Delta i_{L2}/\Delta t = V_{dc} - v_{ac} \end{cases} \tag{25}$$

At steady state, the expression for the duty cycle d is

$$d(t) = 1 - |v_{ac}(t)|/V_{dc} \tag{26}$$

Assuming that the two inductors are the same, there are

$$\begin{cases} L_1 = L_2 = L \\ \Delta t = (1/2 - d)T \\ \Delta i_{in} = \Delta i_{L1} + \Delta i_{L2} \end{cases} \tag{27}$$

Substituting (26) and (27) into (25), the total input current ripple can be obtained as

$$\Delta i_{in} = d(1 - 2d)v_{ac}/[(1 - d)Lf_s] \tag{28}$$

(2) $d > 0.5$

In the stages of [t_0–t_1] and [t_2–t_3], the inductor currents i_{L1} and i_{L2} of both phases increase linearly, corresponding to operating Mode 1 of the converter mentioned above. Therefore, according to the corresponding equivalent circuit, it can be obtained as

$$\begin{cases} L_1 \Delta i_{L1}/\Delta t = v_{ac} \\ L_2 \Delta i_{L2}/\Delta t = v_{ac} \end{cases} \tag{29}$$

Similarly, there are

$$\begin{cases} L_1 = L_2 = L \\ \Delta t = (d - 1/2)T \\ \Delta i_{in} = \Delta i_{L1} + \Delta i_{L2} \end{cases} \tag{30}$$

Substituting (26) and (30) into (29), the total input current ripple can be obtained as

$$\Delta i_{in} = (2d - 1)v_{ac}/(Lf_s) \tag{31}$$

Based on the volt–ampere relationship of the inductor current, it can be obtained by combining (28) and (31) that the input current ripple expression of the interleaved converter in CRM can be obtained as

$$\Delta i_{in} = \begin{cases} d(1 - 2d)v_{ac}/[(1 - d)Lf_s] & d < 0.5 \\ (2d - 1)v_{ac}/(Lf_s) & d \geq 0.5 \end{cases} \tag{32}$$

The ripple current of a single inductor is

$$L\Delta i_L/\Delta t = v_{ac} \Rightarrow \Delta i_L = v_{ac}\Delta t/L = dv_{ac}/(Lf_s) \tag{33}$$

The ratio of the total input current ripple to the current ripple of a single inductor is defined as $\alpha = \Delta I_{in}/\Delta I_L$. Substituting (32) into (33) yields

$$\alpha = \begin{cases} (1 - 2d)/(1 - d) & d < 0.5 \\ (2d - 1)/d & d \geq 0.5 \end{cases} \tag{34}$$

According to (34), the relationship between the current ripple ratio α and the duty cycle d is shown in Figure 18. According to Figure 18, the ripple current is always smaller than the single ripple current (ripple ratio $\alpha < 1$) after interleaving. And when d is around 0.5, the current ripple after interleaving is canceled. Therefore, adopting the interleaved parallel scheme has advantages in reducing the current ripple of the converter in CRM.

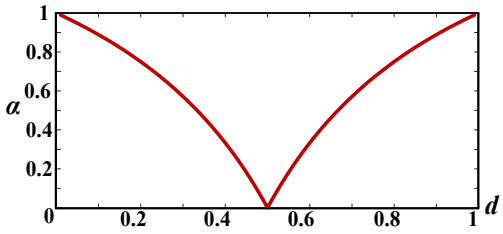


Figure 18. Relationship between current ripple ratio α and duty cycle d.

4.3. Digital Implementation of the Proposed Control Method for Two-Phase Interleaved Parallel Totem-Pole Bridgeless PFC

The control methods of interleaving are mainly divided into open-loop interleaving based on the ZCD circuit and closed-loop interleaving based on a phase-locked loop. Open-loop interleaved parallel connection divides each phase circuit into one main phase and multiple secondary phases, where the main phase circuit works independently like a single-phase PFC converter. It can work in current mode or voltage mode, and the driving signals of each secondary phase are obtained based on the driving signals of the main phase after a certain delay. It can be divided into four categories based on the working mode of the circuit and the synchronization time of each phase: voltage mode on-time synchronization, current mode on-time synchronization, current mode off-time synchronization, and voltage mode off-time synchronization. Closed-loop interleaving adjusts the turning-off time of the secondary phase based on phase error, thereby achieving an interleaving parallel connection. The above two methods require a ZCD circuit on both the primary and secondary phases, increasing the complexity of the circuit.

According to the previously discussed variable-frequency control method without the use of ZCD circuits, the proposed digital control strategy for a two-phase interleaved parallel totem-pole bridgeless PFC is illustrated in Figure 19. As illustrated, this integration enables the control method to achieve ZVS without the need for supplementary sensors, auxiliary circuits, or ZCD circuits, thereby enhancing noise immunity and ensuring precise control. The output voltage of the rectifier is sampled as the feedback of the output voltage loop, and the output of the voltage loop is multiplied with the grid phase to generate the reference of the inner current loop, in which the phase of the current is obtained through a digital PLL unit. The frequency calculation unit calculates the on-time frequency based on the equation shown in (24) and updates the timer in the DSP in each switching cycle. The duty cycle of each switch is calculated based on the output of the inner current loop with a feedforward of the AC voltage.

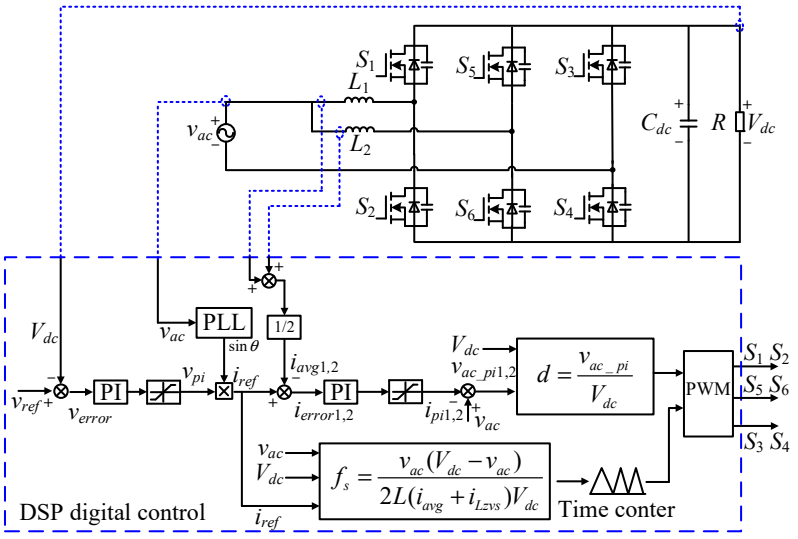


Figure 19. Control block diagram.

5. Experimental Verification

To validate the effectiveness of the proposed control method for the totem-pole bridgeless PFC converter, a 2000 W experimental prototype was designed for practical verification. The experimental prototype is shown in Figure 20. The main parameters of the experimental prototype are provided in Table 1.

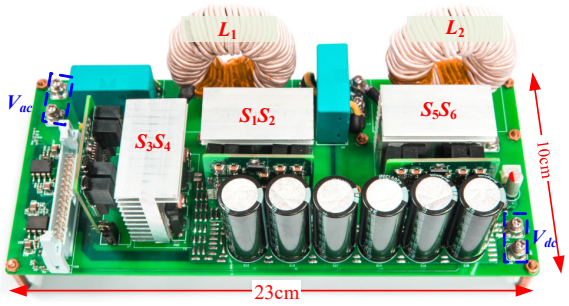


Figure 20. The 2000 W experimental prototype.

Table 1. Main parameters of the prototype.

Parameters	Value	Parameters	Value
AC voltage (v_{ac})	110 V, 50 Hz	DC bus capacitor (C_{dc})	2000 μF
DC voltage (V_{dc})	280 V–370 V	AC inductance (L_1, L_2)	56 μH
Rated power (P_{dc})	2000 W	Operating frequency (f_s)	40–200 kHz

Utilizing the variable-frequency control method, Figure 21 illustrates the forward and reverse power operation waveforms of a single-phase full load (1000 W) under the proposed control method. The output bus voltage on the DC side is 280 V and 370 V in Figure 21a,c and Figure 21b,d, respectively, which show two operation cases for $k > 0.5$ and $k < 0.5$. As seen, the inductor current i_{L1} has a small current bias instead of staying at zero in both positive and negative half cycles for all the waveforms, indicating the effectiveness of the current value control near the zero-crossing point. It can be observed that the inductor current can be negative, which is a crucial characteristic of the additional conduction time.

Comprehensive simulations were conducted to further validate the effectiveness of the proposed variable switching frequency with additional conduction time. As shown in Figure 22a, when the additional conduction time is injected based on (24), the inductor current is negative before S_2 turns on. This negative current plays a crucial role in discharging the switch junction capacitor of S_2, thereby facilitating the achievement of ZVS. In contrast, as depicted in Figure 22b, when the variable-frequency control is implemented without the additional conduction time based on (16), i_L is nearly zero before S_2 turns on, resulting in hard switching.

Figure 23 shows the performance of the current ripple reduction adopting the interleaved structure under different load conditions. As can be seen, after interleaving, the current ripple of the sum of the two inductor currents ($i_{L1} + i_{L2}$) becomes much smaller compared with the one for each single phase (i_{L1} or i_{L2}). Additionally, the expanded waveforms for the three currents are also shown, which demonstrate the effectiveness of the current ripple reduction.

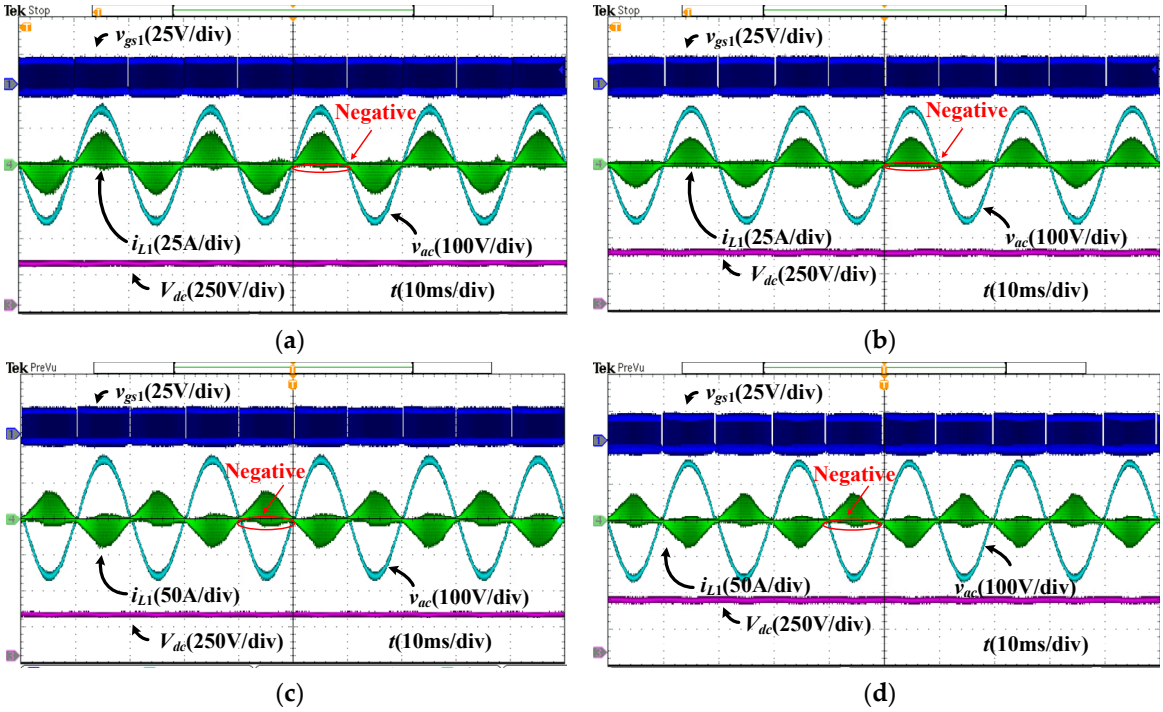


Figure 21. The forward and reverse steady-state waveforms with the proposed variable-frequency control method. (**a**) V_{dc} = 280 V, $k > 0.5$, P_o = 1 kW. (**b**) V_{dc} = 370 V, $k \leq 0.5$, P_o = 1 kW. (**c**) V_{dc} = 280 V, $k > 0.5$, $P_o = -1$ kW. (**d**) V_{dc} = 370 V, $k \leq 0.5$, $P_o = -1$ kW.

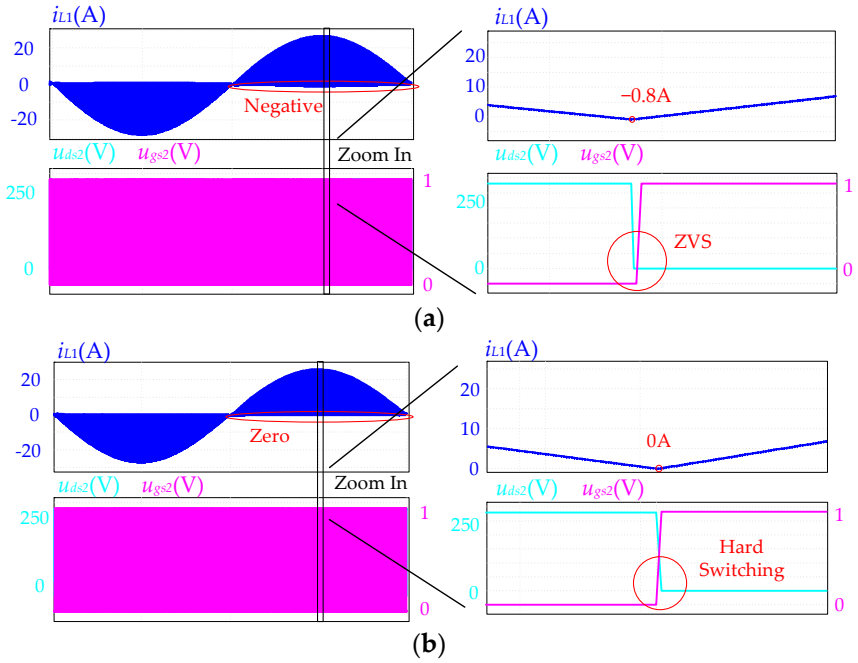


Figure 22. Simulated waveforms of additional conduction time. (**a**) With additional conduction time under the proposed control. (**b**) Without the additional conduction time.

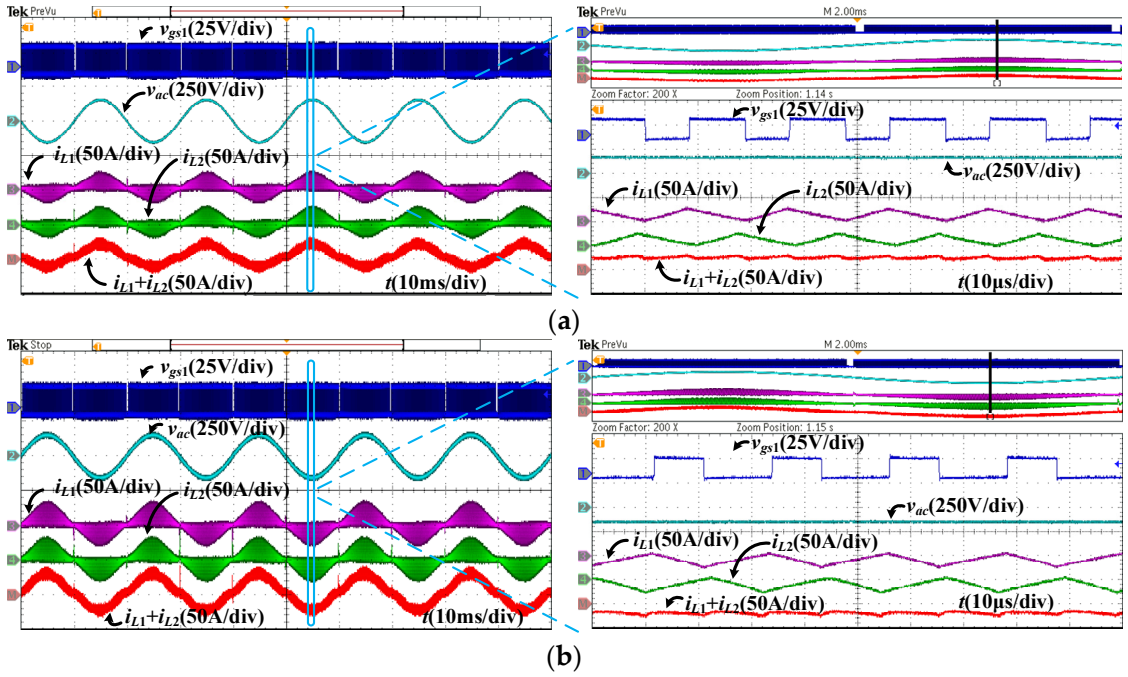


Figure 23. Detailed steady-state waveforms in one switching period: (**a**) 1000 W; (**b**) 2000 W.

Figure 24 shows the ZVS achievement of the two switches S_1 and S_2 on the single-phase full load (1000 W) in the traditional CRM control method. As seen in Figure 24c, S_2 cannot achieve ZVS when $k > 0.5$, indicating that the ZVS region is limited when the converter only operates in CRM and that ZVS cannot be achieved over a wide voltage range.

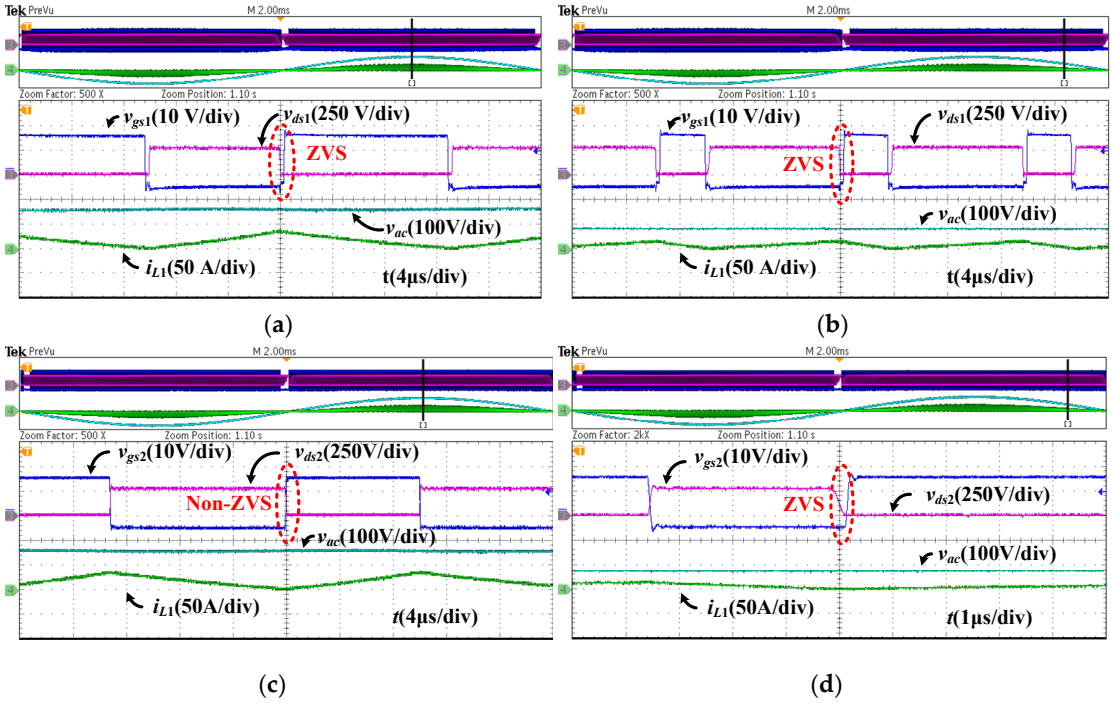


Figure 24. ZVS waveforms in single-phase traditional CRM. (**a**) For S_1, when $k > 0.5$. (**b**) For S_1, when $k \leq 0.5$. (**c**) For S_2, when $k > 0.5$. (**d**) For S_2, when $k \leq 0.5$.

Figure 25 shows the ZVS performance in the main switch with a single-phase full load (1000 W) under the proposed variable-frequency control method for the converter at different DC side output voltages. As shown in Figure 25a,c, if the DC bus voltage is greater

than the AC voltage and the negative bias current is increased, both at V_{dc} = 280 V and V_{dc} = 370 V, when the input voltage is in the positive half cycle, S_2 achieves ZVS turn-on. Similarly, within the negative half cycle, S_1 can also achieve ZVS. Therefore, it is verified that the variable-frequency control without ZCD circuits proposed in this paper can achieve ZVS in the totem-pole bridgeless PFC converter under different output voltages.

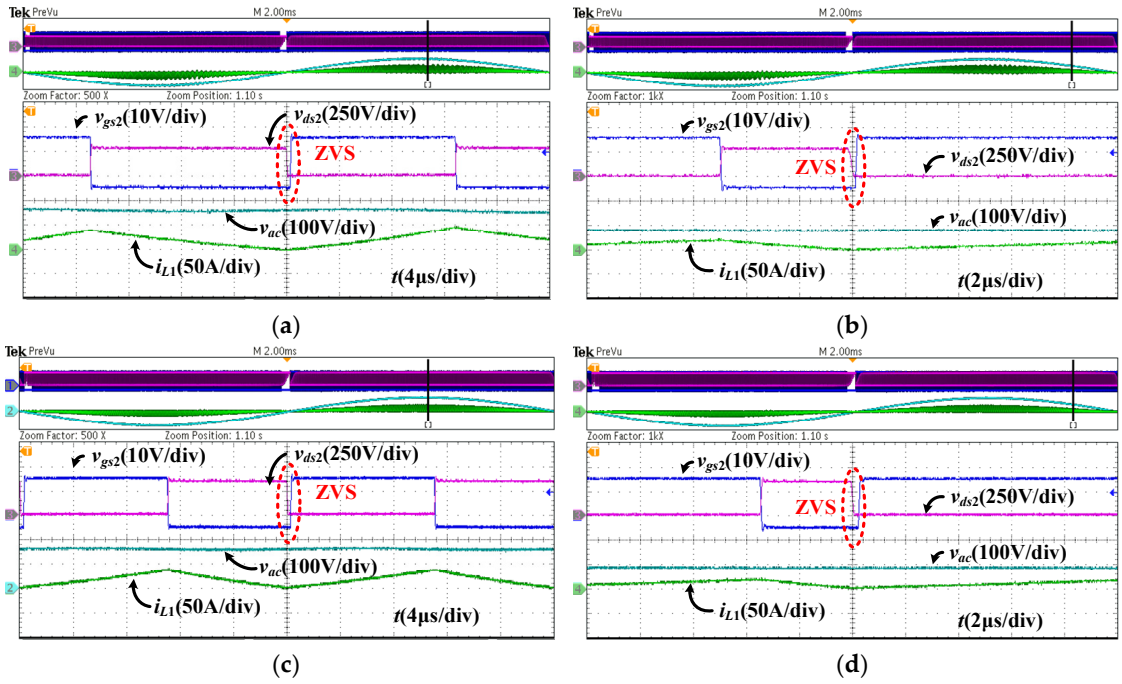


Figure 25. ZVS waveform of S_2 under the proposed variable-frequency control for single-phase full load (1000 W). (**a**) When $k > 0.5$ and V_{dc} = 280 V. (**b**) When $k \leq 0.5$ and V_{dc} = 280 V. (**c**) When $k > 0.5$ and V_{dc} = 370 V. (**d**) When $k \leq 0.5$ and V_{dc} = 370 V.

Figure 26 shows the ZVS implementation for the single-phase half load (500 W) output of the converter under the proposed variable-frequency soft-switching control method. As shown in Figure 26a,b, the main switch S_2 achieved ZVS at different input voltage values and under different voltage conditions during the positive half cycle.

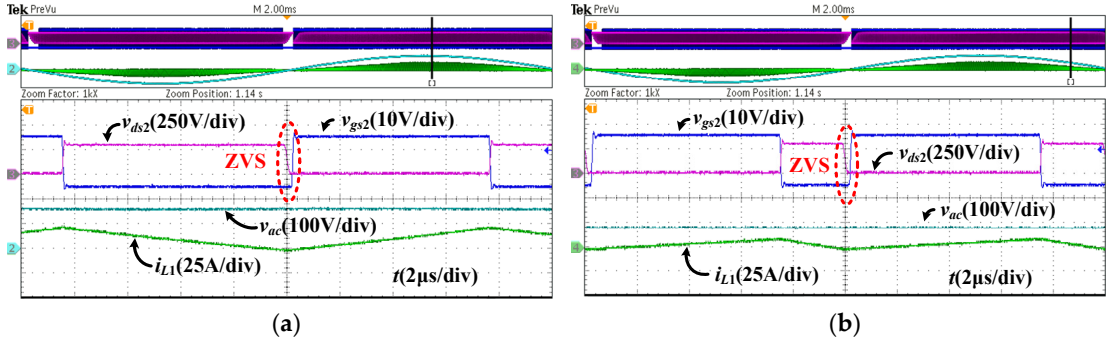


Figure 26. ZVS waveform of S_2 under the proposed variable-frequency control for the single-phase half load (500 W). (**a**) $k > 0.5$. (**b**) $k \leq 0.5$.

Figure 27 shows the power loss breakdown under different loads, including half load (1000 W) and full load (2000 W). These losses can be categorized into three main areas: conduction losses of switches (P_{con}), switching losses (P_{sw}), and core and iron losses of inductors (P_{ind}). Due to the achievement of ZVS, the switching turn-on loss theoretically approaches zero, resulting in a relatively lower P_{sw}. On the other hand, P_{con} emerges as the

dominant factor in the overall loss distribution. Meanwhile, P_{ind} increases as the transferred power increases.

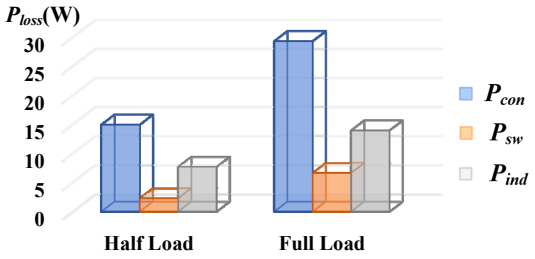


Figure 27. The power loss breakdown under different loads.

The efficiency curve of the two-phase interleaving of the converter is given in Figure 28. With an input AC voltage of 110 V, the efficiency at rated power is 97.72%. The converter can obtain a peak efficiency of 97.78% with the proposed full-range ZVS control strategy.

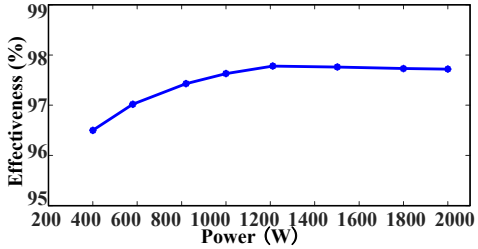


Figure 28. Two-phase interleaving efficiency curve.

Table 2 shows comparisons of the proposed converter and other totem-pole bridgeless PFC converters in the literature. The converters in [2,20,26] are limited to unidirectional power flow applications, with [2,26] requiring additional magnetic components. In addition, a ZCD circuit is needed in [19]. In conclusion, the main advantages of our proposed converter include its control simplicity, the absence of ZCD circuits, and the soft-switching capabilities suitable for bidirectional power flow applications.

Table 2. Comparisons of the proposed method and existing methods.

Article	Number of Switches	Number of Inductor	Number of Diode	Rated Power	Voltage Stress	Peak Efficiency	THD
[2]	4	3	2	1600	V_{dc}	98.2%	6.83%
[19]	6	2	0	2000	V_{dc}	99%	3%
[20]	4	2	2	800	V_{dc}	97.8%	—
[26]	4	3	2	1000	V_{dc}	97%	7%
Proposed	6	2	0	2000	V_{dc}	97.72%	11.39%

6. Conclusions

This paper proposes a variable-frequency control method without the need for ZCD circuits to address issues in existing totem-pole bridgeless PFC converters, such as high circuit cost and complex circuit control due to the use of the ZCD circuit or auxiliary resonant circuit to achieve ZVS. Through a detailed analysis of the ZVS model considering switch junction capacitors, it can be found that, in traditional CRM, when $k > 0.5$, the energy is insufficient to fully charge/discharge the junction capacitors, resulting in the loss of ZVS. After introducing an additional conduction time, the current when the switch is turned on can be increased, providing enough energy to maintain ZVS. Consequently, a variable-frequency control scheme is proposed to provide this additional conduction time. Additionally, an interleaved parallel connection method is adopted to reduce the inductor

current ripple. A digital control block diagram based on this variable-frequency method for the interleaved totem-pole bridgeless PFC converter is given. The experimental results demonstrate the effectiveness of the proposed approach, showing that a wide range of ZVS can be achieved and the current ripple can be reduced.

Author Contributions: Conceptualization and writing—original draft preparation, H.X.; methodology, G.X.; software and validation, L.L.; resources, M.S.; investigation and writing—review and editing, Z.C. All authors have read and agreed to the published version of the manuscript.

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References

1. Tseng, S.-Y.; Fan, J.-H. Bridgeless boost converter with an interleaving manner for PFC applications. *Electronics* **2021**, *10*, 296. [CrossRef]
2. Park, M.-H.; Baek, J.; Jeong, Y.; Moon, G.-W. An interleaved totem-pole bridgeless boost PFC converter with soft-switching capability adopting phase-shifting control. *IEEE Trans. Power Electron.* **2019**, *34*, 10610–10618. [CrossRef]
3. Wu, S.-T.; Chen, F.-Y.; Chien, M.-C.; Wang, J.-M.; Su, Y.-Y. A hybrid control scheme with fast transient and low harmonic for boost PFC converter. *Electronics* **2021**, *10*, 1848. [CrossRef]
4. Kim, J.-W.; Moon, G.-W. Minimizing effect of input filter capacitor in a digital boundary conduction mode power factor corrector based on time-domain analysis. *IEEE Trans. Power Electron.* **2015**, *31*, 3827–3836. [CrossRef]
5. Youn, H.-S.; Park, J.-S.; Park, K.-B.; Baek, J.-I.; Moon, G.-W. A digital predictive peak current control for power factor correction with low-input current distortion. *IEEE Trans. Power Electron.* **2015**, *31*, 900–912. [CrossRef]
6. Salmon. Comparative evaluation of circuit topologies for 1-phase and 3-phase boost rectifiers operated with a low current distortion. In Proceedings of the 1994 Proceedings of Canadian Conference on Electrical and Computer Engineering, Halifax, NS, Canada, 25–28 September 1994; Volume 31, pp. 30–33.
7. Martinez, R.; Enjeti, P.N. A high-performance single-phase rectifier with input power factor correction. *IEEE Trans. Power Electron.* **1996**, *11*, 311–317. [CrossRef]
8. de Souza, A.F.; Barbi, I. High power factor rectifier with reduced conduction and commutation losses. In Proceedings of the 21st International Telecommunications Energy Conference, INTELEC'99 (Cat. No. 99CH37007), Copenhagen, Denmark, 9 June 1999; p. 158.
9. Mansouri, M.; Kaboli, S.H.A.; Selvaraj, J.; Rahim, N.A. A review of single phase power factor correction AC-DC converters. In Proceedings of the 2013 IEEE Conference on Clean Energy and Technology (CEAT), Langkawi, Malaysia, 18–20 November 2013; pp. 389–394.
10. Singh, B.; Singh, B.N.; Chandra, A.; Al-Haddad, K.; Pandey, A.; Kothari, D.P. A review of single-phase improved power quality AC-DC converters. *IEEE Trans. Ind. Electron.* **2003**, *50*, 962–981. [CrossRef]
11. Huber, L.; Jang, Y.; Jovanovic, M.M. Performance evaluation of bridgeless PFC boost rectifiers. *IEEE Trans. Power Electron.* **2008**, *23*, 1381–1390. [CrossRef]
12. Jang, Y.; Jovanovic, M.M. A bridgeless PFC boost rectifier with optimized magnetic utilization. *IEEE Trans. Power Electron.* **2009**, *24*, 85–93. [CrossRef]
13. Muhammad, K.S.; Lu, D.D.-C. Two-switch ZCS totem-pole bridgeless PFC boost rectifier. In Proceedings of the 2012 IEEE International Conference on Power and Energy (PECon), Kota Kinabalu, Malaysia, 2–5 December 2012; pp. 1–6.
14. Le, T.-T.; Lee, J.; Choi, S. Single-Stage Totem-Pole AC-DC Converter based on Boost-Half Bridge Structure for battery chargers. *IEEE Trans. Power Electron.* **2023**, *39*, 1060–1073. [CrossRef]
15. Zhou, M.; Peng, C.; Liang, J.; Fu, M.; Wang, H. Current zero-crossing prediction based critical conduction mode control of totem-pole PFC rectifiers. *IEEE Trans. Power Electron.* **2023**, *38*, 8513–8527. [CrossRef]
16. Yao, K.; Chen, K.; Mao, C.; Tang, H.; Li, L.; Wu, C.; Zhang, Z.; Ma, C. Optimal switching frequency variation range control for critical conduction mode boost power factor correction converter. *IEEE Trans. Ind. Electron.* **2020**, *68*, 1197–1209. [CrossRef]
17. Ren, X.; Zhou, Y.; Guo, Z.; Wu, Y.; Zhang, Z.; Chen, Q. Simple analog-based accurate variable on-time control for critical conduction mode boost power factor correction converters. *IEEE J. Emerg. Sel. Top. Power Electron.* **2019**, *8*, 4025–4036. [CrossRef]
18. Wang, K.; Zhu, H.; Wu, J.; Yang, X.; Wang, L. Adaptive driving scheme for ZVS and minimizing circulating current in MHz CRM converters. *IEEE Trans. Power Electron.* **2020**, *36*, 3633–3637. [CrossRef]
19. Yang, Y.; Li, Z.; Song, D.; Wang, S.; Zhang, Z.; Ren, X.; Chen, Q. SR control with zero current detection delay compensation for GaN CRM totem-pole PFC rectifier. *IEEE Trans. Power Electron.* **2023**, *38*, 7059–7068. [CrossRef]
20. Jeong, Y.; Park, M.-H.; Moon, G.-W. High-efficiency zero-voltage-switching totem-pole bridgeless rectifier with integrated inrush current limiter circuit. *IEEE Trans. Ind. Electron.* **2019**, *67*, 7421–7429. [CrossRef]

21. Belkamel, H.; Kim, H.; Choi, S. Interleaved totem-pole ZVS converter operating in CCM for single-stage bidirectional AC–DC conversion with high-frequency isolation. *IEEE Trans. Power Electron.* **2020**, *36*, 3486–3495. [CrossRef]
22. Lee, Y.-D.; Moon, G.-W.; Baek, J.; Kim, C.-E. A reconfigurable totem-pole PFC rectifier with light load optimization control strategy and soft-switching capability. *IEEE Trans. Power Electron.* **2020**, *36*, 4371–4382. [CrossRef]
23. Tausif, A.; Bakan, A.F.; Dusmez, S. A High Power Density Zero-Voltage-Switching Totem-Pole Power Factor Correction Converter. *IEEE Trans. Power Electron.* **2023**, *39*, 837–849. [CrossRef]
24. Huang, Q.; Yu, R.; Huang, A.Q.; Yu, W. Adaptive zero-voltage-switching control and hybrid current control for high efficiency GaN-based MHz Totem-pole PFC rectifier. In Proceedings of the 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, USA, 26–30 March 2017; pp. 1763–1770.
25. Tang, Y.; Ding, W.; Khaligh, A. A bridgeless totem-pole interleaved PFC converter for plug-in electric vehicles. In Proceedings of the 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 20–24 March 2016; pp. 440–445.
26. Soares, J.W.M.; Badin, A.A. High-efficiency interleaved totem-pole pfc converter with voltage follower characteristics. *IEEE J. Emerg. Sel. Top. Power Electron.* **2022**, *11*, 1879–1887. [CrossRef]

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