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Effects of Fractional Time Delay as a Low-Power True Time Delay Digital Beamforming Architecture

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Abstract: True time delay digital beamforming enables large squint-free bandwidths and high beamcounts, ideal for Low Earth Orbit (LEO) satellite communication links. This work proposes a true time delay architecture using Variable Fractional Delay (VFD). True time delay eliminates many analog beamforming performance constraints including inaccurate beam steering and limited beamcounts, while managing system quantization error. This article presents a method of implementing true time delay using a VFD digital filter with sufficient time resolution to minimize quantization error and enable both gigahertz bandwidths and sampling frequencies. Simulations of antenna patterns utilizing the proposed VFD digital filters demonstrate satisfactory LEO beamforming performance with only a 29-tap filter. The VFD filter was implemented using a Xilinx Virtex Ultrascale FPGA and demonstrated a 1077% reduction in dynamic power and a minimum 498% reduction in logic resources, with only a modest increase in multipliers required when compared to Farrow-based architectures previously proposed in the literature.

Keywords: digital beamforming; true time delay; phased array; variable fractional delay; quantization sidelobes



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1. Introduction

Analog phased-array beamforming is a mature technology that is used frequently in aerospace, defense, and cellular applications [1–4]. For example, analog phased arrays are typically used for SATCOM applications and require both wide bandwidths and high data rates to meet next-generation performance requirements [2,3]. However, when moving toward next-generation technology, the complexity of the necessary RF circuitry limits analog phased-array beamcounts and bandwidths [5]. Analog solutions enable simple implementation of limited numbers of beams with only RF amplifiers, power dividers, and phase shifters [5]. However, the number of phase shifters and power dividers will increase as a function of beamcount which quickly results in impractical circuit designs [4,5]. Further, analog phased-array bandwidths are narrow due to the use of phase shifters as the delay element. Phase shifters allow only the center frequency to be steered to the desired angle, while other frequencies in the band suffer from steering angle error called beamsquint [5,6]. To address these challenges, digital beamforming (DBF) solutions are poised to improve both bandwidth and beamcount with the added trade-off of complex design, high power, and high cost [4]. As Low Earth Orbit (LEO) satellite constellations are increasing in popularity, there exists a need to improve digital beamforming solutions for practical systems that can utilize arbitrarily high beamcounts over wide bandwidths [4]. There exist a few DBF solutions to increase beamcount and/or improve system bandwidth utilizing modifications to traditional techniques [5,7–18]. For example, recent work has focused on using digital signal processing (DSP) to implement true time delays [5,7,8,18,19]. Notably, Jang et al. designed an architecture that first down-converts the RF signal to

baseband for digital processing [7,8]. At baseband, a coarse integer sample delay is applied, and then phase shifters are implemented to reduce quantization error. While this method does reduce beam squint, phase shifter stages only approximate time delay and thus the architecture is limited to a relatively narrow bandwidth of 100 MHz [7,9].

In order to overcome the bandwidth constraints, other works have expanded upon traditional integer delay techniques by using fractional delay [10–12,16–18]. Farrow architecture filters are commonly used for Variable Fractional Delay (VFD) filter designs; however, their complexity increases significantly at higher sampling rates [10–13,16,17]. Canese et al. avoid this constraint by utilizing a multirate Farrow architecture that increases bandwidth through the addition of an upsample and downsample element at each VFD filter [10]. However, this technique also adds complexity to the design that can be costly to integrate into silicon processes. Schmidt et al. propose a peak-to-average power ratio (PAPR)-focused architecture using Lagrange interpolation filters in order to achieve maximum energy efficiency of the output signal [18]. As with any interpolated filter architecture, Lagrange filters suffer from increased computational complexity and frequency response error when compared to lowpass or allpass filters [14,15]. Laakso et al. state that real-time coefficient updates can become too computationally expensive to be realistic for complex Farrow filters, further supporting an alternative architecture [14].

Alternatively, traditional Finite Impulse Response (FIR) lowpass filter structures can be a desirable architecture due to their excellent least-squared approximation error [14,15]. Additionally, FIR filter structures are extremely computationally efficient and can be optimized heavily. In order to overcome the complexity, bandwidth, and beam squint constraints of present VFD and DBF methods, this work will utilize a lowpass FIR filter designed specifically for direct implementation into standard CMOS processes. This novel architecture will use a unique approach to VFD that focuses on minimum power and resource consumption optimizations of the delay unit for use in SATCOM applications. Results will show that the architecture boasts exceptionally low power and resource consumption when compared to similar designs available in the literature, at the expense of some filter and bandwidth performance. The FIR filter design in this work will target a 10 GHz sampling rate (F_s) and 4 GHz bandwidth for LEO applications. The proposed system was implemented in a Field Programmable Gate Array (FPGA) and then compared to the relevant alternative systems available in the literature.

2. Theory of Operation

This section aims to describe the system constraints and relevant key performance parameters that influenced the design of the VFD filter. These key metrics will tie into the use cases of a VFD beamforming solution in order to develop a relevant true time delay (TTD) beamforming architecture. As such, a lowpass FIR filter was utilized due to a deterministic group delay and future ease of integration with standard silicon processes [14,15]. This choice was made due to significant research in literature to develop silicon-based FIR filter architectures that are size and power efficient [20–22]. Additionally, FPGA vendors including Xilinx incorporate purpose-built DSP slices as a standard feature of their integrated circuits for optimized FIR filter implementations [23]. A traditional FIR filter structure produces excellent least-squared approximation error; however, it is also computationally expensive when calculating new filter coefficients to adjust filter parameters [14,15]. Although Farrow filter architectures enable easy adjustment for arbitrary fractional delays, this work aims to provide a method that overcomes some disadvantages of the Farrow architecture by focusing on minimum size and power. As a result, this work will focus on a look-up-table (LUT) approach to filter coefficients. In this method, a modest number of fractional delay steps achieves a fractional delay resolution which enables filter coefficient assignment through an LUT. The LUT-based approach removes the polynomial approximation calculations of the Farrow filter, drastically improving filter implementation size and cost. Additionally, an LUT VFD design can enable multi-gigahertz bandwidths without the need for up- or down-conversion. In order to verify this method, a simulation of an

ideal Uniform Linear Array (ULA) was performed using MATLAB and used to analyze quantization error, sidelobe level, fractional delay, and system accuracy.

As with most digitally reconstructed signals, DBF designs create quantization error which results in spatial noise that manifests as quantization sidelobes. As such, this work utilizes the Digital Video Broadcast (DVB) S2 specifications in order to determine acceptable sidelobe levels [24]. Table 20 DVB states that Direct-To-Home physical layer simulations must have a cross-polarity sidelobe limit of -24 dB [24]. To ensure this DVB specification is met, a 10 dB margin is added, producing a target sidelobe floor of -34 dB max.

In order to determine a performance baseline of time delay quantization resolution, an array was simulated that steered to the minimum beam angle resolution, θ_{RES} , which is defined using Equation (1) for a linear array of N elements with the spacing of $\frac{\lambda}{2}$ [25]

$$\theta_{RES} \propto \sin^{-1} \frac{\phi_{LSB}}{N\pi}, \quad (1)$$

where ϕ_{LSB} is the minimum phase resolution available in the delay unit. The equivalent phase shift of a time delay is a function of the signal frequency, and is defined in Equation (2) [26]

$$\Delta\phi = 2\pi f\Delta t, \quad (2)$$

where Δt is the desired time delay, f is the frequency of the signal, and $\Delta\phi$ is the resulting phase shift. To demonstrate the need for improved time delay quantization resolution with respect to quantization sidelobes, a 30-element system was simulated in two cases: (1) using only integer delays, where half of the elements have 1 sample delay and the other half have no delay, Figure 1a blue curve, and (2) an ideal beam pattern with double precision floating point fractional resolution, Figure 1a orange curve. Note the 25 dB change in the sidelobe floor, -5 dB quantization sidelobe, and steering angle error with only integer delays. This initial simulated array demonstrates that to achieve the desired 4GHz bandwidth and -34 dB sidelobe floor, fractional sample delays must be employed.

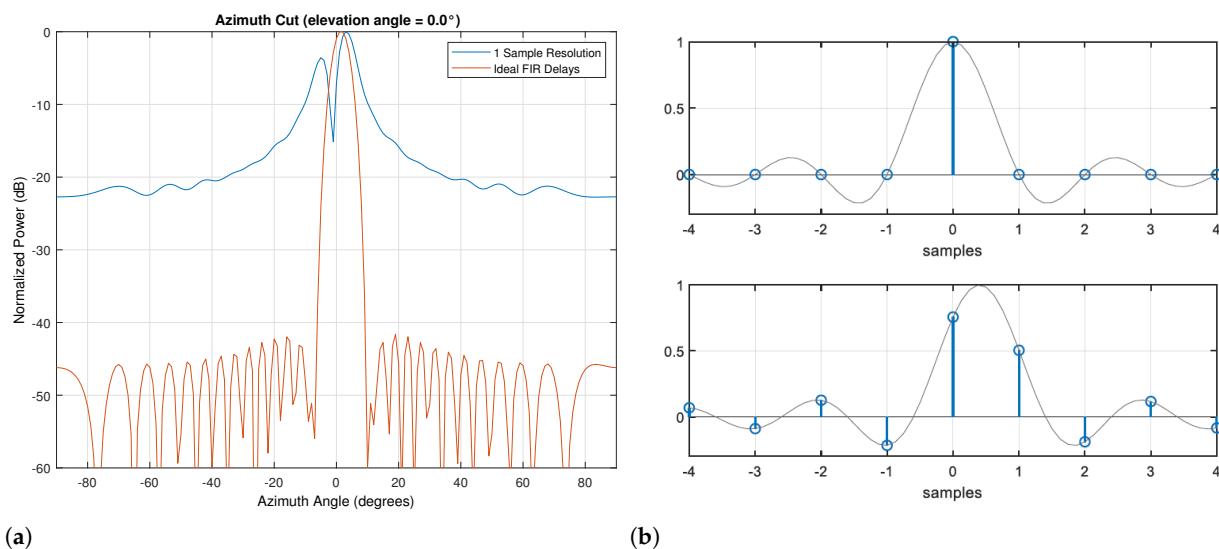


Figure 1. (a): Antenna patterns for two independent systems steering to θ_{RES} , 10 GHz F_s , and 4 GHz signal. Ideal fractional delay (orange) vs. integer only delays (blue), and (b): FIR impulse response with 0 sample fractional delay (top) vs. 0.4 sample fractional delay (bottom).

The proposed fractional delay filters utilize adjustable sinc impulses in the time domain [15] by delaying a rational number of samples, N , as shown in (3)

$$h(n, u) = \frac{\sin(\pi(n - u))}{\pi(n - u)}, -\frac{N}{2} < n < \frac{N}{2}, -0.5 \leq u \leq 0.5, \quad (3)$$

where h is the impulse response of the filter, n is the number of taps, and u is the fractional delay.

Using Equation (3), a fractional delay of 0.4 samples in the impulse response is plotted in Figure 1b. The proposed method of fine delay tuning produces an excellent least-squares approximation error; however, group delay errors occur at the Nyquist bandwidth extremes due to the Gibbs phenomenon, producing quantization sidelobes [14,15]. The Gibbs phenomenon is shown to be mitigated by both implementing lowpass architectures rather than allpass and windowing the impulse response with a bell-shaped non-negative weighting function, further supporting the proposed lowpass FIR architecture [14].

In order to analyze the worst-case sidelobe levels of the system, a case study was designed to maximize quantization error and maximize the periodicity of error. A simulation was performed such that every other element was assigned zero error with the alternate elements being assigned $\frac{LSB}{2}$ error [25]. The DBF was then steered using Equation (4) to produce the maximum possible quantization sidelobe levels (QSL),

$$\theta_{MAXQSL} = \sin^{-1} \frac{\pm x}{2^{BITS}}, \quad (4)$$

where θ_{MAXQSL} is the steering angle that produces the maximum QSL, and $BITS$ is the number of time delay bits in the system. Note that x is a scalar that must be odd and satisfy the condition $n < 2^{BITS}$.

As the proposed architecture utilizes fractional time delay rather than phase shift, the system gains resolution from two factors: (1) the oversampling factor (OSF) of the system and (2) the number of fractional delay bits. This is described in Equation (5), as follows:

$$ENOB = \log_2(OSF * 2^{BITS}), \quad (5)$$

where $ENOB$ is the Effective Number of Bits. Oversampling improves $ENOB$ by lowering the noise floor which increases the signal to noise ratio (SNR) of the sampled signal. In the specific case of this work, a 3-fractional bit system with a 10 GHz sampling rate and 4 GHz bandwidth would produce a system $ENOB$ of 4.32 bits. As a result, Equation (4) can be rewritten, substituting $ENOB$ for $BITS$, as follows:

$$\theta_{MAXQSL} = \sin^{-1} \frac{\pm n}{2^{ENOB}}, \quad (6)$$

The $ENOB$ will then be used to analyze the system.

Finally, proper system resolution is critical to ensure sufficient sidelobe suppression. The maximum QSL of the proposed system can be determined using Equation (7) [25].

$$QSL \propto 20 \log_{10} 2^{-ENOB} \quad (7)$$

In order to produce a maximum QSL of -34 dB for a 10 GHz sampling rate and a 4 GHz bandwidth, the system must have an $ENOB$ of at least 5.65 bits.

3. Design

Using the system and design constraints discussed in Section 2, a minimum length VFD lowpass FIR filter was developed to provide a large bandwidth (4 GHz) with near-constant group delay throughout the passband. The minimum allowable group delay deviation for a given filter occurs where the functional delay of a $+0.5$ sample delay filter becomes negative, and -0.5 sample delay filter becomes positive. At this point, implemented element delays across the array begin to increment in a sawtooth fashion rather than linearly, adding significant quantization sidelobes. This undesirable group delay characteristic for ± 0.5 sample delay filters is shown in Figure 2a for a 5-tap filter design, with the sign change point denoted by the arrow. Therefore, it is necessary to ensure this behavior occurs outside of the desired passband. Through simulation analysis, it is found that designing a system

with a maximum 40% group delay variation produces minimal additional sidelobe level, and will meet system requirements. Parameters used for simulation are outlined in Table 1.

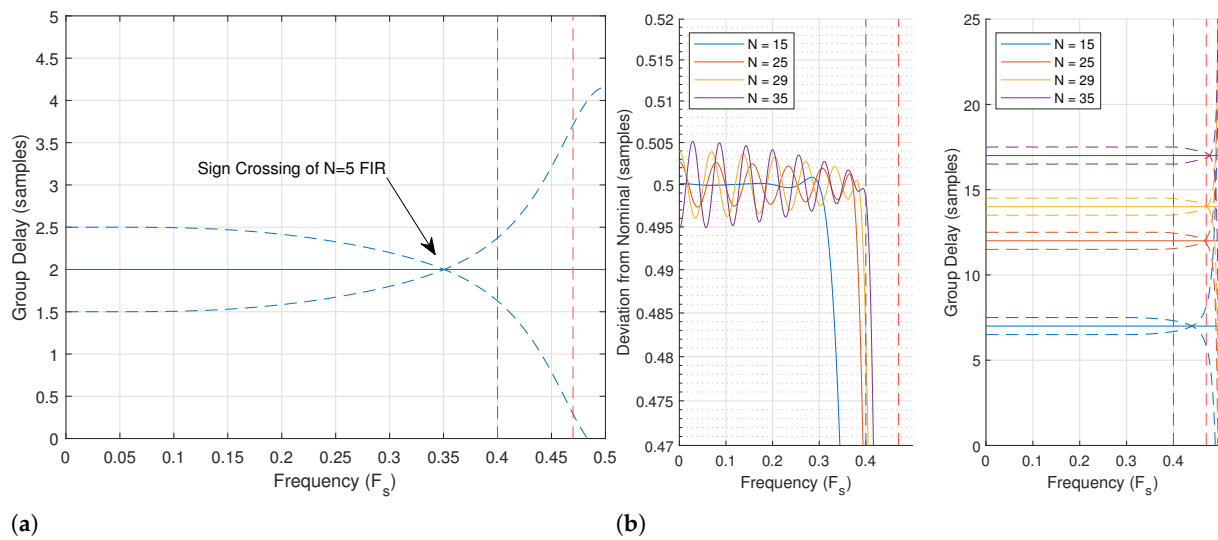


Figure 2. (a): Group delay response for an FIR filter of $N = 5$. Solid trace represents 0 fractional delay and dashed traces represent ± 0.5 sample fractional delay. Arrow denotes sign reversal of the implemented fractional delay. Black dashed line denotes desired functional bandwidth. Red dashed line denotes filter cutoff frequency. (b): Left: filter group delay for a $+0.5$ sample filter for a range of N . Right: range of fractional group delay values from -0.5 to $+0.5$ samples for a range of N .

Table 1. Figure 2 simulation parameters.

Parameter	Value
Sampling Frequency (F_s)	10 GHz
-6 dB Cutoff Frequency (F_c)	$F_s \times 0.47$
Functional Bandwidth	$F_s \times 0.4$
Signal Sample Length	2048

In order to maintain flat response throughout the passband (± 0.1 dB maximum) and minimize attenuation at the edge of the passband, the VFD architecture utilizes a -6 dB cutoff frequency of 47% of the sampling frequency, F_s . The minimum length filter that satisfies these requirements is found to be 29, as shown in Figure 2b. With this $N = 29$ filter design, the maximum group delay variation was determined to be 3.8%, well within the 40% range deemed allowable.

Therefore, for the VFD filter to successfully operate in LEO applications it must have a length of $N = 29$ and cutoff frequency of $0.47F_s$. Additionally, the VFD filter's impulse response utilizes a Chebyshev window with -60 dB sidelobes to minimize mainlobe width while also providing an equiripple passband [27]. Although such large sidelobes are typically undesirable, decreasing the sidelobe level further has the consequence of increasing mainlobe width and reducing the high-frequency resolution of the system. This window choice will also serve to minimize effects of the Gibbs phenomenon, as discussed previously.

In order to meet the *ENOB* requirement of 5.65 bits, 5 fractional bits were needed to provide a -38 dB sidelobe floor and meet the general LEO system requirements. This 5-bit system would produce 32 discrete fractional time delay steps, providing acceptable time delay resolution while minimizing implementation size.

A final block diagram of the $N = 29$, 5-bit system is shown in Figure 3 with key elements including a variable length First In First Out (FIFO) for coarse integer delays and the VFD filter for fractional delays. A detailed block diagram of the highlighted portions

in Figure 3 implemented in Simulink is shown in Figure 4. Simulations of the system were performed using a 35-element ULA with $\frac{\lambda}{2}$ element spacing at a 4 GHz maximum frequency. Beam weights were windowed with a Hamming window to suppress sidelobes an equal amount in the spatial domain [27]. As this paper will not consider a fixed-point representation of filter coefficients for implementation in silicon, an ideal ADC with double precision resolution will be assumed for simulation.

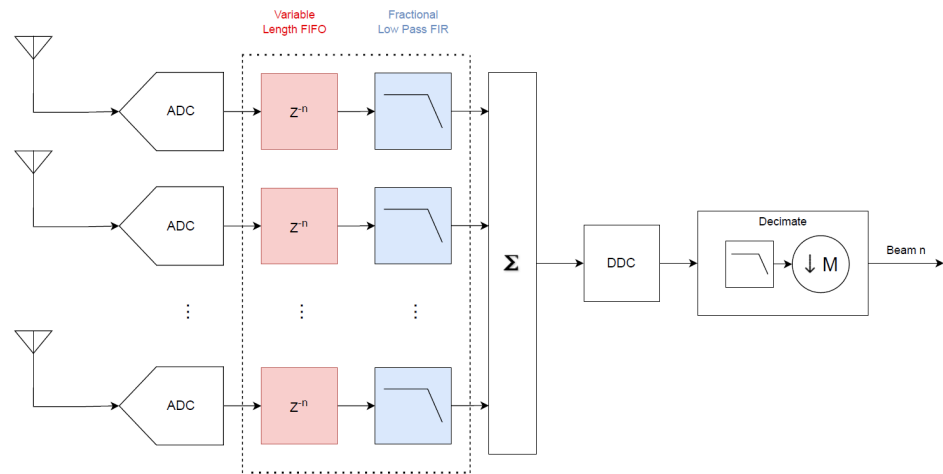


Figure 3. Block diagram of proposed architecture.

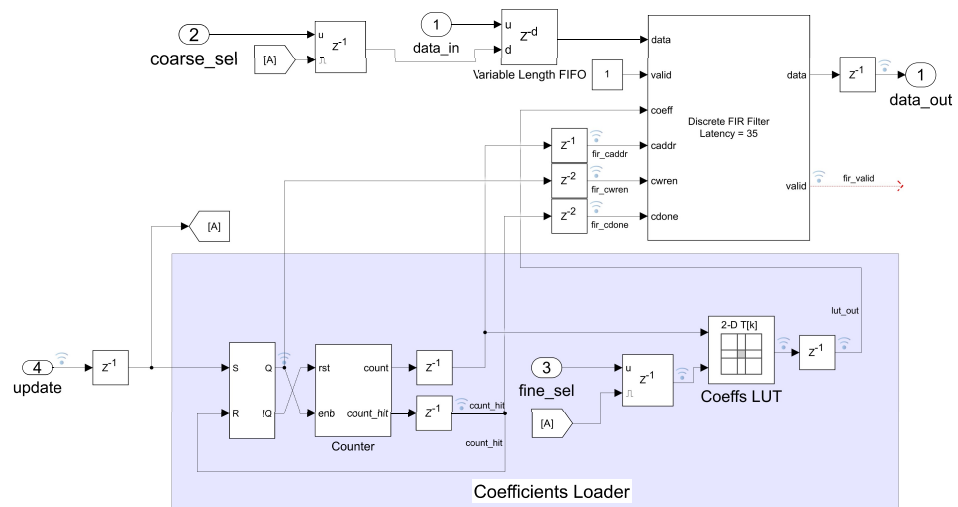


Figure 4. Implemented architecture in SIMULINK.

4. Simulation Results and Analysis

For the proposed $N = 29$ VFD lowpass FIR filter DBF architecture, Figure 5 shows the simulated antenna pattern when steering to θ_{QSL} . The maximum QSL of the system was determined to be at -35.3 dB, which is 2.7 dB poorer than the expected value of -38 dB. This performance decrease can be explained as periodic sawtooth error sampled across the aperture of the array, which causes spatial harmonics to add in phase [25]. When compared to the ideal floating point fractional delay, the VFD lowpass FIR filter architecture is determined to be 9.6 dB worse at the location of the maximum QSL when steering to the same angle. In both cases, a 4 GHz signal will produce the worst-case quantization error, as its period is the shortest within the desired bandwidth, which in turn requires the most fractional time steps in order to steer the array properly.

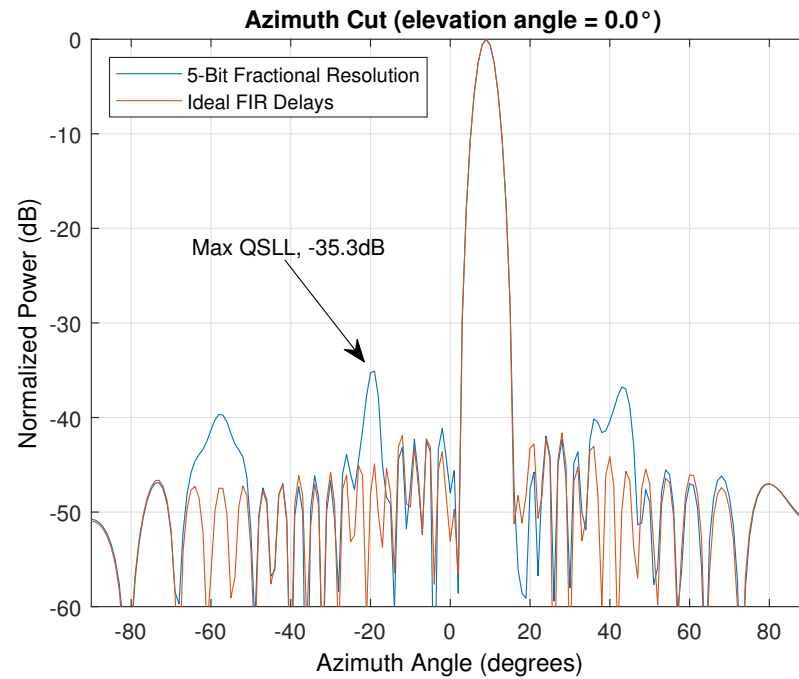


Figure 5. Antenna pattern of proposed architecture when steering to θ_{QSL} . Arrow denotes worst-case quantization sidelobe.

Figure 6 performs a simulation using RF signals of 2–4 GHz. This figure shows that there is no discernible beam squinting of the array across a wide bandwidth. Additionally, it demonstrates that the max QSL and sidelobe floor remain consistent when operating with different signal frequencies, with the 4 GHz signal producing the noisiest result due to the non-linear VFD group delay at 4 GHz.

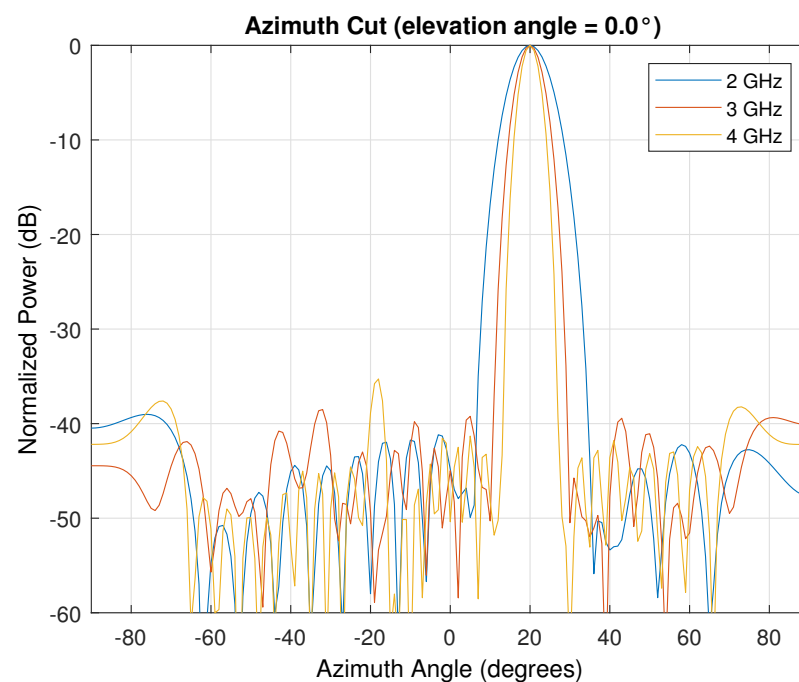


Figure 6. Beamsquint investigation of the proposed architecture.

5. Implementation Results and Analysis

The Simulink fractional delay processing chain in Figure 4 was implemented in Verilog to determine the resource and power consumption for a single channel. An FPGA target

is chosen for quick design and implementation results. While an FPGA will not be able to achieve the desired 10 GHz F_s , it will provide insight when compared to similar peer-reviewed works with respect to resource utilization and power consumption. Synthesis and implementation were performed using a Virtex Ultrascale xcvu440-flgb2377-3-e. To directly compare to [10], the system clock frequency is set to 250 MHz, with 16-bit input data and 16-bit filter coefficients. The results are shown in Table 2.

Table 2. Resource comparison of selected designs.

Work	Slices/CLBs	LUT	LUTRAM	BRAM	FF	DSPs	Bandwidth (MHz)	Dynamic Power (mW)
This Work	298	326	0	0.5	2106	29	117.5	67
[10]	-	8393	952	0	10,489	6	241.6	722
[19], $m = 4$	-	1501	0	6	1131	16	-	-
[16], Ex. 2	748	-	-	-	-	-	226.95	68.57
[17]	17,108	61,342	11,292	0	-	-	12.79	-

Based on FPGA implementation, it was found that the VFD low-pass filter design requires roughly 10 times less dynamic power and has anywhere from a 5- to 25-time reduction in logic resources needed to implement compared to similar designs in the literature. However, the proposed architecture does require approximately 5 times more multipliers (DSP slices) and achieves only 48.6% of usable bandwidth.

6. Analysis

The analysis performed is based on simulated results and FPGA place and route due to the difficulty of empirical testing. As most articles in the literature are based on simulation and place-and-route data, this article aims to provide a valid comparison to the literature and provide a path towards fabrication and experimental verification.

Typically, programmable FIR filters can reduce the number of multipliers required by exploiting the symmetry of the sinc impulse response. For example, sinc functions can be designed such that coefficients of zero always appear in the same location. As a result, these multipliers can be removed from the design. Additionally, coefficients of equal magnitude can use the same multiplier, only needing a sign change. However, the mechanism of fractional delay outlined in Section 2 does not lend itself to these kinds of optimizations. When the sinc function is adjusted in the time domain, these symmetries no longer exist, as demonstrated in Figure 1b.

Bandwidth is also reduced when compared to [10] due to their multi-rate architecture. The multi-rate architecture increases bandwidth at the expense of increased complexity. In order to keep power consumption as low as possible, this work targets a single-rate implementation with the maximum possible bandwidth and throughput.

The proposed architecture is not designed to be an all-encompassing solution. Instead, it provides engineering trade-offs for power and thermally constrained SATCOM applications at the cost of beamforming performance and bandwidth. When comparing the proposed architecture to similar peer-reviewed designs, these trade-offs can be highlighted. Zhang et al. design a filter using a floating point coefficient structure [19]. While this should produce the least possible quantization error, the design is significantly pipelined to keep resource consumption competitive, and thus has high processing latency, from 11.4 μ s to 0.220 μ s, depending on filter configuration. Additionally, this filter is not designed for fractional delay which contributes to its low throughput. Ramirez-Conejo et al. produce a paralleled Farrow architecture with impressive bandwidth and power consumption but requires approximately 350% additional resources compared to this work [16]. These comparisons show that the VFD filter in this work boasts minimum power and resource consumption, at the expense of some filter bandwidth.

To further reduce resource and power consumption, memory optimizations could be performed by reusing filters with an equal magnitude of delay, reducing the number

of entries required by half. Further optimizations could be conducted by determining the minimum required coefficient fixed-point resolution needed to continue minimizing quantization error. If less bandwidth is needed, the length of each filter could be reduced, further eliminating LUT memory requirements, as well as multiplier count.

Future VFD filter research that targets increased filter bandwidth whilst maintaining comparable resource utilization to the proposed architecture could produce a promising well-rounded solution to future SATCOM applications. Additionally, with the development of 6G wireless standards, there is research pressure for architectures that can cover the wide bandwidths of the 6G network whilst maintaining minimum power for satellite applications [28]. This will become increasingly critical as technology moves past 6G into future 7G technologies, currently being developed [29]. Optimizing this architecture further will be the key to enabling these products.

7. Conclusions

This work proposes a fractional time delay DBF architecture using a VFD lowpass FIR filter that has a four gigahertz-wide functional bandwidth, and requires no upsampling or downsampling at the delay unit. Results show that only five fractional time bits are required to achieve acceptable DBF performance. Simulations verify that this new design creates a maximum QSL of -35.3 dB and produces no beam squinting. Additionally, if a narrower bandwidth is desired, filter lengths can be further reduced to optimize implementation complexity. The fractional time delay FIR filter is drastically improved by the adoption of an LUT-based implementation where filter coefficients do not need to be calculated on demand. Additionally, the LUT-based design is easily implemented on standard FPGAs and could be adapted to standard CMOS processes for ASIC designs.

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Conflicts of Interest: Zachary Liebold and Bob Broughton were employed by Analog Device Inc. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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