

Article

A Wideband Hybrid Envelope Tracking Supply Modulator with Slew-Rate-Enhanced Linear Amplifier

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Abstract: A wideband hybrid envelope tracking supply modulator (HETSM) with a slew-rate-enhanced linear amplifier (LA) is described in this work. The proposed slew-rate enhancement (SRE) structure introduces a parallel auxiliary current path directly to the gate of the class-AB output stage, significantly accelerating the charging and discharging processes of the Miller capacitor without modifying the operating point of the remaining LA. The current delivered via this supplementary path shows a rapid increase, with changes in input voltage, culminating in diminished quiescent current levels. The supply modulator is fabricated in a 180 nm CMOS process. The measurement results show that HETSM is able to track a 100 MHz, 16QAM signal accurately, achieving the maximum efficiency of 87.4% at a 5.12 W output power, with a load that consists of a 5 Ω resistor and a paralleled 100 pF capacitor. The proposed LA realizes a slew rate of $-1857/+1239$ V/ μ s and a bandwidth of 226.6 MHz under a 24 mA quiescent current.

Keywords: envelope tracking; wideband hybrid envelope tracking supply modulator; slew-rate enhancement



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1. Introduction

As the demand for data transmission rates continues to increase with modern communication technology, the increasing bandwidth and peak-to-average power ratio (PAPR) pose new challenges for the linearity and efficiency of power amplifiers. Envelope tracking (ET) technology is widely used, aiming to address this challenge by focusing on how to enhance the efficiency while ensuring the linearity of PAs [1–4]. Different from conventional power amplifiers with a fixed drain supply voltage, ET technology utilizes a dynamic drain voltage supply that tracks the envelope waveform [1]. As illustrated in Figure 1, where the green shaded region represents power losses on the power transistor, ET technology significantly reduces power dissipation on the power transistor, thereby improving efficiency [5–8]. HETSM, composed of switching converters (SWC) and LA and incorporating the advantages of both, has become the mainstream in research and applications and has been widely reported on in recent works [9–19].

For large bandwidth requirements, it becomes increasingly challenging for envelope tracking supply modulators to improve the bandwidth and slew rate while maintaining high efficiency [9,20,21]. Works in [22,23] proposed an envelope slew-rate reduction algorithm and demonstrated its beneficial effect on improving the linearity of ET PA. These works indicate the importance of meeting the signal slew-rate requirements for HETSM. Techniques such as adaptive biasing and super-class-AB recycling folded cascode are used to improve the slew rate without increasing the quiescent bias current in studies [20,24–26]. These techniques optimize the slew rate by amplifying the input-stage current during

the transition state. Consequently, the large current needs to be transferred to the final stage via the front stages [9]. Works [9,27,28] introduced the auxiliary circuit injecting slew-rate-enhanced current, which is proportional to the input voltage of LA, to the gate of the output stage without increasing the input-stage current. However, the quiescent current of the auxiliary SRE circuit should be large to achieve a high slew rate.

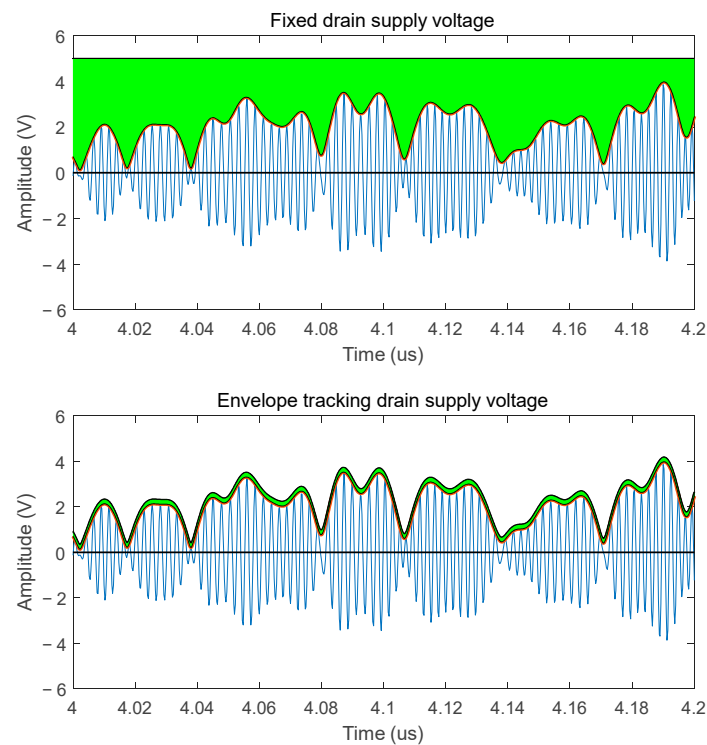


Figure 1. Power dissipation comparison between the ET PA and the traditional PA.

In this work, a wideband HETSM with a slew-rate-enhanced LA is proposed. In the LA with SRE structures, a parallel auxiliary current path is introduced to the gate of the class-AB output stage, significantly accelerating the charging and discharging processes of the Miller capacitor without modifying the operating point of the remaining LA. The current delivered via this SRE path shows nonlinear characteristics, increasing sharply with changes in input voltage, thus reducing the quiescent current levels. The rest of this paper is organized as follows: Section 2 describes the principles and implementation of the recommended HETSM, including the LA with the proposed SRE structure. Measurement results are illustrated in Section 3, and the conclusion is summarized in Section 4.

2. Circuit Design

2.1. Principle of the HETSM System

As depicted in Figure 2, the recommended HETSM is composed of a high-efficiency SWC parallel with an LA, which has large unity-gain bandwidth (UGB). The high-efficiency SWC is responsible for delivering the primary power, catering to the low-frequency current demands of the PA [16]. Simultaneously, a high-speed, high-slew-rate LA precisely tracks the wideband envelope signal, ensuring the linearity of the PA load. The current of the LA's output stage is mirrored out to generate the SW control (SW Ctrl) signal. Additionally, an external clock is used to control the frequency of the SWC, therefore controlling the efficiency of SWC. In this paper, the proposed HETSM is designed for GaAs PAs, which are powered by fixed drain voltages ranging from 4 V to 6 V. The paralleled $5\ \Omega$ resistor (R_{PA}) and 100 pF capacitor (C_{PA}) are utilized as the equivalent PA load for the LA [19,21].

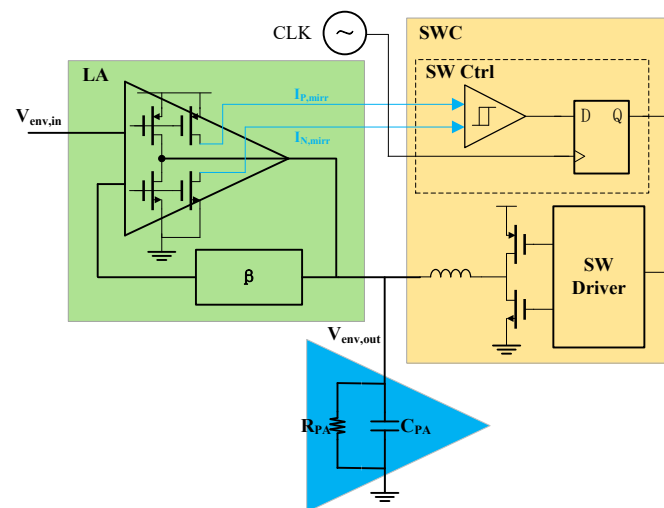


Figure 2. The proposed HETSM diagram.

Assuming that the HETSM system is to track a sinusoidal signal with amplitude A_0 and frequency f_0 , its expression is given in Equation (1):

$$f(t) = A_0 \sin(2\pi f_0 t) \quad (1)$$

Its derivative is shown as Equation (2). Therefore, theoretically, to track the signal $f(t)$, the slew rate needs to reach $2\pi f_0 A_0$.

$$f'(t) = 2\pi f_0 A_0 \cos(2\pi f_0 t) \quad (2)$$

For a GaAs PA load, it is assumed that the maximum supply voltage of the adopted envelope tracking system is 6 V, and the minimum supply is 2 V. Theoretically, according to Equation (2), to track a sinusoidal signal with a peak-to-peak value of 4 V and a frequency of 100 MHz, the slew rate should ideally reach 1257 V/μs. This value is not a practical guiding metric but a theoretical calculation because actual envelope signals are not pure sinusoids. However, it serves as a reference to estimate the required magnitude of the required slew rate.

In this work, a 100 MHz, 16QAM, and 8.49 dB PAPR signal is used for the test. The slew rate distribution of the corresponding envelope signal over a certain period is illustrated in Figure 3. It can be observed that for precise tracking of the envelope signal by the LA, its slew rate should at least exceed ± 800 V/μs and preferably surpass ± 1000 V/μs.

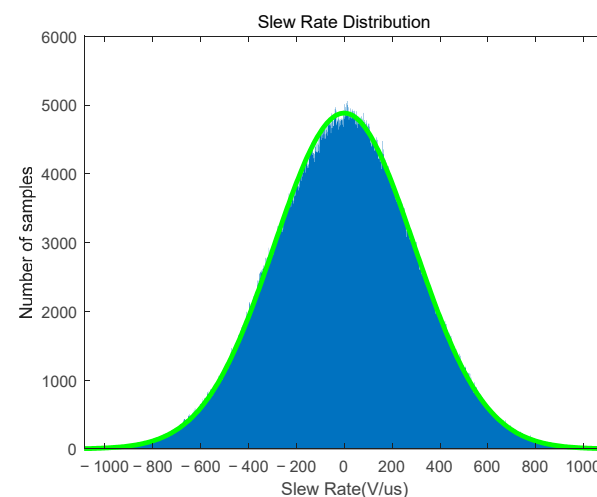


Figure 3. Slew-rate distribution of a 100 MHz, 16QAM envelope signal.

The consumption of the LA P_{Lloss} and the SWC P_{SWloss} forms the consumption of the HETSM. The efficiency of the HETSM can be calculated as:

$$\eta = \frac{P_{out}}{P_{out} + P_{Lloss} + P_{SWloss}} = \frac{1}{1 + \frac{P_{Lloss} + P_{SWloss}}{P_{out}}} \quad (3)$$

For both P_{Lloss} and P_{SWloss} , there is an intrinsic loss, no matter how small the output power is. For the LA, it is called quiescent dissipation, and for the SWC, it is called switching loss. Therefore, it is important to reduce the quiescent current of the LA to improve the efficiency of the HETSM.

2.2. LA Design with an SRE Structure

This paper proposed an LA design assisted by a nonlinear SRE structure, the diagram of which is shown in Figure 4. The nonlinear SRE structure is controlled by the input voltages, V_{INP} and V_{INN} , whose inputs are connected to nodes ① and ②. The input voltage difference, $V_{INP} - V_{INN}$, is converted into nonlinear SRE currents, I_{SRP} and I_{SRN} , through the SRE structure. Due to the Miller compensation, the gates of the output transistors, nodes ③ and ④, become the slew-rate limiting points. Therefore, the output currents of the SRE structure, I_{SRP} and I_{SRN} , are then injected into nodes ③ and ④, accelerating the charging or discharging process of the Miller capacitors (C_1 and C_2).

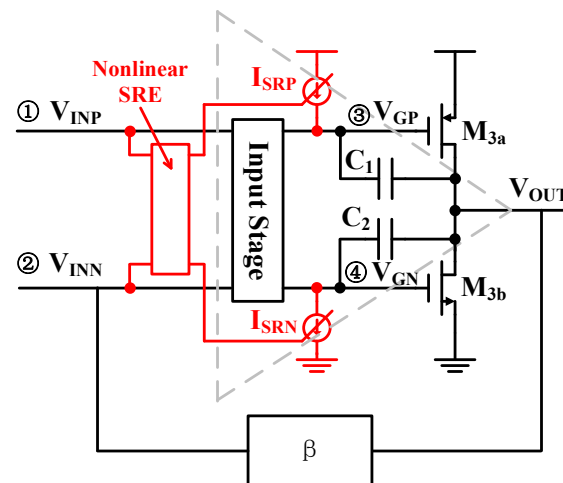


Figure 4. Diagram of the proposed LA design with an SRE structure.

2.2.1. The Proposed SRE Circuit

Figure 5a depicts the overall circuit of the proposed LA with the SRE circuit, which corresponds to the diagram in Figure 4. Figure 5b illustrates the concrete SRE circuit.

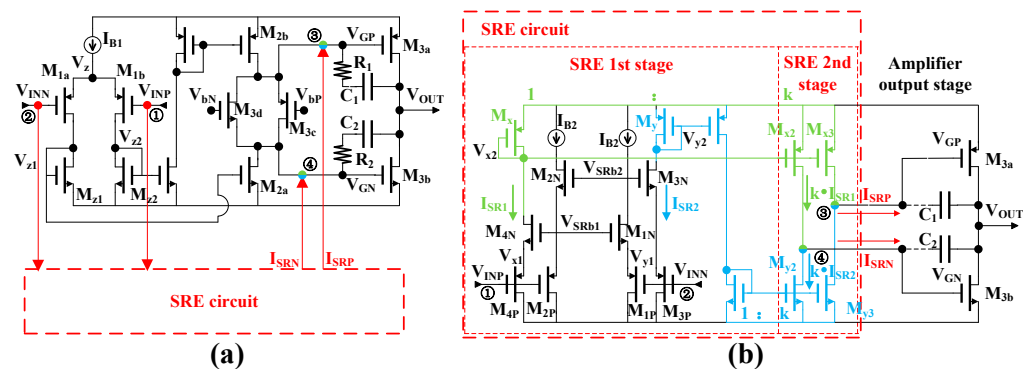


Figure 5. (a) The entire LA circuit. (b) The proposed SRE circuit.

In the first stage of the SRE circuit shown in Figure 5b, the input voltage difference, $V_{INP} - V_{INN}$, is converted into the primary SRE currents, I_{SR1} and I_{SR2} , as demonstrated in the subsequent derivation.

For I_{SR1} , it is determined by the dynamic bias voltage V_{SRb1} and the input voltage V_{INP} , and the dynamic bias voltage V_{SRb1} is determined by the fixed bias current I_{B2} and the input voltage V_{INN} . By observing the branch circuit composed of transistors M_{1P} and M_{1N} , we can obtain Equation (4):

$$V_{SRb1} = V_{INN} + |V_{GS1P}| + V_{GS1N} \quad (4)$$

where:

$$\begin{cases} |V_{GS1P}| = \sqrt{\frac{2I_{B2}}{\mu_P C_{ox}(W/L)_{1P}}} + |V_{thP}| \\ V_{GS1N} = \sqrt{\frac{2I_{B2}}{\mu_N C_{ox}(W/L)_{1N}}} + V_{thN} \end{cases} \quad (5)$$

In Equation (4) and the following equations, V_{GS1P} and V_{GS1N} are the gate-source voltages of transistors M_{1P} and M_{1N} , respectively; $(W/L)_{1P}$ and $(W/L)_{1N}$ are the aspect ratios of transistors M_{1P} and M_{1N} , respectively; μ_P and μ_N are the mobilities of electrons in PMOS transistors and NMOS transistors, respectively; V_{thP} and V_{thN} are the threshold voltages of PMOS transistors and NMOS transistors, respectively; and C_{ox} is the gate oxide capacitance per unit area.

Similarly, by observing the branch circuit composed of transistors M_{4P} and M_{4N} , we can obtain Equation (6):

$$\begin{cases} V_{SRb1} = V_{INP} + |V_{GS4P}| + V_{GS4N} \\ |V_{GS4P}| = \sqrt{\frac{2I_{SR1}}{\mu_P C_{ox}(W/L)_{4P}}} + |V_{thP}| \\ V_{GS4N} = \sqrt{\frac{2I_{SR1}}{\mu_P C_{ox}(W/L)_{4N}}} + V_{thN} \end{cases} \quad (6)$$

Then, by substituting Equation (4) into Equation (6), we can figure out the expression of I_{SR1} , as illustrated in Equation (7).

$$I_{SR1} = \frac{1}{2} \left[\frac{1}{\sqrt{\frac{1}{\mu_P C_{ox}(W/L)_{4P}}} + \sqrt{\frac{1}{\mu_N C_{ox}(W/L)_{4N}}}} (V_{INN} - V_{INP} + \sqrt{\frac{2I_{B2}}{\mu_P C_{ox}(W/L)_{1P}}} + \sqrt{\frac{2I_{B2}}{\mu_N C_{ox}(W/L)_{1N}}})^2 \right] \quad (7)$$

In this design, the dimensions of the transistors satisfy the relationships: $(W/L)_{1P} = (W/L)_{2P} = (W/L)_{3P} = (W/L)_{4P}$, and $(W/L)_{1N} = (W/L)_{2N} = (W/L)_{3N} = (W/L)_{4N}$. Therefore, we can simplify Equation (7):

$$I_{SR2} = \begin{cases} \frac{1}{2} \left(\frac{1}{\sqrt{\frac{1}{\mu_P C_{ox}(W/L)_{1P}}} + \sqrt{\frac{1}{\mu_N C_{ox}(W/L)_{1N}}}} (V_{INN} - V_{INP}) + \sqrt{2I_{B2}} \right)^2, & V_{INP} - V_{INN} \leq V_A \\ 0, & V_{INP} - V_{INN} > V_A \end{cases} \quad (8)$$

where V_A denotes the threshold input voltage difference of the SRE circuit:

$$V_A = \sqrt{\frac{2I_{B2}}{\mu_P C_{ox}(W/L)_{1P}}} + \sqrt{\frac{2I_{B2}}{\mu_N C_{ox}(W/L)_{1N}}} \quad (9)$$

It is worth noting that in Equation (8), when the condition $V_{INP} - V_{INN} \leq V_A$ is satisfied, transistors M_{4P} and M_{4N} are operating in the saturation region. Outside this range, the transistors M_{4P} and M_{4N} are cut off, and as a result, $I_{SR1} = 0$.

Similarly, we can derive the other primary SRE current, I_{SR2} , as illustrated in Equation (10):

$$I_{SR2} = \begin{cases} \frac{1}{2} \left(\frac{1}{\sqrt{\mu_P C_{ox}(W/L)_{1P}} + \sqrt{\mu_N C_{ox}(W/L)_{1N}}} (V_{INP} - V_{INN}) + \sqrt{2I_{B2}} \right)^2, & V_{INP} - V_{INN} \geq -V_A \\ 0, & V_{INP} - V_{INN} < -V_A \end{cases} \quad (10)$$

According to the calculation results, the corresponding curves of the primary SRE currents, I_{SR1} and I_{SR2} , are drawn in Figure 6a. We can see, relative to the value of the quiescent bias current I_{B2} , that the primary SRE currents can be very large when needed.

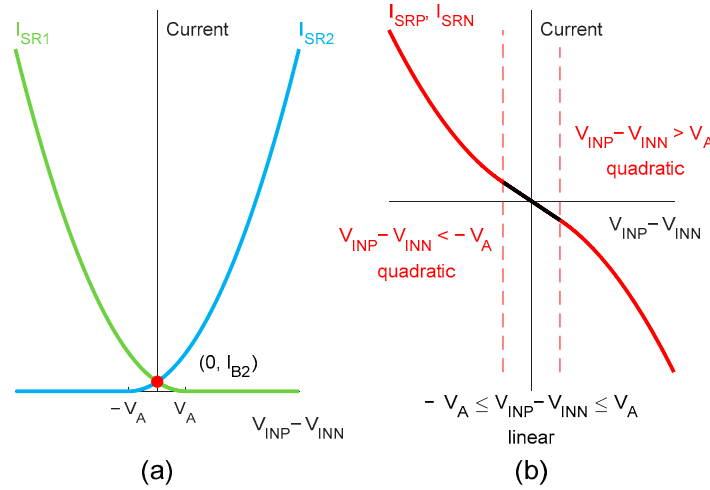


Figure 6. SRE current vs. the input voltage: (a) primary: I_{SR1} and I_{SR2} . (b) Output: I_{SRP} and I_{SRN} .

Then, in the second stage of the SRE circuit shown in Figure 5b, the primary SRE currents, I_{SR1} and I_{SR2} , are amplified k times by current mirrors. Subsequently, they are subtracted to yield the output SRE currents, I_{SRP} and I_{SRN} , as shown in Equation (11).

$$I_{SRP} = I_{SRN} = k(I_{SR1} - I_{SR2}) \quad (11)$$

By substituting Equations (8) and (10) into Equation (11), we obtain the complete expression of the output SRE currents:

$$I_{SRP} = I_{SRN} = \begin{cases} \frac{k}{2} \left(\frac{1}{\sqrt{\mu_P C_{ox}(W/L)_{1P}} + \sqrt{\mu_N C_{ox}(W/L)_{1N}}} (V_{INN} - V_{INP}) + \sqrt{2I_{B2}} \right)^2, & V_{INP} - V_{INN} < -V_A \\ \frac{2k\sqrt{2I_{B2}}}{\sqrt{\mu_P C_{ox}(W/L)_{1P}} + \sqrt{\mu_N C_{ox}(W/L)_{1N}}} (V_{INN} - V_{INP}), & -V_A \leq V_{INP} - V_{INN} \leq V_A \\ -\frac{k}{2} \left(\frac{1}{\sqrt{\mu_P C_{ox}(W/L)_{1P}} + \sqrt{\mu_N C_{ox}(W/L)_{1N}}} (V_{INP} - V_{INN}) + \sqrt{2I_{B2}} \right)^2, & V_{INP} - V_{INN} > V_A \end{cases} \quad (12)$$

Therefore, we can draw the corresponding curve of the output SRE currents, I_{SRP} and I_{SRN} , respectively, in Figure 6b. When the slew rate of the input signal at node ① in Figure 5 is small, the input voltage difference, $V_{INP} - V_{INN}$, is small. From Equation (12) and Figure 6b, we notice that when $V_{INP} - V_{INN}$ is small, which satisfies $|V_{INP} - V_{INN}| \leq V_A$, the SRE currents, I_{SRP} and I_{SRN} , linearly increase with $V_{INP} - V_{INN}$. Especially when $V_{INP} - V_{INN} = 0$, we have $I_{SRP} = I_{SRN} = 0$. In this case, the SRE circuit does not modify the operating point of the remaining LA. When the slew rate of the input signal becomes large, the LA converts from the linear amplification state to the transition state, and the input voltage difference $V_{INP} - V_{INN}$ grows, due to the difficulty of input signal tracking. The corresponding SRE currents, I_{SRP} and I_{SRN} , will quadratically grow with the enlarged input voltage difference. These additionally injected SRE currents can effectively increase the slew rate of the output voltage while maintaining a low quiescent current level.

The operating conditions of the transistors and the current flow during the transition state are shown in Figure 7. When $V_{INP} < V_{INN}$, as shown in Figure 7a, the differential pair transistor M_{1a} is turned off, and all of the tail current I_{B1} flows through transistor M_{1b} . Additionally, the current I_{2b} running through transistor M_{2b} reaches its maximum value I_{B1} , while transistor M_{2a} is turned off with no current passing through. The current I_{2b} is split into two parts: I_{2bP} charges compensation capacitor C_1 , and I_{2bN} discharges compensation capacitor C_2 . Then, the gate voltages of the push–pull output stage's transistors V_{GP} (at node ③) and V_{GN} (at node ④) increase, causing the output voltage V_{OUT} to decrease. Because the change in V_{OUT} is much greater than the changes in V_{GP} and V_{GN} , the charge and discharge rates of C_1 and C_2 will determine the slew rate of the output voltage V_{OUT} . The proposed SRE circuit injects additional nonlinear SRE currents, I_{SRP} and I_{SRN} , into nodes ③ and ④, respectively, which effectively enhances the slew rate. When $V_{INP} > V_{INN}$, as illustrated in Figure 7b, a similar situation occurs.

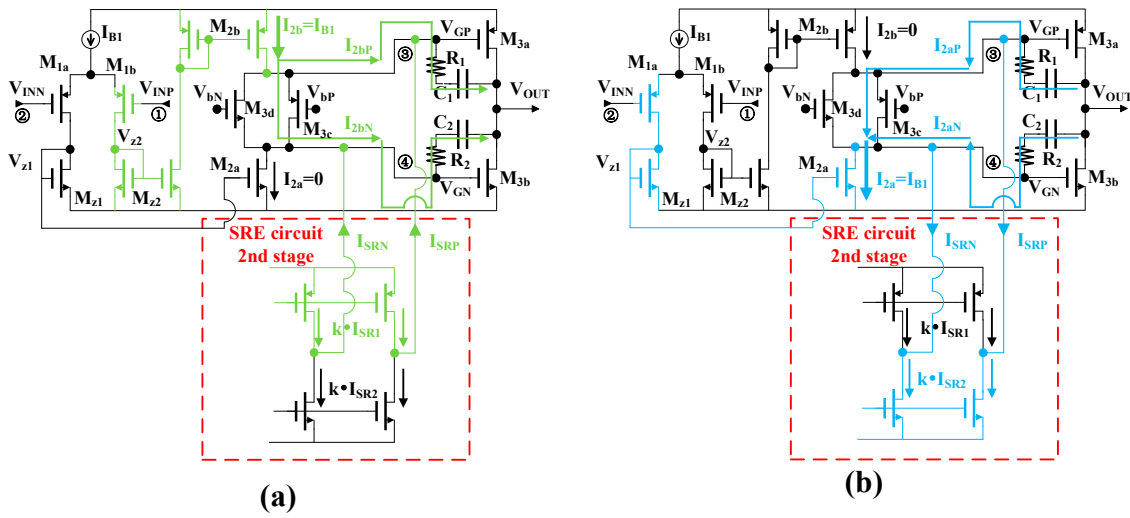


Figure 7. Transition state: (a) $V_{INP} < V_{INN}$ and (b) $V_{INP} > V_{INN}$.

2.2.2. AC Analysis of the LA with the Proposed SRE Circuit

The SRE circuit in Figure 5b can be extracted to a corresponding small-signal model, as shown in Figure 8. In the small-signal models below, unless otherwise specified, g_{mi} , R_{Oi} , and C_i are used to represent the transconductance g_m , output resistance r_{ds} , and output capacitance C_d of transistor M_i , respectively, where i denotes the subscript of the transistor. Due to the symmetrical design of the circuit, we have $g_{m3P} = g_{m4P}$ and $g_{m3N} = g_{m4N}$. The small-signal model in Figure 8 can be simplified to a one-stage amplifier model within the red dashed box in Figure 9. We can derive the relationship given in Equation (13):

$$\begin{cases} g_{mSR} = 2k \frac{g_{m3P}g_{m3N}}{g_{m3P} + g_{m3N}} \\ R_{OSRP} = R_{Ox2} || R_{Oy2}, R_{OSRN} = R_{Ox3} || R_{Oy3} \\ C_{SRP} = C_{x2} + C_{y2}, C_{SRN} = C_{x3} + C_{y3} \end{cases} \quad (13)$$

The detailed derivation process of the small-signal LA model is provided in Supplementary Material.

As derived in Supplementary Material, we can combine the input stage of LA with the SRE circuit to simplify it into the first-stage amplification circuit model shown on the left side of Figure 10. We can derive the relationship shown in Equation (14):

$$\begin{cases} g_{m1} = g_{mSR} + g_{m1Conv} = 2k \frac{g_{m3P}g_{m3N}}{g_{m3P} + g_{m3N}} + \frac{g_{m1a}g_{m1b}}{g_{m1a} + g_{m1b}} \\ R_{O1P} = R_{OSRP} || R_{O2b}, R_{O1N} = R_{OSRN} || R_{O2a} \\ C_{1P} = C_{SRP} + C_{2b} + C_{gs3a}, C_{1N} = C_{SRN} + C_{2a} + C_{gs3b} \end{cases} \quad (14)$$

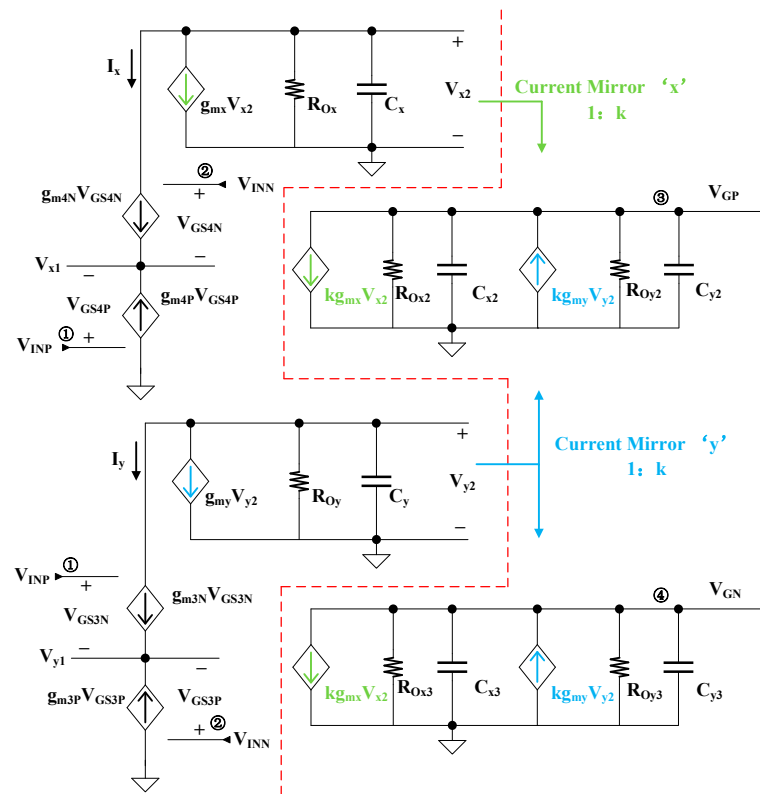


Figure 8. A small-signal model of the SRE circuit.

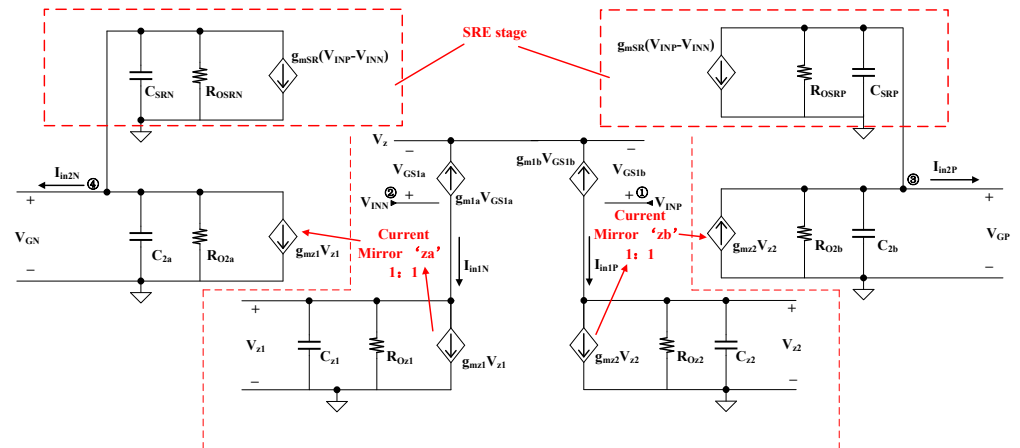


Figure 9. A small-signal model of the proposed LA's input stage.

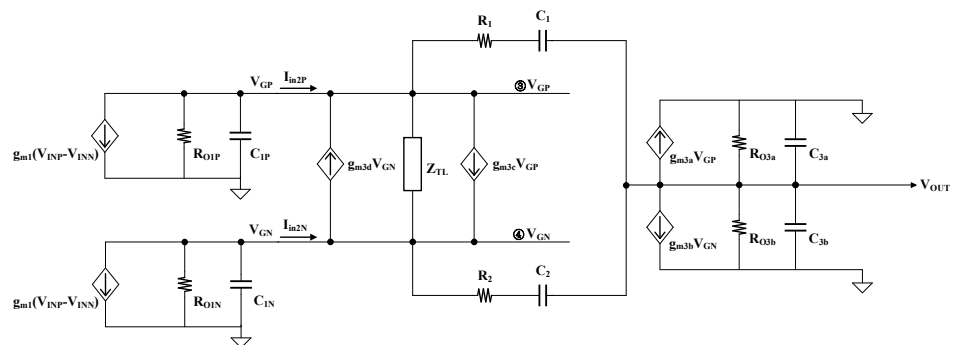


Figure 10. The small-signal model of the entire LA.

The small-signal model of the entire LA after the aforementioned simplification process is shown in Figure 10. If we incorporate the following steps into the LA design, we can achieve symmetry in the circuit to a large extent:

- (1) Let $k_{NP} = \frac{R_{O1N}}{R_{O1P}}$.
- (2) Select the sizes of M3a and M3b, such that $C_{1P} = k_{NP}C_{1N}$.
- (3) Choose the R1/C1 and R2/C2 that satisfy the relation.

Specifically, when $R_{O1N} = R_{O1P}$, we have $k_{NP} = 1$. In this case, we derive that $V_{GP} - V_{GN} = 0$. When $V_{GP} = V_{GN}$, the effects of M_{3c} and M_{3d} cancel each other out because the current $g_{m3d}V_{GN}$ is equal to the current $g_{m3c}V_{GP}$, as shown in Figure 10, and the current through the impedance Z_{TL} equals zero.

Then, due to symmetry, the LA circuit can be simplified to that shown in Figure 11. We find that the small-signal model of the proposed amplifier can be simplified to the well-known two-stage operational amplifier model, simply by substituting the parameters with those in parentheses shown in Figure 11. We can derive the relationship shown in Equation (15):

$$\begin{cases} g_{mI} = 2g_{m1} = 4k \frac{g_{m3P}g_{m3N}}{g_{m3P} + g_{m3N}} + 2 \frac{g_{m1a}g_{m1b}}{g_{m1a} + g_{m1b}} \\ R_I = R_{O1N} || R_{O1P} = (R_{OSRN} || R_{O2a}) || (R_{OSRP} || R_{O2b}) \\ C_I = C_{1P} + C_{1N} = (C_{SRP} + C_{2b} + C_{gs3a}) + (C_{SRN} + C_{2a} + C_{gs3b}) \\ R_c = R_1 || R_2, C_c = C_1 || C_2 \\ g_{mII} = g_{m3a} + g_{m3b} \\ R_{II} = R_{O3a} || R_{O3b}, C_{II} = C_{3a} + C_{3b} + C_L \end{cases} \quad (15)$$

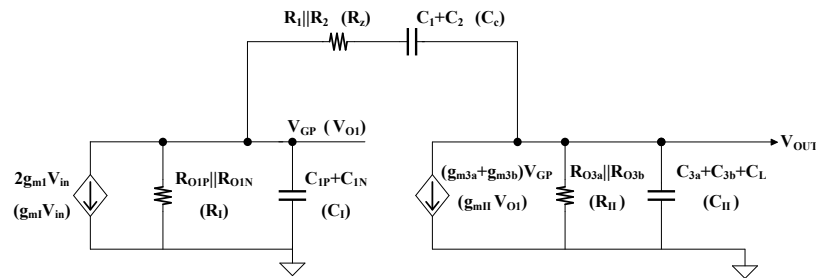


Figure 11. The simplified model of the entire LA.

If the poles are widely spaced, then we can derive the expressions for the zeroes and poles as follows:

$$\begin{cases} p_1 \cong \frac{-1}{g_{mII} R_{II} R_I C_c} \\ p_2 \cong \frac{-g_{mII}}{C_{II}} \\ p_3 = \frac{-1}{R_z C_I} \\ z_1 = \frac{1}{C_c (1/g_{mII} - R_z)} \end{cases} \quad (16)$$

In the AC analysis, the recommended SRE circuit is equivalent to a stage that is parallel to the input stage of the amplifier and can be integrated into the input stage circuit. Therefore, when selecting the compensation capacitor and resistor to adjust the stability of the amplifier, the impact of the SRE circuit must be considered.

In the recommended LA, the slew rate is determined by Equation (17):

$$SR = \frac{I_{B1} + I_{SRP}}{C_1} \quad (17)$$

In the transition state, is much greater than the static current parameter I_{B2} related to the SRE circuit. The recommended LA in our work can achieve a high slew rate with low quiescent power consumption.

The UGB of the proposed LA can be expressed as:

$$UGB \cong \frac{g_{mI}}{C_c} = \left(4k \frac{g_{m3P}g_{m3N}}{g_{m3P} + g_{m3N}} + 2 \frac{g_{m1a}g_{m1b}}{g_{m1a} + g_{m1b}} \right) \frac{1}{C_1 + C_2} \quad (18)$$

Observing Figure 5, we can determine the expression of the quiescent current of the LA:

$$I_Q = (2I_{B1} + I_{Q_{3a}}) + (5I_{B2} + 2kI_{B2}) \quad (19)$$

where $I_{Q_{3a}}$ is the quiescent current of the output stage.

Based on the design targets for UGB and the slew rate, through multiple iterations, we are seeking a design solution that minimizes quiescent power consumption.

2.2.3. Simulation Results

To better understand the effectiveness of the proposed SRE circuit, we compared the simulated LA performances with and without the SRE circuit. As shown in Figure 12, the proposed SRE structure increased the rise slew rate from 122.2 V/μs to 2320 V/μs and the fall slew rate from 178.5 V/μs to 1907 V/μs.

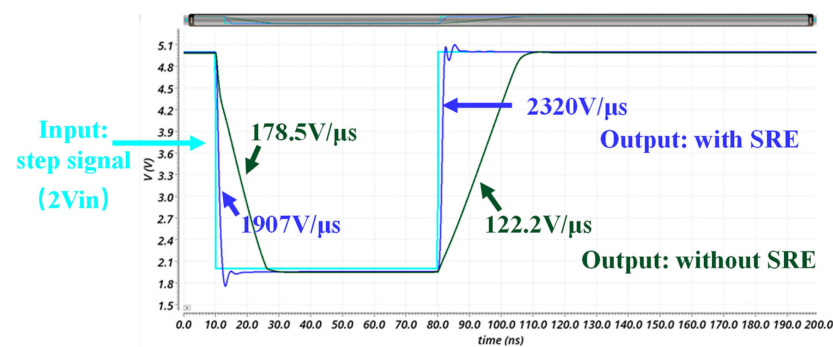


Figure 12. The simulated step response of the LA with the proposed SRE structure.

As shown in Figure 13, the UGB of the proposed LA was 226.6 MHz, which is four times the one without the SRE circuit.

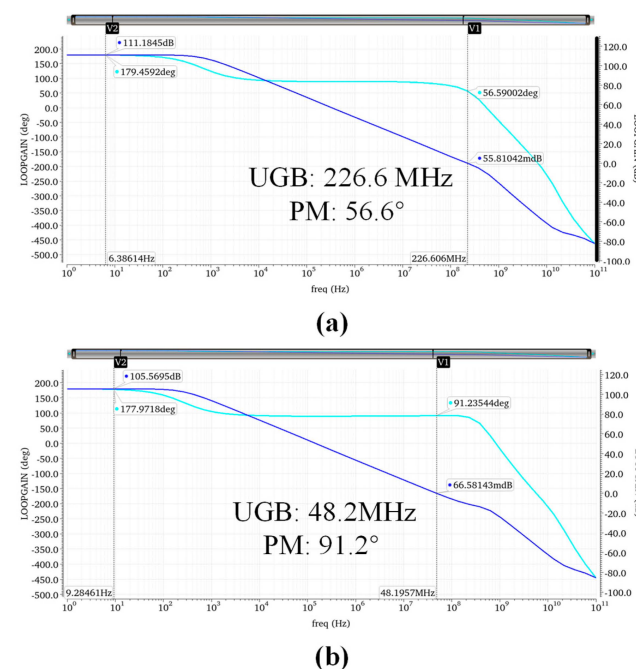


Figure 13. Loop gain of the LA (a) with the proposed SRE structure and (b) without SRE.

Table 1 shows more details of the comparison between the proposed LA and the conventional LA. The proposed SRE circuit brought about an increase in the slew rate of over tenfold, while the quiescent current only increased by 50%.

Table 1. Simulation results of the proposed LA and the conventional LA.

Design	Conventional LA (Without SRE)	The Proposed LA (With SRE)
UGB (MHz)	48.2	226.6
Phase Margin (°)	91.2	56.6
DC Gain (dB)	105.6	111.2
Slew Rate ($V/\mu s$)	−178.5/+122.2	−1907/+2320
Quiescent Current (mA)	16.2	24

To ensure the robustness of the design, simulations were conducted under different process corners and temperatures. The results are shown in Table 2.

Table 2. Performance of LA under different process corners and temperature conditions.

Process	Temperature (°C)	DC Gain (dB)	Phase Margin (°)	UGB (MHz)	Quiescent Current (mA)	Positive Slew Rate (V/us)	Negative Slew Rate (V/us)
ff lib	−40	117	62	209.7	20.1	4311	−3246
	25	108.8	61.3	216.9	26.2	3513	−3738
	85	96.9	60.7	213.3	32.3	1908	−1920
tt lib	−40	118.3	65.3	212.6	19.5	3268	−2454
	25	111.4	58.9	228.6	26.0	2583	−1926
	85	101.8	54.3	227.4	32.3	2034	−1378
ss lib	−40	116.6	62.4	200.5	21.3	2222	−1775
	25	108.5	54.1	202	29.5	1747	−1345
	85	93.8	67.9	153.5	37.4	1325	−983

As we can see, the UGB of the LA was greater than 200 MHz in most cases, and based on the phase margin criteria, the stability of the LA was ensured. The quiescent current increased as the temperature rose. In the worst case (slow process corner and 85°C), the slew rate of the LA still reached approximately 1000 V/ μs .

3. Experimental Results

The proposed HETSM chip was fabricated on a 180 nm CMOS process, of which the die size was 1.98 mm $\times$ 0.9 mm, as depicted in Figure 14. The chip was operating under a 6.5 V power supply, with an off-chip inductor of 4.7 μH .

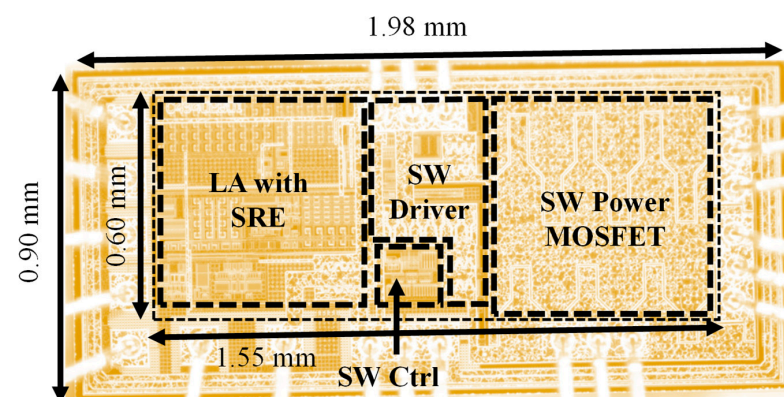


Figure 14. The micrograph of the proposed HETSM.

Figure 15 shows the measured waveforms for a 100 MHz signal, with a 16QAM modulation and an 8.49 dB PAPR. The external clock frequency was set to 20 MHz. The input envelope signal, output signal, and switching node voltage are shown in the figure. The HETSM amplified the amplitude of the input signal by a factor of 2, with an output signal delay of 7.5 ns.

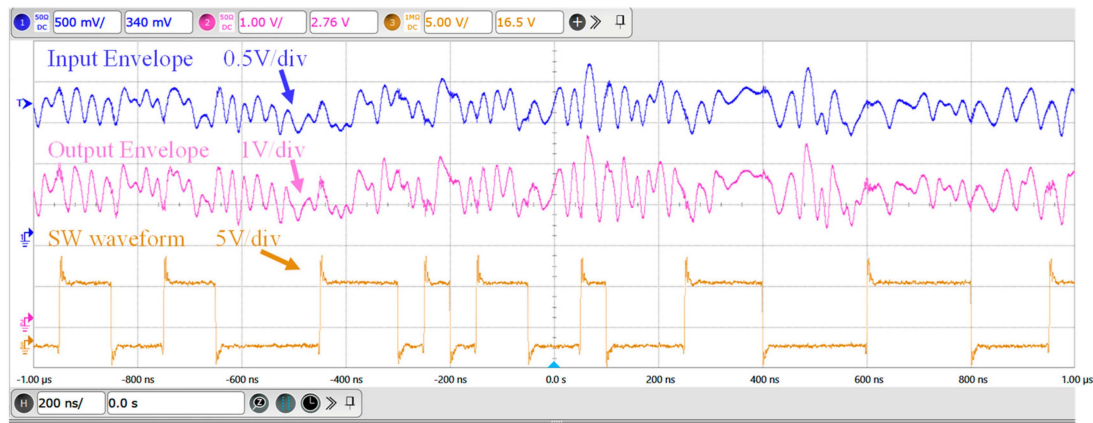


Figure 15. The measured transient response of the ET modulator to the 100 MHz envelope signal.

Figure 16 illustrates the measured step response waveform of the proposed LA with the SRE circuit. A 100 pF capacitor was connected to the output of LA as a capacitive load. The rise time slew rate was measured at $1239 \text{ V}/\mu\text{s}$, while the fall time slew rate was measured at $-1857 \text{ V}/\mu\text{s}$.



(a)



(b)

Figure 16. Measured step responses of the proposed LA with the SRE circuit: (a) fall condition and (b) rise condition.

Figure 17 presents the measured efficiency of the HETSM chip with a $5\ \Omega$ load paralleled with a 100 pF capacitor. For the 100 MHz, 16QAM, and 8.49 dB PAPR signal, the peak efficiency reached 87.4%. When the output power was small, the ratio of these intrinsic losses to the output power was relatively large. According to Equation (3), the efficiency was relatively small under low-power conditions for the large value of the aforementioned ratio, as shown in Figure 17.

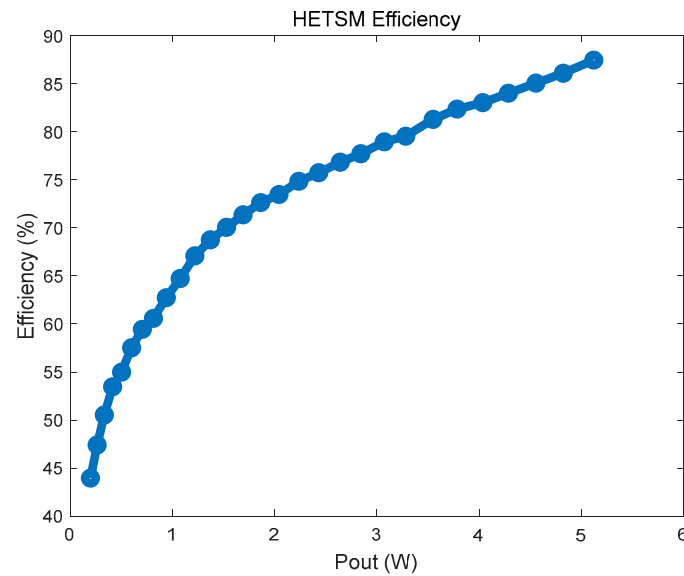


Figure 17. Measured efficiency of the HETSM chip with the 100 MHz envelope signal.

Figure 18 shows the measured error between the output voltage and the ideal output voltage when tracking the 100 MHz, 16QAM envelope signal. The tracking error was less than 3%.

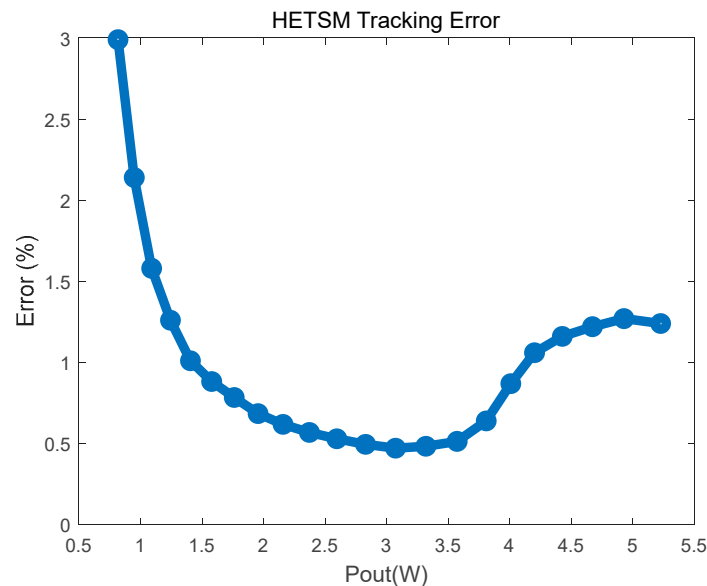


Figure 18. Measured tracking error between the output and the ideal output voltage with the 100 MHz envelope signal.

The comparison of the proposed HETSM with prior works is shown in Table 3. Our work showed the highest slew rate of LA and adapted the 100 MHz wideband signal tracking. Also, it achieved 87.4% efficiency, which is comparable to prior works. The

proposed HETSM provided a maximum voltage of 6 V, which can accommodate GaAs PA applications.

Table 3. Performance comparison with prior works.

Design	Process (nm)	Signal Bandwidth(MHz)	PAPR (dB)	Die Area (mm ²)	LA Architecture	Max ET Voltage (V)	Load Conditions	Slew Rate of LA (V/ μ s)	Max Tracking Error	I_Q of LA (mA)	Max Efficiency of ET System
JSSC2019 [9]	65	LTE 40/80	7.84@40 MHz 8.06@80 MHz	total: $2 \times 2 = 4$ core: $1.6 \times 2.4 = 2.72$	parallel current-mirror SRE path	2.4	4.7 Ω	−307/+325	2.3%@40 MHz 3.2%@80 MHz	NA	93%@40 MHz 91%@80 MHz
MTI2017 [20]	180	LTE 10	7.24	core: $1.05 \times 1.05 = 1.1$	adaptive biasing using the FVF structure	3.4	6 Ω 150 pF	−152.5/+93.4	NA	14	83%
IEICE2020 [21]	180	LTE 10	6	total: $1.55 \times 0.8 = 1.24$ core: 0.78	enhanced current-mirror structure	3	5–20 Ω	−160/+220	1.5%	12	83%
this work	180	100 (16QAM)	8.49	total: $1.98 \times 0.9 = 1.79$ core: $1.55 \times 0.6 = 0.93$	parallel nonlinear current-SRE path	6	5 Ω 100 pF	−1857/+1239	3%	24	87.4%

4. Conclusions

In this work, we designed an HETSM with a slew-rate-enhanced LA. The proposed SRE structure introduced a parallel auxiliary current path directly to the gate of the output stage, significantly accelerating the charging and discharging processes of the Miller capacitor without modifying the operating point of the remaining LA. Assisted by the quadratically growing SRE current, the proposed LA with the SRE circuit achieved a high slew rate and a large bandwidth under low quiescent current conditions. The presented HETSM chip was fabricated using the 180 nm CMOS process. The proposed LA with the SRE circuit achieved a slew rate of 1239 V/ μ s for rising edges and −1857 V/ μ s for falling edges at a quiescent current of 24 mA. Therefore, it established a solid foundation for ET modulators to track the wideband envelope signal. The proposed HETSM achieved a maximum efficiency of 87.4% while tracking a 100 MHz, 16QAM, and 8.49 dB PAPR signal.

Supplementary Materials: The following supporting information can be downloaded at: <https://www.mdpi.com/article/10.3390/electronics13142701/s1>, Document S1: “AC analysis of the linear amplifier (LA) with the proposed SRE circuit”.

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