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Mobility Extraction Using Improved Resistance Partitioning Methodology for Normally-OFF Fully Vertical GaN Trench MOSFETs

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Abstract: In this work, fully vertical GaN trench MOSFETs were fabricated and characterized to evaluate their electrical performances. Transistors show a normally-OFF behavior with a high I_{ON}/I_{OFF} (~10^9) ratio and a significantly small gate leakage current (10^{-11} A/mm). Thanks to an improved resistance partitioning method, the resistances of the trench bottom and trench channel were extracted accurately by taking into account different charging conditions. This methodology enabled an estimation of the effective channel and bottom mobility of 11.1 $cm^2/V{\cdot}s$ and 15.1 $cm^2/V{\cdot}s$, respectively.

Keywords: GaN; MOSFET; vertical device; resistance partitioning

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Citation: Ackermann, V.; Mohamad, B.; El Rammouz, H.; Maurya, V.; Frayssinet, E.; Cordier, Y.; Charles, M.; Lefevre, G.; Buckley, J.; Salem, B. Mobility Extraction Using Improved Resistance Partitioning Methodology for Normally-OFF Fully Vertical GaN Trench MOSFETs. *Electronics* **2024**, *13*, 2350. https://doi.org/10.3390/electronics13122350

Academic Editors: Yimeng Zhang, Yuming Zhang and Lejia Sun

Received: 19 May 2024
Revised: 11 June 2024
Accepted: 12 June 2024
Published: 15 June 2024

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1. Introduction

Over recent years, vertical gallium nitride (GaN) power transistors have demonstrated increasing potential for efficient power switching applications. The wide-bandgap GaN material is known to have superior intrinsic material properties over its silicon (Si) and silicon carbide (SiC) material counterpart. Indeed, its larger critical electric field, higher electron mobility, and higher saturation velocity favor the technological development of high breakdown voltage and low on-state resistance devices. In addition, the vertical topology is expected to be more adapted for high-power switching applications compared to the lateral one (like the HEMT), due to its capability of reaching higher breakdown voltages, its robustness to high electric fields, and its potentially higher power capability.

Nowadays, different vertical technology concepts have been under development, such as the CAVET [1,2], the semipolar gate structure [3], the fin-FET [4], or the well-known vertical power trench MOSFET [5–7]. Among these architectures, the vertical power trench MOSFET shows even higher potential regarding the benefits granted by MOS gate technology (high switching capability, low gate leakage current, gate robustness to voltage overshoot...).

To improve its quality (and also its control), different research groups have tried to fabricate vertical GaN trench MOSFETs and study the effects of MOS gate module variation on the devices' electrical performance (p-GaN doping [8], GaN trench surface optimization [9,10], GaN trench orientation [7,11], gate stack comparison [12–14]). Some studies have demonstrated, for instance, groundbreaking results with devices showing adequate normally-OFF operation (V_{th} ~ 3–8 V [5,7]), very low $R_{ON,sp}$ (<10 $m\Omega.cm^2$ [6,7]), a high I_{ON}/I_{OFF} ratio (~10^9), a significantly low gate leakage current (<10^{-11} $A.mm^{-1}$

for instance), as well as encouraging channel mobility results (~10–130 $cm^2/V{\cdot}s$ [5,7]). However, for the latter key parameter, the common methodology used in the literature to estimate it is based on the calculation of the transconductance, extracted from the transfer characteristic in the MOSFET linear stage of operation [7,10]. While this method allows us to easily extract the effective field-effect mobility on a single device, its main drawback is that it overestimates the channel mobility value considering the drift layer mobility contribution in the output current value during the mobility calculation.

On the other hand, mobility extraction methods related to the more mature lateral recessed MOS-HEMT use either the transconductance method [15,16], the Y-function method [17], or the resistance partitioning one [18,19]. For the latter method, the resistance and effective mobility are evaluated for the trench bottom and trench sidewalls separately. To do so, sheet resistance and carrier density of the different trench regions must be evaluated under the assumption of a uniform carrier density and identical electrostatic behavior between the trench bottom and trench sidewall. While this methodology can be used in the case of a lateral recessed MOS-HEMT, it is not the case for a vertical GaN MOSFET since it does not take into account the difference in electrostatic behavior between the n^- GaN trench bottom and the p-GaN trench sidewall is this technology.

In this study, we present an improved methodology that aims to separate the resistance contributions in the trench region and then extracts the effective mobilities of the trench channel and trench bottom. Firstly, the fabrication and electrical characterization of fully vertical GaN trench MOSFETs are reported. The transistors' key parameters are extracted by means of vertical I-V and C-V measurements, showing devices with a threshold voltage V_{th} of ~1 V, a significantly small gate leakage I_G (10^{-11} A/mm), and adequate switching capability ($I_{ON}/I_{OFF} \sim 10^9$). Then, using an improved resistance partitioning methodology that takes into account the difference in electrostatic behavior between the trench bottom and trench channel, we evaluate the effective mobilities of both of these areas as being 15.1 $cm^2/V{\cdot}s$ and 11.1 $cm^2/V{\cdot}s$, respectively.

2. Materials and Methods

The epitaxy layers were grown on a free-standing (FS) 2-in n-type GaN wafer using metal–organic vapor phase epitaxy (MOVPE). From bottom to top, the different doped GaN layers were grown as follows: 100 nm n^+ GaN drain layer (Si, 1×10^{19} cm^{-3}), 10 µm n^- GaN drift layer (Si, 1×10^{16} cm^{-3}), 700 nm p-GaN (Mg, $N_A - N_D = 3.5 \times 10^{18}$ cm^{-3}), and 200 nm n^+ GaN source layer (Si, 6×10^{18} cm^{-3}).

The process flow starts with the deposition of a 1 µm SiO_2 hardmask by PECVD. Then, the drain contact is fabricated with a Ti/Al/Ni/Au metal stack deposited on the wafer backside by e-beam evaporation. The deposition is followed by rapid thermal annealing (RTA) at 750 °C in N_2 atmosphere for 3 min 30 s.

The process continues with the patterning through photolithography of the GaN gate trench and a mesa structure that will terminate the n-p-n heterostructure. Firstly, the resist pattern is transferred into the hardmask by performing CF4 dry etching in an inductive couple plasma reactor (ICP-RIE). Secondly, the GaN trenches and the mesa are etched to a depth of 1.1 µm through the epi layers by ICP-RIE using a Cl_2 dry-etch process. Afterwards, 10 min RTA at 600 °C in O_2 atmosphere is performed for p-GaN layer activation.

To reduce the etch-induced damages and remove the etch residues on the trench sidewalls, a HCl pre-deposition wet surface treatment is applied to the sample for 4 min at an ambient temperature. Immediately after this step, 20 nm of thermal Al_2O_3 is deposited by ALD at 300 °C using a trimethylaluminium (TMA) precursor and H_2O vapor oxidant for the deposition. A total of 40 nm of TiN is then deposited as the gate metal through sputtering. To finalize gate fabrication, the metal gate is patterned and etched on top of the mesa structures by ion beam etching (IBE). Finally, 3 min RTA at 400 °C in N_2 is performed on the sample.

The process flow is followed by the fabrication of the source contacts. A dry-etch fluorocarbide process is used to open the gate oxide as well as the SiO_2 hardmask in the

source contact region. The source contact is made of a Ti/Al metal stack defined by a lift-off step to finalize MOSFET processing.

A schematic diagram of a processed vertical MOSFET along with its top-view SEM image is shown in Figure 1a. As can be seen, the resulting MOS gate is located inside the trench as well as all around the mesas, as a consequence of the deposition and etching steps of the gate dielectric and gate metal. The dimension of the expected gate trench width (W_{tr}) varies from 1 to 6 µm depending on the device studied. In addition to these test structures, planar capacitors located on the drift layer are also included in the initial layout, as illustrated in Figure 1.

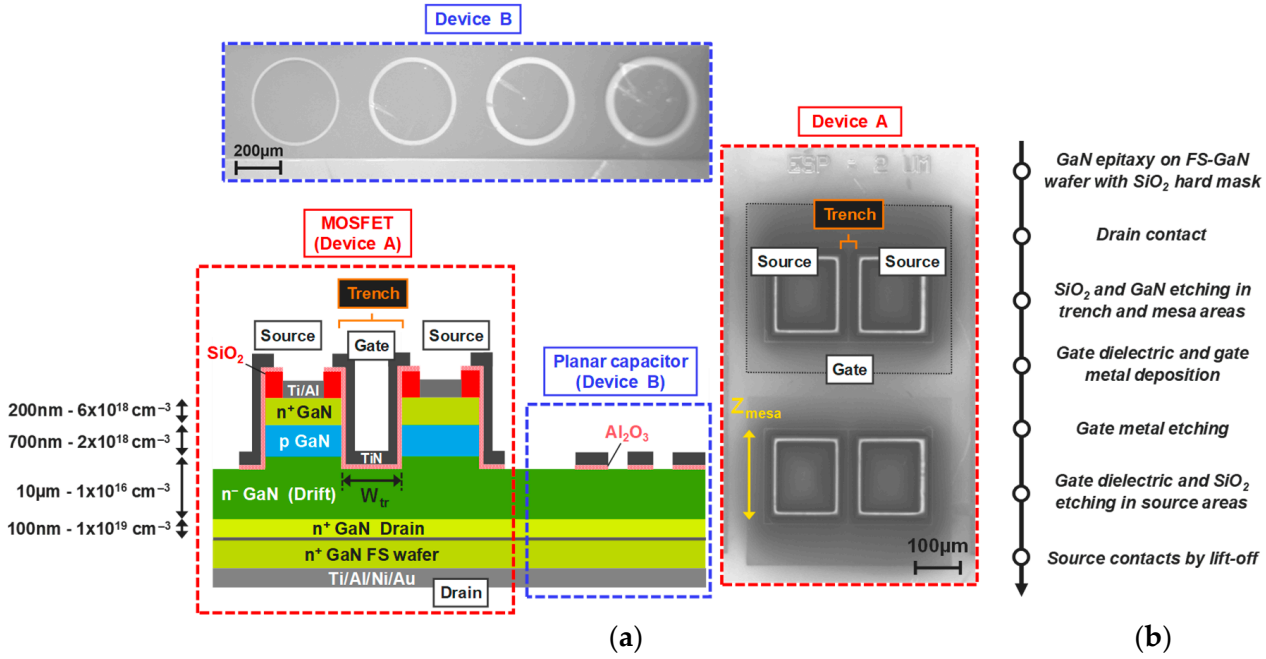


Figure 1. (**a**) A cross-sectional schematic of a given processed vertical MOSFET (device A) and planar capacitor (device B) test structures, each device being linked to their top-view SEM image (**b**). The main process flow steps to fabricate the vertical MOSFETs and planar capacitor test structures.

The high-angle annular dark field (HAADF)-STEM image in Figure 2a shows the gate of a given processed trench MOSFET. While the dielectric and gate metal deposited seems sufficiently conformal with the GaN surface, etch-induced non-uniformities can still be observed along the trench sidewalls, as observed in Figure 2b.

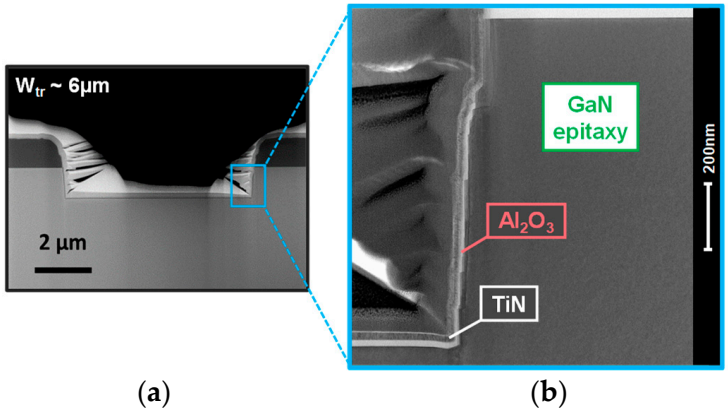


Figure 2. HAADF-STEM images of (**a**) the cross-section of a given vertical MOSFET and (**b**) the right trench sidewall of the device.

3. Results and Discussion

The transfer characteristics of a given fully vertical MOSFET are shown in Figure 3, with the current values normalized to the mesa width (Z_{mesa}, cf. Figure 1a). The transfer characteristic on a linear scale (Figure 3a) confirms the transistor behavior and demonstrates the normally-OFF switching operation of the device with a threshold voltage (V_{th}) of ~1 V, determined through extrapolation of the linear region of the characteristic at V_D = 2 V (correlation factor *r* of the fitting as being around ~1). As shown in Figure 3b, the device demonstrates a good ON/OFF current ratio of 10^9 and a significantly low gate leakage current of 10^{-11} A/mm, indicating the benefits of both the n-p-n heterostructure and the MOS gate building blocks. The value of the subthreshold slope calculated is around ~139 mV/dec.

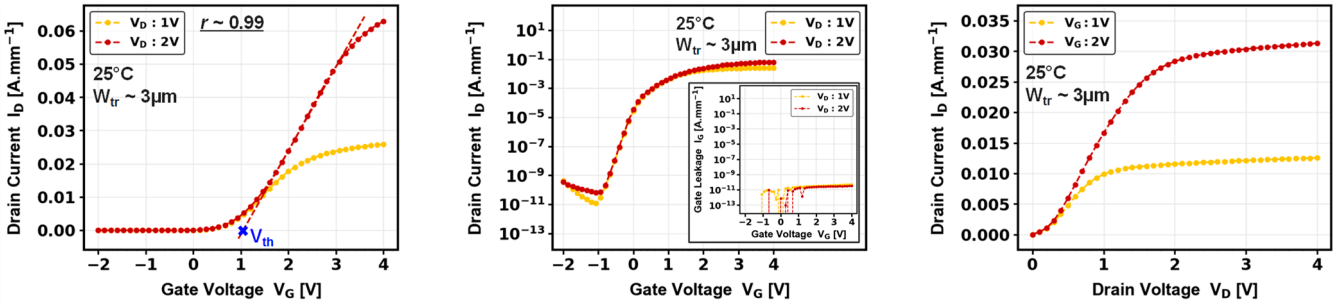


Figure 3. (**a**) Linear and (**b**) semi-log transfer characteristics: gate leakage current versus applied gate voltage; (**c**) output characteristics of given vertical GaN-on-GaN MOSFET.

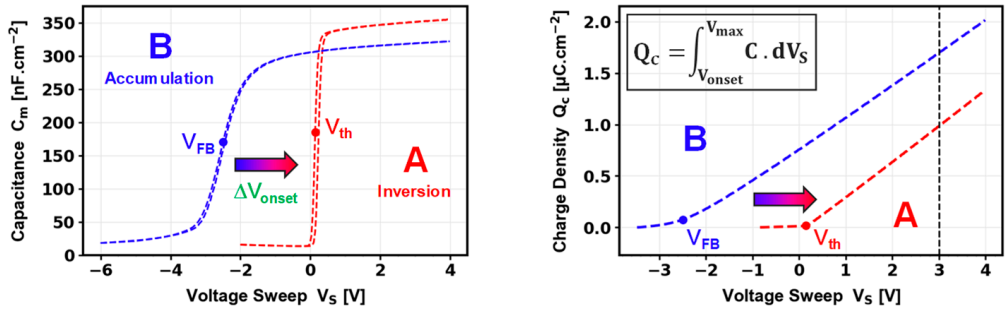
Focusing on the V_{th} value, different hypotheses can be made to explain its origins. In our case, this V_{th} result could be related to the thinner gate dielectric (~20 nm) compared to what can be found in previous works (80–100 nm [6,7,20]). Also, the presence of a positive charge density trapped at the dielectric/GaN interface or inside the dielectric bulk could have a detrimental effect on the V_{th} by shifting it toward negative values [21–23], thus reducing the V_{th} of the device. Finally, the issue of the insufficient electrically activated Mg doping concentration is still a major process concern nowadays, since a low Mg doping concentration drastically reduces the V_{th} value [6,8,24].

The normalized C-V curves related to both the MOSFET and planar capacitor are illustrated in Figure 4a. Firstly, a different capacitance behavior is clearly noticed as device A is based on charge inversion and device B on charge accumulation. Consequently, a higher V_{th} is observed for device A compared to the V_{FB} for device B. This result can be explained due to the p-type GaN layer integrated into the MOSFET heterostructure that should enhance the work function of the GaN and thus enhance the V_{FB}. A small hysteresis of ~100 and ~47 mV is shown for device A and B, respectively, suggesting a dielectric/GaN interface of good quality, despite the sidewall macroscopic roughness observed in Figure 2b.

Since the capacitance is by definition related to a variation in charge with the applied voltage V_S, one can calculate the charge density (Q_c) simply by combining the capacitance from the onset voltage value V_{onset} (defined either by V_{FB} (device B) or V_{th} (device A)) with the maximum voltage value V_{max} of the applied voltage sweep, as described in Equation (1):

$$Q_c = \int_{V_{onset}}^{V_{max}} C.dV_S \quad (1)$$

Thus, Figure 4b represents the calculated charge density as a function of the applied voltage. Since the onset of the charge inversion (V_{th} ~ 0.14 V) in the channel regions for device A occurs at a different gate voltage than the charge accumulation in the bottom region (V_{FB} ~ −2.64 V), a difference in charge densities is clearly noticed at a given voltage value.



(**a**) (**b**)

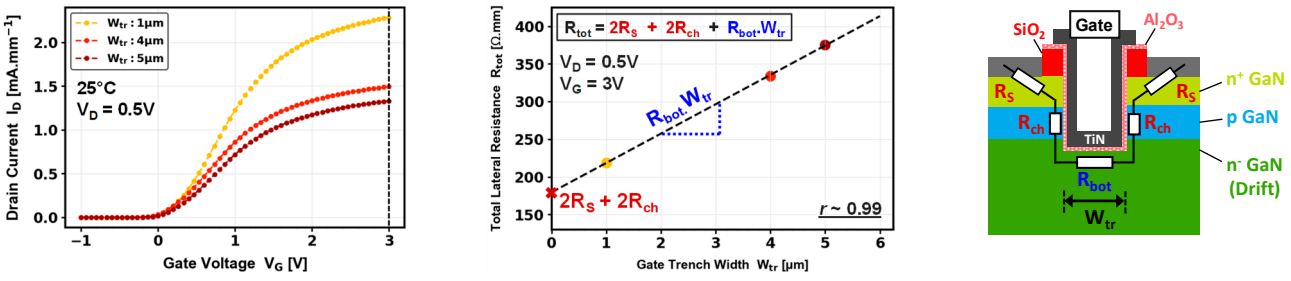
Figure 4. (**a**) The capacitance–voltage characteristics measured at 10 kHz for device A and device B (cf. Figure 1a for the schematic diagram of the test structures' cross-section). (**b**) The evolution of the calculated characteristics with applied voltage, calculated at the V_{th} (A) or V_{FB} (B) for the same set of devices.

To extract the mobility contributions in the trench region, based on our test structures, we used an improved resistance partitioning method that takes into account the evolution of the output current with the gate trench width [17,18], as well as the different electrostatic conditions of device A and B illustrated in Figure 4. To do so, lateral I_D-V_G characteristics based on the planar MOSFET configuration were measured. In this measurement configuration, one of the source electrodes was considered the drain on our MOSFET devices, which means the current flows laterally from one source to the other.

Figure 5a shows the lateral $I_D - V_G$ characteristics as a function of the gate trench width at V_D = 0.5 V. A clear reduction in output current is visible when increasing the gate trench width (i.e., the trench bottom), meaning the total lateral resistance R_{tot} should increase as well with this parameter. Thus, in Figure 5b, a visible linear dependence of the total lateral resistance on the gate trench width can be observed (for I_D values selected at V_G = 3 V, symbolized by the dashed line in Figure 5a). Since the current flows laterally (Figure 5c), R_{tot} can be divided into different resistance contributions, defined as follows:

$$R_{tot} = 2R_S + 2R_{ch} + R_{bot}.W_{tr} = 2(R_{acc} + R_{con}) + 2R_{ch} + R_{bot}.W_{tr} \quad (2)$$

where R_S is the source resistance, R_{acc} is the access resistance, R_{con} is the contact resistance, R_{ch} is the channel resistance, and R_{bot} is the trench bottom resistance.



(**a**) (**b**) (**c**)

Figure 5. (**a**) The transfer characteristics of a lateral GaN-on-GaN MOSFET with different gate trench widths, when one of the source contacts of the MOSFET is considered the drain. (**b**) The evolution of the total lateral resistance with the expected gate trench width, calculated for I_D values at V_G = 3 V. (**c**) A schematic diagram of resistance partitioning around the trench area in the planar MOSFET configuration.

The R_{bot} term can be directly determined by the slope of the fitted curve shown in Figure 5b and is evaluated as ~39.0 Ω·mm. The sheet resistance $R_{sheet,bot}$ is then easily deduced as being around ~39.0 kΩ·sq. In addition, one can estimate through extrapolation

the resistance value for which W_{tr} tends to 0 (i.e., a very thin gate), symbolized by the red cross on the *y*-axis. In that case, the associated resistance value is estimated at around ~179.4 Ω·mm and takes into consideration the source and channel resistance components from the left and right trench sidewalls. The source contribution R_S can then be measured with transfer length measurements (TLMs), as shown in Figure 6. From these measurements, for one source electrode, the contact and access resistance contributions can be calculated, estimated as being around ~7.1 Ω·mm and ~5.9 Ω·mm, respectively.

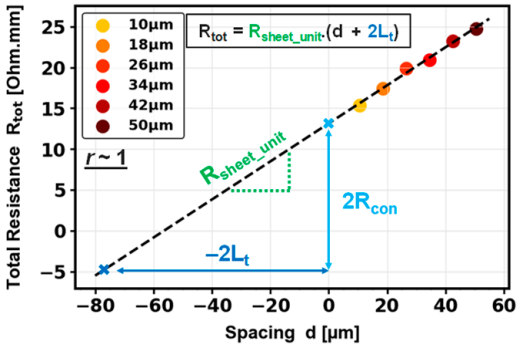


Figure 6. Transfer length measurements on n^+ GaN source layer of GaN-on-GaN epitaxy.

After removing the R_S contribution (measured with TLMs as being around ~13 Ω·mm for one source electrode) from the R_{tot}, and by considering the thickness of the p-GaN layer, we estimated a channel sheet resistance $R_{sheet,ch}$ of ~91.0 kΩ·sq.

At this point, since the resistance contributions and the charge densities are known, one can extract the mobilities (µ) from the trench bottom and trench channel areas with Equation (3):

$$\mu = \frac{1}{QR_{sheet}} = \frac{1}{qNR_{sheet}} \quad (3)$$

where ρ is the material resistivity, Q is the charge density, q is the elemental charge, N is the charge carrier density, and R_{sheet} is the sheet resistance. The charge density and the charge carrier density values chosen for devices A and B correspond to those selected at V_S = 3 V by the black dashed line in Figure 4b (i.e., the same gate voltage used for the previous R_{tot} calculation in Figure 5b). Finally, synthesis of the main parameters extracted from resistance partitioning (cf. Figure 5) and the C-V measurements (cf. Figure 4) is exposed in Table 1.

Table 1. Synthesis of parameters extracted from improved resistance partitioning method for trench bottom and trench sidewall areas.

Trench Area	Sheet Resistance (kΩ·sq)	Q ($C\cdot cm^{-2}$)	N (cm^{-2})	µ ($cm^2/V\cdot s$)
Channel	~91.0	9.86×10^{-7} (A)	6.15×10^{12} (A)	11.1
Bottom	39.0	1.70×10^{-6} (B)	1.06×10^{13} (B)	15.1

Consequently, applying Equation (3) with the parameters in Table 1 leads to the extraction of the effective trench bottom and channel mobilities of 15.1 and 11.1 $cm^2/V\cdot s$, respectively. As explained in [25], this poor channel mobility value could be mainly related to the damaged trench sidewalls following the GaN trench etching step, which is a critical process step for the fabrication of vertical GaN trench MOSFETs [7,26,27]. This should result, on the one hand, in carrier scattering coming from surface roughness (as seen in Figure 2b), and on the other hand, in oxide interface traps at the dielectric/GaN interface, significantly reducing channel mobility.

Finally, a way higher channel mobility of 30 $cm^2/V{\cdot}s$ is obtained when using the transconductance method defined as follows:

$$\mu_{ch} = g_m \cdot \frac{L}{Z} \cdot \frac{1}{C_{ox}} \cdot \frac{1}{V_D} \quad (4)$$

where g_m is the transconductance, Z is the channel width of 200 µm, L is the channel length of 0.7 µm, C_{ox} is the gate oxide conductance of 354.8 $nF.cm^{-2}$, and V_D is the drain voltage defined at 1 V. This low channel mobility is in agreement with the values reported in the literature for state-of-the-art vertical GaN MOSFETs. Indeed, among the research groups that extracted the mobility using the transconductance method, studies from Khadar et al. [7], Ishida et al. [10], and Zhu et al. [28] have fabricated vertical GaN MOSFETs that demonstrate channel mobilities ranging from 15 to 41 $cm^2/V{\cdot}s$, while the current record has been reached by Otake et al. [5], with a channel mobility of ~131 $cm^2/V{\cdot}s$.

Consequently, the mobility results estimated in this study pave the way for further improvements, especially by applying a finer post-etch GaN surface treatment to mend the trench sidewalls from etching damages [10], or by improving the critical dielectric/GaN interface with a higher-quality gate dielectric [13].

4. Conclusions

This study aimed to evaluate the electrical performances of a fully vertical GaN trench by means of I-V and C-V measurements. We first proved the normally-OFF behavior (V_{th} ~ 1 V), the adequate switching operation (I_{ON}/I_{OFF} ~ 10^9), as well as the significantly small gate leakage current (10^{-11} A/mm) of our devices. Then, the resistances of the trench bottom and trench channel were also extracted using an improved resistance partitioning method. Subsequently, by considering the difference in electrostatic behavior between the devices linked to these trench areas, we estimated the effective channel and bottom mobilities to be 11.1 $cm^2/V{\cdot}s$ and 15.1 $cm^2/V{\cdot}s$, respectively. These mobility values are promising and act as a starting point to be improved upon thanks to the optimization of the gate module, with, for instance, a well-controlled trench etching process, a better pre-deposition GaN surface treatment, or the integration of an alternative alumina dielectric into the MOS gate.

Author Contributions: Conceptualization, V.A., H.E.R., V.M., E.F., Y.C., M.C., J.B., and B.S.; methodology, V.A. and B.M.; investigation, V.A., B.M., B.S., and J.B.; writing—original draft preparation, V.A.; writing—review and editing, V.A., B.M., H.E.R., V.M., E.F., Y.C., M.C., G.L., J.B., and B.S.; visualization, V.A.; supervision, B.S., B.M., and J.B. All authors have read and agreed to the published version of the manuscript.

Funding: This study was partially supported by the Labex GANEXT (ANR-11-LABX-0014), the VERTIGO project supported by the French Agence Nationale de la Recherche as part of France 2030 with reference ANR-22-PEEL-0004, and the French RENATECH network through the PTA technological platforms.

Data Availability Statement: The original contributions presented in the study are included in the article, further inquiries can be directed to the corresponding authors.

Conflicts of Interest: The authors declare no conflicts of interest.

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