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Brief Report

A Simple Scan Driver Circuit Suitable for Depletion-Mode Metal-Oxide Thin-Film Transistors in Active-Matrix Displays

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Abstract: Metal-oxide (MOx) thin-film transistors (TFTs) require complex circuit structures to cope with their depletion mode characteristics, making them applicable only to large-area active matrix (AM) displays despite their low manufacturing cost and decent performance. In this paper, we report a simple MOx 10T-2C scan driver circuit that overcomes the depletion mode characteristics using a series-connected two transistor (STT) configuration and clock signals with two kinds of low-voltage levels. The proposed circuit has a wide operating range of TFT characteristics, i.e., $-2.8\ V \leq V_{TH} \leq +3.0\ V$. Through the measurement results of the manufactured sample, it was confirmed that the performance and area of our circuit are suitable for high-resolution mobile displays.

Keywords: mobile active-matrix (AM) display; metal-oxide (MOx) thin-film transistor (TFT); scan driver circuit; depletion mode characteristics

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1. Introduction

Active-matrix (AM) display panels, including liquid crystal displays (LCD) and organic light-emitting diode (OLED) displays, are widely used in various electronic devices such as smartphones, tablets, laptops, desktop monitors, and televisions [1]. These display panels consist of an array of thin-film transistors (TFTs) that control the brightness of the individual pixels. Low-temperature polycrystalline silicon (LTPS) TFTs and amorphous metal-oxide (MOx) TFTs are widely used as a backplane technology of AM displays [2–5]. A LTPS TFT has the advantages of high reliability and a small circuit area owing to its high carrier mobility. However, the excimer laser process of a LTPS TFT is a critical obstacle to reducing the manufacturing cost [2,3] so it has been primarily used in small-area mobile displays [6–8].

On the other hand, the MOx backplane can be manufactured at a relatively low cost because MOx TFTs do not require the expensive laser crystallization process. However, n-type MOx TFTs often have depletion mode characteristics, i.e., the threshold voltage (V_{TH}) is lower than 0 V. So, if a peripheral driving circuit of the AM display such as the scan driver is composed only of MOx TFT, the TFT does not turn off when the gate-source voltage (V_{GS}) is 0 V due to the depletion mode characteristics, causing the circuit to malfunction and increasing the power consumption. To cope with the depletion mode characteristics, the peripheral driving circuit requires additional techniques such as STT structure and negative voltage clock, resulting in a more complex circuit structure and a larger area [9–14]. Therefore, MOx TFT-based scan driver circuits have not been utilized for high-resolution—e.g., over 600 ppi—mobile displays with narrow bezels.

In this paper, we report a simple scan driver circuit composed of only ten TFTs and two capacitors, which can be integrated into a small bezel area of a high-resolution mobile display even with MOx TFTs, in contrast with the previous circuit [9–14]. We tried to devise an

optimal solution that minimizes the area increase and provides an improved device margin considering the practical operation conditions of the high-resolution mobile displays. Its improved performance ensures robust operation over a wide V_{TH} range from the depletion mode to the enhancement mode of the TFT. The SPICE simulation and measurement results of the fabricated scan driver circuit are detailed in the following sections.

2. Conventional Scan Driver Circuit

Figure 1 shows the schematic of a conventional p-type LTPS 8T-2C scan driver circuit from Samsung Display Co., Ltd. of Republic of Korea. which has been widely used in mobile AMOLED displays. The scan driver circuit consists of eight TFTs and two capacitors. It is not difficult to make the LTPS TFT maintain enhancement mode characteristics. Therefore, no countermeasure against depletion mode characteristics is required, and it can be implemented with such a simple structure. However, when it is converted directly to the n-type MOx TFT version as shown in Figure 2, it may not work properly due to the zero-bias current paths through the depletion mode TFTs. During the output pull-up period of the MOx 8T-2C scan driver circuit shown in Figure 2a, T6 should be turned off when T7 transmits a high CK2 voltage to Scan[n]. However, T6 is not completely turned off due to the following two reasons when the n-type MOx TFTs have depletion mode characteristics. First, V_{GS} = 0 V does not turn off T6 because V_{TH} is lower than 0 V. Second, the voltage of QB[n] is slightly pulled up by T5 that is also weakly turned on with V_{GS} = 0 V. In addition, the positive charge on the Q[n] node leaks through T1 and T2 that should be turned off but are not, which degrades the current driving capability of T7. Therefore, the Scan[n] voltage cannot reach VGH, and the power consumption increases due to the current flow through T6 and T7. On the other hand, Figure 2b shows the state of the TFTs and the bias condition during the output hold-down period. The QB[n] node needs to maintain a high voltage for the strong and stable activation of T6. However, if T4 has a negative V_{TH}, the positive charge on the QB[n] node leaks through T4. Accordingly, the QB[n] node voltage may drop and T6 will not turn on fully. Then, Scan[n] becomes more vulnerable to external voltage fluctuations such as the capacitive coupling of CK2. For these reasons, the n-type MOx TFT version of the conventional 8T-2C scan driver circuit is inadequate for use, and a new circuit structure is required for small-area mobile AM displays.

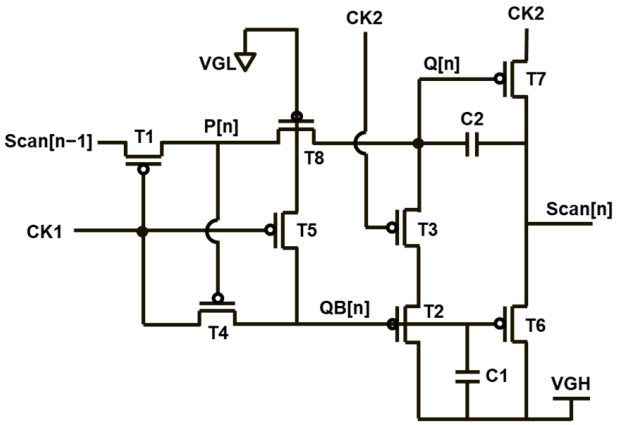


Figure 1. Schematic of the conventional p-type LTPS 8T-2C scan driver circuit.

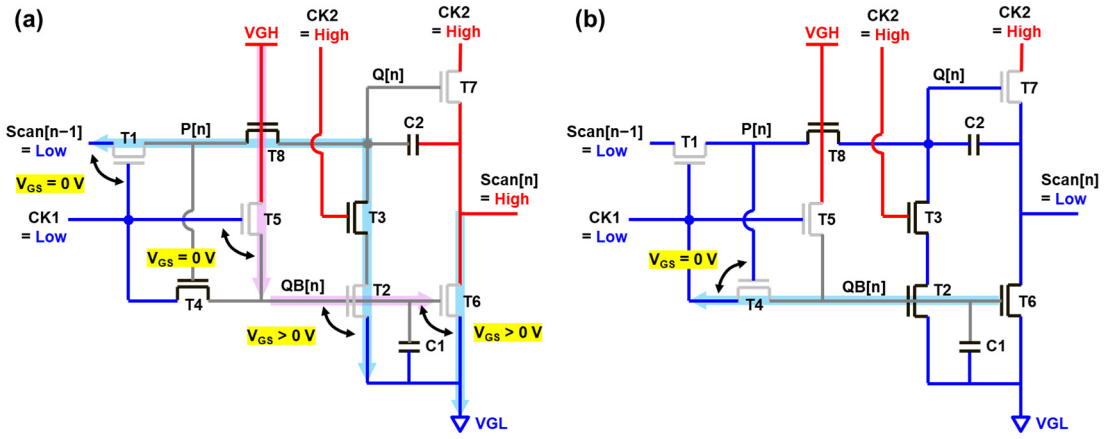


Figure 2. Incomplete turn-off cases of n-type MOx TFT in conventional 8T-2C scan driver circuit due to its depletion-mode characteristics, which result in circuit operation error. (**a**) During output pull-up period and (**b**) during output hold-down period.

3. Proposed Scan Driver Circuit

Figure 3 shows the schematic and the timing diagram of the proposed n-type MOx 10T-2C scan driver circuit. The circuit comprises ten TFTs and two capacitors. In comparison to the conventional MOx 8T-2C circuit, the proposed 10T-2C circuit has two more clock signals, i.e., CKL1 and CKL2. They have the same timing and the same high voltage level as CK1 and CK2, but the low voltage level is different. The low voltage level of CKL1 and CKL2 is VGLL, while that of CK1 and CK2 is VGL. VGLL is lower than VGL to cope with the depletion mode characteristics of MOx TFTs. In the 10T-2C scan driver circuit, the source voltage of every TFT is equal to VGL or higher. When CKL1 or CKL2 is applied to the gate node of the MOx TFT, it turns off completely even if its V_{TH} is slightly negative, because V_{GS} is lower than 0 V. Therefore, T1 is turned off completely during the output pull-up period and the Q[n] node voltage may rise reliably by effective bootstrapping. At the same time, the voltage of QB[n] maintains VGL because T5 is completely turned off by negative V_{GS}. Therefore, the Scan[n] voltage can reach VGH more stably.

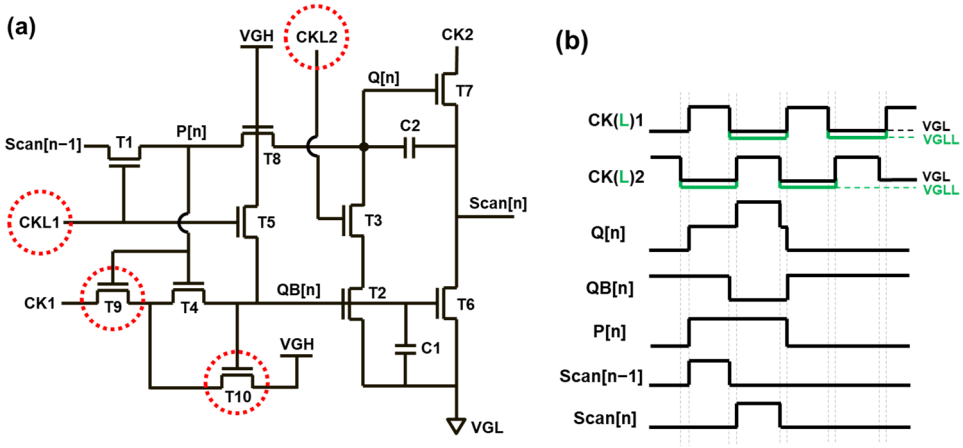


Figure 3. (**a**) Schematic and (**b**) timing diagram of the proposed n-type MOx 10T-2C scan driver circuit.

Two more TFTs, T9 and T10, are added to maintain the high voltage of QB[n] during the output hold-down period. Since T4 is turned off with the gate voltage of VGL, not VGLL, it may not turn off completely if V_{TH} is negative. The two added TFTs, T9 and T10, make the source voltage of T4 VGH with the so-called series-connected two transistors (STT) configuration [12]. Accordingly, T4 can be turned off completely by negative V_{GS}

as shown in Figure 4. The overall operation of the proposed 10T-2C scan driver circuit in Figure 3 is as follows.

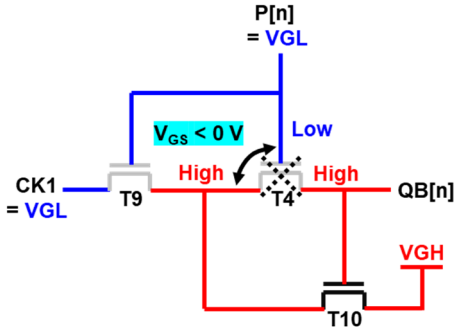


Figure 4. Operation principle of the series-connected two-transistor (STT) configuration in the proposed 10T-2C scan driver circuit.

3.1. Pre-Charging

When CKL1 and Scan[n−1] are high, the P[n] and Q[n] nodes are pre-charged with a high voltage through T1. Since T3 is turned off by CKL2, the pre-charged voltage does not drop even if T3 has a slightly negative V_{TH}. The QB[n] node maintains a high voltage during this period. Then, when CK1 and CKL1 become low before CK2 and CKL2 rise, the QB[n] voltage is discharged through T4 and T9, turning T6 off. At this moment, CKL1 turns off T1 completely even if T1 has a slightly negative V_{TH}. Therefore, the pre-charged Q[n] voltage can be maintained by CKL1 and CKL2, which guarantees a stable bootstrapping operation and makes Scan[n] rise to VGH.

3.2. Output Pull-Up and Pull-Down

Next, CK2 rises to VGH, so the Q[n] voltage is boosted much higher than VGH by bootstrapping, e.g., exceeding the sum of VGH and V_{TH}. This makes the Scan[n] voltage fully reach VGH. During this period, since T1 and T5 are stably turned off by CKL1, the bootstrapped high voltage Q[n] and discharged low voltage QB[n] are maintained respectively as they should be. Therefore, even if T6 has a slightly negative V_{TH}, it does not pull-down Scan[n] significantly and T7 pulls up Scan[n] almost completely. Then, as CK2 goes down, Scan[n] is pulled down by T7.

3.3. Output Hold-Down

In order to hold-down Scan[n] stably, T6 should remain turned on after the pull-down operation. For this, T5 periodically connects the QB[n] node to VGH and the high QB[n] voltage is preserved by the STT configuration composed of T4, T9, and T10. In addition, T7 should not turn on when CK2 rises. However, when CK2 changes from VGL to VGH, the Q[n] node voltage might momentarily rise due to the capacitive coupling through gate-to-drain parasitic capacitance (C_{GD}) of T7. This situation should be prevented by discharging the Q[n] node voltage to VGL through T2 and T3 when CK2 and CKL2 rise. However, in the conventional MOx 8T-2C scan driver circuit, T2 cannot be turned on strongly because the QB node is discharged through T4 if it has a negative $V_{TH,}$ as shown in Figure 2b. Therefore, T7 may slightly turn on, which leads to the undesirable fluctuation of the Scan[n] voltage. On the contrary, this situation is prevented by the STT configuration in the proposed 10T-2C scan driver circuit, even when T4 has negative V_{TH}.

4. Results and Discussions

4.1. SPICE Simulation

The operation of the proposed 10T-2C scan driver circuit against V_{TH} variation was verified by SPICE simulation using SmartSpice 5.4.0.R of Silvaco Inc. Figure 5 shows the measured transfer characteristics of n-type MOx TFT and its SPICE model when the

drain-to-source voltage (V_{DS}) is 0.1 V, 1 V, and 10 V. The RPI polysilicon TFT model of level = 36 was used and the model parameters such as VTO, MU0, MU1, MUS, ETA, etc. were modified to fit the measured device parameters such as V_{TH}, carrier mobility, and subthreshold swing. The V_{TH} of the SPICE model is 0 V and the off-current is about 10 fA regardless of V_{GS} and V_{DS} variation. The specifications of the 10T-2C circuit are listed in Table 1. The three voltage levels, VGH, VGL, and VGLL were selected as 7 V, −6 V, and −9 V, respectively. All TFTs have the same channel length (L) of 3 µm, but the channel width (W) varies according to the specific requirements for optimized circuit operation. The output buffer T7, responsible for both the pull-up and pull-down of the Scan[n] node, has the largest W of 400 µm. The capacitance of the C1 and C2 is same as 190 fF, and C_{LOAD} and R_{LOAD} attached to every Scan[n] node are 25 pF and 2 kΩ, respectively. The ideal pulse width of Scan[n], determined by the high-voltage duration of CK1/2, is set to 2.8 µs considering a commercial mobile AMOLED display with a vertical resolution of 3 K operating at a refresh rate of 120 Hz.

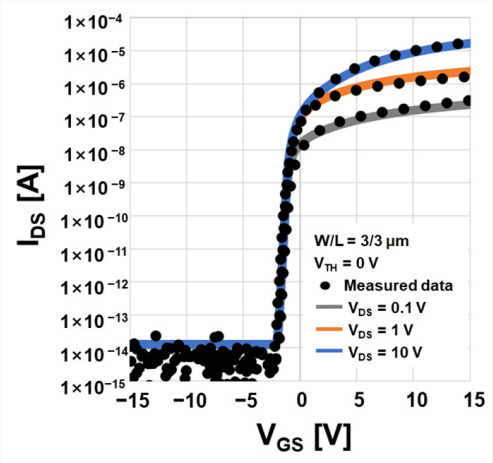


Figure 5. Measured transfer characteristics of n-type MOx TFT and SPICE model with V_{DS} variation from 0.1 V to 10 V when V_{TH} = 0 V.

Table 1. Design parameters of the proposed 10T-2C scan driver circuit.

Parameter	Value
VGH	7 V
VGL	−6 V
VGLL	−9 V
CK1, CK2	7 V/−6 V
CKL1, CKL2	7 V/−9 V
W/L of T6	200/3 µm
W/L of T7	400/3 µm
W/L of T1, T8	6/3 µm
W/L of T2, T3, T5	5/3 µm
W/L of T4, T9	8/3 µm
W/L of T10	2/3 µm
C1, C2	190 fF
C_{LOAD}	25 pF
R_{LOAD}	2 kΩ

Figures 6 and 7 show the SPICE simulation results of the conventional MOx 8T-2C scan driver circuit and the proposed MOx 10T-2C scan driver circuit for various V_{TH} values. The test circuits for the SPICE simulation were composed of twenty stages of the unit circuit in Figure 3. The 18th output signals of the two circuits are shown in Figure 6. The black line is for the 8T-2C circuit, and the red line is for the 10T-2C circuit. When the V_{TH} of every TFT

in the circuits is between 0 V and +3 V, both circuits work normally. However, when the TFTs have depletion mode characteristics, the 10T-2C circuit considerably outperforms the 8T-2C circuit. It can be compared assuming the criteria of normal operation; for example, as the peak voltage of the output pulse is above 6.6 V—approximately 3% drop—and the fall time smaller than 500 ns. Applying these criteria, the operation margin of the 8T-2C circuit is only $V_{TH} \geq -1$ V. If V_{TH} changes further in the negative direction, e.g., −2.8 V—the operation limit of 10T-2C circuit, the output pulse collapses as shown in Figure 6. The main reason of output pulse degradation is the leakage current through T1 which discharges the Q[n] node rapidly as illustrated in Figure 7a. As a result, T7 is turned off before the OUT[n] pull-down and the fall time increases, and the pulse height also degrades. On the contrary, for the proposed 10T-2C circuit, the operation margin is significantly improved to $V_{TH} \geq -2.8$ V. Since T1 is completely turned off with negative V_{GS} and the Q[n] node voltage can be remained sufficiently high, the output pulse meets the criteria of normal operation even if V_{TH} is −2.8 V.

During the output hold-down period, Scan[n] should maintain the VGL level. However, if V_{TH} is below 0 V, T7 will turn on slightly and Scan[n] may fluctuate whenever CK2 rises. This problem becomes more serious due to the capacitive coupling through C_{GD} of T7. To minimize the output voltage fluctuation, the Q[n] voltage should remain pulled down to VGL and QB[n] should be maintained at a high voltage when CK2 is high. However, in the conventional 8T-2C circuit, the QB[n] node is discharged through T4 as shown in Figure 7a, so T2 cannot sufficiently pull down the Q[n] node, which makes the Q[n] node more vulnerable to the capacitive coupling. Accordingly, a large output ripple appears as shown in Figures 6 and 7a. On the contrary, in the proposed 10T-2C circuit, the QB[n] node maintains a high voltage as shown in Figure 7b owing to the STT structure composed of T4, T9 and T10. Therefore, the Q[n] voltage fluctuation is reduced, and the output voltage ripple is also reduced as shown in Figures 6 and 7b. Our SPICE simulation results confirm that the proposed 10T-2C scan driver circuit operates stably over a wide V_{TH} range of $-2.8\ V \leq V_{TH} \leq +3.0$ V.

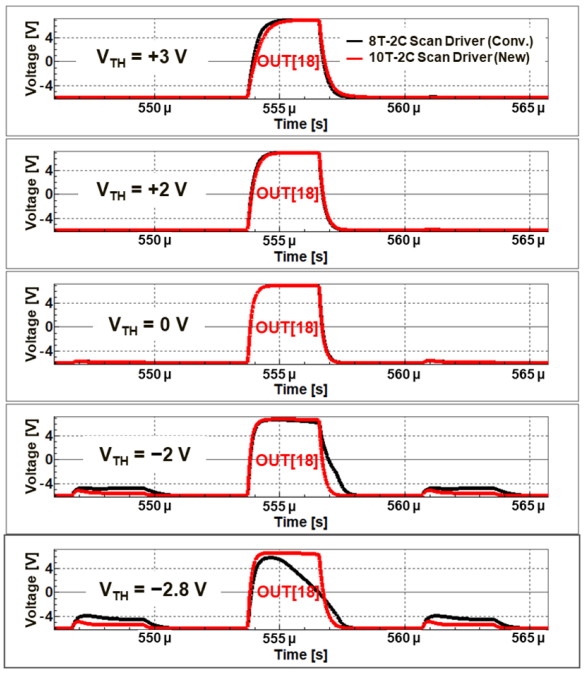


Figure 6. Comparison of SPICE simulation results of the conventional MOx 8T-2C scan driver circuit and the proposed MOx 10T-2C scan driver circuit over a wide V_{TH} variation range of $-2.8\ V \leq V_{TH} \leq +3.0$ V.

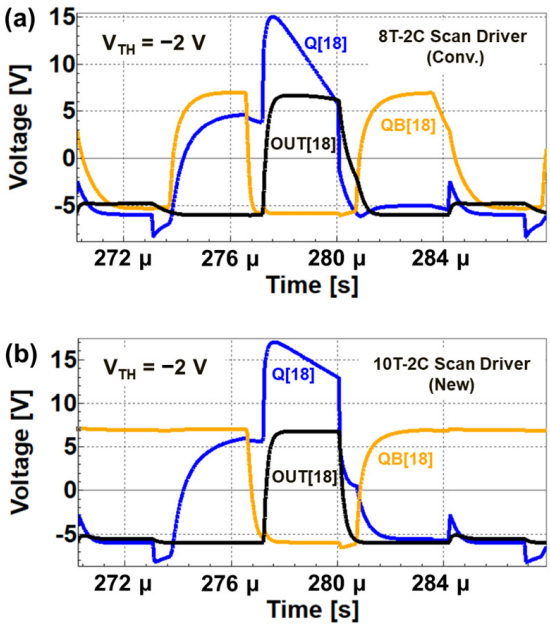


Figure 7. SPICE simulation results of (**a**) the conventional MOx 8T-2C scan driver circuit, and (**b**) the proposed MOx 10T-2C scan driver circuit when $V_{TH} = -2$ V.

4.2. Fabrication and Measurement

A test sample of the proposed MOx 10T-2C scan driver circuit was fabricated to verify whether its area and performance are suitable for mobile displays. The MOx TFTs have top-gate coplanar structure with an amorphous indium-gallium-zinc-oxide (a-IGZO) channel layer and a SiO_2 gate insulator. Molybdenum gate electrode and Ti/Al/Ti source/drain metal were used. The layout of the scan driver circuit was drawn according to the 2 µm design rule that is widely used in recent mobile AMOLED displays. Figure 8 shows the layout drawing and fabrication results of a unit stage circuit. The unit stage area is 40 µm × 240 µm assuming a 40 µm pixel pitch, i.e., 635 ppi. It should be noted that despite being composed only of MOx TFTs, the circuit area width is as small as 240 µm due to its simple structure. The performance of the test sample was evaluated using a probe station in a dark shielding box. The clock signals and supply voltages were generated by a pulse generator, EEC-P772 of ELP Corp, Republic of Korea. The output pulses were measured using an oscilloscope, MSO2024B of Tektronix, Inc.

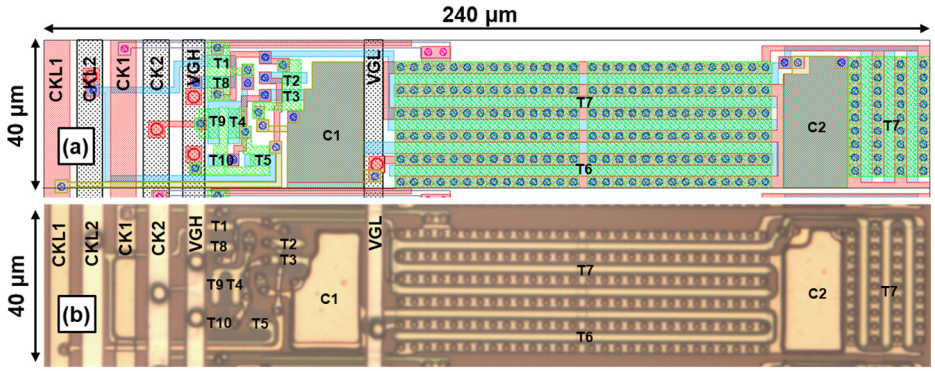


Figure 8. (**a**) Layout drawing and (**b**) micrograph showing the unit stage of the proposed MOx 10T-2C scan driver circuit.

The test sample has twenty stages cascaded and the operation conditions are listed in Table 1. Figure 9a shows the measured output signals of the 18th and the 19th stage. The peak of the output pulse is equal to a VGH of 7 V, as expected, and the low voltage

level maintains a VGL of −6 V without ripple for 1 s. The rise and fall times are 2.4 µs and 2.2 µs, respectively. They are longer than the simulation results, possibly due to the large probing capacitance of the measurement system. In addition, instead of CKL1/2, we applied CK1/2 to the gate nodes of T1, T3, and T5 to check the effect of the lower-level clock signals. In this case, the peak of the output pulse does not reach VGH and the rise and fall times increase to 2.7 µs and 2.7 µs, respectively, as shown in Figure 9b. These results can be explained by two reasons: the poor bootstrapping and weak pull-down action of T7 due to the depletion mode characteristics of the MOx TFTs. Since the bootstrapped Q[n] node voltage is not maintained, the output pulse does not reach VGH and the rise and fall times increase compared with the results of Figure 9a. Therefore, it is confirmed that the lower-level clock signals, CKL1/2, are effective in overcoming the depletion mode characteristics of the MOx TFTs.

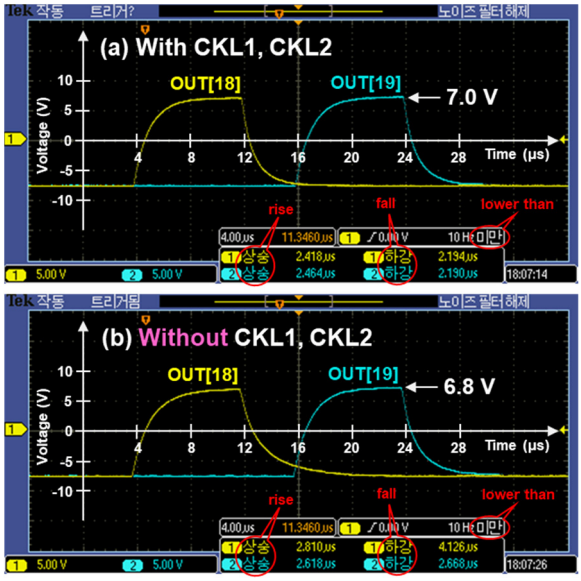


Figure 9. Measured output signals of the proposed MOx 10T-2C scan driver circuit.

The purpose of this study is to devise an optimal solution that minimizes the area increase and to provide an acceptable device margin while considering the practical operation conditions of MOx TFT based-high-resolution mobile displays. Table 2 compares our proposed 10T-2C scan driver circuit with other previous scan driver circuits. The width of all previous circuits is wider than 500 µm, making it difficult to apply them to mobile displays with narrow bezels. On the other hand, the proposed 10T-2C scan driver circuit has the narrowest width of 240 µm owing to its simple structure consisting of only ten TFTs and two capacitors. In addition, the negative limit of TFT V_{TH} is compared according to the criteria of normal operation described in Section 4.1. Typical V_{TH} values of MOx TFTs vary from -1.0 V to 1.0 V depending on the manufacturing process conditions [15–17]. For a fair comparison, we set the operating voltages of the circuits to be the same, i.e., VGH = 7 V, VGL = −6 V, and VGLL = −9 V, respectively. The dimensions of the buffer TFTs and the output load conditions were also set to be the same. The simulation results show that the V_{TH} limit of our 10T-2C circuit is as low as −2.8 V, while that of the previous circuits in Table 2 is −2.1 V [9], −0.9 V [13], and −0.4 V [14], respectively. In summary, our 10T-2C MOx TFT scan driver circuit is suitable for high-resolution mobile displays with a small bezel width and provides robustness against depletion mode MOx TFTs. However, the static current flow from VGH to VGL when the TFTs have negative V_{TH} has not been completely solved in our circuit, and the power consumption may increase in proportion to the static current flow of the depletion mode MOx TFT. For example, when V_{TH} is −0.5 V, −1.5 V, and −2.8 V, the power consumption of the proposed scan driver circuit composed

of 3k stages and operated at 120 Hz frame rate, increases to 38.6 mW, 78.0 mW, and 147 mW, respectively.

Table 2. Comparison of the proposed 10T-2C scan driver circuit with previous scan driver circuits.

Reference	TFT Type	Structure	Width of Scan Driver Circuit	Negative Limit of TFT V_{TH}
[9]	n-type a-IGZO	15T-1C	1200 μm	−2.1 V
[13]	n-type a-IGZO	11T-1C	3500 μm	−0.9 V
[14]	n-type a-IGZO	15T-1C	1000 μm	−0.4 V
This work	n-type a-IGZO	10T-2C	240 μm	−2.8 V

5. Conclusions

We report a simple 10T-2C scan driver circuit suitable for a high-resolution mobile display, which overcomes the depletion mode characteristics of n-type MOx TFTs by employing lower-level clock signals and the STT configuration. SPICE simulation results show that its operation margin is the V_{TH} range of $-2.8\ V \leq V_{TH} \leq +3.0\ V$, which is a significantly improved performance compared with the conventional scan driver circuit that has a negative V_{TH} limit of −2.1 V or higher. The fabricated circuit worked successfully, and the lower-level clock signals were proven to reduce the rise and fall times of the output signals. We expect that the proposed 10T-2C scan driver circuit suitable for the depletion mode characteristics of MOx TFTs can be utilized in high-resolution mobile AM displays, reducing the manufacturing cost.

Author Contributions: Conceptualization, Y.Y. and K.P.; methodology, Y.Y. and K.P.; software, Y.Y.; validation, Y.Y.; formal analysis, Y.Y.; investigation, Y.Y.; resources, K.P.; data curation, K.P.; writing—original draft preparation, Y.Y.; writing—review and editing, Y.Y. and K.P.; visualization, Y.Y. and K.P.; supervision, K.P.; project administration, K.P.; funding acquisition, J.L., K.S., J.K., Y.K., K.L. and K.C. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: Data available in a publicly accessible repository.

Conflicts of Interest: Authors Junhyung Lim, Kyoungseok Son, Jaybum Kim, Youngoo Kim, Kyunghoe Lee, and Kyunghoon Chung were employed by the company Samsung Display Co., Ltd. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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