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A Hierarchical Driving Control Strategy Applied to Parallel SiC MOSFETs

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Abstract: SiC (silicon carbide) MOSFETs have been extensively used in the power electronics industry due to their exceptional characteristics. First, it was found in this study that their driving loss is larger than their conduction loss in high-frequency applications. Based on this finding, this study proposes a hierarchical driving control strategy for improving the parallel-converter efficiency of SiC MOSFETs under light loads. Efficiency under light loads is of great importance for battery-based energy storage systems. To minimize the sum of the conduction loss and driving loss in parallel devices, this study proposes a current-monitoring hierarchical driving strategy based on an active-clamped flyback converter. By monitoring the output current of the converter, the strategy minimizes the sum of the driving and conduction losses by switching the driving state under different loads. The results of simulations indicate the effectiveness of the load-current-monitoring strategy. To verify the effectiveness of this method, a principle prototype of two SiC MOSFETs connected in parallel at 12 V/5 A was fabricated and tested, and the test results showed that there was a maximum improvement of 1.4% in the converter's efficiency when the load current was in the range of 0.5–1.5 A.

Keywords: parallel SiC MOSFETs; conduction loss; driving loss; hierarchical driving

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1. Introduction

Excessive emissions of greenhouse gases have led to global warming and a resultant increase in the frequency of extreme weather, heat waves, floods, and other natural disasters, which have jeopardized the survival of all of humankind. With the deterioration of the natural environment, the suppression of climate change has become the center of focus of research in the mainstream scientific community [1,2]. Clean energy is one of the main solutions. However, clean energy sources, such as wind and solar power, are subject to external conditions, and their operating conditions fluctuate greatly. An effective solution is the application of battery energy storage systems. Battery energy storage systems must maintain high efficiency in all load ranges, especially under medium and light loads [3–5]. SiC MOSFETs offer dynamic characteristics superior to those of Si (silicon) MOSFETs and IGBTs, resulting in significant improvements in their energy conversion efficiency and power density. At the same voltage and current levels, SiC MOSFETs have the advantages of a small on-resistance, small gate charge, low input and output capacitance, and small switching loss compared with those of Si MOSFETs [6–11].

Compared with Si MOSFETs, the performance advantages of SiC MOSFETs are mainly reflected in their smaller gate charge and faster switching speed, enabling the development of high-performance converters with a higher frequency, higher efficiency, and higher power density [12–14]. Due to the low electron mobility of the SiC material itself, it requires a higher gate drive voltage to generate enough channel carriers to achieve a low on-resistance [15,16]. This means that the gain of the lower on-resistance of SiC MOSFETs comes at the cost of a higher drive voltage. Under such conditions, a higher drive voltage means that the driver circuit needs to provide a higher pulse current and

greater losses. At the same time, SiC MOSFETs have significantly lower conduction and switching losses than those of Si MOSFETs, and drive losses play a more important role in the total power consumption. The change in the loss relationship is more pronounced in high-frequency applications of SiC MOSFETs, as the drive loss increases linearly with the operating frequency. In high-current applications, where multiple MOSFETs are connected in parallel, the drive loss increases exponentially with the number of devices connected in parallel. The driving loss of a device is comparable to the conduction loss in a certain load current range, so during the application of SiC MOSFETs, the driving loss becomes a necessary consideration in the converter design, especially for light loads.

SiC MOSFETs are employed in synchronous boost converters to meet the need for both high-voltage applications and soft switching under light loads [4]. Their topology utilizes a quasi-square-wave zero-voltage switching technique to improve the efficiency of the converter. When a converter is operating under light loads, the fixed-operating-frequency mode of operation causes the converter to lose its soft switching and significantly increases the reactive power. In this case, the use of SiC MOSFETs to increase the switching frequency ensures that the power device achieves soft switching without increasing the reactive power. The authors of [17] proposed a three-phase dual active bridge converter using SiC MOSFETs. This scheme improved the conventional single-phase phase-shift scheme by creating a hybrid duty cycle and phase-shift control scheme from the control method, which ensured the soft switching of the switches while increasing the operating frequency of the converter and, thus, improved the converter's efficiency under light loads. Such schemes optimize the converter's operating frequency from the perspective of topology, and SiC MOSFETs are adopted only to improve the operating frequency; their design focuses on switching losses, which are related to the realization of soft switching. The relationships between the conduction loss, driving loss, and switching loss in the application of SiC MOSFETs have not been analyzed.

The authors of [18] conducted an in-depth analysis of the driving loss and driving power structure of SiC MOSFETs. A method for the estimation of the driving loss according to the device manual was provided. The nonlinear variations in the device's gate capacitance and the distribution of the driving loss were analyzed. The driving loss was correlated with the drive voltage, the total gate charge, and the switching frequency. The report quantitatively analyzed the driving loss of SiC MOSFETs and quantitatively calculated the loss distribution in different operating states, which paved the way for a subsequent loss analysis and targeted designs for specific operating conditions. This study proposed a scheme for separating the design of a device's turn-on and turn-off gate resistors based on the device's operating state. It focused on the relationship between the driving loss and the device parameters in a single switch, but the relationship between the driving loss and the conduction loss was not examined.

The authors of [19] optimized the design of SiC MOSFETs with respect to the drive voltage versus the efficiency and reliability. This study showed that SiC MOSFETs are dominated by drift resistance and channel resistance in the on-resistance of the MOSFET due to the high critical electric field. A high gate drive voltage is required to realize the complete inversion of a device and reduce the on-resistance of a MOSFET. According to this study, the relatively high drive voltage recommended in the device manual could effectively reduce the on-resistance and turn-on loss of the device, which have a significant effect on its overall loss reduction. The relationship between the switching loss and conduction loss in a specific MOSFET was analyzed, but parallel devices were not considered.

The above studies investigated SiC MOSFETs at different drive voltages, in different drive modes, with driving loss distributions, and with drive soft-switching technology, and their contents are of great significance for the application of single SiC MOSFETs. However, there is a lack of targeted research on the driving of SiC power devices under high-current and high-frequency operating conditions. When SiC MOSFETs are used in parallel in high-current and high-frequency converters, their on-resistance decreases under the same withstanding voltage, and an increase in the switching speed leads to a significant decrease

in the on-state and switching losses compared with those of Si MOSFETs. Although the gate charge of SiC MOSFETs has been reduced in comparison with that of Si MOSFETs, the increase in the drive voltage makes the driving loss a larger part of the device loss, which is different from the loss characteristics of conventional Si MOSFETs.

This study analyzes the relationship of the switching and the conduction losses in the application of SiC MOSFETs connected in parallel and proposes a hierarchical driving strategy to minimize the total loss. The strategy is verified with simulations and experiments. The experimental results showed that the loss was reduced by up to 9.4% for light loads, and the efficiency was not affected by heavy loads.

2. Quantitative Analysis of Losses and the Design of the Switching Point

The strategy was validated by applying it to an active-clamped flyback topology, which is shown in Figure 1. Since the operating principle of active-clamped flyback converters is familiar to that of engineers, this study focused on the operating mechanism of a hierarchical driving control strategy for parallel SiC MOSFETs. For heavy-load applications, parallel MOSFETs are the main solution for improving efficiency by reducing the conduction loss. However, parallel MOSFETs introduce driving loss under light loads.

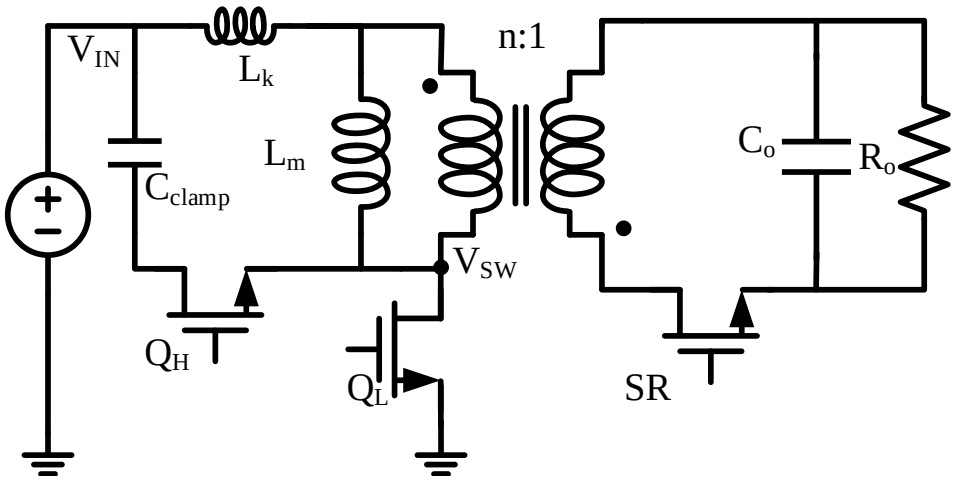


Figure 1. The topology of the active-clamped flyback converter.

A quantitative analysis of the driving and conduction losses of silicon and silicon carbide MOSFETs in parallel applications is presented. MOSFETs with a voltage rating of 1200 V and a current rating of 30 A were chosen for comparison. The CREE C3MP0075120D SiC MOSFET and Microsemi APT28M120L Si MOSFET were used to calculate the driving and conduction losses of the devices at the designed operating conditions. Since the active-clamped flyback converter has the characteristic of soft switching, the advantage of SiC MOSFETs in terms of switching characteristics can be neglected. So, this study only quantitatively analyzes the driving loss and conduction loss.

The conduction loss of the MOSFET can be expressed as (1).

$$P_{con} = \frac{1}{n}\bar{I}^2 R_{ds} \tag{1}$$

where n represents the number of MOSFETs driven and $\bar{I}$ denotes the rms current through the device. In a converter in steady-state operation, the rms current through the MOSFET can be expressed as (2).

$$\bar{I} = \sqrt{\frac{\int_0^{DT} i^2\, dt}{T}} \tag{2}$$

According to the relevant parameters of the two MOSFETs, the conduction losses of SiC and Si MOSFETs can be expressed as $P_{con-SiC} = 75\bar{I}^2$ mW and $P_{con-Si} = 450\bar{I}^2$ mW, respectively.

The driving loss can be expressed by Equation (3).

$$P_{dri} = n \cdot V_{DD} \cdot Q_G \cdot f_{SW} \tag{3}$$

where n represents the number of MOSFETs driven, V_{DD} represents the driving voltage of the MOSFETs, and Q_G represents the amount of charge stored in the gate capacitance per cycle. f_{SW} represents the switching frequency of the MOSFETs. The operating frequency is normalized to 100 KHz, allowing the frequency coefficient $\kappa = f_{SW}/100$ KHz to be defined, under which the driving losses of SiC and Si MOSFETs in a single comparison device can be expressed as $P_{dri-SiC} = 102.6 \cdot \kappa$ mW and $P_{dri-Si} = 300 \cdot \kappa$ mW.

Based on the qualitative analysis, the conduction loss of a Si MOSFET is 1.5 times the driving loss at 100 KHz/1 A. Parallel-connected Si MOSFETs can reduce the sum of the conduction and driving losses. For SiC MOSFETs, the driving loss is 1.37 times the conduction loss at 100 KHz/1 A, and parallel-connected SiC MOSFETs introduce more loss into the load. Additionally, the working frequency of the SiC MOSFETs can reach several MHz, making the driving loss higher. A loss comparison is made between APT28M120L and C3MP0075120D in dual-MOSs application; the results are shown in Table 1. The highest frequency represents the recommended highest working frequency, and the effective current represents the effective current range at the recommended highest working frequency. The hierarchical driving control strategy only can work effectively in 0–0.87 A in parallel Si MOSFET applications.

Table 1. The driving and conduction loss comparison between APT28M120L and C3MP0075120D.

Device Type	Device Part Number	Highest Frequency	Effective Current
Si MOSFET	APT28M120L	100 KHz	0–0.83 A
SiC MOSFET	C3MP0075120D	2 MHz	0–7.95 A

The CPM309000065B SiC MOSFET chip was used for the design of the prototype, and its specific electrical parameters are shown in Table 2.

Table 2. The key parameters of the CPM309000065B SiC MOSFET.

Symbol	Parameter	Typical Value	Test Conditions
R_{ds}	On-state resistance	65 mΩ	V_{GS} = 15 V
Q_G	Total gate charge	30.4 nC	V_{DS} = 400 V, V_{GS} = −4/15 V, I_D = 20 A
V_{DS}	Drain-source breakdown voltage	900 V	I_{DS} = 100 μA

Referring to the previous equations for the driving and conduction losses of power MOSFETs and the relevant parameters of the prototype, we plotted the total power consumption of the driving and conduction losses of the single-MOSFET and dual-MOS operating states at 100 KHz (Figure 2) and looked for the root-mean-square currents when the power consumption of the two modes was equal to determine the state-switching point.

The conduction and driving losses of the single MOSFET and the dual-MOSs were parabolas centered at x = 0 with only the second quadrant. The offset of the driving loss was at y = 0, and the number of parallel devices determined the total on-resistance, that is, with a constant parameter for the quadratic term, which determined the size of the parabola's "mouth"; a greater total on-resistance resulted in a smaller mouth and a quicker increase in power consumption with the continuation of the current. The intersections of the driving power consumption of the single MOSFET and dual-MOSs were equal. As shown in the figure, the power consumption of the single MOSFET's drive was smaller;

with the increase in the current, the on-resistance loss accounted for a proportion of the total loss, and the single MOSFET's driving loss increased more quickly. Under the operating condition of 200 KHz, the state-switching point of the converter was 1.89 A, and the total power consumption of driving and conduction was 347.5 mW.

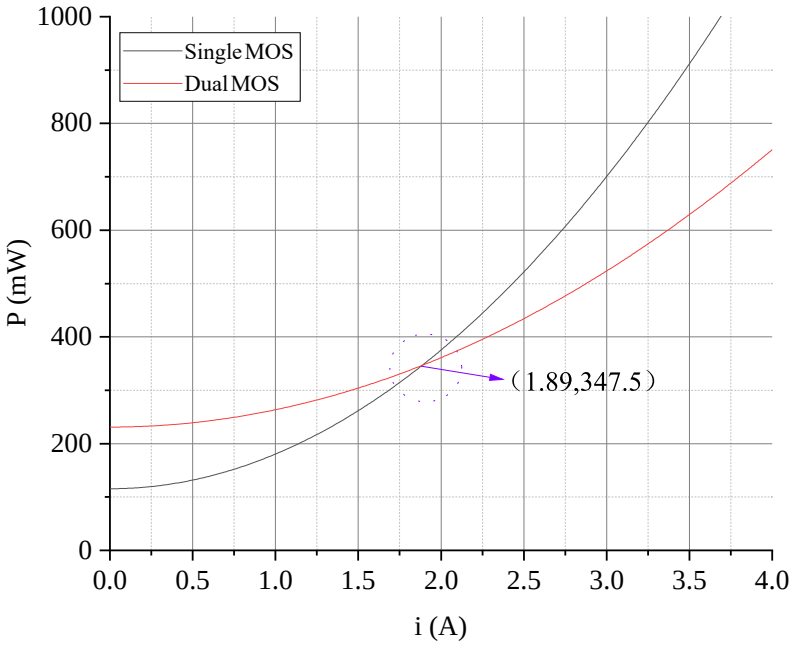


Figure 2. The sum of the driving and conduction losses in dual-MOSs at 200 KHz under different loads.

Based on the loss analysis, the state-switching point was generalized to plot the total power consumption of conduction and drive for single- and dual-MOS drive under operating frequency conditions of 100 KHz–1 MHz, and the results are depicted in Figure 3.

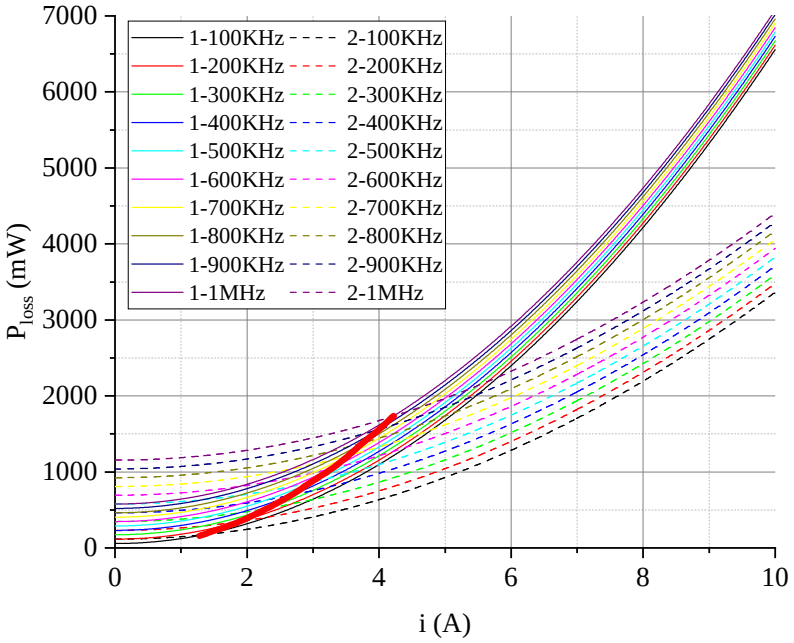


Figure 3. The sum of the driving and conduction losses at different frequencies under different loads.

The red line in the figure depicts the transformation of the state-switching point with the single- and dual-MOS drive as the operating frequency increased. The state-switching

current increased as the operating frequency increased. At an operating frequency of 1 MHz, the state-switching point was 4.21 A, and the total power consumption of driving and conduction at this time was 1729.667 mW. The effective range of the hierarchical driving strategy increased with the increase in the operating frequency.

To minimize the total conduction and driving losses, the strategy divided the mode of operation into those of single MOS, dual-MOSs, and triple-MOSs in hierarchical driving applications with three parallel MOSFETs. The design of the switching points of the three parallel MOSFETs at 200 KHz is shown in Figure 4. The effective range of the hierarchical driving strategy increased with the increase in the number of parallel MOSFETs.

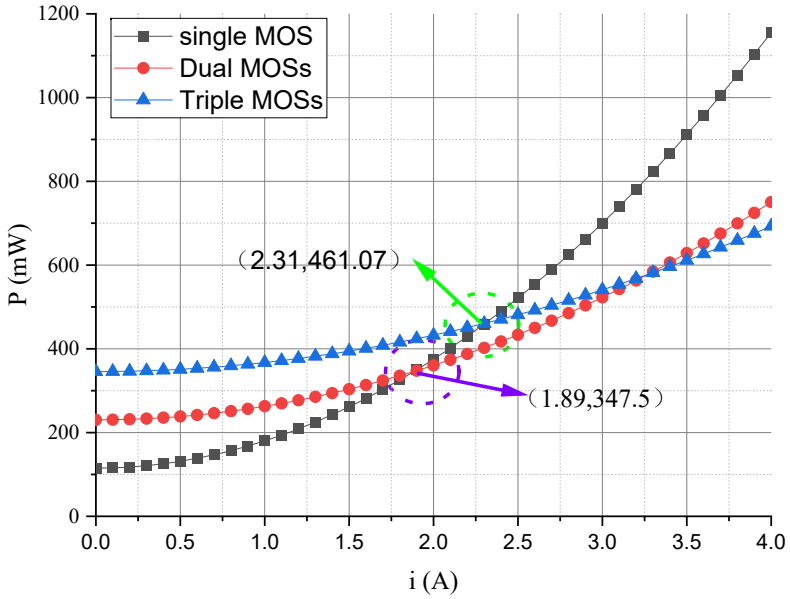


Figure 4. The sum of the driving and conduction losses in triple-MOSs at 200 KHz under different loads.

The effective range of the hierarchical driving control strategy increased with the increase in the operating frequency and number of parallel devices. The increase in the operating frequency matched the trend towards higher power densities, and the increase in the number of parallel devices matched the high current requirements.

3. Operating Principle of the Hierarchical Driving Strategy

According to the above analysis, the single-MOSFET working mode had the lowest conduction and switching losses under a load of 1.89 A, and the dual-MOS mode had better efficiency under loads above 1.89 A at 200 KHz. The hierarchical driving strategy aimed to realize switching in the single-MOSFET and dual-MOS modes under a load of 1.89 A.

Since the output current directly reflected the load state, an output-current-monitoring method could improve the sensitivity of the converter to load changes. In addition, the load had low fluctuation during steady-state operation, which contributed to the stability of the switching point.

In applications with precise input voltage requirements and real-time status detection, a system power management and protection module should be added to the output of the finished power supply module. The protection module has to monitor the output voltage and current in real time. The vice-side current detection method has compatibility with this system's power management and protection module and only needs to externalize the current detection signal of the protection module to realize the multiplexing of the functions. The current detection circuit is schematically shown in Figure 5.

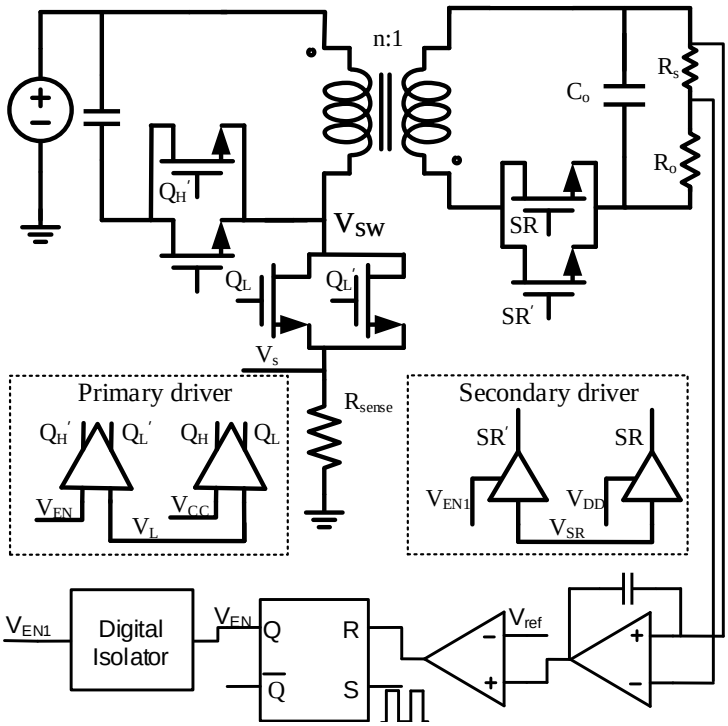


Figure 5. Schematic of the current detection circuit.

Here, Q_H and $Q_H^{'}$ are the parallel high-end MOSFETs on the primary side, and Q_L and $Q_L^{'}$ are the parallel low-end MOSFETs on the primary side. SR and $SR^{'}$ are the parallel synchronous rectification MOSFETs on the secondary side. *driver*1 is the driver of Q_H and Q_L, *driver*2 is the driver of $Q_H^{'}$ and $Q_L^{'}$, *driverSR*1 is the driver of SR, and *driverSR*2 is the driver of $SR^{'}$. Q_H, Q_L, *driver*1, SR, and *driverSR*1 represent the first set of MOSFETs and drivers. $Q_H^{'}$, $Q_L^{'}$, *driver*2, $SR^{'}$, and *driverSR*2 represent the second set of MOSFETs and drivers. R_s represents the sense resistor for monitoring the output current. V_{EN} is the enable signal of the driver2, and V_{EN1} is the enable signal of driverSR2.

In the current detection scheme, a stable output current produced a stable voltage drop across R_s. The converter's output current was generally stable and only fluctuated when the load was switched. A schematic of the operating waveform in the current detection strategy is shown in Figure 6.

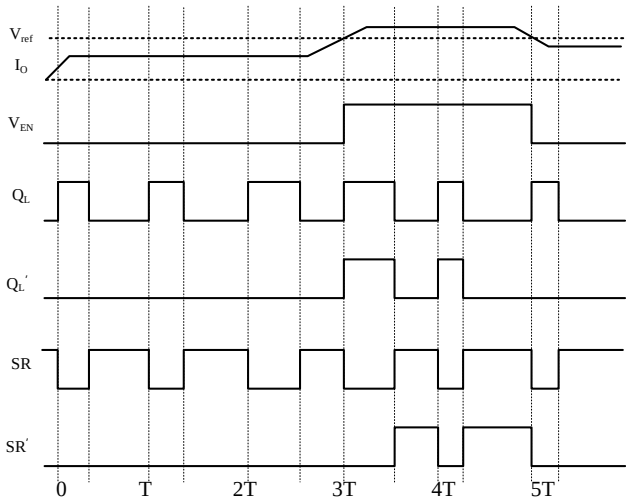


Figure 6. The schematic waveforms of the current detection circuit.

As shown in Figure 6, *driver*1 and *driverSR*1 worked in the entire load range. The working states of *driver*2 and *driverSR*2 depended on the load current. When the load current was higher than the reference value, the enabling signal V_{EN}, output V_{EN1}, *driver*2, and *driverSR*2 worked. The two sets of MOSFETs worked together to reduce the sum of the driving and conduction losses and improve the efficiency.

4. Simulations and Experimental Results

Based on the above analysis, the effectiveness of the hierarchical driving strategy was verified with simulations and experiments. The active-clamped flyback topology was used to complete the verification of the hierarchical drive control method. The relevant parameters of the prototype designed in this section are shown in Table 3.

Table 3. The key parameters of prototype.

Characteristic	Symbol	Typical Value
Input voltage	V_{IN}	100 V
Output voltage	V_{OUT}	12 V
Output current	I_O	5 A
Working frequency	f_{SW}	200 KHz
Driving voltage	V_{dri}	15 V
Primary excitation inductance	L_m	220 µH
Primary leakage inductance	L_k	10 µH
Resonant capacitance	C_c	10 µF

4.1. Simulation Results

Simulations were used to verify the effectiveness of the current-monitoring scheme. The simulation model was set based on the designed prototype, and the hierarchical driving strategy was constructed in the Pspice17.2 from the Cadence company (San Jose, CA, USA). Some devices without simulation files were replaced by devices with the same function. The simulation models used in the simulation were downloaded from the manufacturer and are listed in Table 4. The transformer was modeled from the library files in the software.

Table 4. The main models used in the prototype.

Device	Manufacturer	Part Number
Current Sense Amplifiers	INA180	TEXAS INSTRUMENT
SiC MOSFET	IMW120R060M1H	infineon
MOSFET driver	UCC20225	TEXAS INSTRUMENT
Digital isolator	ISO7721DR	TEXAS INSTRUMENT

The simulation results are shown in Figure 7. The simulation results mainly contained I_O, V_{OUT}, the representative driving signal of the second set of MOSFETs (V_{SR2}), and the representative driving signal of the first set of MOSFETs (V_{SR1}).

From the simulation results, it can be seen that at 34.01 ms, the load current started to rise from 0.1 A to 5 A with a slope of 50 A/ms; the load current was maintained at 5 A for 1 ms, and then it started to fall to 0.1 A with a slope of 50 A/ms. The whole process of the variation in the load current was maintained for 3 ms. During this process, the range of fluctuation in the output voltage ΔV_{OUT} was 0.5 V, which met the design requirements. During the whole working process, the synchronous rectifier driver of the first set, V_{SR1}, always maintained a normal output. When the load current reached 1.9 A, the synchronous rectifier driver of the second set, V_{SR2}, started to enable the output. The specific waveform of the output-enabling process is shown in the upper-left corner of the figure (V_{SR2}), and the output-disabling process is shown in the upper-right sub-figure. When the load current dropped from 5 A to 2.1 A, V_{SR2} stopped outputting, which was mainly caused by the inconsistency between the turn-on and turn-off voltages of the driver's enabler.

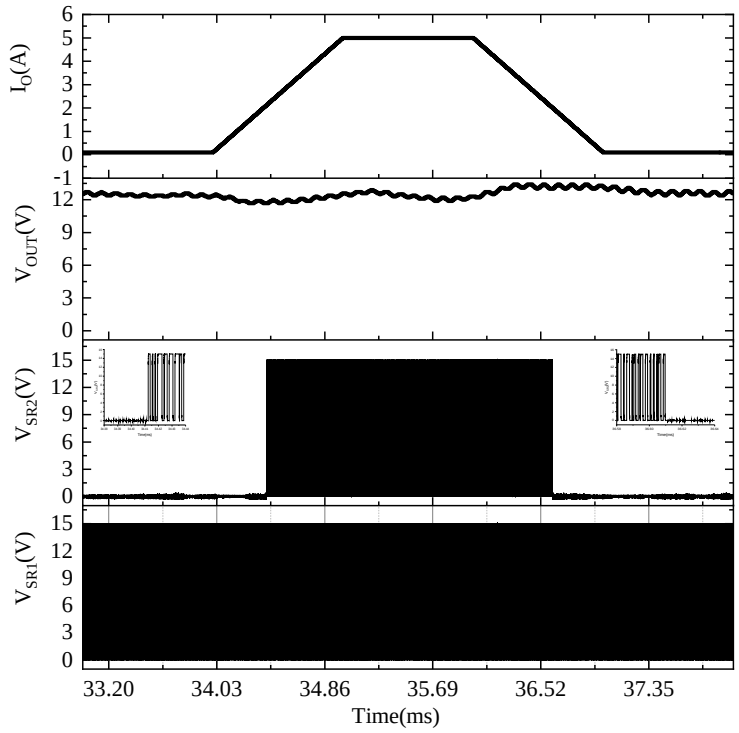
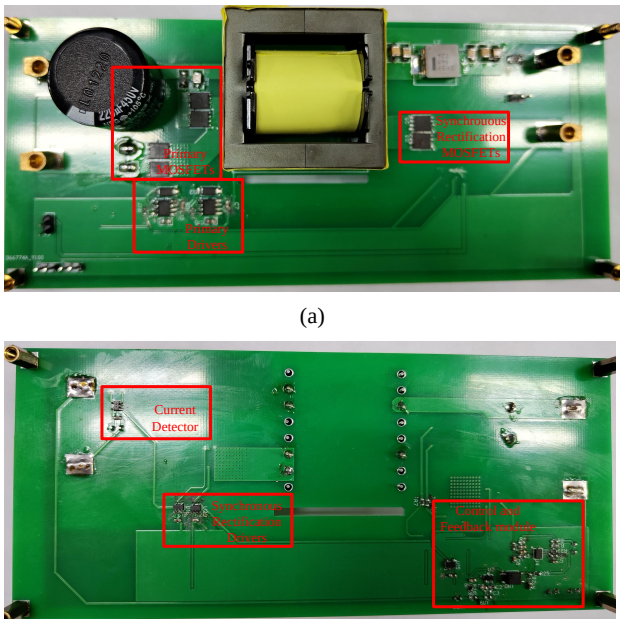


Figure 7. The simulation results of the hierarchical driving control strategy.

4.2. Experimental Results

After the experimental scheme was effectively verified with simulations, we fabricated and tested a prototype to verify the hierarchical driving strategy. The experimental prototype is shown in Figure 8. The power circuit of the power module was mainly distributed on the front side of the prototype, and the control logic was distributed on the back side of the prototype, thus realizing the separation of power and control and reducing the influence of the power circuit on the feedback and control logic. The drivers and power switches of the prototype were in the form of a single package, and each driver corresponded to one power switch, thus realizing driver control with a single switch. An output-current-monitoring module monitored the output current in real time, and its output allowed enabling the control of the second-stage driver to meet the requirements of the hierarchical drive control scheme. The test waveform and the working details are shown in Figure 9.

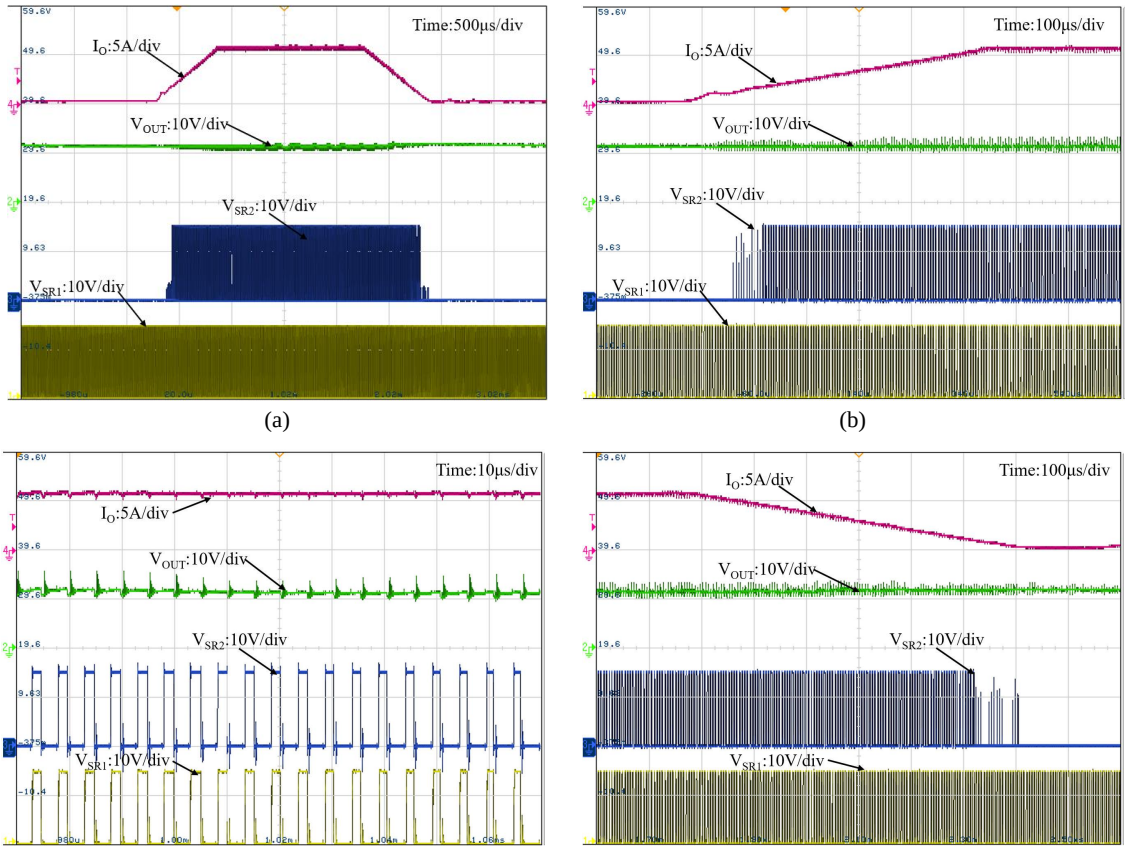
The test waveform included I_O, V_{OUT}, V_{SR2}, and V_{SR1}. The load current started to rise from 0.1 A to 5 A with a slope of 5 A/ms in the first 1.5 ms; the load current was maintained at 5 A for 1.5 ms and then started to fall to 0.1 A with a slope of 5 A/ ms. Throughout the process of variation in the load, the output voltage fluctuated in the range of $\Delta V_{OUT} \leq 0.5$ V, and its dynamic response to changes in the load met the design requirements. V_{SR1} always worked normally in all of the load fluctuation processes. Under a load of 2 A, V_{SR2} started to enable the output. When the load current dropped from 5 A to 1.6 A, V_{SR2} stopped outputting. The asymmetry between the enabling and disabling thresholds was due to the different turn-on and turn-off thresholds of the drive-enabling signals [20], which limited the responsiveness of the hierarchical driving strategy. In the vicinity of the enabling and disabling thresholds of the second-level drive, the second-level drive signal was discrete, which was due to the continuous output current transformation; the gain of the current detection chip was fixed, and there was a period of inaccurate judgment of the enabling port voltage threshold of the driver chip. The overall scope of the hierarchical drive strategy allowed it to realize the function of single-MOSFET operation under light loads and dual-MOSs operation under heavy loads.



(a)

(b)

Figure 8. The experimental prototype: (**a**) the front side; (**b**) the back side.



(a) (b)

(c) (d)

Figure 9. The working process of the hierarchical driving strategy: (**a**) the whole working process; (**b**) the turning-on process; (**c**) the working details; (**d**) the turning-off process.

After the functional validation of the proposed strategy, the efficiency of this study's converter and the conventional converter was tested under different load conditions to

evaluate the improvement in efficiency of the proposed scheme for the converter. The efficiency of the converter was defined according to (4).

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \cdot I_O}{V_{IN} \cdot I_{IN}} \tag{4}$$

where P_{OUT} is the output power and P_{IN} is the input power; the input voltage V_{IN}, input current I_{IN}, output voltage V_{OUT}, and output current I_O were tested with an MSOX4154A oscilloscope from Keysight.

Graphs of the efficiency tests on the two converters are shown in Figure 10. According to these graphs, it can be seen that in the light-load state—especially with a load current in the range of 0.5–1.5 A—the control scheme proposed in this study effectively improved the efficiency of the converter; the most obvious effect was at 0.5 A, where the efficiency improvement reached 1.4%. With the increase in the load current, the loss brought about by the drive accounted for a smaller and smaller proportion of the total loss, so the efficiency improvement became smaller and smaller. When the load current was 2 A, the control scheme proposed in this study lost its effect on the improvement in efficiency, and the efficiency of the traditional parallel-drive converter was slightly higher than that of this experimental scheme, which was mainly caused by the additional control losses brought about by it. With the further increase in the load, the proportion of the extra loss introduced in the total loss became smaller and smaller, and the efficiency of the two schemes was almost equal.

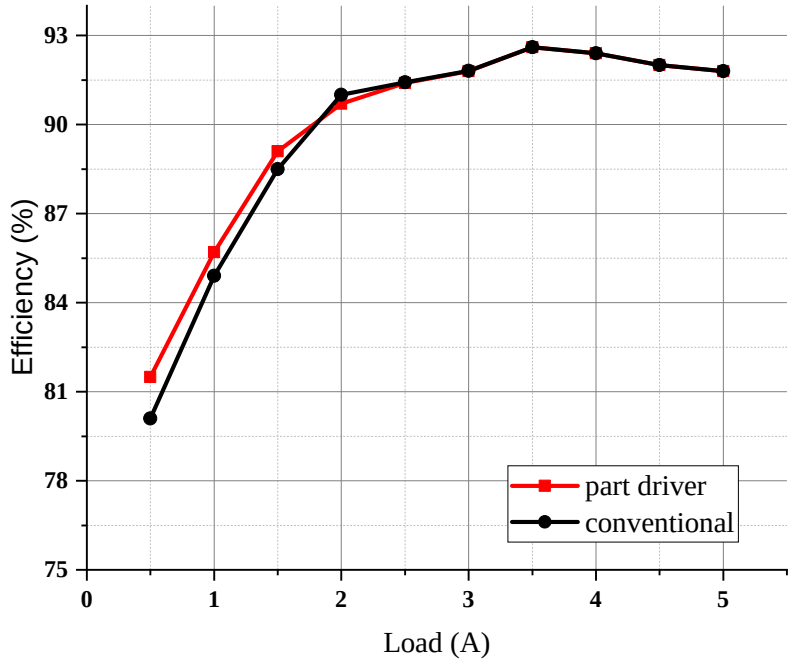


Figure 10. The efficiency results.

The real-world challenges of manufacturing variations and environmental factors must be considered. To reduce the power loss of the sense resistor, the gain of the current sense amplifier needed to be large enough. Manufacturing deviations in the sampling resistor and temperature coefficients of the current sense amplifier can cause a shift in the switching point of the hierarchical driving control strategy, which has an impact on the maximum gain of efficiency with the hierarchical driving control method. The efficiency improvement of this strategy was tested at different temperatures, and the test results are shown in Figure 11. This strategy worked effectively in the range from −25 °C to 75 °C. There were small fluctuations in the efficiency improvement at different operating

temperatures, which were affected by the temperature characteristics of the key devices, such as the SiC MOSFET, the current sense amplifier, and the sense resistor.

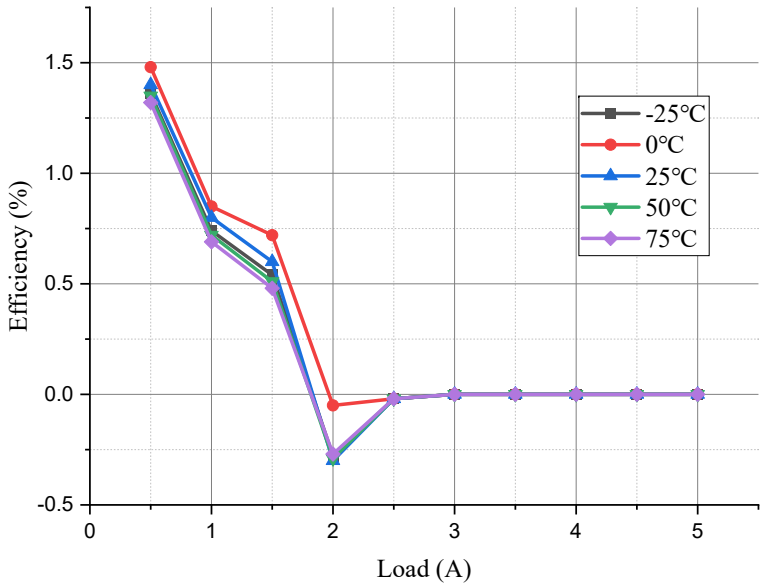


Figure 11. The efficiency improvements at different temperatures.

A comparison was made between state-of-the-art approaches and the approach proposed in this work; the results are shown in Table 5. The approaches proposed in [3,17] only verified the effectiveness of their modulation strategies, and efficiency was not mentioned. The approach proposed in [5] caused a 3% efficiency improvement at most with the optimal switching point design, but the highest efficiency was 85%. The authors of [4] introduced SiC MOSFETs to widen the ZVS range, and a 1.1% efficiency gain was realized with this strategy. All of the strategies focused on the number of converter cells, which was different from this work. Compared with the state-of-the-art approaches, this work had an improvement of 1.4% in efficiency with a negligible impact on the function under heavy loads.

Table 5. Comparison among state-of-the-art approaches.

State-of-the-Art Approach	Working Mode	Efficiency Gains
This work	Hierarchical driving control	1.4%
[3]	Multi-level state control scheme	Only verified the modulation strategy
[5]	Phase-shedding control scheme	3%
[4]	Phase-shedding control for QSW-ZVS	1.1%
[17]	Modulation strategy for 3P-DAB	Only verified the modulation strategy

5. Conclusions

In this study, for the first time, we analyzed the problem regarding the relationship of driving and conduction in high-frequency parallel applications with SiC MOSFETs. Based on the problems found in the loss analysis, a hierarchical driving strategy was proposed. As verified with simulations and experiments, the strategy was able to improve the efficiency by up to 1.4% under light loads and had almost no effects on the efficiency under heavy loads. This was the first time that SiC MOSFETs' drive and conduction losses were quantitatively analyzed, and a relative strategy was proposed to complete the optimization of efficiency under light loads. The application of high-frequency SiC MOSFETs can effectively improve the efficiency of converters under light loads, which is of great significance for giving full play to the performance advantages of SiC MOSFETs under

high-frequency and high-current conditions. The application range of this hierarchical driving strategy is mainly in applications with large load ranges, such as in electric drive systems for electric vehicles, battery systems for the generation of new energy, and control processor power supply systems.

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