electronics

MDPI

Article

New Method for Logarithmic Analogue-to-Digital Conversion Using Switched Capacitors with a Variable Logarithmic Base

Zynoviy Mychuda [1], Mykola Mykyichuk [2], Igor Zhuravel [3], Lesia Mychuda [3], Adam Szcześniak [4,*] and Zbigniew Szcześniak [5]

[1] Department of the Computer-Assisted Systems of Automation, Lviv Polytechnic National University, 79-000 Lviv, Ukraine; zynovii.r.mychuda@lpnu.ua
[2] Faculty of Computer Technology, Automation and Metrology, Lviv Polytechnic National University, 79-000 Lviv, Ukraine; mykola.m.mykyichuk@lpnu.ua
[3] Department of Information Technology Security, Lviv Polytechnic National University, 79-000 Lviv, Ukraine; ihor.m.zhuravel@lpnu.ua (I.Z.); lesia.z.mychuda@lpnu.ua (L.M.)
[4] Faculty of Mechatronics and Mechanical Engineering, Kielce University of Technology, 25-314 Kielce, Poland
[5] Faculty of Electrical Engineering, Automation and Computer Science, Kielce University of Technology, 25-314 Kielce, Poland; z.szczesniak@tu.kielce.pl
* Correspondence: a.szczesniak@tu.kielce.pl

Abstract: This article is devoted to the development of a new method of logarithmic analogue-to-digital conversion using switched capacitors with a variable logarithmic base. The essence of the method and its implementation are presented. Mathematical models have been developed, analysis has been carried out and errors have been assessed. It has been demonstrated that the developed converters, using the proposed method, significantly outperform known analogous converters: for input voltages ranging from 1 mV to 10 V, the processing error does not exceed 0.001% with a processing time not greater than 105 µs (microseconds).

Keywords: logarithmic analogue-to-digital conversion; method; functional processing; switched capacitors; accuracy

check for updates

Citation: Mychuda, Z.; Mykyichuk, M.; Zhuravel, I.; Mychuda, L.; Szcześniak, A.; Szcześniak, Z. New Method for Logarithmic Analogue-to-Digital Conversion Using Switched Capacitors with a Variable Logarithmic Base. *Electronics* **2024**, *13*, 29. https://doi.org/10.3390/electronics13010029

Academic Editor: Yuhua Liang

Received: 21 September 2023
Revised: 17 December 2023
Accepted: 18 December 2023
Published: 20 December 2023

Copyright: © 2023 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0/).

1. Introduction

In processing variable signals over a wide dynamic range, logarithmic analogue-to-digital converters (ADC) are used, and these ADCs are further divided into logarithmic (LADC) and quasi-logarithmic (QLADC) converters. They differ in their structure. In the structural scheme of a QLADC, it is possible to separate the logarithmic circuit from the ADC, whereas this is not possible in an LADC. As a result of this design in the QLADC, the relative processing error changes when the value of the input signal changes, as it does in linear ADCs. In an LADC, the relative error has a constant value over the entire range of input signals. The other main properties of QLADCs and LADCs are similar: a wide range of input signals, the ability to linearize the characteristics of various devices, and the ability to process the conversion results in logarithmic arithmetic. The last property offers the possibility of significantly increasing the speed of digital information processing, as the lengthy operations of linear arithmetic (multiplication, division) are reduced to the fast operations (addition, subtraction) of logarithmic arithmetic. This is especially important for real-time systems, where the processing time should be kept to a minimum. It should be emphasised that, compared to QLADCs, the use of LADCs allows for increased precision in the processing of multiplication and division information since, in LADCs, both large and small input signals are processed with an equal relative error. Currently, the most common converters are logarithmic ADCs encoded bit-by-bit with pulse feedback, recursive, and pipelined. In order to enhance the metrological characteristics and increase the technological feasibility, when implementing ADCs as integrated circuits, these converters (ADCs) are mainly made using switched capacitors.

A comparison of logarithmic and linear ADCs is given in paper [1] based on biomedical applications where the signals have a wide range. It has been shown that logarithmic ADCs are better in the area of smaller signals. However, for large amplitudes, linear ADCs have a smaller absolute error.

In paper [2], a significant increase in the accuracy of ADCs has been achieved with weight redundancy and converter calibration algorithms.

A novel low-power, 6-bit successive approximation logarithmic ADC for biomedical applications has been designed and simulated in [3]. A two-step successive approximation method is proposed to obtain a piecewise linear approximation of the desired logarithmic transfer function.

In the patent in [4], the error correction of the ADC is implemented by means of an error signal, which is obtained by integrating the difference between the input charge and the feedback pulses.

The results of the LADC tests on switched capacitors with successive approximations are provided in papers [5–7], in which the principles of the operation, construction, modelling, and error analysis of these converters were developed.

Paper [8] gives a summary of research on the theory, practical methods, and means of functional analogue-to-digital conversion using switched capacitors.

Paper [9] describes a logarithmic compression ADC using a sub-ranging TDC and the transient response of a comparator. The settling time of the comparator is inversely proportional to the logarithm of the input voltage. In the proposed ADC, the input voltage is converted into a pulse, whose width represents the settling time of the comparator. Subsequently, the TDC converts the pulse width into a binary code.

Paper [10] presented research on a logarithmic voltage-to-time converter for use in novel logarithmic analogue-to-digital converter architectures that do not require analogue blocks, such as amplifiers, with signal processing being carried out in the time domain to the maximum possible extent. The time domain resolution increases.

In the patent in [11], a large measurement range of LADCs in an RC circuit was achieved as a result of the inclusion of an amplifier between the capacitor and the comparator. A mathematical compensation of time constant errors in the RC circuit and voltage imbalance is performed based on the previous measurements of two reference voltages.

In the patent in [12], double integration was used to increase the accuracy of an LADC.

An increase in the processing speed of LADCs was achieved in patent [13] based on a neural network that uses a recursive algorithm.

In papers [14,15], microphotographs that describe pipeline LADCs, implemented as integrated circuits were provided; the output code is 8-bit, and the energy consumption does not exceed tens of microwatts.

The results of tests on linear ADCs with indirect voltage–time conversion, using Dickson charge pumps, are given in papers [16–19]. It is shown that this approach results in a simplified technical solution and increases the technological possibilities when building ADCs as integrated circuits.

In [16], a simple method was developed for the design of device systems based on linear charge pumps to reduce energy consumption during processing. For this purpose, the amplitude of the clock signal is selected below the supply voltage.

The handbook in [17], following load pumping topologies in low-power devices, provides an overview of the most modern integrated topologies.

A linear ADC with indirect voltage–time processing was proposed in paper [18]. Low-level signals are amplified with Dickson pumps. The ADC is implemented with simple functional nodes. The test results of an implemented prototype of such an ADC are presented.

The linear ADC [19] uses a Dickson charge pump for voltage–time conversion. The ADC is realised using low-complexity digital circuits without the use of analogue amplifiers.

In [20], SAR ADCs have been proposed that are based exclusively on standard digital circuits. As a result, the integration of these ADCs into various functional units is facilitated. Nonlinearity compensation and correction of excess errors were performed.

In [21], configurable asynchronous processing is used to increase the flexibility of speed and resolution tradeoffs in SAR ADCs. The mismatch of the 80 MS/s 10 b, 40 MS/s 11 b, and 20 MS/s 12 b channels is canceled using a digital calibration technique. The characteristics of the ADC prototyped in the 180 nm CMOS process are given.

A continuous-time pipelined analog-to-digital converter was proposed in [22]. This is a new architecture that implements the equivalent of an anti-alias filter followed by an ADC. It is shown that the SNDR of the proposed ADC is much higher than that of traditional ADCs. This theory was verified using macro-model and transistor-level simulations.

An energy-efficient SAR ADC 14 b 20 MS/s using 65 nm CMOS technology for portable medical ultrasound systems is described in [23]. To improve the linearity of the SAR ADC, a digital background mismatch calibration technique was used. In addition, a compact noise reduction technique is proposed.

In [24], a 7-bit, two-channel, time-interleaved, two-step flash ADC with a speed of 3 GS/s was presented. The ADC has a built-in voltage reference source based on a capacitive DAC and an advanced offset calibration technique. The ADC prototype was implemented in a 40 nm CMOS process.

In [25], a compact and energy-efficient SAR ADC is described, in which noise is reduced by using error feedback (EF). The ADC prototype was made using 65 nm 1P9M CMOS technology.

In our paper, we propose a method of logarithmic analogue-to-digital conversion using switched capacitors with a variable logarithmic base to enhance precision and speed. The function of this method is to compare, on each sub-scope, the compensation voltage with a preset level, resulting in the selection of the last compensation voltage level on the previous sub-scope.

The novelty of this article compared to known methods [2,4,7,10] lies in the following:

- In order to increase the accuracy and speed of processing, in each processing cycle, the absolute processing error is compensated until the error setpoint is reached;
- Electrical models of the LADC implementing the proposed method and mathematical error models for these LADCs have been developed.

The aim of the article is to develop a new method for logarithmic analogue-to-digital conversion using switched capacitors with a variable logarithmic base to enhance precision and processing speed.

The research used equations derived from known laws of electrotechnology and electrostatics, which were used for computer modelling of the converters and for research on errors and processing time.

2. The Essence of the Proposed Method for Logarithmic Analogue-to-Digital Conversion Using Switched Capacitors with a Variable Logarithmic Base

The essence of the proposed method for logarithmic analogue-to-digital conversion lies in the particular implementation of the balancing process, in which the processing range is divided into sub-scopes. During processing, a compensation voltage is formulated, U_κ, by varying the charge on the storage capacitor with a periodically repeated dosage of energy in each step. On the first sub-scope, the initial value of the compensation voltage, U_κ, is set equal to the reference voltage, U_o. The compensation voltage level is then changed, U_κ, to pass through the input signal level. This is followed by a transition to the second sub-scope. The weight value, ν_c, of any c-sub-scope is selected according to the formula $\nu_c = a^{m-c}$, where a is any positive number greater than unity and m is the number of the last sub-scope. The base value of the logarithm, ζ_c, which defines the dosage of the energy quantity on any c-sub-scope, according to the formula $\zeta_c = \exp(\frac{\nu_c U_{IN_{\min}}}{U_{IN_{\max}}} \ln \frac{U_{IN_{\min}}}{U_o})$, is set. The number of steps, n_c, is counted, and the product of the number of steps and the

weight of this sub-scope is determined. The processing result is determined as the sum of the products obtained according to the formula $N = \sum_{c=1}^{m} (-1)^{c-1} n_c \nu_c$. During processing, the last compensation voltage level, $U_к$, in each sub-scope is remembered. A transition from the c-sub-scope to the next (c+1)-sub-scope is carried out after the compensation voltage, $U_к$, level has passed through the set level. The quality of the set level uses the last compensation voltage level in the (c-1)-sub-scope. The initial value of the compensation voltage in the c-sub-scope is set equal to the last level of the compensation voltage in the (c-2)-sub-scope. The initial value of the compensation voltage in the second sub-scope is set equal to the input voltage.

The essence of the proposed method is illustrated by the voltage diagrams given in Figure 1.

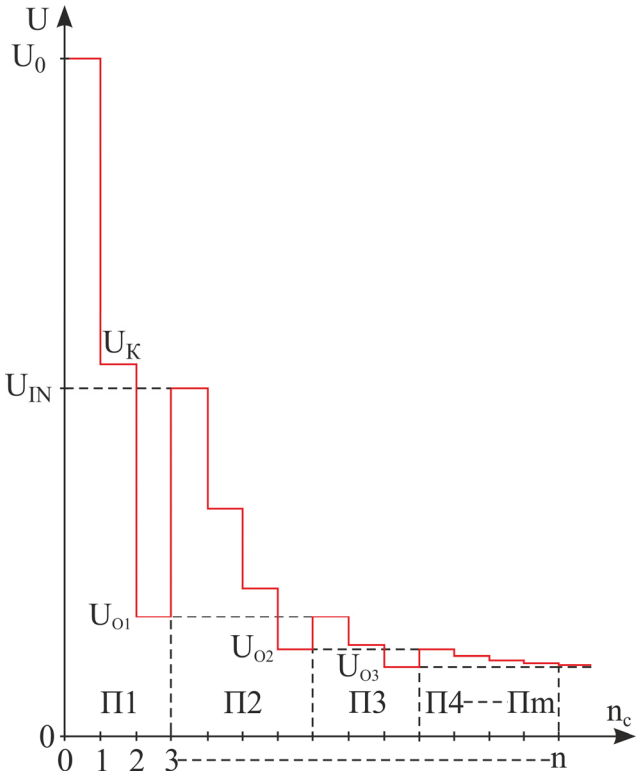

Figure 1. Voltage diagrams that illustrate the essence of the proposed logarithmic analogue-to-digital conversion method with a variable logarithm base.

The implementation of the proposed logarithmic analogue-to-digital conversion method is carried out so that the compensation voltage levels are used during the processing, which are on the accumulation capacitor cells of each sub-scope.

The capacitance of the capacitor cells set the permissible values of the processing error on each sub-scope. When moving to the next sub-scope, the mode of feeding the comparison voltages to the comparator is changed, with the result that in each subsequent sub-scope the processing error decreases until it reaches the set value.

3. Physical Model of an LADC Implementing the Proposed Logarithmic Analogue-to-Digital Conversion Method Using Switched Capacitors with a Variable Logarithmic Base

A simplified functional diagram of the LADC which implements the proposed logarithmic analogue-to-digital conversion method using switched capacitors with a variable logarithmic base is shown in Figure 2.

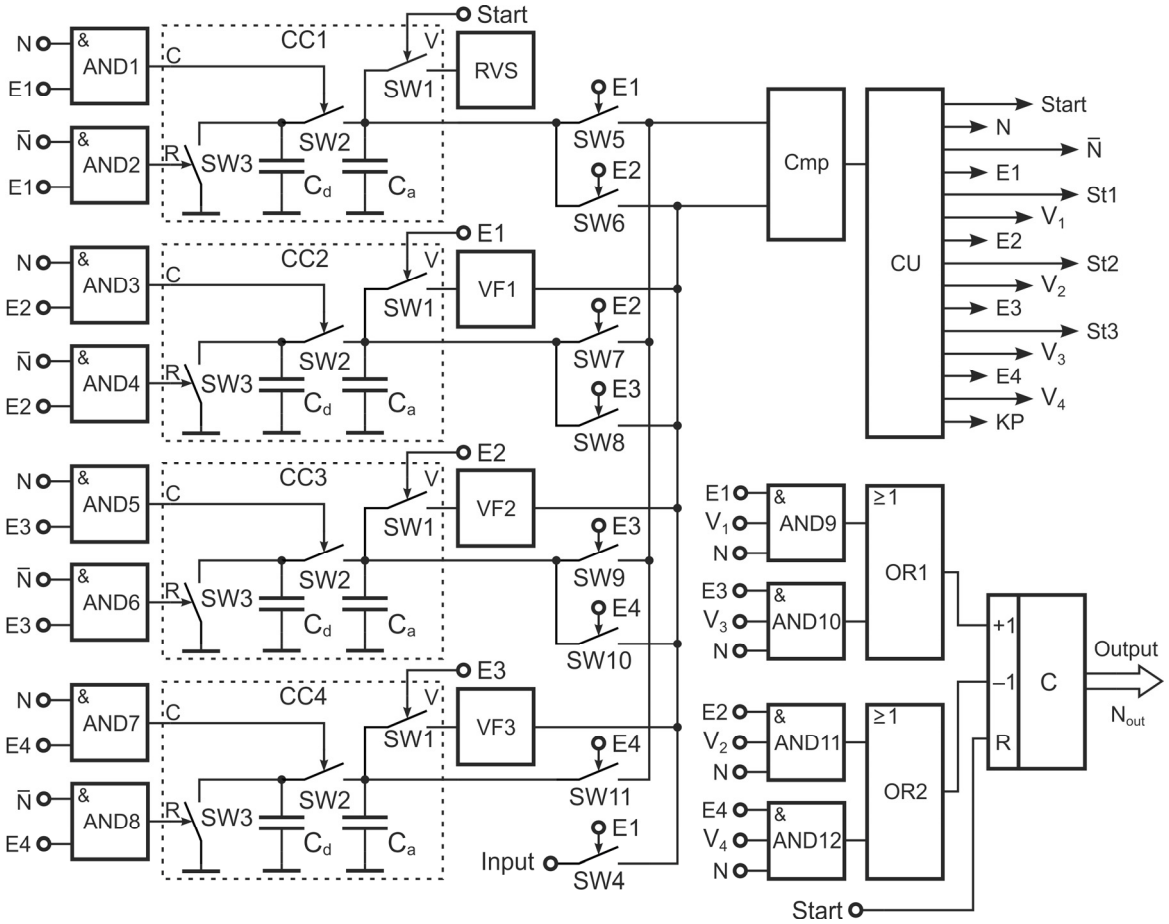

Figure 2. Simplified functional diagram of the LADC implementing the proposed logarithmic analogue–digital processing method using switched capacitors with variable logarithmic base.

The LADC includes: CU—a control block; C—a counter; Cmp—a comparator; RVS—a reference voltage source; CC1-CC4—capacitor cells 1–4; AND1-AND15—AND gates 1–15; OR1 and OR2—OR gates 1–2; SW1-SW12—analogue switches 1–12; and VF1-VF3—voltage doublers 1–3, with each capacitor cell containing a dose capacitor, C_d, an accumulation capacitor, C_a, and analogue switches SW1-SW3.

The proposed logarithmic analogue-to-digital conversion method is implemented using the diagram shown in Figure 2.

The "Start" impulse of the CU (control block) resets the state of the counter, C, and activates the SW1 switch of the CC1 cell. Through the activated SW1 switch, the capacitor Ca accumulates charge, and the CC1 cells charge from the RVS source to the level of the reference voltage, U_o.

The processing begins once the "Start" impulse is finished.

It should be emphasised that (1) during processing (Figure 1), a voltage is always applied to the first input of the Cmp (comparator), which is compared with the compensating voltage, U_κ, (U_{IN}—in the first, U_{o_1}—in the second, U_{o_2}—in the third, and U_{o_3}—in the fourth sub-scope), and the compensating voltage U_κ is always applied to the second input of the Cmp (comparator); (2) voltage doublers VF1-VF3 are used to avoid discharging the capacitors Ca of accumulating capacitor cells when switching switches SW5, SW7, SW9, and SW11.

In the first sub-scope, the CU (control block) forms the E1 pulse of the processing call and the "St1" (start-up impulse). During the operation of the "St1" impulse, a logical zero level is established at the simple output of the control block, and an inversion is established at the logical unit level, as a result of which the SW3 switch of the CC1 cell

is activated and the dose capacitor, Cd, of the CC1 cell discharges to zero. With the E1 processing-enabling impulse, switches SW4 and SW5 are activated, through which the input voltage and compensating voltage in the first sub-scope (the latter is the output voltage of the first CC1 cell) are, respectively, applied to the first and second inputs of the comparator, Cmp.

When the start-up impulse, "St1", is applied from the control block, the input voltage level is written via the AND9 product element switching on switch SW1 of cell CC2 on the Ca (accumulation capacitor) of cell CC2.

At the end of the "St1" impulse in the CC1 cell, the process of charge re-distribution between the accumulation capacitor, Ca, and the dose capacitor, Cd, begins with each step impulse of order N, the accumulation capacitor, Ca, gives up part of its charge to the dose capacitor, Cd, lowering the compensation voltage level in it. In the interval between N impulses, the control block forms sequence impulses, $\overline{N}$, which turn on the SW3 switch, and the dose capacitor, Cd, discharges to zero. The clock sequence impulses, N, pass through the product element AND9 (opened by the call pulse E1), where they are multiplied by the weight, ν_1, of the first sub-scope and then applied to the addition input of counter C via the element OR1.

When the compensation voltage level, U_κ, on the Ca (accumulation capacitor) of cell CC1 passes through the input signal level and becomes equal to U_{o_1} (Figure 1), the comparator, Cmp, goes into a logic zero state, and then the control block, CU, generates the signal E1 = 0 and blocks the further passage of the clock sequence impulses, N, through the AND9 product element.

The last compensation voltage level in the first sub-scope is

$$U_{o_1} = \zeta_1^{n_1} U_o \tag{1}$$

The number of steps (n_1) in the first sub-scope is equal to the number of pulses of order N that have passed to the input of the AND9 product element from the time the "St1" impulse ends until the comparator, Cmp, transitions to a logic zero state

$$n_1 = \frac{1}{\log \zeta_1} \log \frac{U_{IN}}{U_o} \tag{2}$$

where $\zeta_1 = \frac{C_{a_1}}{C_{d_1} + C_{a_1}}$, whereas $C_{d_1} << C_{a_1}$.

In the AND9 product element, the number of steps, n_1, is multiplied by the weight, ν_1, of the first sub-scope, and this product is fed via the OR1 element to the addition input of counter C. In this way, counter C, when processing in the first sub-scope is complete, will store the code

$$N_1 = n_1 \nu_1 \text{ or } N_1 = \frac{\nu_1}{\log \zeta_1} \log \frac{U_{IN}}{U_o} \tag{3}$$

On the second sub-scope, the control block forms the E2 processing-enabling impulse and the "St2" start-up impulse.

The processing-enabling impulse E2 activates the switches SW6 and SW7, through which, respectively, the last compensation voltage level, U_{o_1}, in the first sub-scope and the compensation voltage, U_κ, in the second sub-scope (the latter being the output voltage of the second CC2 cell) are fed to the first and second cells of the Cmp (comparator) inputs, respectively.

When the start-up pulse, "St2", is applied from the CU (control block), the last compensation voltage level, U_{o_1}, on the first sub-scope is written via the SW1 switch of cell CC3, activated by the element AND11 on the Ca (accumulation capacitor) of cell CC3.

At the end of the "St2" impulse in the CC2 cell, the process of charge redistribution between the Ca (accumulation capacitor) and the Cd (dose capacitor) begins. This process is carried out analogously to in the CC1 cell, with the difference that the step impulses of the N sequence are provided by the "E2" enable impulse, triggered by the elements AND11

and OR2, to the subtraction input of the counter, C. In the AND11 product element, these pulses are multiplied by the weight, ν_2, of the second sub-scope.

When the compensation voltage level on the Ca (accumulation capacitor) of the CC2 cell passes through the signal level, U_{o_1}, the comparator, Cmp, enters a logic zero state, which causes the control block to generate the signal E2 = 0 and blocks the further passage of the clock sequence impulses, N, through the product element AND11.

The last compensation voltage level in the second sub-scope is

$$U_{o_2} = \zeta_2^{n_2} U_{IN} \tag{4}$$

The number of steps (n_2) in the second sub-scope is equal to the number of impulses of order N that have passed to the input of the AND11 product element from the time the "St2" pulse ends until the comparator transitions to the logic zero state

$$n_2 = \frac{1}{\log \zeta_2} \log \frac{U_{o_1}}{U_{IN}} \tag{5}$$

For the processing time on the second sub-scope, the counter, C, will store the code

$$N_2 = -n_2 \nu_2 \text{ or } N_2 = -\frac{\nu_2}{\log \zeta_2} \log \frac{U_{o_1}}{U_{IN}} \tag{6}$$

So, when the processing on the first and second sub-scopes is complete, the counter, C, will store the code

$$N = N_1 + N_2, \text{ that is} \tag{7}$$

$$N = n_1 \nu_1 - n_2 \nu_2 \text{ or } N = \frac{\nu_1}{\log \zeta_1} \log \frac{U_{IN}}{U_o} - \frac{\nu_2}{\log \zeta_2} \log \frac{U_{o_1}}{U_{IN}} \tag{8}$$

The transformation on the third and fourth sub-scopes is carried out analogously. Finally, the processing result is equal to the algebraic sum of the aforementioned products on the individual sub-scopes

$$\begin{gathered} N = \nu_1 \cdot n_1 - \nu_2 \cdot n_2 + \nu_3 \cdot n_3 - \nu_4 \cdot n_4 \text{ or} \\ N = \frac{\nu_1}{\log \zeta_1} \log \frac{U_{IN}}{U_o} - \frac{\nu_2}{\log \zeta_2} \log \frac{U_{o_1}}{U_{IN}} + \frac{\nu_3}{\log \zeta_3} \log \frac{U_{o_2}}{U_{o_1}} - \frac{\nu_4}{\log \zeta_4} \log \frac{U_{o_3}}{U_{o_2}} \end{gathered} \tag{9}$$

The last compensation voltage level on the fourth sub-scope is

$$U_{o_4} = \zeta_4^{n_4} U_{o_3} \tag{10}$$

whereby the absolute processing error shall not exceed the last compensation voltage increment in the fourth sub-scope, i.e.,

$$\Delta_4 = \zeta_4^{n_4 - 1} (\zeta_4 - 1) U_{o_3} \tag{11}$$

By increasing the weight, ν_c, of the sub-scope and setting the base value of the logarithm, ζ_c, accordingly on the c-sub-band, we decrease the number of steps, i.e., increase the speed of the logarithmic analogue-to-digital converters.

By increasing the number of sub-scopes, we increase the precision (accuracy) of the processing method.

4. Mathematical Modelling of a New Logarithmic Analogue-to-Digital Conversion Method Using Switched Capacitors with a Variable Logarithmic Base

The disadvantage of known variable-base logarithm converters is the need to set, for each of the processing sub-scopes, their minimum and maximum level values, between which the compensating voltage changes. With four processing sub-scopes, it is necessary to store three voltage values. In addition, when increasing the processing accuracy by

increasing the number of processing sub-scopes to five, the processing length increases to 50 steps.

The proposed new analogue-to-digital processing method with a variable logarithm base is devoid of these drawbacks. In this method, at the end of the first processing sub-scope, the last value of the compensation voltage becomes the minimum, and the maximum is the value of the input voltage.

Therefore, in the second sub-scope, a sweeping descending waveform is formed, reducing the compensation voltage. In each subsequent sub-scope, the difference between the maximum and minimum values of the previous sub-scope's compensating voltage is compensated. This makes it possible to use a sweeping, one-sided falling waveform without additional memorisation of the compensation voltage value in each processing step (as is the case with known methods). In doing so, an increase in speed is achieved, as processing stops when the set accuracy is reached.

For the proposed new analogue-to-digital processing method, the essence of which is illustrated by the voltage diagrams shown in Figure 1, a functional processing algorithm has been developed, as shown in Figure 3.

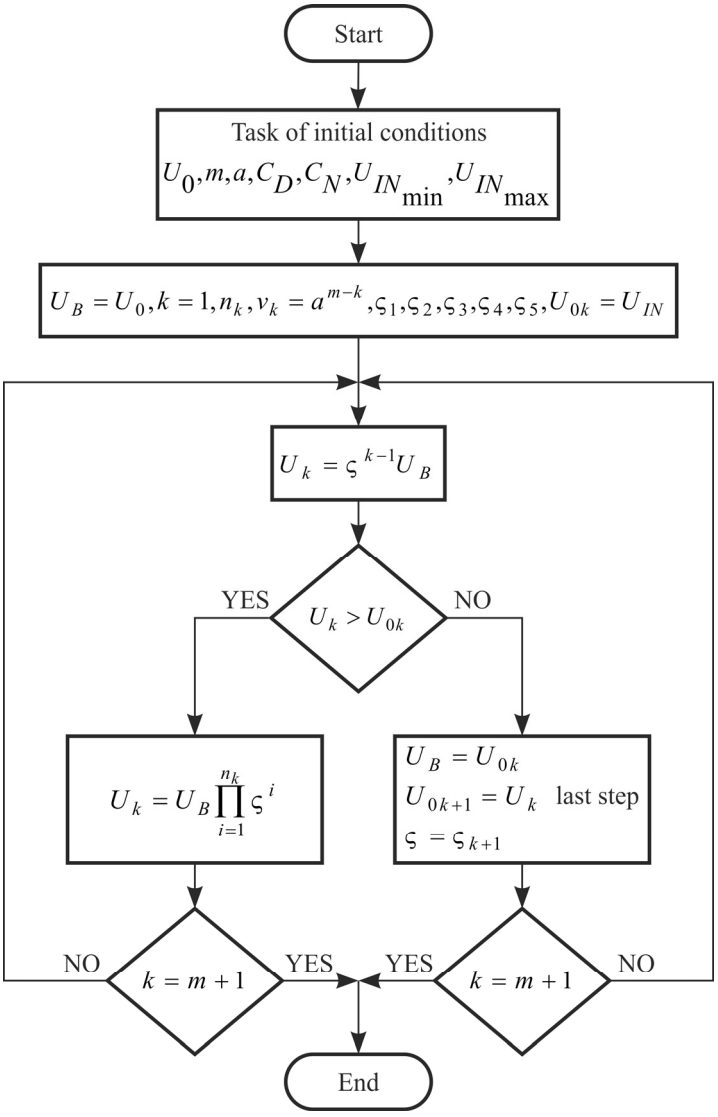

Figure 3. Block diagram of the functional algorithm of the proposed logarithmic analogue–digital processing method using switched capacitors with a variable logarithmic base.

The initial data inputs are the values of the reference voltage, U_0, the number of desired processing sub-scopes, **k**, and the values of the logarithm base in each sub-scope, ζ1, ζ2, ζ3...ζk. The maximum number of steps allowed per sub-scope is 10.

The possibility of pre-determining the logarithm base simplifies the technical implementation of the capacitor cell, as it allows the necessary capacitances for connection to be selected in advance. This is another advantage of the proposed new method. The value of the logarithm base depends on the set error in this sub-scope. We set a processing error $\delta = 0.1\%$. Then, the values of the logarithm bases in the sub-scopes are $\zeta_1 = 0.3981$, $\zeta_2 = 0.912$, $\zeta_3 = 0.9908$, and $\zeta_4 = 0.999$ (the base of the fourth sub-scope, ζ_4, corresponds to the error $\delta = 0.1\%$).

Modelling was carried out from a reference voltage of 10 V over a processing range of 1 mV to 10 V for any eight input voltage values. Three of these were in the 1 mV–1 V range.

The compensation voltage variation is shown with separate asterisks, as this representation accurately reproduces the discrete nature of the variation in LADC processing results.

The modelling diagrams of the operation of the new LADC with a variable logarithm base are given in Figure 4. The essence of the new method is the much shorter processing length, which is less than 25 steps, and the fact that all graphs converge not to the value of the input quantity but to the error value. This article presents some of the error graphs obtained. As for the usual method with a logarithm basis transformation, the errors of the first processing sub-scopes do not determine the final error or the corresponding accuracy. Therefore, next to the error plots over the entire input voltage scope, error graphs for the last two processing sub-scopes are given.

Figure 5 shows the relative processing error at the input voltage value $U_{IN} = 9.5$ V. If on the first processing sub-scope the error is 55% (for a value so close to the upper limit of the processing scope of the input voltage value, the first sub-scope will execute in one step), on the second it will already decrease to 2%, on the third to 0.15%, and on the fourth it will not exceed the set 0.1%. The final processing error is equal to 0.035%.

The errors for other input voltages undergo similar changes. In particular, for an input voltage of $U_{IN} = 5$ V (Figure 6), the first sub-scope of processing also takes place in one step, but the error obtained there is close to 10%. In the second sub-scope, this reduces to 1.88%, in the third sub-scope it reduces to 0.265%, and the final processing error obtained in the fourth sub-scope will be 0.037%.

Below are graphs for input voltages at the lower end of the processing scope, namely for $U_{IN} = 1$ V (Figure 7) and $U_{IN} = 0.001$ V (Figure 8). It is worth noting that for these input voltage values, the first sub-scope of processing takes place over all of the maximum 10 steps allowed.

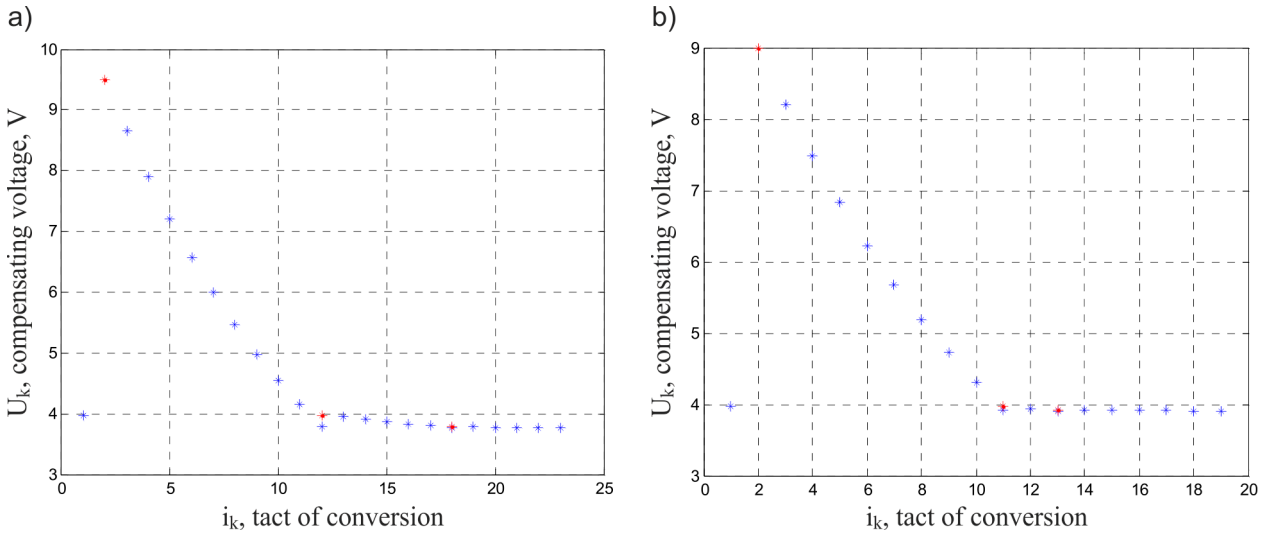

Figure 4. *Cont.*

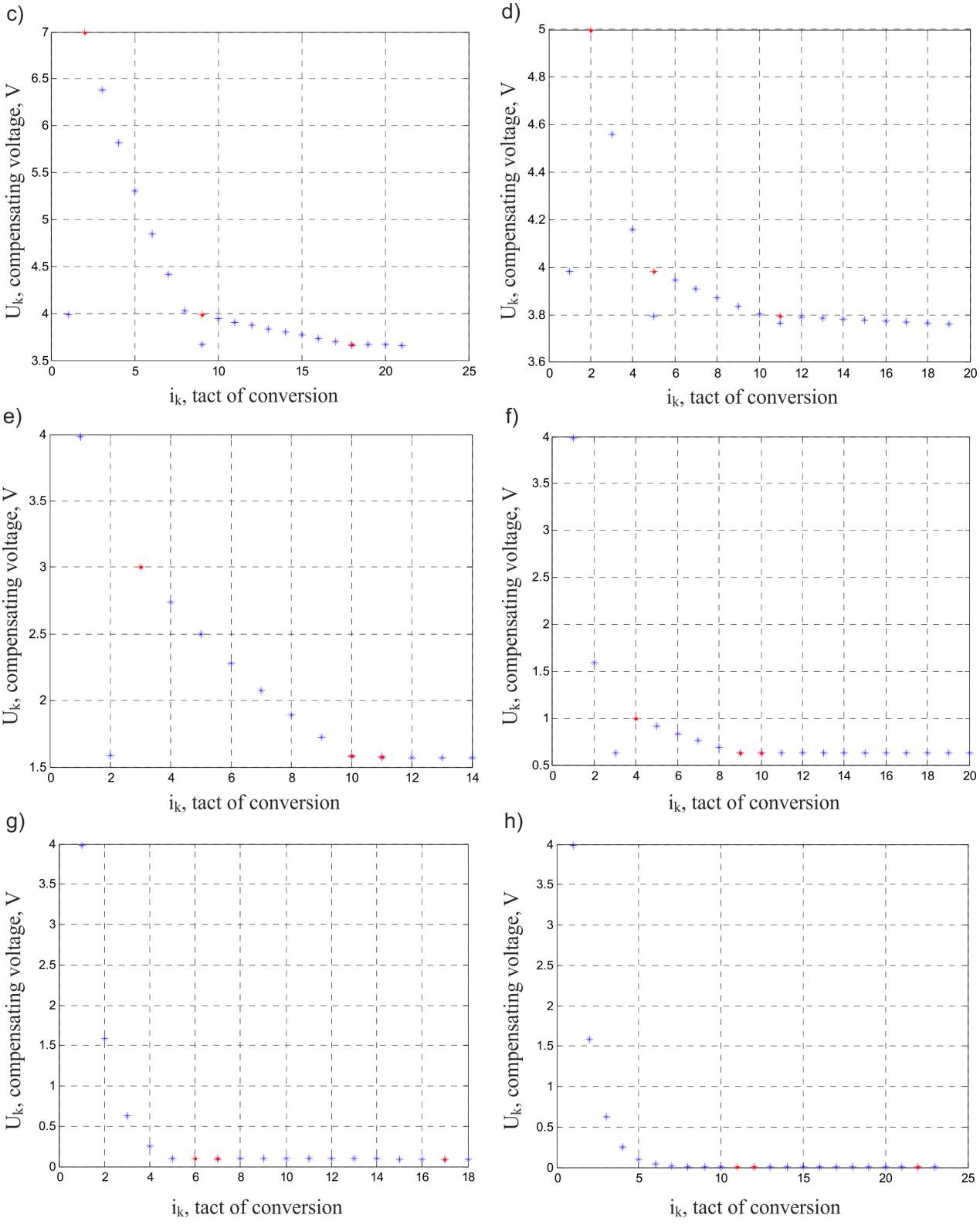

Figure 4. Modelling graphs of the operation of the new LADC with a variable logarithm base at input voltage values: (**a**) U_{IN} = 9.5 V; (**b**) U_{IN} = 9 V; (**c**) U_{IN} = 7 V; (**d**) U_{IN} = 5 V; (**e**) U_{IN} = 3 V; (**f**) U_{IN} = 1 V; (**g**) U_{IN} = 0.1 V; and (**h**) U_{IN} = 0.001 V.

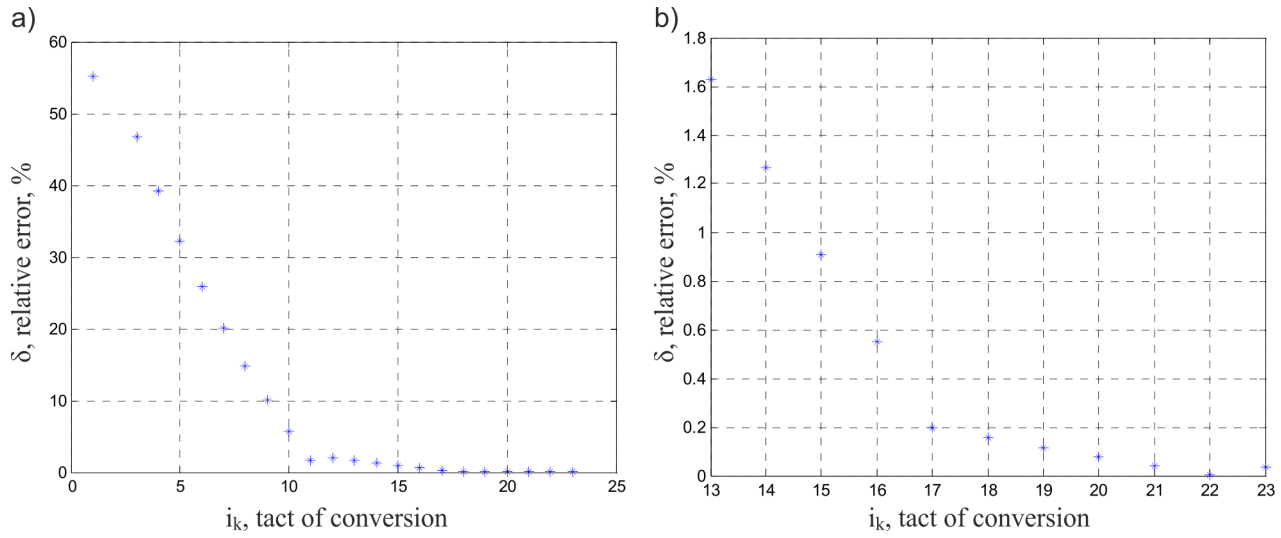

Figure 5. Graphs of the relative processing error of the new LADC with a variable logarithm base at an input voltage value of U_{IN} = 9.5 V (**a**) in the entire scope and (**b**) in the last two sub-scopes.

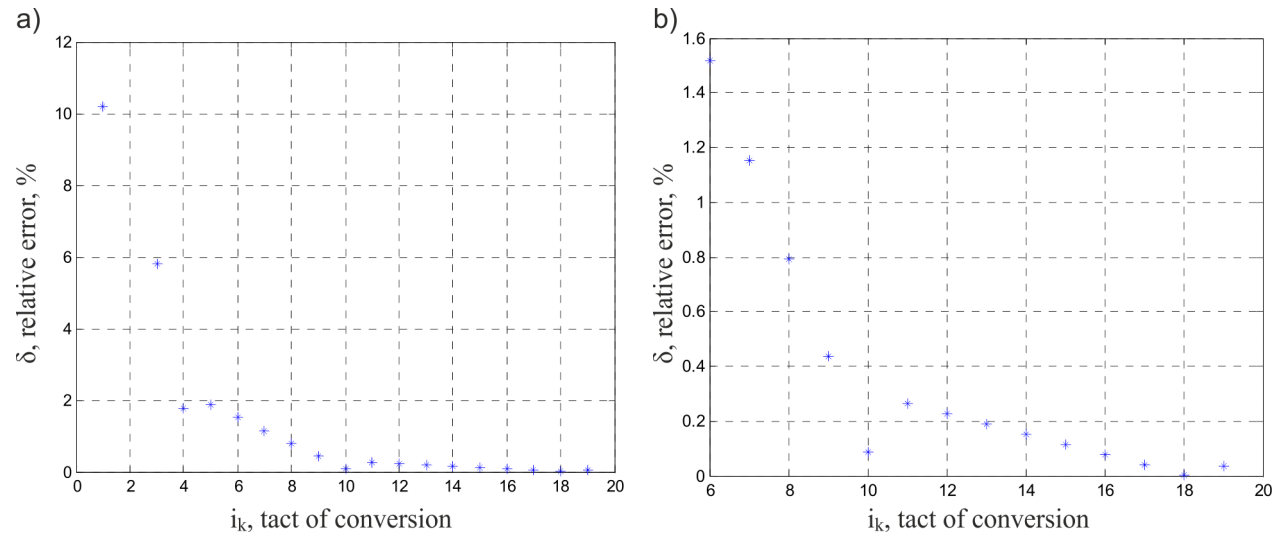

Figure 6. Graphs of the relative processing error of the new LADC with a variable logarithm base at an input voltage value of U_{IN} = 5 V (**a**) in the entire scope and (**b**) in the last two sub-scopes.

For an input voltage of U_{IN} = 1 V, the error values decrease in the first sub-scope from 29% to almost 4%, in the second sub-scope to 0.6%, and in the third sub-scope to less than 0.06%. The final error at the end of the fourth sub-scope will be 0.005%. Note that such a value will correspond to better converters, as 14-bit ADCs have an error of 0.00625%. For an input voltage of U_{IN} = 0.001 V, the voltage error for a period of ten steps of the first sub-scope decreases from 39% to 0.001%; the second sub-scope takes place in one step, and the error is 0.00087%. During the third sub-scope (processing takes place in one step), the voltage error reduces to 4.4736×10^{-6}%. This value is retained over the course of the only step in the fourth processing sub-scope.

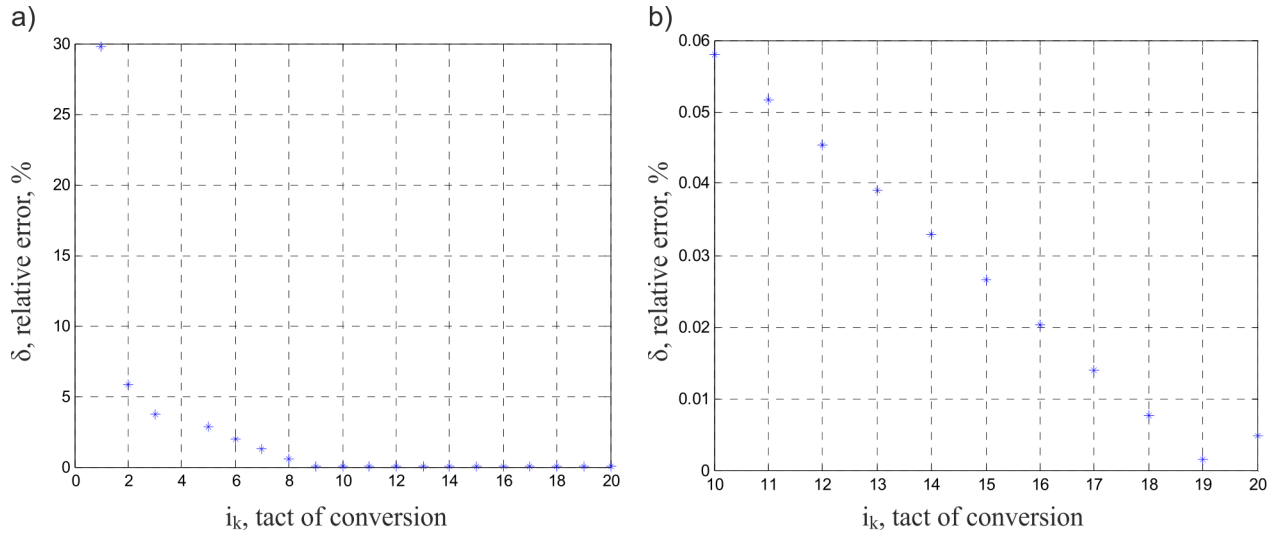

Figure 7. Graphs of the relative processing error of the new LADC with a variable logarithm base at the input voltage value U_{IN} = 1 V (**a**) in the entire scope and (**b**) in the last two sub-scopes.

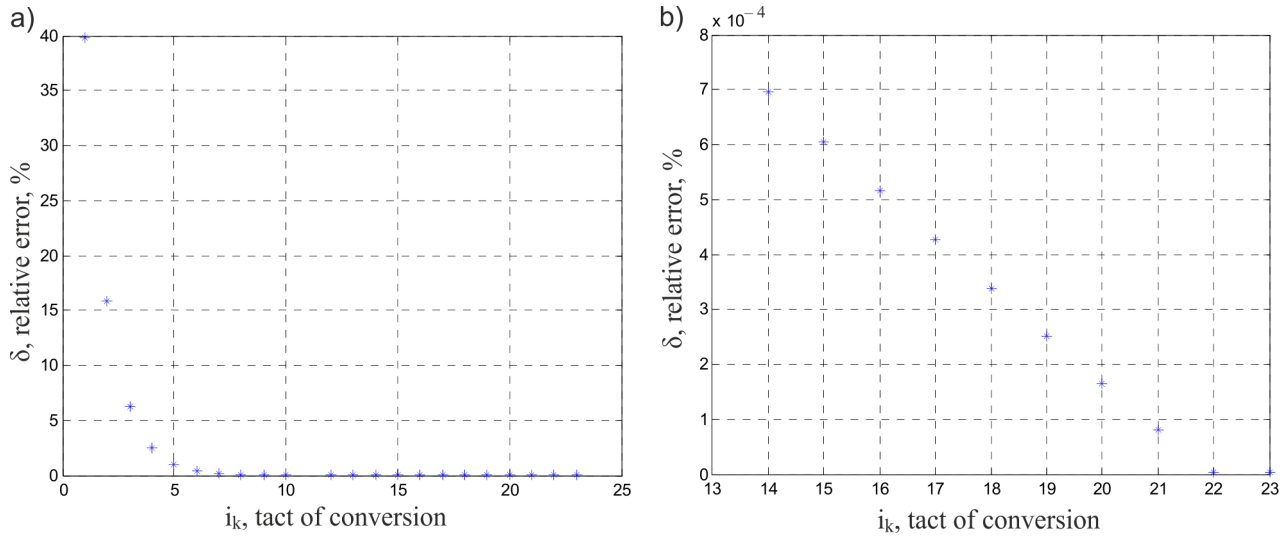

Figure 8. Graphs of the relative processing error of the new LADC with a variable logarithm base at the input voltage value U_{IN} = 0.001 V (**a**) in the entire scope and (**b**) in the last two sub-scopes.

The ideal value of the output code is expressed using the formula

$$N = \frac{1}{\log \zeta} \cdot \log \frac{U_{IN}}{U_o} \tag{12}$$

while the nominal value of the output code is determined using the same formula, substituting the input and reference voltages with the minimum and nominal values of the input signals respectively,

$$N_n = \frac{1}{\log \zeta} \cdot \log \frac{U_{IN_{\min}}}{U_{IN_n}} \tag{13}$$

The output code error is determined at the end of processing.

The output code for four sub-scopes is determined from formula (9), and for five sub-scopes, there will be one more component in the output code expression

$$N = \nu_1 \cdot n_1 - \nu_2 \cdot n_2 + \nu_3 \cdot n_3 - \nu_4 \cdot n_4 + \nu_5 \cdot n_5 \tag{14}$$

A general graph of the voltage error over the entire input voltage range, namely from 1 mV to 10 V, is given in Figure 9.

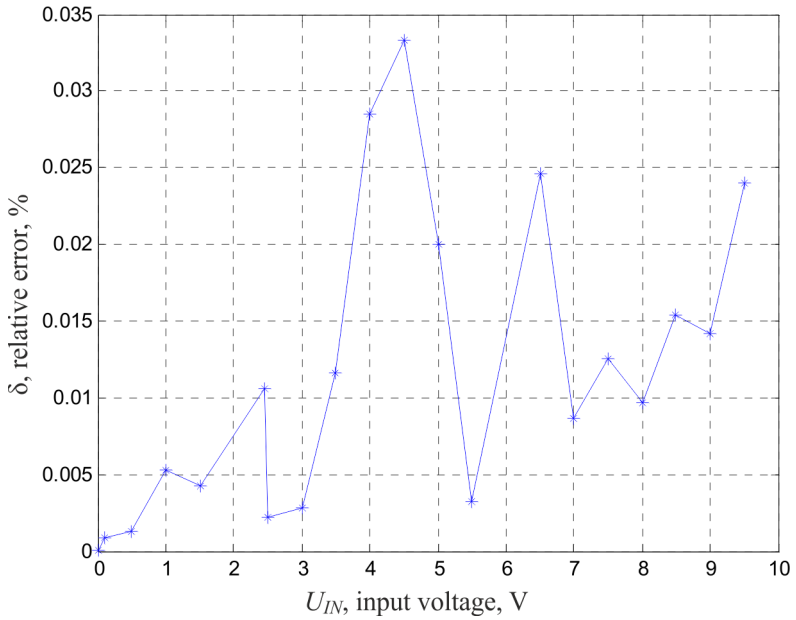

Figure 9. Graphs of the relative voltage processing error of the new LADC with a variable logarithm base at input voltages from 1 mV to 10 V.

Graph of the output code error is given in Figure 10.

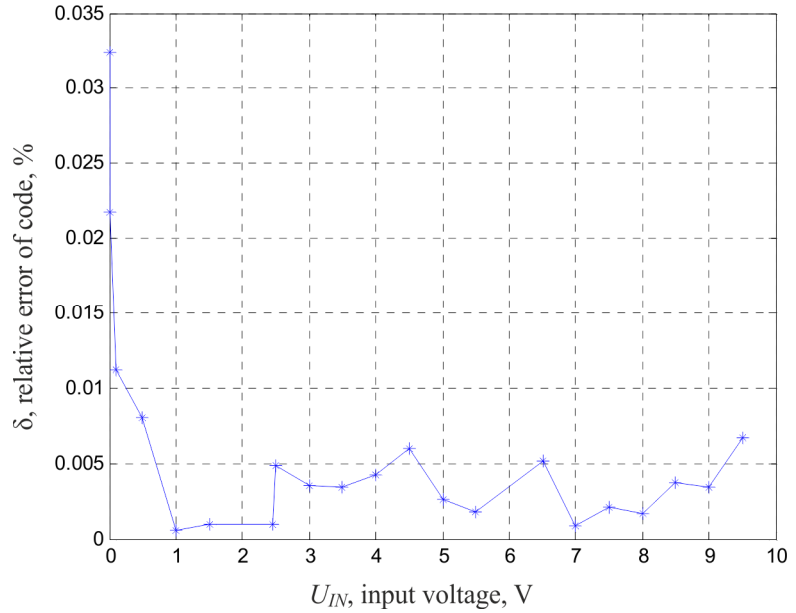

Figure 10. Graph of the relative output code error of the new LADC with a variable logarithm base at input voltages from 1 mV to 10 V.

It can be seen from the above that in the input voltage range up to 1 V, the accuracy of the new variable base logarithm converter corresponds to that of 12-bit converters. In the range from 1 V to 10 V (Figure 11), its error is within 0.0005–0.007%, which corresponds to the accuracy of 13–14-bit converters.

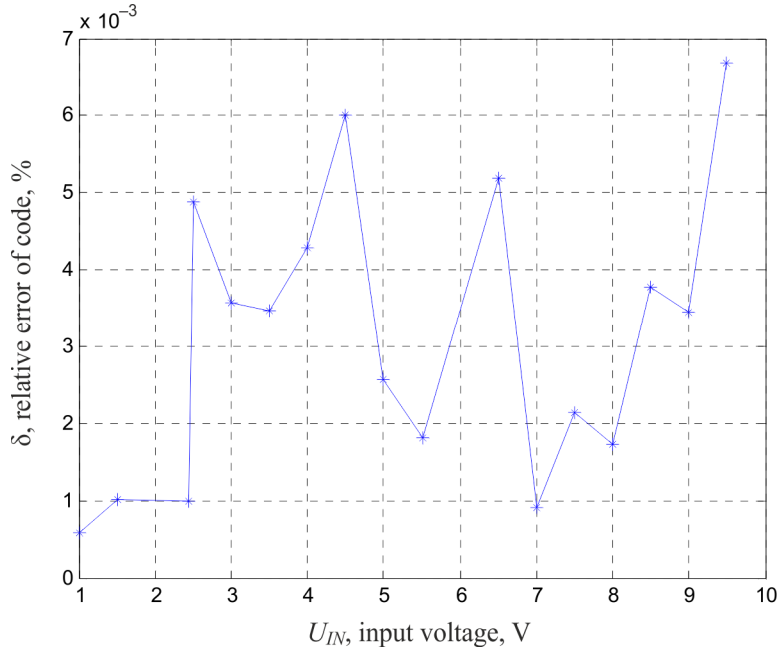

Figure 11. Graphs of the relative error of the output code of the new LADC with a variable logarithm base at input voltages from 1 V to 10 V.

At the same time, the speed of the new converter exceeds not only that of known analogue converters but also that of the classic variable-base logarithm converters considered above (Figure 12). The extreme values in the input voltage range have the longest processing length, while processing for all input voltages ends in the range of 22–26 steps, corresponding to 55–65 μs.

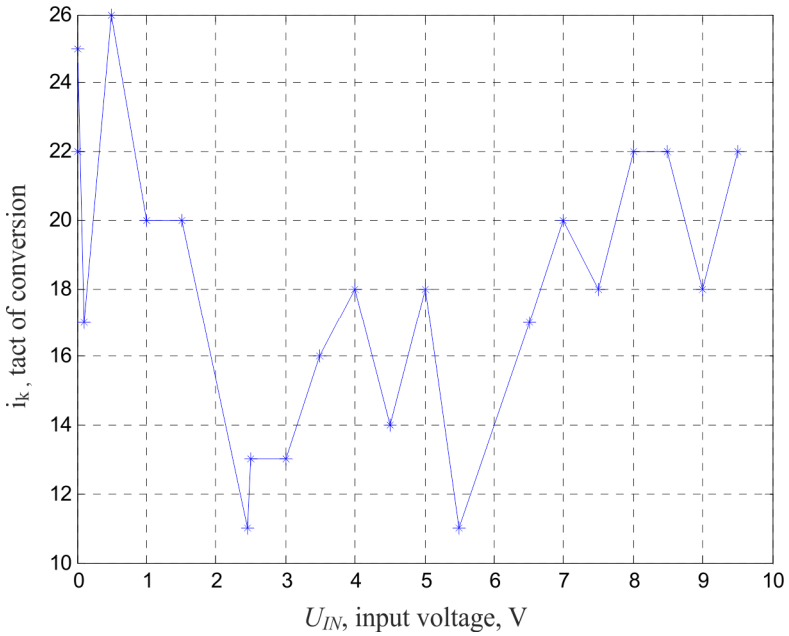

Figure 12. Graphs of the number of processing steps of the new LADC with a variable logarithm base at input voltages from 1 mV to 10 V.

Since the developed LADC with a variable logarithm basis has a high processing speed and the errors that satisfy us are in the lower half of the scope, we carried out tests on the converter for an increased number of processing sub-scopes.

The number of sub-scopes was increased to five. The logarithm base for the fifth sub-scope was $\zeta = 0.9999$. The maximum number of steps remained equal to 10 in each sub-scope.

We obtained LADC performance graphs and relative processing error graphs, analogous in principle to those for converters built with processing on four sub-scopes. We carried out the modelling for the same input voltages as in the four sub-scopes, in particular: $U_{IN} = 9.5$ V; $U_{IN} = 9$ V; $U_{IN} = 7$ V; $U_{IN} = 5$ V; $U_{IN} = 3$ V; $U_{IN} = 1$ V; $U_{IN} = 0.1$ V; and $U_{IN} = 0.001$ V. Considering the error value for each of the input voltages on the last fifth sub-scope, graphs of the relative conversion error of the converter are shown (Figure 13).

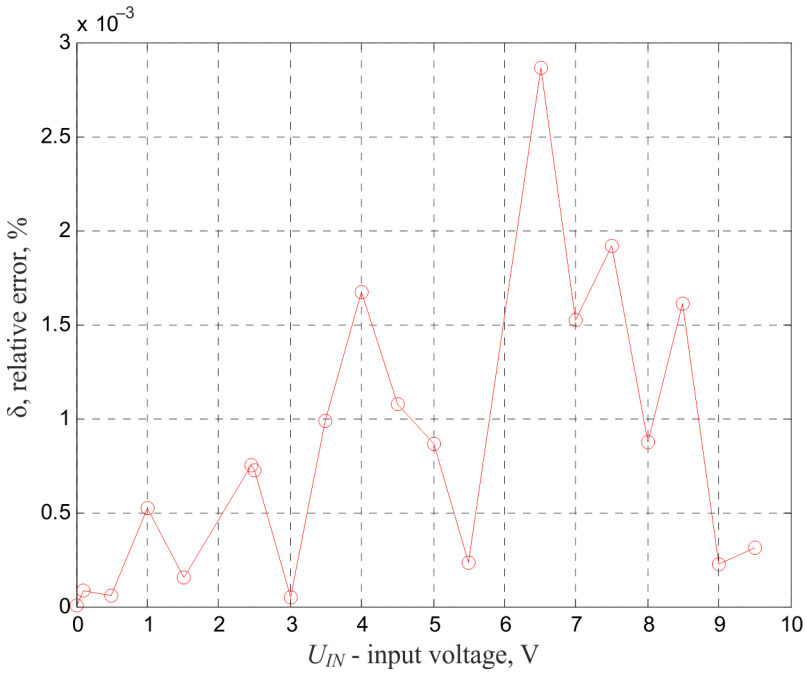

Figure 13. Graphs of the relative voltage conversion error of the new LADC with a variable logarithm base in the input voltage scope from 1 mV to 10 V for five sub-scopes.

The highest relative error values were obtained in the upper part of the scope (Figure 11). When processing on five sub-scopes, the relative error decreased several times. For example, the relative processing error for $U_{IN} = 9.5$ V in the final phase of the first sub-scope is 0.002%, as opposed to 2% when processing in four sub-scopes. Graphs of the relative processing errors for processing in five sub-scopes are shown in Figure 13.

Relative voltage processing errors do not exceed 0.0027%, and for most input voltages, they are less than 0.002%.

For the relative error of the output code, the values are in the range of 0.0003% to 0.001% when processing in five sub-scopes of input voltages from 1 mV to 10 V (Figure 14). This corresponds to the accuracy of a 16-bit converter. It should be noted that if you limit the input voltage scope in the range from 1 V to 10 V, the relative error value of the output code will not exceed 0.00085%.

As suspected, the processing duration increased compared to processing on the four sub-scopes. However, at the upper end of the input voltage scope, the processing time does not exceed 72.5 µs (29 steps), and at the lower end, from 1 mV to 1 V, it is in the range of 82.5 µs (33 steps) to 107.5 µs (43 steps) (Figure 15). In the input voltage range of 1 V to 10 V, the processing time is less than 75 µs (30 steps). That is to say, in the range from 1 V to 10 V, we obtained a shorter processing time compared to a classical variable-base logarithmic analogue-to-digital converter.

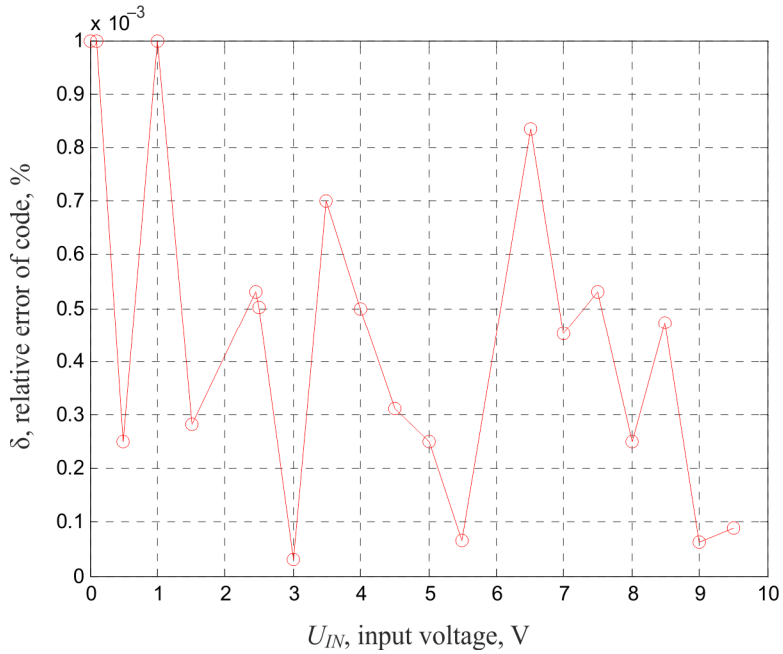

Figure 14. Graphs of the relative output code error of the new LADC with a variable logarithm base at input voltage from 1 mV to 10 V with 5 sub-scopes.

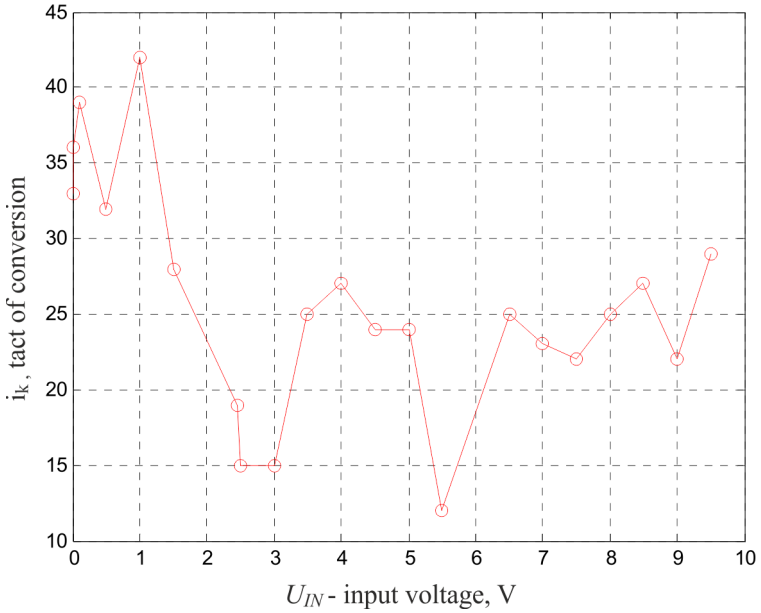

Figure 15. Graphs of processing duration (number of steps) of the new LADC with a variable logarithm base at input voltage from 1 mV to 10 V with 5 sub-scopes.

The graphs of the relative voltage conversion error (Figure 16), relative output code error (Figure 17), and conversion duration (Figure 18) show the relationships obtained for four sub-scopes (in blue) and for five sub-scopes (in red).

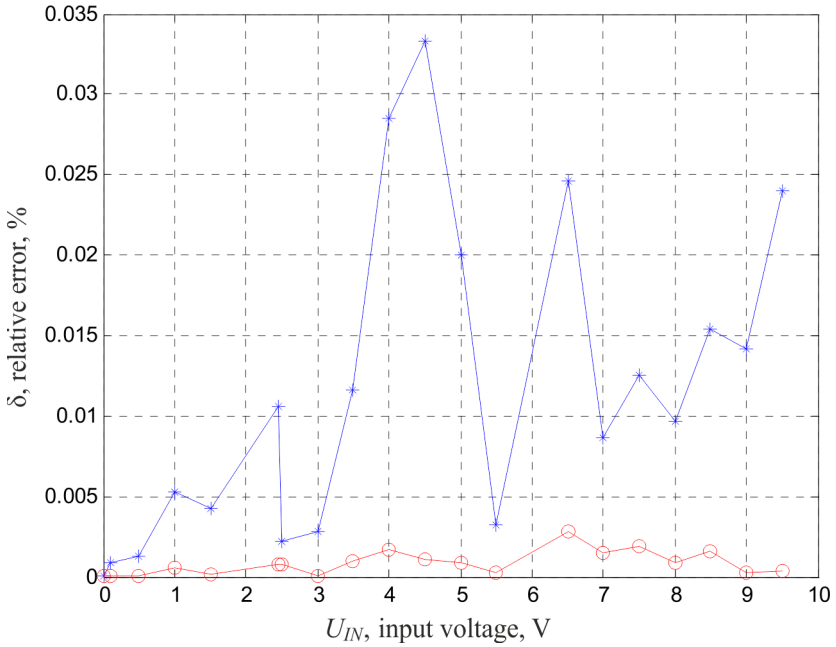

Figure 16. Comparative graphs of the relative voltage processing error of the new LADC with a variable logarithm base in the input voltage range from 1 mV to 10 V, with processing in 4 sub-scopes (blue *) and 5 sub-scopes (red o).

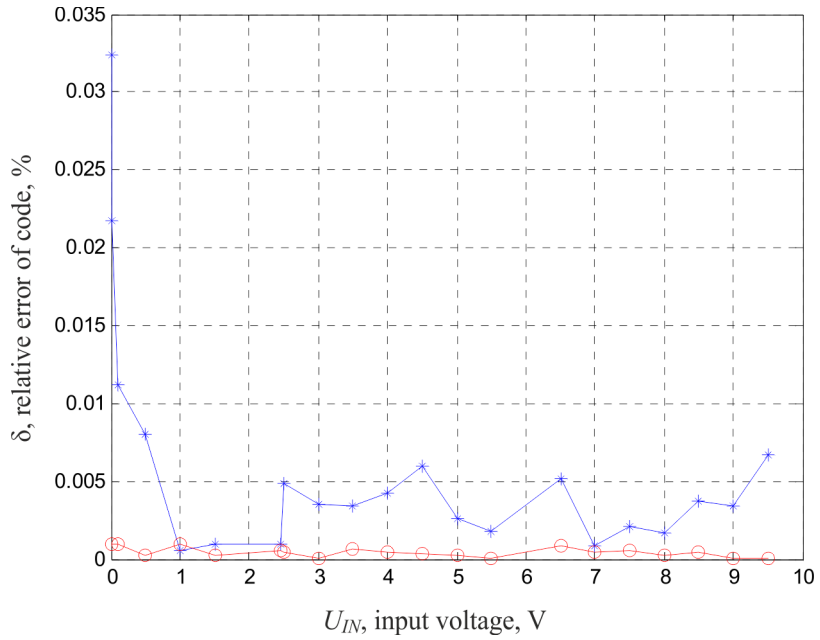

Figure 17. Comparative graphs of the relative error of the output code of the new LADC with a variable logarithm base in the input voltage range from 1 mV to 10 V with 4 sub-scopes (blue *) and 5 sub-scopes (red o).

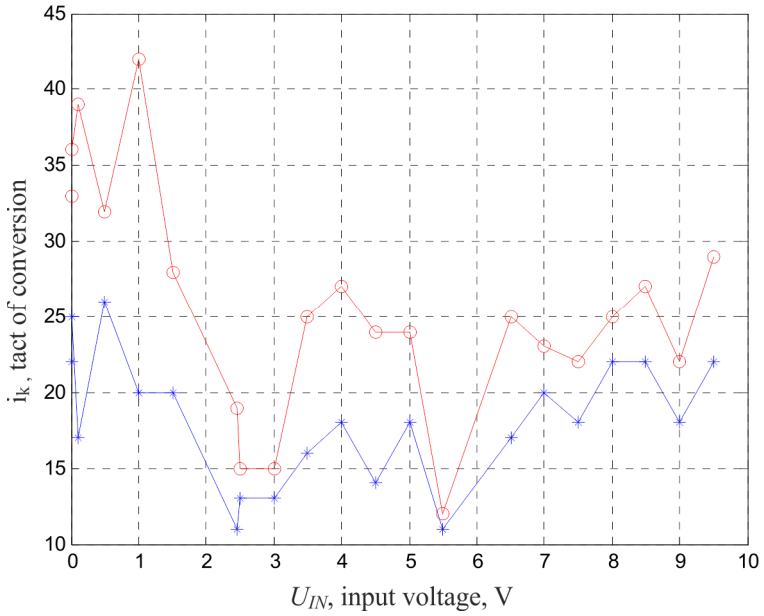

Figure 18. Comparative graphs of the processing duration (number of steps) of a new LADC with a variable logarithm base in the input voltage range from 1 mV to 10 V, with processing in 4 sub-scopes (blue *) and 5 sub-scopes (red o).

Table 1 provides a comparison between known LADCs and new LADCs, in which the proposed logarithmic analogue-to-digital processing method was implemented using switched capacitors with a variable logarithmic base.

Table 1. Comparison of known and new LADCs.

LADC	Logarithm Base	Input Voltage Scope	Number of Sub-Scopes	Output Code Error, δN	Number of Steps and Processing Time
1	3	4	5	7	8
Known [6] LADC with SA	variable	1 mV–10 V	-	0.025% (12 bit)	-
Known [7] LADC with SA	variable	1 mV–10 V	-	0.0015% (16 bit)	-
Known [15] LADC	variable	1 mV–10 V	4	0.01%	40 steps; 100 µs
Proposed LADC	variable	1 mV–10 V	4	0.01%	26 steps; 65 µs
		1 mV–1 V	4	≤0.03%	
		1 V–10 V	4	≤0.007%	
		1 mV–10 V	5	≤0.001%	42 steps; 105 µs
		1 mV–1 V	5		+3 steps; 7.5 µs
		1 V–10 V	5		−11 steps; 27.5 µs

In summary, it can be concluded that, compared to a classic converter with a variable logarithm base, increasing the number of sub-scopes increases accuracy and reduces processing speed, and one may recommend the developed new LADC for use precisely with the number of sub-scopes increased to five. Its relative output code error will not exceed 0.001% over the entire input voltage scope, namely from 1 mV to 10 V.

The increase in accuracy does not significantly worsen the speed. In the range from 1 mV to 1 V, it exceeds by 7.5 µs (3 steps) the processing time of a classical converter with a variable logarithm base for four sub-scopes. In contrast, in the 1 V to 10 V range, the

processing time is 27.5 µs (11 steps) less than that of a classical LADC with a variable logarithm base.

The research confirms that the proposed LADC with a variable logarithm base, compared to known analogues, increases the accuracy and speed of processing and gives the user the ability to select these parameters in advance.

5. Conclusions

The study of the new logarithmic analogue-to-digital conversion method using switched capacitors with a variable logarithmic base shows that:

1. A logarithmic analogue-to-digital processing method was developed for the first time, in which in each processing step, the absolute processing error is compensated until the set value is reached, which increases the speed and accuracy of processing.

2. LADCs realized by the proposed method are characterised by the following:

- The desired speed is determined by setting the appropriate number of steps;
- The choice of accuracy is determined by selecting the number of sub-scopes;
- They have a higher speed in the 1 mV to 10 V input voltage range compared to known analogues:

(a) With four sub-scopes, their processing time does not exceed 65 µs (26 steps), with an error of not more than 0.01%, and in analogues, the processing time reaches 40 steps;
(b) With five sub-scopes, the processing time shall not exceed 105 µs (42 steps), with an error of not more than 0.001%, and in analogues, the processing time reaches 50 steps.

3. LADCs implemented on the basis of the new logarithmic analogue–digital method of processing, using switched capacitors with a variable logarithm base, are converters with high accuracy and rapid action.

Author Contributions: Conceptualization, Z.M., M.M., I.Z., L.M., A.S. and Z.S.; methodology, Z.M., I.Z., M.M., L.M., A.S. and Z.S.; writing—original draft preparation, Z.M., M.M., I.Z., L.M., A.S. and Z.S.; writing—review and editing, Z.M., M.M., I.Z., L.M., A.S. and Z.S.; visualization, Z.M., M.M., I.Z., L.M., A.S. and Z.S.; supervision, Z.M., M.M., I.Z., L.M., A.S. and Z.S.; funding acquisition, A.S. and Z.S. All authors have read and agreed to the published version of the manuscript.

Funding: The research was carried out as part of the research work: Analysis of the operation of power and control systems in the systems of the Industry 4.0 directive—source of financing: 03.0.21.00/1.02.001 SUBB.EKUE. 23.002, Poland.

Data Availability Statement: Data are contained within the article.

Acknowledgments: The article was created as part of scientific cooperation between Kielce University of Technology and Lviv Polytechnic National University.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Pagin, M.; Ortmanns, M. Evaluation of logarithmic vs. linear ADCs for neural signal acquisition and reconstruction. In Proceedings of the 39th Annual International Conference of the IEEE Engineering in Medicine and Biology Society, Jeju, Republic of Korea, 11–15 July 2017; pp. 4387–4390.
2. Azarov, O.D.; Bilichenko, N.O.; Zakharchenko, S.M. *High-Speed High-Precision ADC with Charge Redistribution with Self-Calibrating Weight Redundancy: Monograph*; VNTU: Vinnytsia, Ukraine, 2016; 140p, ISBN 978-966-641-665-3.
3. Sundarasaradula, Y.; Constandinou, T.G.; Thanachayanont, A. A 6-Bit, Two-Step, Successive Approximation Logarithmic Adc for Biomedical Applications. 2016. Available online: https://madlab.cpe.ku.ac.th/ThailandResearch/?itemID=120927 (accessed on 15 September 2023).
4. Petilli, E.M. Logarithmic Analog to Digital Converter Devices and Methods Thereof. U.S. Patent 20170179972, 22 June 2017.
5. Zakharchenko, S.M. Structures of Integral Capacitors as a Basis for Construction of Capacitor Matrices for ADC with Charge Redistribution with Weight Redundancy/S. M. Zakharchenko//Scientific Works of VNTU. 2009. No 4. Available online: http://praci.vntu.edu.ua/index.php/praci/article/view/163 (accessed on 15 September 2023).
6. Szcześniak, A. *Analiza Przetwarzania Sygnałów Logarytmicznego Przetwornika Analogowo-Cyfrowego z Sukcesywną Aproksymacją*; Kielce University of Technology: Kielce, Poland, 2019; ISBN 978-83-65719-48-5.

7. Mychuda, Z.; Zhuravel, I.; Mychuda, L.; Szcześniak, A.; Szcześniak, Z.; Yelisieieva, H. Mathematical modelling of the influence of parasitic capacitances of the components of the logarithmic analogue-to-digital converter (LADC) with a successive approximation on switched capacitors for increasing accuracy of conversion. *Electronics* **2022**, *11*, 1485. [CrossRef]
8. Mychuda, L.Z. *Theory and Practice of Analog-to-Digital Functional Converters on Switched Capacitors. Thesis for a Sc.D. (Doctor of Technical Sciences) Degree by Speciality 05.13.05—Computer Systems and Components*; Lviv Polytechnic National University, Ministry of Education and Science of Ukraine: Lviv, Ukraine, 2019; p. 40.
9. Inagaki, Y.; Sugimori, Y.; Ioka, E.; Matsuya, Y. Logarithmic Compression ADC Using Transient Response of a Comparator/IEICE TRANSACTIONS on Electronics. *IEICE Trans. Electron.* **2017**, *E100-C*, 359–362. [CrossRef]
10. Santos, M.; Guilherme, J.; Horta, N. *Logarithmic Voltage-to-Time Converter for Analog-to-Digital Signal Conversion*; Springer International Publishing: Berlin/Heidelberg, Germany, 2019; Available online: https://www.springerprofessional.de/en/logarithmic-adc/16620222 (accessed on 15 September 2023).
11. Offen, R. Logarithmierender Analog-Digital Wandler. Patent No. DE102008007207A1, 6 August 2009.
12. Moon, J.H.; Kim, D.Y.; Song, M.K. Logarithmic Single-Slope Analog Digital Convertor, Image Sensor Device and Thermometer Using the Same, And Method for Logarithmic Single-Slope Analog Digital Converting. Patent No. KR20110064514A, 15 June 2011.
13. Watson, B. Analog to Digital Conversion Using Recurrent Neural Networks. Patent No. US007345604B2, 18 March 2008.
14. Lee, J.; Rhew, H.G.; Kipke, D.R.; Flynn, M.P. A 64 Channel Programmable Closed-Loop Neurostimulator with 8 Channel Neural Amplifier and Logarithmic ADC. *IEEE J. Solid-State Circuits* **2010**, *45*, 1935–1945. [CrossRef]
15. Sirimasakul, S.; Thanachayanont, A.; Jeamsaksiri, W. Low-Power Current-Mode Logarithmic Pipeline Analog-to-Digital Converter for ISFET based pH Sensor. In Proceedings of the 2009 9th International Symposium on Communications and Information Technology, Icheon, Republic of Korea, 28–30 September 2009; pp. 1340–1343.
16. Ballo, A.; Grasso, A.D.; Palumbo, G. A Simple and Effective Design Strategy to Increase Power Conversion Efficiency of Linear Charge Pumps. *Int. J. Circuit Theory Appl.* **2020**, *48*, 157–161. [CrossRef]
17. Ballo, A.; Grasso, A.D.; Palumbo, G.; Tanzawa, T. Charge Pumps for Ultra-Low-Power Applications: Analysis, Design, and New Solutions. *IEEE Trans. Circuits Syst. II Express Briefs* **2021**, *68*, 2895–2901. [CrossRef]
18. Esmailiyan, A.; Schembari, F.; Staszewski, R.B. A 0.36-V 5-MS/s Time-Mode Flash ADC with Dickson-Charge-Pump-Based Comparators in 28-Nm CMOS. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2020**, *67*, 1789–1802. [CrossRef]
19. Esmailiyan, A.; Du, J.; Siriburanon, T.; Schembari, F.; Staszewski, R.B. Dickson-Charge-Pump-Based Voltage-to-Time Conversion for Time-Based ADCs in 28-Nm CMOS. *IEEE Open J. Circuits Syst.* **2021**, *2*, 23–31. [CrossRef]
20. Park, J.-E.; Hwang, Y.-H.; Jeong, D.-K. A 0.5-V Fully Synthesizable SAR ADC for On-Chip Distributed Waveform Monitors. *IEEE Access* **2019**, *7*, 63686–63697. [CrossRef]
21. Shen, Y.; Zhu, Z.; Liu, S.; Yang, Y. A Reconfigurable 10-to-12-b 80-to-20-MS/s Bandwidth Scalable SAR ADC. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2017**, *65*, 51–60. [CrossRef]
22. Kumar, C.; Pavan, S. Power-Noise Trade-Offs in Continuous-Time Pipelined ADCs and Active Filters. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2023**, *70*, 3832–3842. [CrossRef]
23. Liang, Y.; Li, C.; Liu, S.; Zhu, Z. A 14-b 20-MS/s 78.8 dB-SNDR Energy-Efficient SAR ADC With Background Mismatch Calibration and Noise-Reduction Techniques for Portable Medical Ultrasound Systems, in IEEE TBioCAS. *IEEE Trans. Biomed. Circuits Syst.* **2022**, *16*, 200–210. [CrossRef] [PubMed]
24. Oh, D.R.; Seo, M.J.; Ryu, S.T. A 7-Bit Two-Step Flash ADC With Sample-and-Hold Sharing Technique. *IEEE J. Solid-State Circuits* **2022**, *57*, 2791–2801. [CrossRef]
25. Yi, P.; Liang, Y.; Liu, S.; Xu, N.; Fang, L.; Hao, Y. A 625kHz-BW, 79.3dB-SNDR Second-Order Noise-Shaping SAR ADC Using High-Efficiency Error-Feedback Structure. *IEEE Trans. Circuits Syst. II Express Briefs* **2021**, *69*, 859–863. [CrossRef]

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.