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A H-Bridge-Multiplexing-Based Novel Power Electronic Transformer

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Abstract: Cascaded H-bridge power electronic transformers (CHB-PET) play a pivotal role in distribution grids and their efficient operation. The input series and output parallel (ISOP) configurations result in a huge number of power switching devices, high-frequency transformers (HFT), and capacitors in high-voltage, high-capacity CHB-PET, leading to the need for high hardware costs and huge-sized CHB-PET, which further poses a significant challenge to the engineering feasibility and marketability of the CHB-PET. To address these issues, a CHB-PET topology is proposed in this paper. The novel topology exploits the concept of multi-frequency modulation to achieve power decoupling and power unit multiplexing through reasonable LC resonant frequency selection, which optimizes the ISOP structure and ultimately reduces the hardware cost and size of the CHB-PET. In this study, the effectiveness of reducing the number of power switching devices and HFT is firstly analyzed, and after describing its working principle, the control strategy of each power conversion link of PET is discussed before the correctness and effectiveness of the CHB-PET topology and control strategy proposed in this paper are verified via simulation.

Keywords: cascade H-bridge; power electronic transformer; mixed frequency modulation; power unit multiplexing

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1. Introduction

In the pursuit of "carbon neutrality", there is a global expansion in the scale and utilization of renewable energy sources such as solar energy and wind energy. As the development and utilization of new energy forms emerge, the deployment of smart grids [1–3] has emerged as a powerful strategy to achieve "carbon neutrality." Within the framework of the smart grid, the power electronic transformer assumes a pivotal role in facilitating the bidirectional flow of electrical energy and providing interfaces for various forms of new energy [4,5]. Consequently, extensive research is being conducted to explore the topology and control strategies of power electronic transformers, owing to their significant implications.

Presently, in the design of power electronic transformers (PET), various universities and institutes [6–12] have widely adopted the topology depicted in Figure 1. When a PET is employed in distribution networks, the H-bridge can be cascaded to enhance the voltage level of the rectifier when the power semiconductor device's voltage capability is limited. This cascaded structure, known as Cascade H-bridge PET (CHB-PET), incorporates a number of high-frequency transformers (HFT) aligned with the cascaded units. Among the multiple cascaded cells, an input series output parallel (ISOP) configuration is adopted. Each individual cascaded cell, referred to as a submodule, consists of an AC/DC converter connected in series with a dual active bridge DC/DC converter. While this structure improves the performance of the PET, it necessitates the use of a larger number of power switching devices and HFTs. Consequently, this increased hardware demand directly results in higher costs and larger volumes, which hampers the engineering implementation and marketability of PETs [13–15].

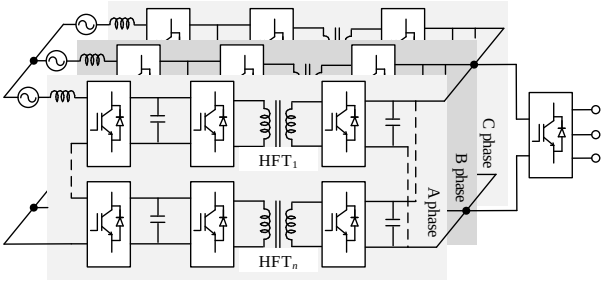


Figure 1. Traditional three-phase CHB-PET topology.

One of the developmental directions of CHB-PET focuses on improving the power density of the entire PET system by reducing the number of power conversion stages, power switching devices, and HFTs [16–20]. In addressing the limitations of CHB-PET in distribution networks, the topology can be enhanced by multiplexing the bridge arm of the H-bridge configuration. In a previous study [16], a high-power-density PET suitable for medium and high voltage distribution networks was designed. The frequency selection functionality of series resonance was employed to effectively reduce the usage of power devices and HFTs. Furthermore, in another study [17], the concept of mixing modulation was introduced, leading to the design of two novel cascaded PET topologies. Additionally, in a different research work [18], a full-bridge compensation module was introduced to devise a single-phase cascaded PET topology.

H-bridge multiplexing is one idea for developing a new CHB-PET, and one study [21] designed a PET based on time-sharing multiplexing by analogy with the time-sharing multiplexing of channels through communication collars. In this paper, under the same idea, a new three-phase CHB-PET topology is proposed, which is shown in Figure 2. Compared with the topology in [21], the novel structure designed in this paper adopts the idea of frequency division multiplexing and uses a passive network for demodulation, which reduces the difficulty of control.

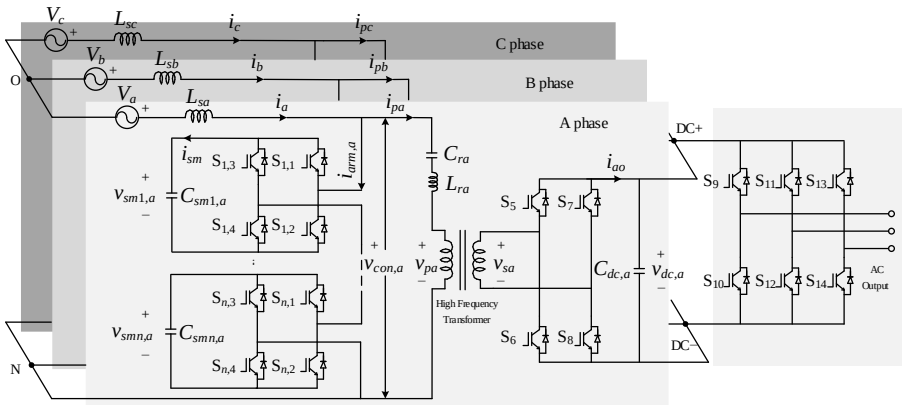


Figure 2. Novel three-phase cascade PET topology.

The novel topology of Figure 2 adopts the full bridge as the submodule, enabling the input-side converter to transmit both power frequency and high-frequency power by multiplexing the H-bridge arm. In comparison to the traditional three-stage PET [22–30], this novel topology retains the DC bus port while eliminating the H-bridge on the input side of the dual active bridge (DAB) converter. Compared with the ISOP structure, the number of power devices and HFTs is reduced, effectively lowering the hardware cost and overall machine volume, while simultaneously improving the power density and compactness of the PET.

The subsequent section provides a detailed description of this novel topology and elucidates its operational principles. The control structure design and main circuit parameter

considerations are discussed extensively in Sections 3 and 4, respectively. Finally, according to the topologies shown in Figures 1 and 2, the corresponding simulation models are built in PLECS, respectively, and an in-depth simulation analysis is carried out via comparison.

By comprehensively evaluating the performance of the proposed topology and verifying its effectiveness through simulation analysis, this study contributes to the advancement of CHB-PET technology. The results obtained from this research will facilitate the deployment of more efficient and compact power electronic transformers, fostering their wider adoption in practical applications.

2. Proposing a Novel Topology

2.1. Description of Topology

The proposed novel topology, depicted in Figure 2, showcases the isolation of the power grid and the load through the utilization of high-frequency transformers. In phase A, the primary side of the HFT comprises a cascade of n full-bridge modules, while the secondary side consists of a single full-bridge configuration (S5–S8). The filter inductor L_{sa} acts as a low-pass filter, effectively attenuating high-frequency currents and providing reactive connection. The resonant capacitor C_r and resonant inductor L_r form a band-pass filter, which effectively suppresses power frequency currents while offering a low-impedance pathway for high-frequency currents. The structure of phases B and C mirrors that of phase A. Upon parallel connection of the DC bus, the full bridge configuration (S9–S14) is employed for AC output inversion. For the sake of convenience, the circuit preceding the DC bus is collectively referred to as the front circuit, whereas the inverter and load form the back circuit. Considering the positioning of the high-frequency transformer, the front circuit is further categorized into the primary side circuit and the secondary side circuit. By establishing a clear and well-defined circuit distinction between the front and back circuits and the primary and secondary side circuits, the proposed topology facilitates a comprehensive understanding and analysis of the system's operation and performance. The subsequent sections will delve into a detailed discussion of each circuit's control strategy, ensuring a holistic exploration of the proposed topology's effectiveness and functionality.

2.2. Topology Evolution and Working Principle

The proposed topology in this study is a conceptual integration of the PWM voltage source rectifier (VSR), DAB DC-DC converter, and PWM voltage source inverter (VSI). Figure 3a shows the internal structure of the cascade unit in Figure 1, including the AC/DC conversion and DAB links. In the AC/DC link, when PWM modulation is used, the H-bridge arm voltage is a superposition of multiple frequency voltages when two and more frequency signal waves are used as modulating waves. As shown in Figure 3b, the superposition of signal waves with frequencies of f_{lf} and f_{hf} can drive the H-bridge to output voltages of two frequencies, v_{lf} and v_{hf}. In the DAB link, the equivalent circuits on both sides of the HFT are shown in Figure 3c, which transform the high-frequency voltage v_p into v_k.

The combination of VSR and DAB is the key aspect of the novel topology, as depicted in Figure 3d. According to the previous analysis, the bridge arm of the AC/DC link can be connected to the mains via the low-pass filter L_{sa} and at the same time to the HFT via the LC resonant circuit. The joint action of the low-pass filter and the LC resonant circuit allows the AC voltage components v_{lf} and v_{hf} to be transmitted to the power supply vs. and the HFT, respectively. Zero current switching can be achieved when the frequency of vhf matches the resonant frequency of the LC circuit and the switching frequency of the full-bridge (S5–S8). At this point, the AC square wave nature of v_{hf} aids in reducing losses and improving the efficiency of PET energy conversion. Ultimately, the topology accomplishes power decoupling and enables the reuse of power units.

By establishing this novel topology, this study significantly advances the state of the art in power electronic transformer design and offers enhanced power decoupling

capabilities and power unit reuse. The subsequent sections will provide in-depth analyses of the proposed topology's performance, control strategies, and efficiency evaluation to validate its effectiveness in practical applications.

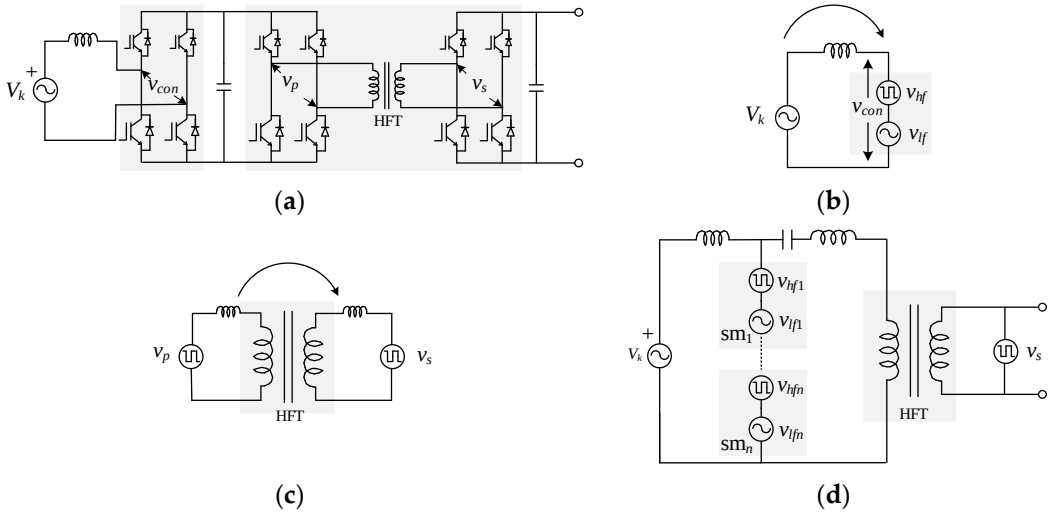


Figure 3. Evolution of the novel CHB-PET topologies. (**a**) The internal structure of the cascade unit; (**b**) sub-module equivalent circuit. (**c**) DAB equivalent circuit; (**d**) novel AC/DC converter structure combining (**b**,**c**).

2.3. Mathematical Models and Switching Signals

Regarding the three-phase PET topology depicted in Figure 2, the rear circuit is associated with a resistive load connected to the low-voltage DC bus. Since the control strategy of the front circuit remains unaffected, the focus of this paper is solely on the analysis of the front circuit. Recognizing that the correlation analysis of three-phase inverters has reached a mature stage, this study exclusively examines the front circuit, which can be represented by its equivalent circuit illustrated in Figure 4.

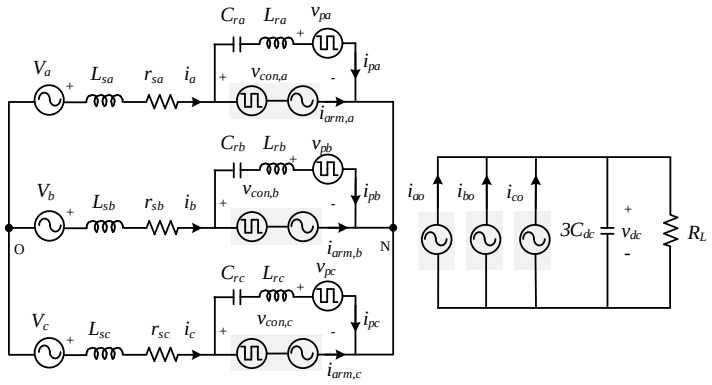


Figure 4. Equivalent circuit of the front stage of CHB-PET.

In this, the AC side inductance L_{sk} (k = a,b,c) includes the inductance of the external reactor and the internal inductance of the power supply; the resistance r_{sk} includes the resistance of the external reactor and the internal resistance of the power supply; inductance L_{rk} comprises an external reactor inductance and a high-frequency transformer leakage inductance; capacitor C_{rk} and inductance L_{rk} form the LC filter.

To facilitate analysis, it is assumed that the parameters of each phase inductor, LC filter, high-frequency transformer, and submodule are identical. Additionally, the subharmonic component of the switching frequency is neglected.

Following a comprehensive examination of the equivalent circuit depicted in Figure 4, equations based on KVL can be derived as follows:

$$L_s \frac{di_k}{dt} = v_k - r_s i_k - v_{con,k} - v_{NO}, \tag{1}$$

where voltage v_k is the three-phase power grid voltage on the AC side and current i_k is the input current on the AC side. $v_{con,k}$ is the mid-point voltage of the bridge arm, which can be decomposed into the components $v_{k,lf}$ and $v_{k,hf}$ whose frequencies are 50 Hz and f_h, respectively, and satisfying $v_{con,k} = v_{k,lf} + v_{k,hf}$.

Equation (1) can be expressed as follows:

$$L_s \frac{di_k}{dt} = v_k - r_s i_k - v_{k,lf} - v_{k,hf} - v_{NO}, \tag{2}$$

Then, after a simple operation, the following equation can be obtained:

$$L_s \frac{d}{dt}(i_a - i_b) + r_s(i_a - i_b) = (i_a - i_b) - (v_{a,lf} - v_{b,lf}) - (v_{a,hf} - v_{b,hf}), \tag{3}$$

where the voltage quantities v_a, v_b, $v_{a,lf}$, and $v_{b,lf}$ are all of industrial frequency. When $v_{a,hf} = v_{b,hf}$, there are only industrial frequency components in i_a and i_b.

Similarly, when $v_{a,hf} = v_{c,hf}$, there are only industrial frequency components in i_a and i_c. Therefore, if the three-phase grid current is not required to contain high-frequency harmonics, it is necessary to satisfy the equation $v_{a,hf} = v_{b,hf} = v_{c,hf}$, and for ease of representation, the voltage is noted as v_{hf}.

For the CHB in Figure 2, the total bridge arm current $i_{arm,k}$ can be decomposed into the components i_k and i_{pk} whose frequencies are 50 Hz and f_h, respectively. Since the LC filter resonant frequency is f_h, then the voltages of the filter should be $v_{k,lf}$, and the voltage at the primary side of the HFT is $v_{k,hf}$. Meanwhile, the current at the primary side of the HFT is i_{pk}, and i_{pk} is in phase with $v_{k,hf}$. The previous analysis found that the voltage components of each phase should meet $v_{a,hf} = v_{b,hf} = v_{c,hf}$. Since the same load is used in each phase, the transformer primary current should meet $i_{pa} = i_{pb} = i_{pc}$, and for ease of representation, the current is recorded as i_p.

According to Equation (2), the following equations can be written as follows:

$$L_s \frac{d}{dt} \sum_{k=a,b,c} i_k + r_s \sum_{k=a,b,c} i_k = \sum_{k=a,b,c} v_k - \sum_{k=a,b,c} v_{k,lf} - \sum_{k=a,b,c} v_{k,hf} - 3v_{NO}, \tag{4}$$

The expansion module depicted in Figure 4 adopts a PWM control strategy. When a power frequency sinusoidal signal wave is employed as the modulated waveform, the condition $v_{a,lf} + v_{b,lf} + v_{c,lf} = 0$ is satisfied. Additionally, owing to the three-phase symmetry of the AC power supply on the input side, it satisfies, $v_a + v_b + v_c = 0$, $i_a + i_b + i_c = 0$. The following relationship can be derived:

$$v_{NO} = -\frac{1}{3} \sum_{k=a,b,c} v_{k,hf}, \tag{5}$$

Equation (1) can be resolved:

$$L_s \frac{di_k}{dt} = v_k - r_s i_k - v_{k,lf}, \tag{6}$$

If the voltage across a single H-bridge shunt capacitor is v_{sm}, the AC side of a single H-bridge can exhibit three voltage states when the H-bridge is modulated with unipolar modulation: "v_{sm}", "$-v_{sm}$", and "0". The A-phase circuit is analyzed below: the high-voltage side cascades n sub-modules as a whole, numbering the switches within the nth sub-module as $S_{n,1}$, $S_{n,2}$, $S_{n,3}$, and $S_{n,4}$. Assuming that the circuit parameters of the n

sub-modules are the same, when $S_{n,1}$ and $S_{n,4}$ are switched on, the ac side voltage $v_{con,a}$ is given by $v_{con,a} = n\, v_{sm}$; when $S_{n,2}$ and $S_{n,3}$ are switched on, $v_{con,a} = -n\, v_{sm}$; when either $S_{n,1}$ and $S_{n,3}$ or $S_{n,2}$ and $S_{n,4}$ are switched on, $v_{con,a} = 0$. To simplify the analysis, the switching function s_k is introduced. When the switch is on, the device state is denoted as 1; otherwise it is denoted as 0. Thus, $s_k = S_{n,1} - S_{n,3}$ or $s_k = S_{n,4} - S_{n,2}$.

For the structure presented in Figure 2, the input-side cascade unit undergoes PWM modulation. The modulating waveforms with frequencies f_{lf} and f_{hf}, respectively, are overlaid to create the new modulating waveform. As a result of the multi-frequency frequency modulation, the H-bridge bridge arm voltage is a coupling of two voltage components. The first component is the voltage v_{lf} with a frequency of f_{lf}, and the corresponding switching function that generates this voltage is denoted as $s_{k,lf}$. The other component is the voltage vhf at the frequency of f_{hf}, and the corresponding switching function that generates this voltage is denoted as $s_{k,hf}$. In simpler terms, it is possible to separate the switching function s_k into $s_{k,lf}$ and $s_{k,hf}$. To ensure the equality of the high-frequency voltage components across all phase bridge arm voltages, it is required that $s_{a,hf} = s_{b,hf} = s_{c,hf} = s_{hf}$. The voltage of the AC side bridge arm and the current flowing through the submodule capacitor can be expressed as follows:

$$\begin{cases} v_{k,lf} = \sum_{i=1}^{n} s_{k,lf} v_{smi,k} = s_{k,lf} n v_{sm} \\ v_{hf} = \sum_{i=1}^{n} s_{hf} n v_{smi,k} = s_{hf} n v_{sm} \\ i_{sm} = s_k i_{arm,k} = (s_{k,lf} + s_{hf})(i_k - i_p) \end{cases}, \tag{7}$$

where $v_{smi,k}$ is the voltage across the i-th submodule capacitor in a k-phase cascade. When the hardware parameters of each submodule are the same, it satisfies $v_{smi,k} = v_{sm}$.

Within a switching cycle T_s, the DC voltage v_{sm} at the capacitor terminals experiences minimal variation and can be considered constant. The switching functions $s_{k,lf}$ can be represented by the duty ratio $d_{k,lf}$. Consequently, the average model can be derived from Equation (6) as follows:

$$L_s \frac{di_k}{dt} = v_k - r_s i_k - d_{k,lf} n v_{sm}, \tag{8}$$

The AC-side variables are characterized by time-varying AC quantities, which poses challenges for subsequent controller design. To facilitate the design of the control system, the average mathematical model in the abc coordinate system is transformed into the dq coordinate system. This transformation allows for the conversion of all sinusoidal variables into relative DC variables. By applying the Park transformation to both sides of Equation (8), the average mathematical model is expressed in the rotating coordinate system of dq as follows:

$$L_s \frac{d}{dt} \begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} V_d \\ V_q \end{bmatrix} - \begin{bmatrix} r_s & -\omega_g L_s \\ \omega_g L_s & r_s \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} - n v_{sm} \begin{bmatrix} d_{d,lf} \\ d_{q,lf} \end{bmatrix}, \tag{9}$$

where Y_d and Y_q represent variables Y in the static coordinate system and corresponding variables in the dq coordinate system.

Within a switching cycle T_s, the average model of submodules can be obtained from Equation (6) as follows:

$$C_{sm} \frac{d}{dt} v_{sm} = d_{k,lf} i_k + d_{hf} i_k - d_{k,lf} i_p - d_{hf} i_p, \tag{10}$$

Equation (10) reveals that the current passing through the submodule capacitor encompasses both high-frequency square wave and power frequency sine components. Considering that the switching period T_h is significantly smaller than T_s, the variables i_k and $d_{k,lf}$ experience minimal changes within T_h and can be treated as constants. Moreover, the

mean values of variables i_p and d_{hf} within T_h are determined to be zero. Consequently, the capacitance current of the submodule can be represented as follows:

$$C_{sm}\frac{d}{dt}v_{sm} = \frac{1}{3}\sum_{k=a,b,c} d_{k,lf}i_k - d_{hf}i_p, \tag{11}$$

Since i_p and d_{hf} have the same frequency and phase, Equation (11) can be expressed as follows:

$$C_{sm}\frac{d}{dt}v_{sm} = \frac{1}{3}\sum_{k=a,b,c} d_{k,lf}i_k - (1-\lambda)m|i_p|, \tag{12}$$

where m is the modulation ratio, which can be obtained by Equation (13). λ is the sinusoidal voltage amplitude output by the submodule, which can be obtained by Equation (14).

$$m = \frac{v_{a,lf,max} + v_{hf,max}}{nv_{sm,ref}}, \tag{13}$$

$$\lambda = \frac{v_{a,lf,max}}{v_{a,lf,max} + v_{hf,max}}, \tag{14}$$

Park transformation is applied to both sides of Equation (12), and the average mathematical model under the dq coordinate system can be written as follows:

$$C_{sm}\frac{d}{dt}v_{sm} = \frac{1}{2}(i_d d_{d,lf} + i_q d_{q,lf}) - (1-\lambda)m|i_p|, \tag{15}$$

Assuming the turns ratio of the high-frequency transformer is denoted as k_T, the secondary side voltage of the high-frequency transformer satisfies the relationship $v_{sa} = v_{sb} = v_{sc} = v_h/k_T$, while the secondary side current is given by $i_{sa} = i_{sb} = i_{sc} = k_T\, i_p$.

Regarding the H-bridge configuration on the secondary side of the A-phase, the upper and lower switches of each bridge arm exhibit complementary on and off states, whereas the switches positioned diagonally are synchronized in their on and off states. When S5 and S8 are turned on, the AC side voltage corresponds to $v_{sa} = v_{dc}$. Conversely, when S6 and S7 are activated, v_{sa} takes the value of $-v_{dc}$. To simplify the analysis, we introduce the switch function s_h, which assumes a value of 1 when the switch is on and 0 when it is off. Therefore, we can express s_h as s_h = S5–S7. Within a switching cycle T_h, the switching function can be equivalently represented using the duty ratio, given by the following expression:

$$\begin{cases} v_{hf} = k_T d_h v_{dc} \\ C_{dc}\frac{d}{dt}v_{dc} = k_T d_h i_p - \frac{v_{dc}}{3R_L} \end{cases}, \tag{16}$$

The switching function s_h is in the same frequency and phase as the high-frequency square wave voltage vhf and the high-frequency sinusoidal current i_p, giving the following:

$$C_{dc}\frac{d}{dt}v_{dc} = k_T|i_p| - \frac{v_{dc}}{3R_L}, \tag{17}$$

Figure 5 illustrates the average model of the preceding circuit stage in the dq coordinate system, which is derived based on Equations (9), (15) and (17).

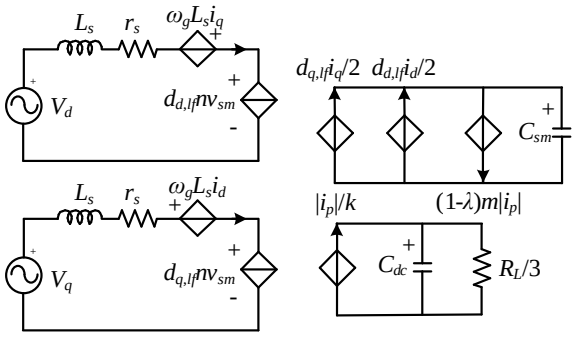


Figure 5. The average model of the preceding circuit in the dq coordinate system.

3. Control Structure

Equation (9) presents the mathematical model in the dq coordinate system, revealing the interdependence between the d-axis and q-axis variables. This coupling hinders the controller design process. To address this issue, a feedforward decoupling control strategy for i_{d} and i_{q} is introduced, enabling the compensation of $v_{\mathrm{d,lf}}$ and $v_{\mathrm{q,lf}}$. By employing a PI regulator in the current control loop, the governing equation can be expressed as follows:

$$\begin{cases} v_{\mathrm{d,lf}}^{*} = -\left(k_{\mathrm{p1}} + \frac{k_{\mathrm{i1}}}{s}\right)\left(i_{\mathrm{d}}^{*} - i_{\mathrm{d}}\right) + \omega L_{\mathrm{s}} i_{\mathrm{q}} + V_{\mathrm{d}} \\ v_{\mathrm{q,lf}}^{*} = -\left(k_{\mathrm{p1}} + \frac{k_{\mathrm{i1}}}{s}\right)\left(i_{\mathrm{q}}^{*} - i_{\mathrm{q}}\right) - \omega L_{\mathrm{s}} i_{\mathrm{d}} + V_{\mathrm{q}} \end{cases}, \tag{18}$$

where k_{p1} and k_{i1} are proportional and integral adjustment gains of the current loop, respectively. i_{d}* and i_{q}* are the current commands of axis d and axis q, respectively.

Equation (15) elucidates the mathematical model in the dq coordinate system. By setting the reactive current to zero, the system operates at a per-unit power factor, enabling the grid-side current to track the voltage without any static error. When employing a PI regulator for the voltage regulation, the governing equation can be expressed as follows:

$$\begin{cases} i_{\mathrm{d}}^{*} = \left(k_{\mathrm{p2}} + \frac{k_{\mathrm{i2}}}{s}\right)\left(v_{\mathrm{smref}} - v_{\mathrm{sm}}\right) \\ i_{\mathrm{q}}^{*} = 0 \end{cases}, \tag{19}$$

where k_{p2} and k_{i2} are proportional and integral regulation gains of the submodule voltage loop, respectively. v_{smref} is the reference value of the capacitor voltage of the submodule.

By substituting Equations (18) and (19) into Equations (9) and (15), respectively, we can derive the system equation for the primary side circuit.

$$\begin{cases} L_{\mathrm{s}} \frac{\mathrm{d}}{\mathrm{d}t} i_{\mathrm{d}} + r_{\mathrm{s}} i_{\mathrm{d}} = \left(k_{\mathrm{p1}} + \frac{k_{\mathrm{i1}}}{s}\right)\left(i_{\mathrm{d}}^{*} - i_{\mathrm{d}}\right) \\ L_{\mathrm{s}} \frac{\mathrm{d}}{\mathrm{d}t} i_{\mathrm{q}} + r_{\mathrm{s}} i_{\mathrm{q}} = \left(k_{\mathrm{p1}} + \frac{k_{\mathrm{i1}}}{s}\right)\left(i_{\mathrm{q}}^{*} - i_{\mathrm{q}}\right) \\ 2C_{\mathrm{sm}} \frac{d}{dt} v_{\mathrm{sm}} = \left(k_{\mathrm{p2}} + \frac{k_{\mathrm{i2}}}{s}\right)\left(v_{\mathrm{sm}}^{*} - v_{\mathrm{sm}}\right) - (1-\lambda) m \left|i_{\mathrm{p}}\right| \end{cases}, \tag{20}$$

When the output voltage regulator uses a PI regulator, the governing equation can be expressed as follows:

$$v_{\mathrm{hf,max}}^{*} = \left(k_{\mathrm{p3}} + \frac{k_{\mathrm{i3}}}{s}\right)\left(v_{\mathrm{dcref}} - v_{\mathrm{dc}}\right), \tag{21}$$

where k_{p3} and k_{i3} are proportional and integral control gains of the output voltage loop, respectively. v_{dcref} is the reference value of the output DC voltage.

The control block diagram of the three-phase CHB-PET can be constructed based on Equations (18)–(21). Figure 6 illustrates the control structure of the preceding circuit. The first control loop generates a sinusoidal AC signal wave $u_{\mathrm{k,lf}}$, operating as follows:

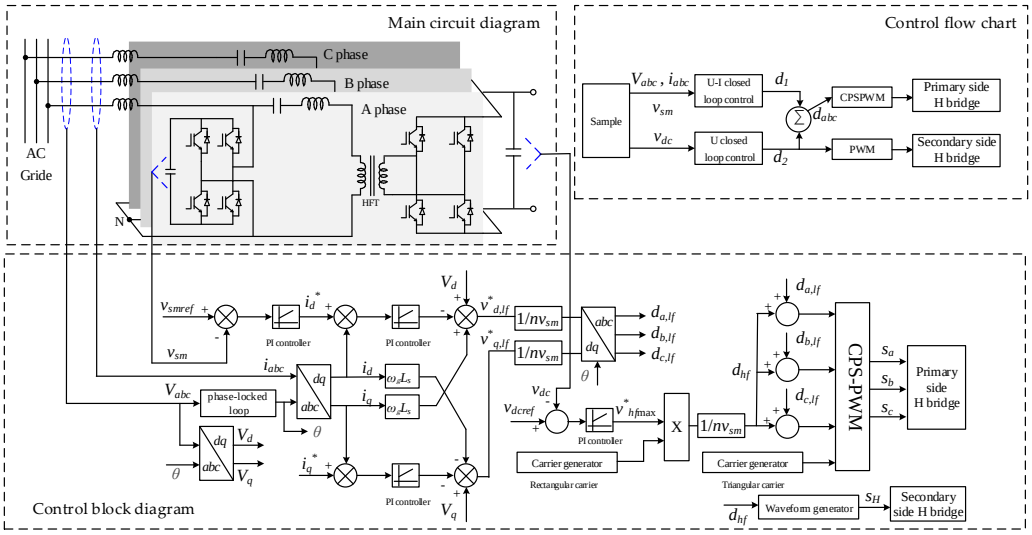


Figure 6. Control block diagram and control flow chart of the new CHB-PET.

Equation (20) demonstrates the complete decoupling of active and reactive currents. Due to the small value of $r_s i_d$, when the active current id is less than the reference current i_d*, $L_s di_d/dt > 0$, resulting in a gradual increase in active current. Conversely, the active current gradually decreases. The principle of reactive current control is analogous. Both active and reactive power instruction currents are continuous flows. The given value of the active current is derived from the output of the voltage loop, while the corresponding value of the reactive current can be set as desired. The voltage loop employs a PI controller to regulate the average value of the DC capacitor voltage of the cascade submodule, which serves as the reference value to obtain the active current instruction value for the current loop. When the reactive current is set to zero, the system operates at unity power factor, enabling the current on the grid side to track the voltage without static deviation.

The second part of the control loop focuses on controlling the H-bridge to generate a square wave voltage with the same frequency and phase as the high-frequency voltage signal v_{hf}. By utilizing a PI controller to adjust the output DC voltage v_{dc} as a reference value, the reference value for the v_{hf} peak is obtained. This leads to the generation of a bipolar square wave signal, which is superimposed with the sine wave $u_{k,lf}$ to form a new signal wave.

It should be noted that the cascade link consists of n H-bridge submodules. In this study, the CPS-PWM modulation method is employed, which sequentially shifts the triangular carrier of each power unit by 1/n carrier period. The shifted triangular carrier is then compared with the same signal wave to obtain the PWM control signal for each power unit. This modulation scheme enhances the high-frequency harmonic components in the output voltage spectrum and significantly reduces the size of the filter inductance. Since L_r and C_r form a series resonant circuit, the H-bridge switch tube can operate in the zero current switching state. The detailed design of the controller loop will be discussed in the following sections.

3.1. Current Loop Design on the Input Side

Equation (20) reveals the symmetry between the i_d current loop and the i_q current loop. The same design methodology can be applied when designing the current loop. Considering that the command signal for the current control loop originates from the voltage control loop, it is essential to prevent current distortion caused by grid voltage fluctuations. Therefore, the current controller adopts a quasi-proportional resonance controller. The current loop operates with a sampling period denoted as T_i. It takes into account the characteristics of calculation delay and zero-order hold, and the PWM control is treated

as a low-inertia component. Consequently, the structure of the id current loop in the dq coordinate system is depicted in Figure 7.

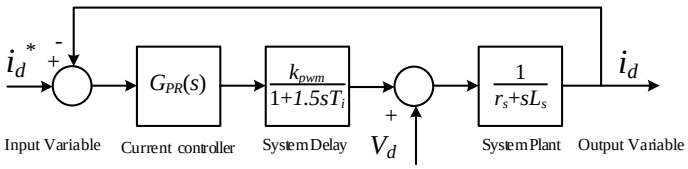


Figure 7. Current control loop structure.

Neglecting the influence of power supply disturbances, we can derive the open-loop transfer function of the id current loop as follows:

$$\begin{cases} i_{\mathrm{d}}^{*} = \left(k_{\mathrm{p2}} + \frac{k_{\mathrm{i2}}}{s}\right)(v_{\mathrm{smref}} - v_{\mathrm{sm}}) \\ i_{\mathrm{q}}^{*} = 0 \end{cases}, \tag{22}$$

where the equivalent gain of PWM control $k_{pwm} = 1$, $G_{PR}(s)$ can be expressed as follows:

$$G_{\mathrm{PR}}(s) = k_{\mathrm{p}} + \frac{2k_{\mathrm{r}}\omega_{\mathrm{c}}s}{s^2 + 2\omega_{\mathrm{c}}s + \omega_{\mathrm{g}}^2}, \tag{23}$$

3.2. Submodule Voltage Loop Design on the Input Side

Equation (20) highlights the direct correlation between the transfer of active energy and the voltage across the capacitors. In the overall control perspective, the design of the voltage loop aims to determine the required current to stabilize the average submodule capacitance voltage at the desired value. Assuming the sampling period of the voltage loop as T_{v}, the voltage controller adopts a PI controller, and the current loop can be represented as a first-order inertia link, denoted as $G_{\mathrm{i}}(s)$. Figure 8 illustrates the structure of the voltage loop in the dq coordinate system.

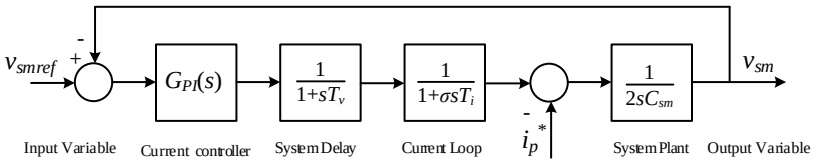


Figure 8. Voltage control loop structure.

Neglecting disturbances, the open-loop transfer function of the submodule voltage loop can be expressed as follows:

$$G_2(s) = \frac{G_{\mathrm{PI}}(s)}{2sC_{\mathrm{sm}}[1 + s(T_{\mathrm{v}} + \sigma T_{\mathrm{s}})]}, \tag{24}$$

4. Design and Simulation

4.1. Input-Side Inductance Value Selection

The filter inductance value on the input side plays a crucial role in enabling the four-quadrant operation of the converter while ensuring satisfactory tracking performance of transient currents and effective suppression of harmonic currents. Specifically, for the A-phase circuit, neglecting the network-side resistance r_{s}, Equation (1) can be simplified to a more concise form:

$$L_{\mathrm{s}}\frac{d}{dt}i_{\mathrm{a}} = v_{\mathrm{a}} - v_{\mathrm{a,lf}}, \tag{25}$$

Figure 9 illustrates the vector relationship diagram under steady-state conditions. It reveals that by precisely controlling the amplitude and phase of the voltage component $v_{a,lf}$ of the bridge arm, the converter can achieve four-phase limited operation.

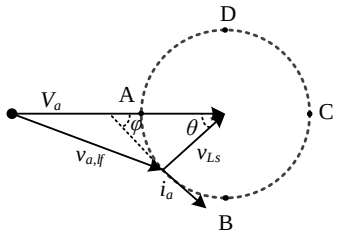


Figure 9. Input-side vector relationship under steady state condition.

Taking into account the phase relationships among the vectors depicted in Figure 9, the cosine theorem is employed to derive the following equation:

$$|v_{a,lf}|^2 = |v_a|^2 + \omega^2 L_s^2 |i_a|^2 - 2\omega L_s |v_a||i_a| \cos\theta = |v_a|^2 + \omega^2 L_s^2 |i_a|^2 - 2\omega L_s |v_a||i_a| \sin\varphi, \tag{26}$$

After arithmetic operations, one can obtain the following:

$$L_s = \frac{|V_a| \sin\varphi + \sqrt{|V_a|^2 \sin^2\varphi + |v_{a,lf}|^2 - |V_a|^2}}{\omega |i_a|} = \frac{V_m \sin\varphi + \sqrt{V_m{}^2 \sin^2\varphi + V_{a,lf,m}^2 - V_m{}^2}}{\omega I_m}, \tag{27}$$

The maximum utilization rate of phase voltage is represented as M (M = 1/2 when SPWM is employed). Therefore, the voltage component $v_{a,lf}$ and v_{sm} must satisfy the condition $V_{a,lf,max} \leq M\, n\, v_{sm}$. Based on this constraint, the value of L_s can be determined as follows:

$$L_s \leq \frac{V_m \sin\varphi + \sqrt{V_m{}^2 \sin^2\varphi + M^2 n^2 v_{sm}^2 - V_m{}^2}}{\omega I_m}, \tag{28}$$

When the inductor current is at its zero crossing point, it exhibits the highest rate of change, necessitating a sufficiently small inductance value to ensure fast current tracking. Figure 10a illustrates the waveform during a switching period near the zero crossing point of the inductive current. Throughout the entire period, the value of v_a is zero. For the interval $0 \leq t \leq T_1$, where $L_s\, di_a/dt > 0$ and $s_{a,lf} = -1$, the change in current is denoted as $\Delta i1$. During the period $T_1 \leq t \leq T_s$, where $L_s\, di_a/dt < 0$ and $s_{a,lf} = 1$, the duration is labeled as T_2, and the change in current is represented as Δi_2.

$$L_s \frac{\Delta i_1}{T_1} = n v_{sm}, L_s \frac{\Delta i_2}{T_2} = -n v_{sm}, \tag{29}$$

The conditions that satisfy the current tracking rapidity are as follows:

$$\frac{||\Delta i_1| - |\Delta i_2||}{T_s} \geq \frac{I_m sin(\omega_g T_s)}{T_s}, \tag{30}$$

By using the above equation, the range of values of inductance Ls can be obtained as

$$L_s \leq \frac{n v_{sm}(2T_1 - T_s)}{I_m \omega_0 T_s}, \tag{31}$$

When the inductor current reaches its peak, the pulsation of harmonic current is most pronounced. Therefore, the inductance value should be sufficiently large to effectively suppress harmonic current. Figure 10b illustrates the waveform of the inductor current during a switching period near its peak value. Throughout the entire period, the value of v_a is V_m. For the interval $0 \leq t \leq T_3$, where $L_s\, di_a/dt > 0$ and $s_{a,lf} = -1$, the change in

current is denoted as Δi_3. During the period $T_3 \leq t \leq T_s$, where $L_s\, di_a/dt < 0$ and $s_{a,lf}$ =1, the duration is labeled as T_4, and the change in current is represented as Δi_4.

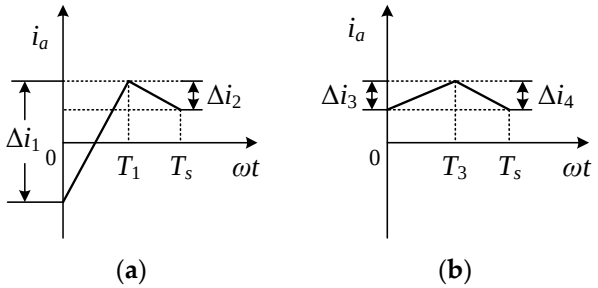
$$\begin{cases} L_s \frac{\Delta i_3}{T_3} = V_m + n v_{sm} \\ L_s \frac{\Delta i_4}{T_4} = V_m - n v_{sm} \end{cases}, \tag{32}$$

By applying the equation $\Delta i_3 + \Delta i_4 = 0$, the value of T_3 can be expressed as follows:

$$T_3 = \frac{n v_{sm} - V_m}{2 n v_{sm}} T_s, \tag{33}$$

If the peak value of harmonic current is set as Δi_{max}, the value range of L_s can be obtained by the inequality $\Delta i_3 \leq \Delta i_{max}$.

$$L_s \geq \frac{(n v_{sm})^2 - V_m^2}{2 n v_{sm} \Delta i_{max}} T_s, \tag{34}$$



(**a**) (**b**)

Figure 10. Inductive current waveform in a switching period. (**a**) Near zero current crossing; (**b**) near the peak of the current.

4.2. Current Loop Design on the Input Side

The voltage range of the A-phase bridge arm is $[-n\ v_{sm}\ n\ v_{sm}]$, where v_{sm} represents the nominal voltage of the submodule. The total number of submodules in the cascade link is denoted as n.

$$n \geq \frac{v_{a,lf,max} + v_{hf,max}}{v_{sm,ref}}, \tag{35}$$

where $v_{hf,max} = k_T\, v_{dc}$. $v_{a,lf,max}$ can be obtained with the following:

$$v_{a,lf,max} = \sqrt{V_m^2 + \omega_g^2 L_s^2 I_m^2} = \sqrt{V_m^2 + \omega_g^2 L_s^2 \left(\frac{\sqrt{2} P_a}{V_{a,RMS}}\right)^2}, \tag{36}$$

Let the network-side current be the following:

$$\begin{cases} i_a = I_m \cos(\omega_g t) \\ i_b = I_m \cos(\omega_g t - 2\pi/3) \\ i_c = I_m \cos(\omega_g t + 2\pi/3) \end{cases}, \tag{37}$$

When the switching frequency significantly exceeds the fundamental frequency of the grid electromotive force, the harmonic components introduced by pulse width modulation (PWM) can be neglected. In this case, the duty ratio $d_{k,lf}$ can be expressed as follows:

$$\begin{cases} d_{a,lf} = \lambda m \cos(\omega_g t - \theta) \\ d_{b,lf} = \lambda m \cos(\omega_g t - \theta - \frac{2\pi}{3}) \\ d_{c,lf} = \lambda m \cos(\omega_g t - \theta + \frac{2\pi}{3}) \end{cases}, \tag{38}$$

For phase A, neglecting the high-frequency component, the fundamental frequency double component and DC component of the capacitor current in the cascade submodule can be derived from Equation (9).

$$i_{\mathrm{sm}} = d_{\mathrm{a,lf}} i_{\mathrm{a}} = \frac{\lambda m I_{\mathrm{m}}}{2}\left[\cos(2\omega_{\mathrm{g}} t - \theta) + \cos(\theta)\right], \tag{39}$$

Then, the maximum frequency doubling fluctuation of capacitor voltage caused by fundamental AC output is as follows:

$$\Delta v_{\mathrm{sm,max}} = \left[\frac{\lambda m I_{\mathrm{m}}}{2C_{\mathrm{sm}}}\int \cos(2\omega_{\mathrm{g}} t - \theta)dt\right]_{\max} = \frac{\lambda m I_{\mathrm{m}}}{4\omega_0 C_{\mathrm{sm}}}, \tag{40}$$

The value range of C_{sm} can be obtained.

$$C_{\mathrm{sm}} \geq \frac{\lambda m I_{\mathrm{m}}}{4\Delta v_{\mathrm{sm,max}}\omega_{\mathrm{g}}} \tag{41}$$

4.3. Simulation Analysis

In order to evaluate the effectiveness of the new topology in 6 kV (50 Hz) distribution networks, simulation models of CHB-PET, including PET-I based on the new topology and PET-II based on the conventional topology, are designed in this paper, and the corresponding simulation models are built using PLECS 4.1 software. Some parameters of the simulation models are shown in Table 1.

Table 1. Parameters of the simulation models.

Type	Parameter	Values (Units)	Parameter	Values (Units)
PET-I	Grid line voltage rms	6 kV	Output-side DC voltage	750 V
	Input-side filter inductance	9 mH	Output-side Capacitance	15 mF
	Ratio of HFT	3.2	LC filter inductance	3.166 mH
	Sub-module capacitance	2 mF	LC filter capacitance	0.5 μF
	Sub-module capacitance voltage	750 V	Number of sub-modules on A phase	12
PET-II	Grid line voltage rms	6 kV	Output-side DC voltage	750 V
	Input-side filter inductance	5 mH	Ratio of HFT	1
	Output-side capacitance	2 mF	Number of HFT on A phase	12
	Output-side capacitance voltage	750 V	Number of sub-modules on A phase	12

Figures 11–15 depict the simulation results for some physical quantities on the primary and secondary sides of PET-I and PET-II. Specifically, Figure 11 gives the waveforms of the three-phase currents and voltages on the AC side of the PET-I. It is clear that the peak value of the current is 40.8 A and the power factor is kept at 1. An FFT analysis of the AC side current was also performed, and the results show that the THD is 4.6%.

The capacitor voltages in PET-I and PET-II are given in Figures 12 and 13. Figure 12 shows the capacitor voltage waveforms of the input-side sub-module of PET-I and the input-side capacitor voltage of PET-II, and the simulation results show that the input-side capacitor voltages of both PET-I and PET-II are maintained at the design value of 750 V, which satisfies the design requirements. Figure 13 shows the output-side capacitor voltages of PET-I and PET-II, and the simulation results show that the output-side voltages of PET-I and PET-II are kept at the design value of 750 V, which meets the design requirements. The maximum voltage fluctuation of the input-side capacitor voltage of PET-I can be seen from the local zoomed-in figure to be 20 V, and the maximum ripple of the output-side capacitor voltage to be 10 V, which both satisfy the design requirements, so the new structure of PET-I can be considered to have practical value. It can also be seen that compared with PET-II, the control method in PET-I has deficiencies in robustness and stabilization speed.

Therefore, the control method of PET-I needs to be further optimized, which will be the next research direction.

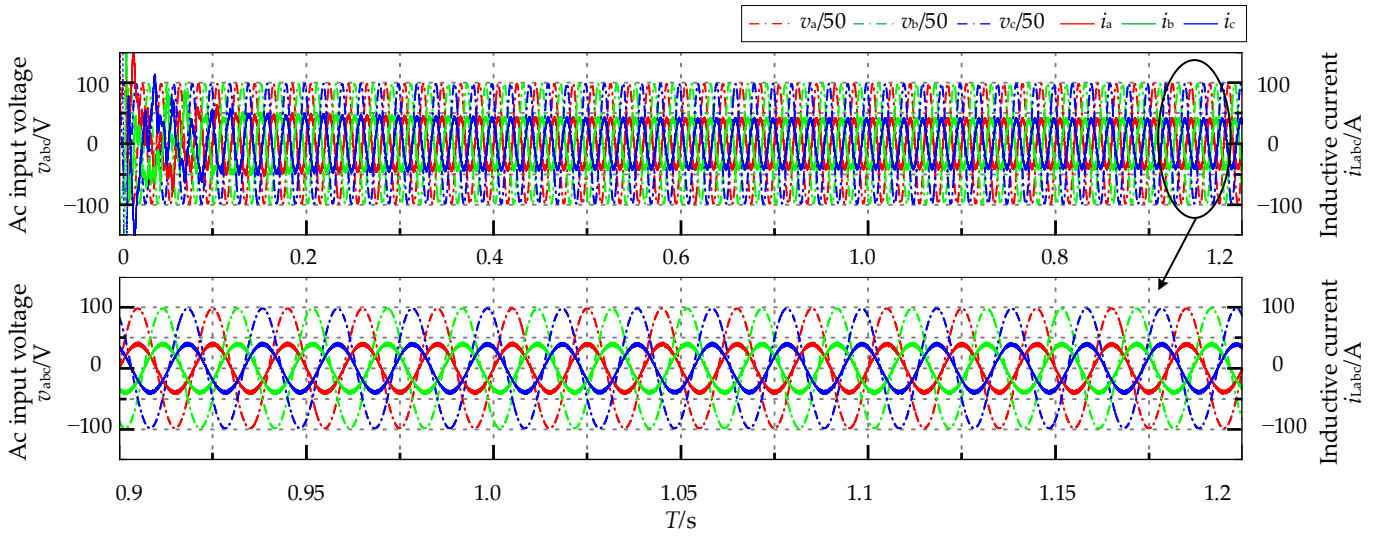


Figure 11. AC-side input voltage waveform and inductive current waveform of the PET-I and local amplification.

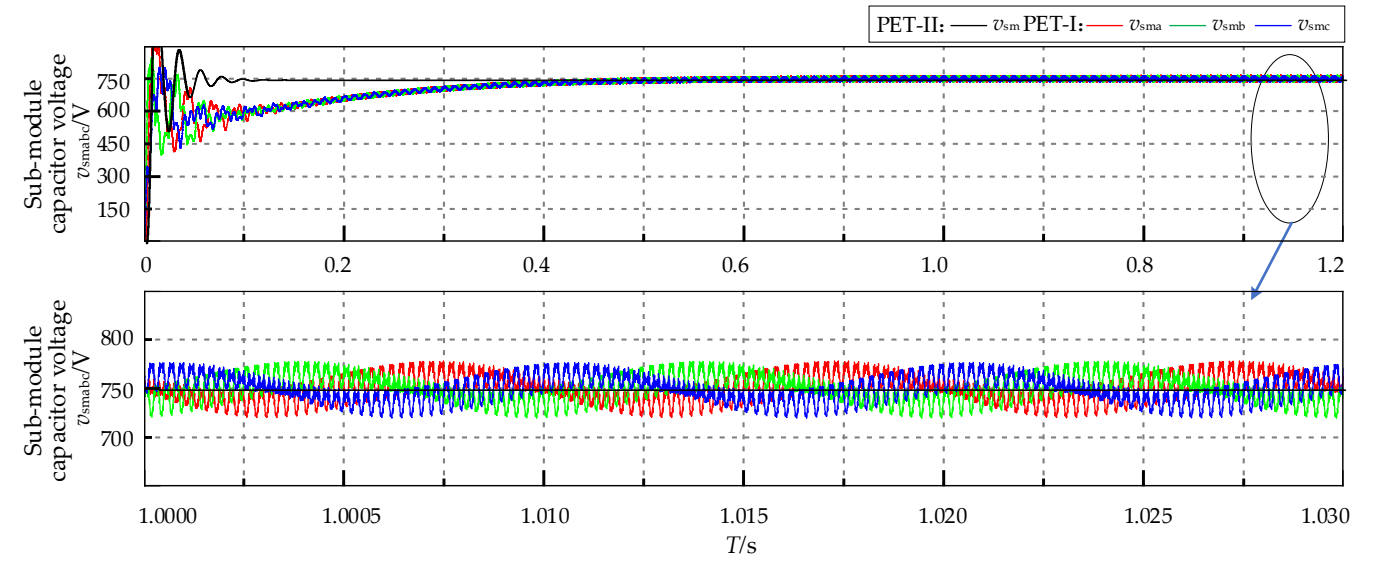


Figure 12. Output-side capacitor voltage waveform of the PET-I and PET-II and local amplification.

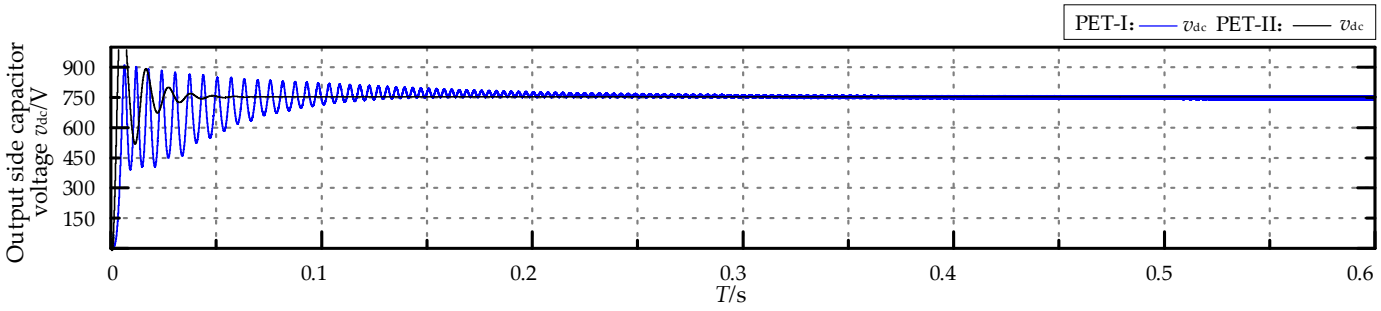


Figure 13. Output-side capacitor voltage waveform of the PET-I and PET-II.

Figure 14 gives the voltage and current waveforms and local amplification waveforms of the primary side of the A-phase HFT in PET-I. The voltage and current have the same frequency, and the h-bridge switching tube at the output side is in a zero-current switching state. It was determined through the previous analysis that the high-frequency component vhf of the h-bridge arm voltage at the input side is equivalent to the HFT primary voltage. From Figure 14, the maximum value of the voltage vhf can be seen to be 2400 V. The modulation ratio of the PET is calculated to be 0.81.

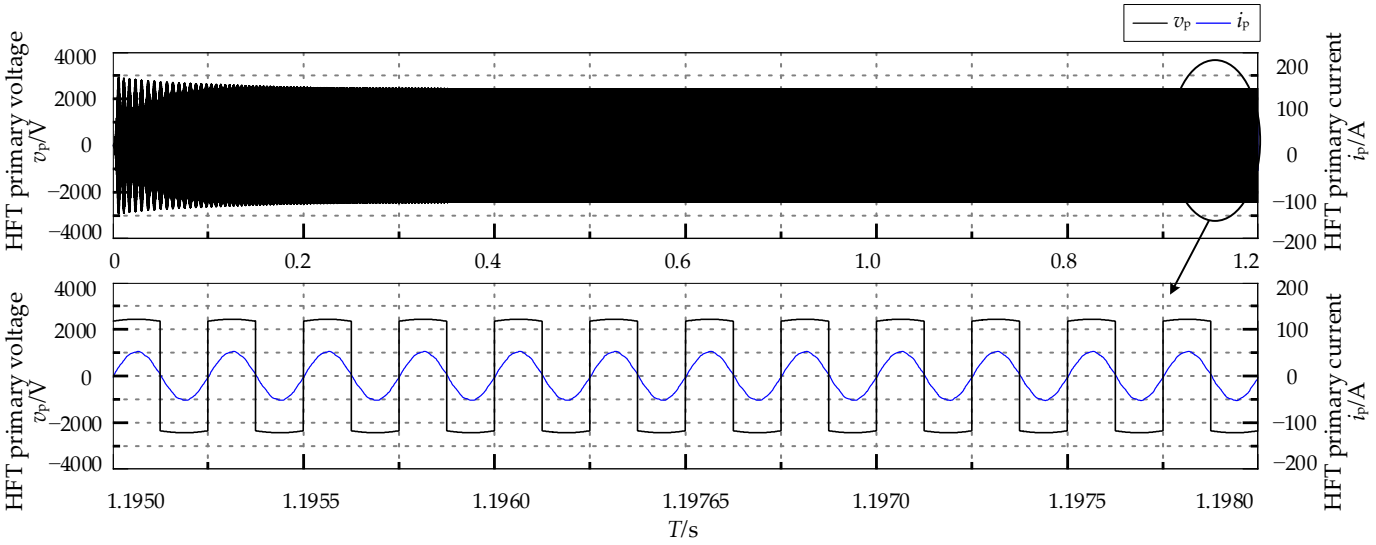


Figure 14. HFT primary voltage and current waveform of the PET-I.

Lastly, Figure 15 shows the duty cycle waveform of the h-bridge on the input side in PET-I. The duty cycle of the a-phase circuit can be divided into $d_{a,lf}$ and d_{hf}, where $d_{a,lf}$ have a frequency of 50 Hz and d_{hf} has a frequency of 4 kHz. In this phase, the bridge arm voltage can be divided into two components: a sinusoidal waveform $v_{a,lf}$ and a square waveform v_{hf}. The frequency of these voltages corresponds to the frequency of the $d_{a,lf}$ and d_{hf} frequencies.

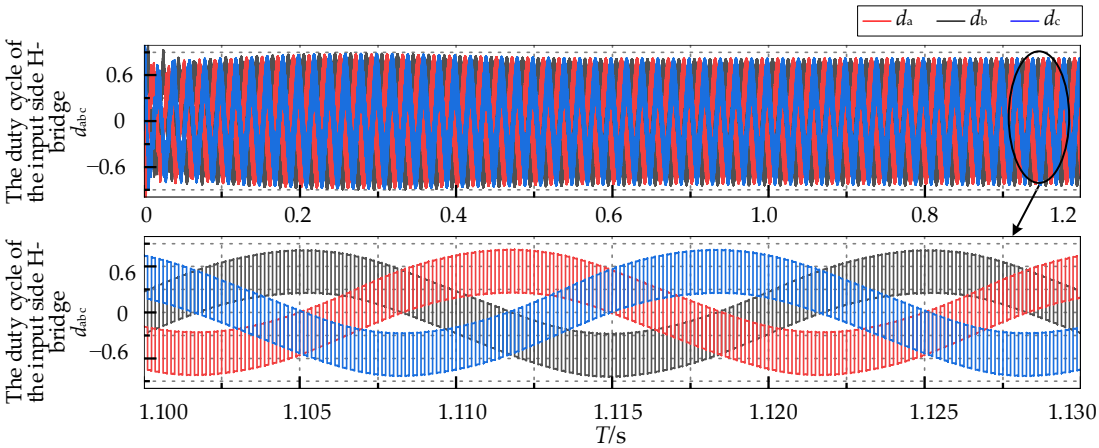


Figure 15. The duty cycle waveform of the input-side H-bridge of the PET-I.

5. Conclusions

This paper introduces a novel three-phase power electronic transformer (PET) topology. Building upon the existing cascaded H-Bridge PET (CHB-PET) structure, this topology enhances the input series output parallel (ISOP) configuration through the efficient reuse of H-bridges. Consequently, it significantly reduces the number of power switch tubes and

high-frequency transformers employed in the entire system. The proposed topology not only maintains the DC bus port of the PET machine but also lowers hardware costs and minimizes the overall volume. Moreover, it effectively enhances the power density and compactness of the PET system. The unit power operation on the input side is achieved through power feedforward decoupling control. By employing series resonance, the H-bridge zero current switching (ZCS) operation on the output side can be realized with straightforward control techniques. As a result, the control strategy of the novel PET topology is simplified, making it highly suitable for widespread application.

Future research efforts will focus on exploring voltage equalization strategies in scenarios where there are discrepancies in submodule circuit parameters. Additionally, circuit analysis will be conducted to examine the impact of phase loss on the input side of the grid and non-resistive loads on the output side. These investigations will further enhance the understanding and performance of the proposed PET topology.

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