

Article

Design of a Ka-Band Heterogeneous Integrated T/R Module of Phased Array Antenna

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Abstract: The central element of a phased array antenna that performs beam electrical scanning, as well as signal transmission and reception, is the transceiver (T/R) module. Higher standards have been set for the integration, volume, power consumption, stability, and environmental adaptability of T/R modules due to the increased operating frequency of phased array antennas, the variability of application platforms, and the diversified development of system functions. Device-based multichannel T/R modules are the key to realizing low-profile Ka-band phased array antenna microsystem architecture. The design and implementation of a low-profile, high-performance, and highly integrated Ka-band phased array antenna T/R module are examined in this paper. Additionally, a dependable Ka-band four-channel T/R module based on Si/GaAs/Low Temperature Co-fired Ceramic (LTCC), applying multi-material heterogeneous integration architecture, is proposed and fabricated. The chip architecture, transceiver link, LTCC substrates, interconnect interface, and packaging are all taken into consideration when designing the T/R module. When compared to a standard phased array antenna, the module's profile shrunk from 40 mm to 8 mm, and its overall dimensions are only 10.8 mm × 10 mm × 3 mm. It weighs 1 g, and with the same specs, the single channel volume was reduced by 95%. The T/R module has an output power of ≥ 26 dBm for single-channel transmission, an efficiency of $\geq 25\%$, and a noise factor of ≤ 4.4 dB. When compared to T/R modules based on System-on-Chip (SOC) devices, the RF performance has significantly improved, as seen by an increase in single channel output power and a decrease in the receiving noise factor. This work lays a foundation for the devitalization and engineering application of T/R modules in highly reliable application scenarios.

Keywords: Ka-band; T/R module; phased array antenna; heterogeneous integration architecture



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1. Introduction

The phased array antenna is widely used in the field of communication [1–6]. Its flexible and agile beam scanning technology accomplishes directional communication between fast-moving and highly dynamic objects, while guaranteeing the tracking accuracy of high-speed mobile platform communication. Simultaneously, low sidelobe and bare nulls in directional diagrams can be achieved using array synthesis, enhancing the system's ability to withstand interference and producing more dependable and stable communication lines. Because of their outstanding performance and rapid development, phased array antennas are gaining importance and are extensively applied in the field of advanced military [7–10] and commercial applications [11–14].

The central element of a phased array antenna that performs beam electrical scanning, as well as signal transmission and reception, is the T/R module. Higher standards have been set for the integration, volume, power consumption, stability, and environmental

adaptability of T/R modules due to the increased operating frequency of phased array antennas, the variability of application platforms, and the diversified development of system functions [15–18].

It is essential to improve the T/R components integration to meet the development trend of phased array antennas. Due to their complicated manufacturing and assembly processes, lengthy process flows, and multiple levels of interconnection ranging from chip circuits to system integration, traditional phased array antennas have trouble meeting the cost and profile requirements of modern information systems. In contrast, millimeter-wave phased array antenna microsystems with low profile and markedly improved functional density can effectively satisfy the requirements of modern information systems for the high integration and performance of phased array antennas, making them one of the research hotspots in the industry. Among them, the devitalization of the multichannel T/R modules is the key to achieving a low-profile phased array antenna microsystem architecture.

Radar's capacity to acquire a large instantaneous bandwidth and, consequently, improve imaging and detection accuracy can be facilitated by raising the operating frequency. The long wavelength and large bandwidth of millimeter-waves provide massive communication bandwidth attainment, enhance real-time transmission and anti-interference capabilities, and speed up communication system response [19–22]. In order to attain a broad scanning angle in a two-dimensional electric scanning array, it is imperative to reduce antenna size and enhance device integration, as the separation between array elements must be around half wavelength [23]. As demonstrated in Figure 1, millimeter-wave frequency antennas with the same aperture can attain greater SNR and EIRP values, allowing the terminal antenna to be smaller, while maintaining improved performance and energy accumulation [23].

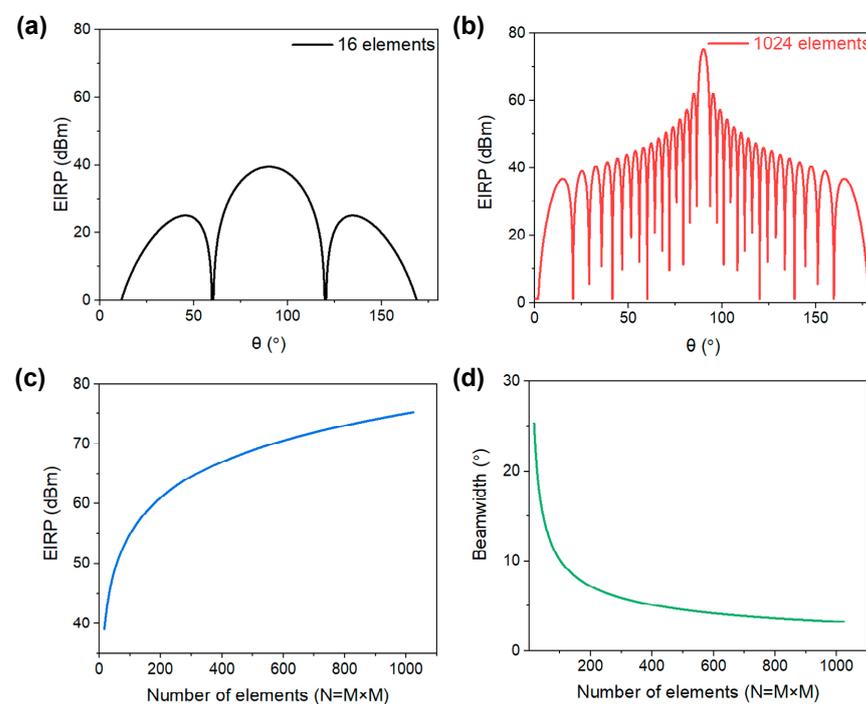


Figure 1. EIRP of phased array antenna with 16 (a) and 1024 (b) phased-array elements. (c) The EIRP grows as $N \times N$, while (d) the beamwidth reduces as N versus the number of phased-array elements in a square array. Images reproduced from the literature [23].

Furthermore, the system must integrate more electronic devices with varying functions due to the devitalization and development trend of phased array antenna application scenarios. Higher requirements have been put forward to improve the integration and devitalization of T/R modules, and a low profile has become a very important factor to

be considered in the design process of phased array antennas in order to avoid antenna equipment taking up too much volume on the flight platform, which affects the overall structural continuity and aerodynamic performance.

2. Related Works

Recently, both domestically and abroad, Ka-band phased array front-end microsystems were created. Table 1 lists the noteworthy accomplishments.

Table 1. Research achievements of Ka-band T/R modules domestically and internationally.

Time	Institution	Module	Technique	Size	Output Power (dBm)	Noise Factor (dB)	Other Parameter	Reference
2014	University of Electronic Science and Technology of China	Ka-band 6-channel switching delay line module	LTCC	84 mm × 47 mm × 15 mm	\	\	\	[24]
2015	The 13th Research Institute, CETC	Ka-band 16-channel transmission module	PCB multilayer wiring technique and multi-chip assembly technique	60 mm × 80 mm × 4.8 mm	>25	\	Linear gain > 25 dB	[25]
2015	Institute of Telecommunication Satellite, CAST	Ka-band T/R module	LTCC	36 mm × 20 mm × 1.1 mm	>24.6	<4.2	Receiving gain ~33 dB, output gain > 25 dB	[26]
2016	Beijing Institute of Technology	Ka-band T/R array	LTCC	Single channel cross-section 6 mm × 25 mm	>10.5	<4.5	\	[27]
2016	Xi'an Research Institute of Navigation Technology	Ku-band 3D miniaturized T/R module	LTCC, BGA	9.5 mm × 9.5 mm × 3.8 mm	>24.5	<3.5	Receiving gain > 25 dB	[28]
2016	Ching-Yun Chu	Ka-band 4-channel T/R chip	65 nm CMOS technique	4 mm × 2.5 mm	~18.5	~4.4	\	[29]
2017	Nanjing Research Institute of Electronics Technology	Ka-band 8-channel T/R module	LTCC	43 mm × 39.5 mm × 3.5 mm	\	\	Return loss > 15 dB	[30]
2020	Southwest China Institute of Electronic Technology	Ka-band circularly polarized phased array antenna	LTCC	46 mm × 44 mm × 2.8 mm	\	\	\	[31]
2020	Nanjing Research Institute of Electronics Technology	Ka-band 64-channel phased array antenna	Silicon based packaging integration, chip embedded packaging	\	\	\	\	[32]
2020	Chengdu radio wave technology Co., Ltd.	Ka-band 128-unit tile phased array antenna	Integrated packaging of Si-based multifunctional and GaAs transceiver chips	93 mm × 93 mm × 52 mm	>20	<6.5	\	[33]
2021	Aerospace Information Research Institute, Chinese Academy of Sciences	Ka-band 4-channel T/R module	LTCC, BGA, multi-material heterogeneous integration	10.8 mm × 10 mm × 3 mm	≥26	≤4.4	Efficiency ≥ 25%	This work
2023	The 13th Research Institute, CETC	Ka-band 4-channel T/R module	Silicon-based MEMs, TSV, 3D integration	18 mm × 19.5 mm × 3 mm	≥30	≤4.6	\	[34]

The comparison above makes clear how well the TR module developed in this work performs in terms of the noise coefficient, output power, and single channel volume. With a

weight of 1 g and an overall dimension of only 10.8 mm × 10 mm × 3 mm, this device-based design greatly enhances T/R module integration when compared to conventional phased array antenna T/R modules. The volume of a single channel drops by 95% with the same specs. When compared to T/R modules based on SOC devices, the RF performance has significantly improved, manifested by an increase in single-channel output power and a decrease in the receiving noise factor. The single-channel output power is >26 dBm, the efficiency is ≥25%, and the noise factor is <4.4 dB thanks to the comprehensive optimization from aspects of chip architecture, transceiver link, LTCC substrate, interconnection interface, and packaging architecture design.

A majority of the modules in earlier studies were created and integrated using single materials like silicon, PCBs, and LTCC. Despite being the most widely used and developed solutions for compact sizing requirements, CMOS, SiGe, and multilayer PCB technologies still struggle to balance the low loss, low noise, large output power, and high transmission of RF signals, among other things. Numerous levels of interlayer interconnections, intricate manufacturing and assembly processes, considerable signal losses, and noise introduced at the interlayer interconnections are among the factors that typically limit the reduction of component volume and profile, leading to large single-channel volume. In this regard, this article designed and implemented a highly reliable Ka-band device-based four-channel T/R module based on multi-material heterogeneous integration architecture applying Si/GaAs/LTCC. With its high integration, straightforward interface, and high output power per unit volume, the device-based T/R module presented in this paper offers a practical and efficient design example for device-based multichannel T/R modules with dependable applications below Ka-band frequency.

3. Architecture Design

3.1. Architecture Scheme of 3D Heterogeneous Integration

At present, silicon-based circuit integration, three-dimensional heterogeneous integration, brick or tile type, and three-dimensional heterogeneous flat plate type are the most common phased array antenna microsystem architectures [32,35,36]. Brick and tile types are classic phased array antenna microsystem designs that accomplish hybrid circuit integration, chip mechanical support, and environmental protection by using metal shells as packaging carriers for different functional modules. Their advantages include inexpensive research and development investment cost and high single-channel output power; yet there are several tiers of connections, significant manufacturing complexity, and challenges in cutting costs and profiles. Silicon-based circuit integration and heterogeneous integration belong to chip-level and wafer-level integration. Enhancing qualification ratios (like stacking success ratios), resolving problems with thermal mechanical reliability (such as mismatches in thermal expansion coefficients), and enhancing interconnection performance are the main challenges associated with these two approaches. They also call for sophisticated machinery, intricate procedures, and significant investments in research and development. Through a three-dimensional assembly interconnection, the three-dimensional heterogeneous flat panel scheme integrates circuits based on diverse functional materials that are made independently. This can combine the benefits of various high-integration techniques and simplify connectivity.

Table 2 summarizes the characteristic indicators of the antenna microsystem architecture mentioned above. The three-dimensional heterogeneous flat plate scheme may not have the highest integration when compared to other architectures, but it has a flexible design and a strong universal system architecture, satisfies real-world needs, and has comparatively low research and development costs. It may successfully address the needs of the application, while taking into account a number of limitations, including those related to performance, cost, space, and reliability. This results in high integration and small size, making it a workable option for systems and devices with superior stability and high efficiency.

Table 2. Comparison of phase array antenna microsystem architecture.

Integrated Architecture of Phased Array Antenna Microsystems	Requirements for Chip Integration	Technique Requirements	Single Channel Output Power	Testability	Research and Development Cost	Million Level Batch Production Cost
Brick and wafer type	Low	Metal shells with multi-chip planar packaging; high- and low-frequency cable interconnection	High	Good	Low	High
Three-dimensional heterogeneous flat plate type	Relatively high	Ceramic, silicon, and glass adapter plates; embedded packaging; hybrid multilayer boards; and surface assembly	Relatively high	Relatively good	Relatively low	Relatively low
Silicon based RF circuit integration	High	SOC chips and their packaging techniques based on Si Complementary Metal Oxide Semiconductor (CMOS) and SiGe BiCMOS	Low	Relatively good	High	Low
heterogeneous integration	High	Si CMOS and SiGe BiCMOS wafer-based technique; direct heterojunction of silicon compounds	Low	Bad	Very high	Low
2016	Xi'an Research Institute of Navigation Technology	Ku-band 3D miniaturized T/R module	LTCC, Ball Grid Array (BGA)	9.5 mm × 9.5 mm × 3.8 mm	Transmission output power > 24.5 dBm, receiver gain > 25 dB, and receiving noise factor < 3.5 dB	[17]

Based on this, this article adopts a three-dimensional heterogeneous flat panel integration scheme for T/R module to achieve devitalization.

3.2. Link Design of T/R Module

The link design of T/R module needs to meet the requirements of high integration, large output power, and low loss. The functional modules of the transceiver link are divided after carefully weighing the benefits and drawbacks of Si and GaAs-based technologies in order to further enhance the integration of the T/R module. The Ka-band 0.5 W four-channel five-chip architecture, or the 1.25 chips per channel method, is employed in this article. It consists of one Si-based four-channel amplitude-phase multifunctional chip and four 0.5 W GaAs transceiver multifunctional chips. A 6-bit phase shifter, a 6-bit attenuator, a driver amplifier, and a transceiver switching interface are integrated inside each channel of the four-channel Si-based amplitude-phase multifunctional chip, as seen in Figure 2. A power amplifier, a low-noise receiving amplifier, and a transceiver switch are all internally integrated within the GaAs transceiver multifunctional device.

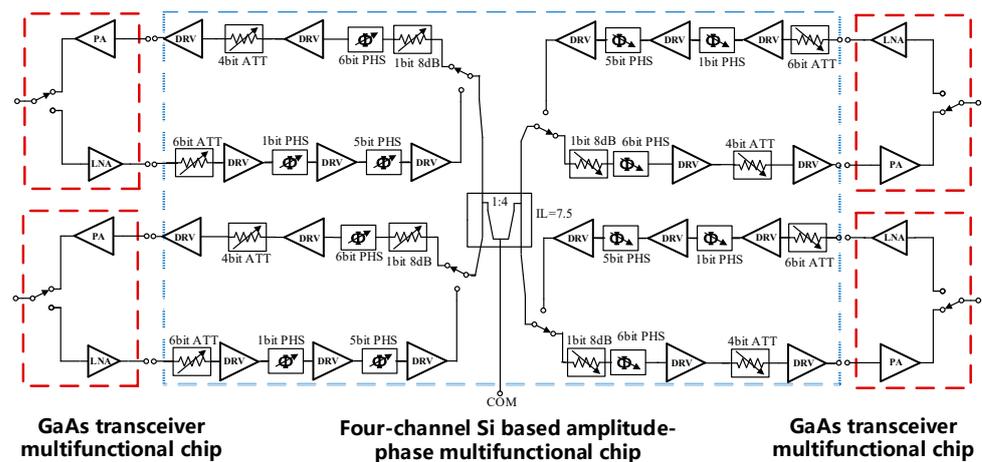


Figure 2. Schematic block diagram of Ka-band 0.5 W four-channel T/R module.

The GaAs transceiver multifunctional chip uses a two-stage amplification structure for its power amplifier, and a four-stage amplification and five-stage matching structure for its low-noise amplifier, which incorporates feedback networks. In order to increase the low-noise amplifier's stability, feedback networks are also added at the input and output ends of all stages of amplification. At the input stage, noise-coefficient matching is utilized to obtain good noise factors. The transceiver switch adopts a single pole double throw switch structure. The traditional Wilkinson power divider model is utilized by the four-channel Si-based amplitude-phase multifunctional power divider, which has an insertion loss of roughly 2 dB (not counting the 6 dB distribution loss). In order to improve channel isolation and make it easier to accurately calibrate the amplitude and phase of phased array antenna channels, the switch employs a single-pole three-throw switch, which has three states: transmission, reception, and load. Drive amplifiers 2 and 3 use an RC negative feedback structure to ensure a large output power, while amplifier 5 uses a two-stage amplification structure and negative feedback to achieve a high gain, while ensuring output power. Drive amplifiers 1 and 4 adopt a traditional amplifier structure due to their small input power. For the purpose of increasing the input P-1dB, the receiving phase shifter has a passive phase shifter structure, with a large displacement phase loss of roughly 3 dB and a small displacement phase loss of about 9.5 dB. The transmission phase shifter adopts an active phase shifter structure to reduce the size, with a loss of approximately 2.5 dB. The attenuator adopts a traditional single-ended structure and adds parallel capacitors for phase compensation. The receiving large-bit attenuation of 16 dB is achieved by cascading two 8 dB attenuation circuits. Both chips are internally integrated with active bias, eliminating the need for additional power modulation circuits, which can save on the number of peripheral devices and simplify the assembly and production.

This design uses Si-based technology to achieve low-power and small-size amplitude-phase control and power management circuits, as well as GaAs technology to achieve excellent amplifier output power, efficiency, and noise factor.

Compared with single-chip integrated architecture, the discrete 1.25-chip architecture can fully exploit the advantages of various process technologies, effectively balancing integration, process feasibility, functionality, and performance. When it comes to large-scale and affordable production, the discrete 1.25-chip architecture is superior to the multi-chip discrete architecture because it can significantly improve integration, simplify the T/R module layout design, streamline the production and assembly process, and guarantee amplitude and phase consistency across channels. The discrete 1.25 chip architecture achieves a high performance, high integration, and good process implementation of the T/R module. The four-channel amplitude-phase multifunctional chip adopts the 55 nm Si CMOS technique, with a size of $3.50 \times 5.00 \times 0.10$ mm, while the transceiver multifunctional

chip uses a 0.25 μm GaAs p-type high-electron mobility transistor (pHEMT) technique, measuring 2.42 mm × 1.85 mm × 0.10 mm.

Based on the above four-channel and five-chip T/R chip architecture, a device-based four-channel T/R module is constructed, consisting of one Si-based amplitude-phase multifunctional chip, four GaAs transceiver multifunctional chips, and a passive conversion structure. Under the guidance of wave control signals, each T/R channel is capable of independently achieving receiving phase shift and attenuation, transmission phase shift, and receiving/transmission/load state switching. Figure 3 displays the indication allocation and link design. IL, NF, G, Pin, and Pout denote insertion loss, noise factor, gain, input power, and output power, respectively. It can be observed that the active gain of the receiving channel is greater than 30 dB, and the noise factor is less than 4.4 dB. The transmission channel's saturated output power is higher than 26 dBm.

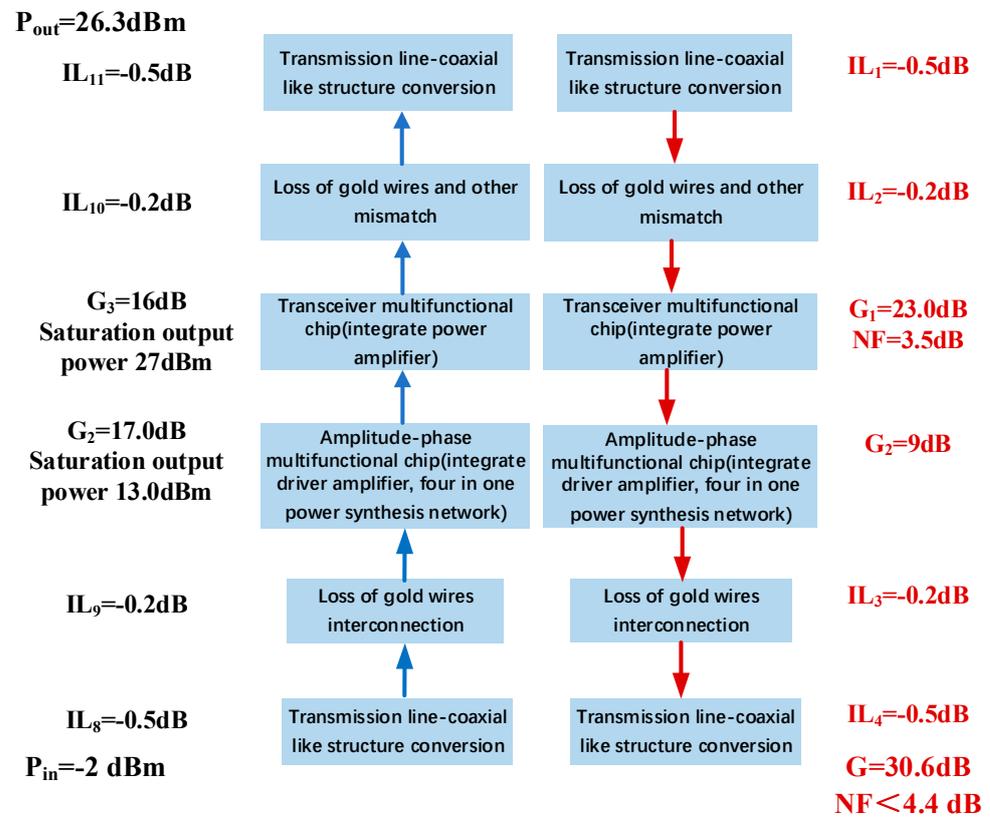


Figure 3. T/R module transmitting and receiving link design and indicator allocation.

The amplitude-phase multifunctional chip and transceiver multifunctional chip of the T/R module described in the paper are placed in the reserved slots of the LTCC multilayer substrate, and the LTCC substrate multilayer wiring provides electrical interconnection, heat dissipation channels, and mechanical support. The LTCC multilayer substrate material is FST07, with a relative dielectric constant of 6.6 and a loss angle tangent of 0.002. There are fifteen LTCC layers in total, and each layer is 96 μm thick, as shown in Figure 4a. Silver-based slurry is utilized on ceramic substrates to produce high-precision, high-density microwave and low-frequency circuits. The second layer of the LTCC substrate is a large-area grounding pad. Punch the substrate from the surface layer to the second layer and then stack and press them to form a blind cavity. Place the four-channel T/R sleeve on the large area grounding pad in the cavity, so that the chips and the surface pads are basically on the same horizontal plane, facilitating bonding operations and shortening the length of gold wires. The conductors from the third-to-fifth layers of the substrate form the power and control circuits, connected to the surface and bottom conductors through the conductor through holes, providing power and control signals for the four-channel T/R chips. The

sixth-to-fifteenth layers of the LTCC substrate are Ka-band signal horizontal transmission layers, where the sixth layer is the upper ground layer for the stripline, isolating the microwave signal layer and the low-frequency signal layer to enhance shielding. The eleventh layer is the Ka-band signal horizontal transmission line layer. The bottom layer serves as the lower ground plane for the stripline, and the sixth ground plane is connected to the bottom ground plane through the conductor through holes arranged on both sides of the stripline, playing a shielding role. A Ka-band signal, power supply, and control signal pad are also located on the bottom layer. The BGA solder balls implanted on the bottom pad are interconnected with external circuit boards to achieve both high- and low-frequency signal input and output. The last surface coating layer is an electroless Ni/Pd/Au film that is utilized for bonding pads for bare chips, surface-mounted resistive and capacitive devices, wire-bonding connecting pads, and bonding pads for metal frame packaging. Figure 4b exhibits the printing and punching layout for each layer.

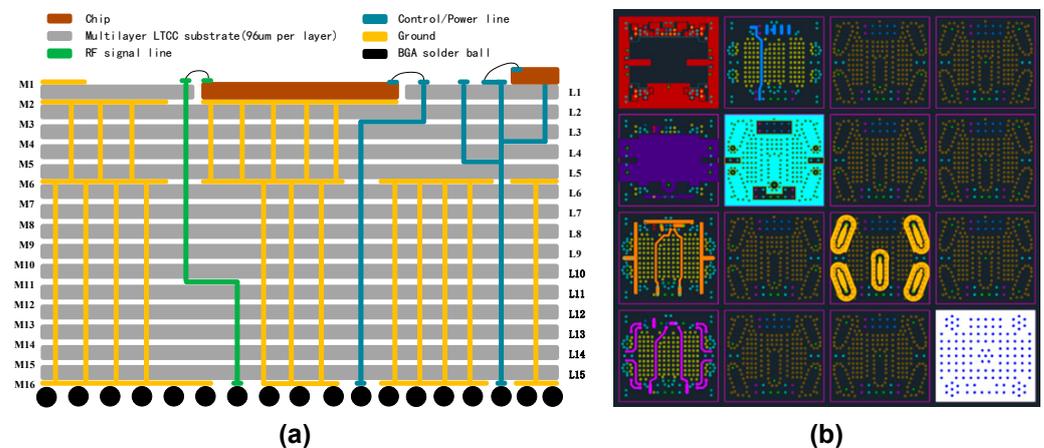


Figure 4. Schematic and layout of multilayer LTCC substrate: (a) schematic of multilayer LTCC substrate and (b) layout of LTCC substrate.

3.3. Device-Based Packaging Design

The four-channel T/R module adopts device-based packaging. As shown in Figure 5, the device-based T/R module uses an LTCC substrate as the packaging substrate, and the 4J29 Kovar alloy with a similar thermal expansion coefficient to the LTCC substrate within a wide temperature range ($-70\sim 500\text{ }^{\circ}\text{C}$) is selected as the enclosure material. The electrical interconnection interface adopts the BGA form, and the LTCC substrate is coated with Ni/Pd/Au film on the surface and then welded with gold tin alloy solder to form an airtight packaging for the metal enclosure and cover plate. The device-based T/R module achieves functional integration of mechanical support, 3D wiring, and heat dissipation by utilizing the dielectric characteristics, mechanical strength, thermal conductivity, and sealing qualities of the ceramic materials themselves. The components are interconnected with external circuits through a surface mount assembly, saving the size and weight of high- and low-frequency connectors and improving the integration of phased array antenna systems. The silver slurry is used as the conductor of 3D wiring, and the surface is coated with an electroless Ni/Pd/Au-plating process to meet the assembly requirements of various components and greatly reduce the process cost.

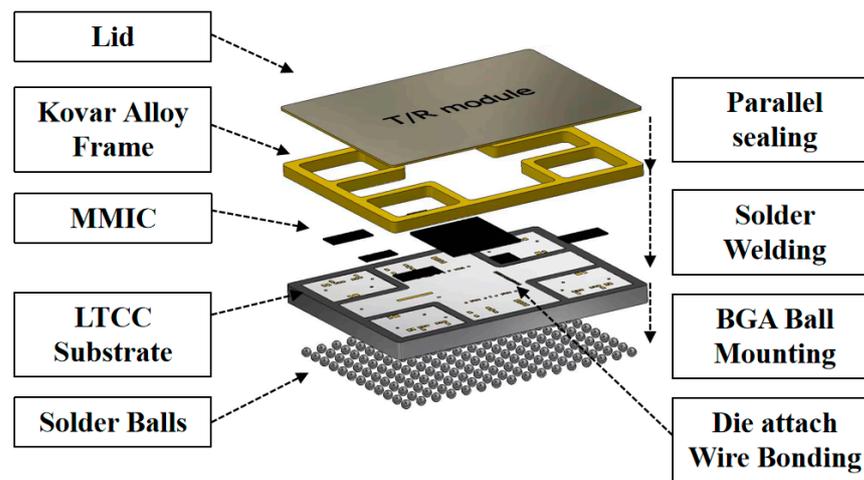


Figure 5. Schematic of tile four-channel T/R module.

4. Optimization of Interconnection Structure

4.1. Design of Device Based Interconnection Interface

When mounting and interconnecting components of this device-based T/R module, the interconnection is required to occupy a small area of the multifunctional board, have low millimeter-wave RF transmission loss, and have good isolation inside and among modules. In order to satisfy the high-performance and low-profile connecting requirements of phased array antenna microsystems, the T/R module referred to in this article uses a BGA as its interconnection interface for signal transmission, regardless of frequency.

BGA packaging can accomplish high-density RF and low-frequency connections by using solder balls in place of conventional metal leads or connectors. The balls are arranged in a two-dimensional array on the back of the packing substrate. Its short signal transmission path and minimal cable parasitic impact help to achieve a good transmission performance. BGA solder balls can be arranged in a coaxial-like structure, as seen in Figure 6, with a solder ball located in the center to replace the inner conductor of the coaxial line, and a circle of solder balls on the periphery to replace the grounding shielding layer of the standard coaxial line. The coaxial-structure BGA interface can achieve great shielding of electromagnetic wave signals in the Ka-band range, as shown in Figure 6, thereby achieving high isolation between RF ports. Figure 7 presents HFSS models comparing electric fields, as well as magnetic field distributions of the quasi-coaxial structure and coaxial structure, showing excellent and similar performance in confining the electromagnetic field inside for both structures.

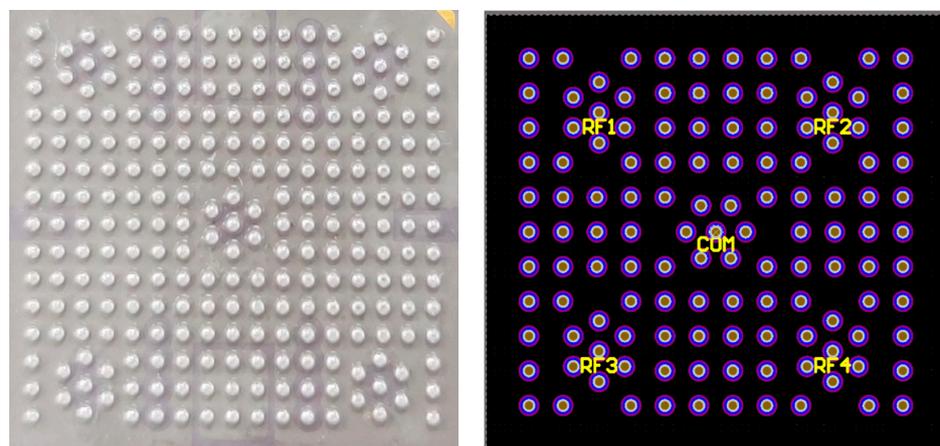


Figure 6. Device-based four-channel T/R module BGA interconnection interface, applying coaxial like structure.

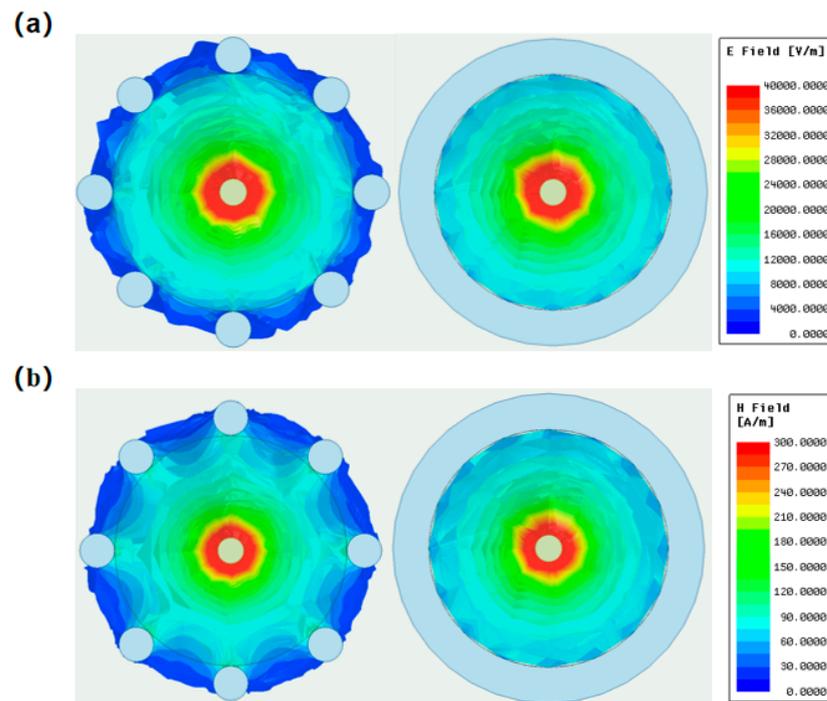


Figure 7. Comparison of electromagnetic field distributions between quasi-coaxial structure and coaxial structure: (a) electric fields and (b) magnetic fields.

4.2. Design of RF Full-Path Interconnection

In the article, the transceiver multifunctional chip is connected to LTCC through wire bonding after being pasted to a large-area solder pad, using conductive adhesive. The millimeter-wave signal is transmitted from the surface to the BGA solder ball output at the bottom of the LTCC substrate in three-dimensional form. It is necessary to optimize the design of the millimeter-wave signal full path interconnection structure of “chip–gold wire–LTCC surface–vertical interconnection–stripline–vertical interconnection–BGA solder ball”.

The high-frequency structural simulator (HFSS) model’s simulation results demonstrate that an impedance mismatch arises from the discontinuous structure between the bonding wire and the pad when chips are directly bonded through gold wire to the inner conductor of a vertical coaxial structure. This leads to a notable decline in the performance of signal transmission. Z_{in} is also in a state of impedance mismatch. Since this degradation is more noticeable at higher frequencies, the transmission performance must be improved on successive striplines by conducting impedance matching.

As illustrated in Figure 8a, a model of the RF path “chip–gold wire–coaxial structure–stripline–coaxial structure–BGA solder ball” was established for the device-based T/R module in order to optimize the interconnection structure. This was achieved by adding multiple matching structures with varying line widths and lengths to the stripline.

Figure 8b presents the simulation findings. It can be seen that, in the wide frequency range of 20–30 GHz, the reflection coefficient is less than -20 dB, and the transmission loss is less than 0.4 dB. The electric field distribution results are shown in Figure 8c and show that the electromagnetic field is confined to the transmission path, indicating that the interconnection structure has an excellent transmission performance.

The difference between the RF input channel and output interface of the device-based T/R module is that the overall port of the amplitude-phase multifunctional chip on the RF input channel has larger wiring space, and the LTCC substrate’s surface can accommodate the addition of a coplanar waveguide. The HFSS simulation model is shown in Figure 9a.

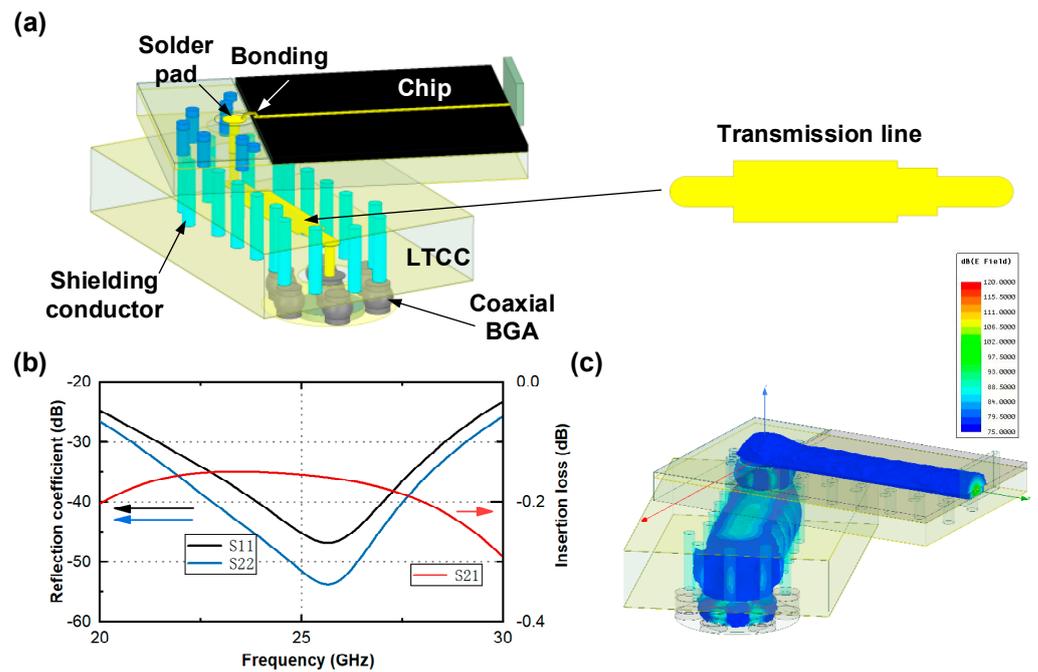


Figure 8. (a) HFSS model of radio frequency output interconnection structure. (b) Simulation results of radio frequency output interconnection structure. (c) Simulation results of electric field distribution in interconnection structure.

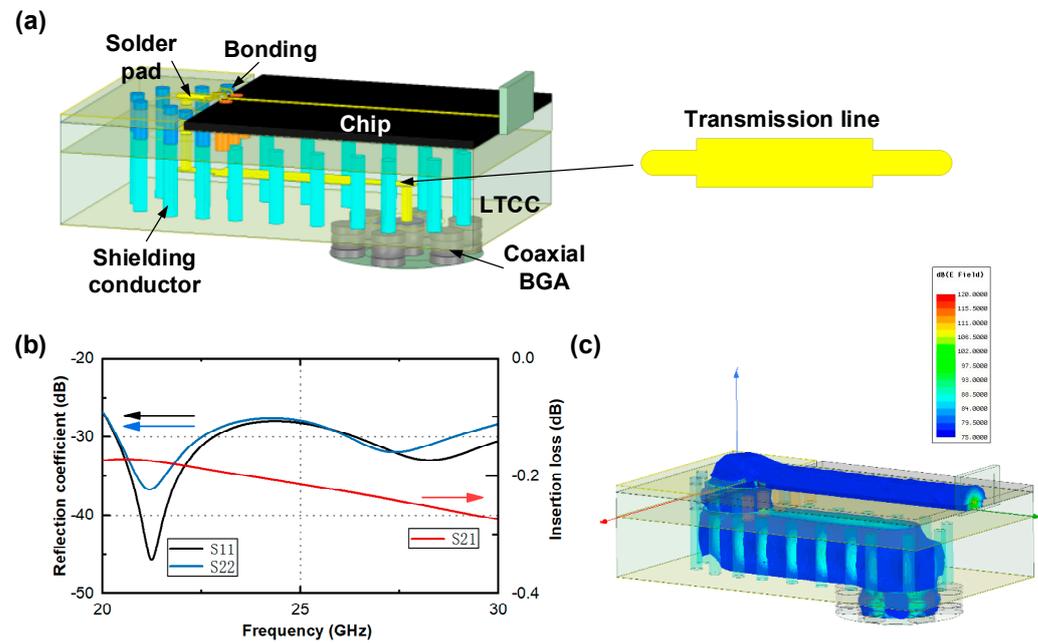


Figure 9. (a) HFSS model of radio frequency input interconnection structure. (b) Simulation results of tile T/R module radio frequency input interconnection structure. (c) Simulation results of electric field distribution in interconnection structure.

Simulation results are shown in Figure 9b, where the reflection coefficient is less than -20 dB and the transmission loss is less than 0.4 dB in the wide frequency range of 20–30 GHz. The electric field simulation model is shown in Figure 9c, presenting that the electromagnetic field is also well confined to the transmission path.

5. Testing the Key Parameters of the Device-Based T/R Module

Figure 10 displays the device-based T/R module's photo and testing environment. The module weighs 1 g and has overall dimensions of $10.8 \times 10 \times 3$ mm. The testing results are summarized in Table 1.

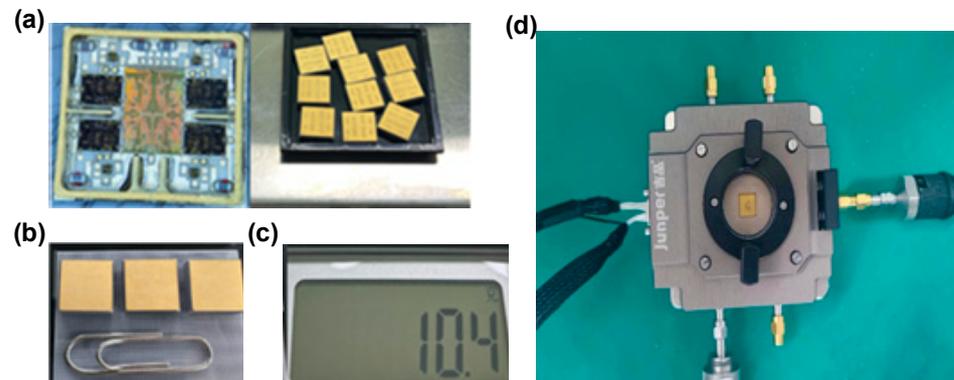


Figure 10. (a) Fabricated prototype of tile T/R module. (b) Size comparison between T/R modules and a clip. (c) A T/R module weight of 10.4 g. (d) Test environment of tile T/R module.

To measure the receiving performance of the module's single channel, put the other three channels into receiving standby mode, meaning that the receiving amplifier is turned off; and put the RF port into load mode.

The results of the single-channel ground-state receiving test are shown in Figure 11, and it can be seen that the in-band receiving gain exceeds 26 dB. Considering that the four-in-one power synthesis network introduces an additional insertion loss of about 6 dB, the in-band receiving gain for a single channel ground state is greater than 33 dB, which matches the predicted value 30.6 dB in Figure 3 well. The in-band noise factor is less than 4.4 dB, agreeing with the value 4.4 dB put forward in Figure 3. The test results meet our expectations.

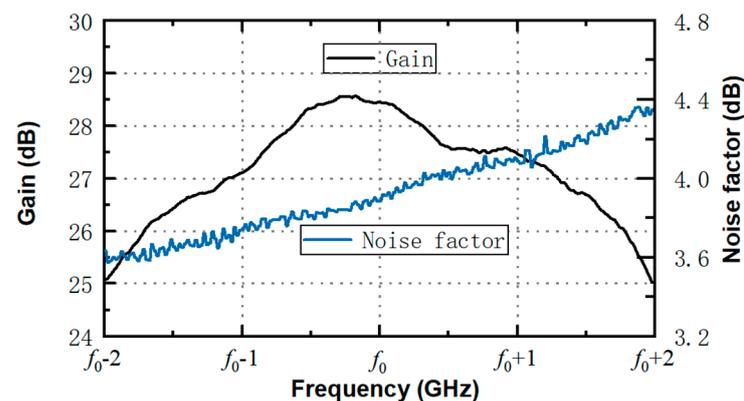


Figure 11. Measurement results of single-channel base-state reception.

The test results of the 6-bit attenuator and phaser are shown in Figure 12. The amplitude or phase measured following a particular amplitude modulation (a) or phase modulation (b) on the basis of a single-channel ground state is represented by each curve in Figure 12, with the particular amplitude modulation or frequency modulation value shown on the label of the curve. It is shown that the test results agree well with the set values within a wide band range ($f_0 - 2 \sim f_0 + 2$ GHz, $f_0 = 24$), verifying that this T/R module has stable and accurate attenuation and phase-shifting effects.

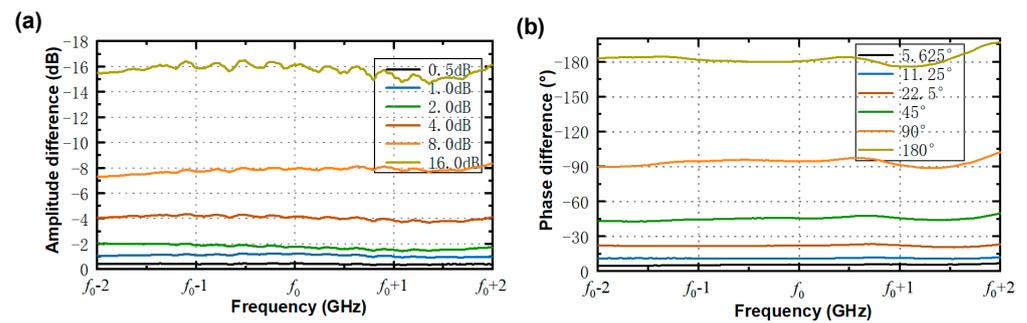


Figure 12. Measurement results of phase shift and attenuation. (a) amplitude modulation. (b) phase modulation.

Set the RF port to the load state and the other three channels to the transmitting standby state—that is, with the transmitting amplifier turned off—when evaluating the transmission performance of the module’s single channel.

The test results of the single-channel transmission output power and current are shown in Figure 13. It can be seen that the output power of the device-based four-channel T/R module within a single channel 4 G bandwidth is greater than 26.2 dBm, which is superior, as seen from the comparison in Table 1. Additionally, the emission current, which has a maximum value of 300 mA and is related to efficiency at different frequencies, has an efficiency of more than 25%. The test results comply with the design values in Figure 3, considering a 6 dB insertion loss induced by the one-to-four power divider.

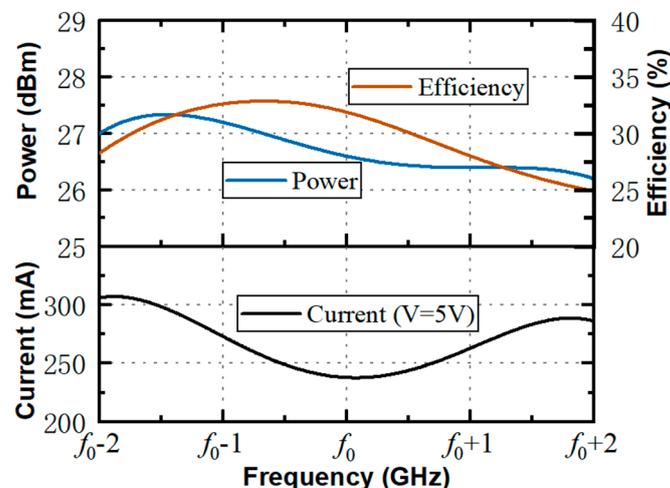


Figure 13. Measured results of output power, efficiency, current with single channel transmitting.

6. Conclusions

This work offers a device-based four-channel T/R module scheme based on a multi-material heterogeneous integration architecture incorporating Si/GaAs/LTCC to meet the demand for the devitalization of T/R modules in the millimeter-wave phased array antenna microsystem architecture design. By designing the chip architecture, connections, wiring, packaging, interfaces for interconnection, and full path interconnection, millimeter-wave four channel T/R modules are devitalized, and their critical parameters are tested. This module breaks through the device-based packaging of millimeter-wave signal full-path three-dimensional transmission interconnection, achieving a four-channel module overall size of 10.8 mm × 10 mm × 3 mm, weight of 1 g, single-channel transmission output power ≥ 26 dBm, efficiency ≥ 25%, and noise factor ≤ 4.4 dB, meeting the high-performance T/R module requirements of Ka-band phased array antenna microsystems for high dynamic platform communication. When compared to other T/R modules, this one has advantages

like simple integration, a straightforward interface for connecting, and a high output power per unit volume.

With its low profile, high power, and low loss, this research offers a practical and workable design example for a device-based multichannel T/R module design. It has a wide range of applications and enormous potential, but more research and development are required.

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