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Low-Power Current Integrating Flat-Passband Infinite Impulse Response Filter for Sensor Read-Out Integrated Circuit in 65-nm CMOS Technology

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Abstract: Low-power current integrating infinite impulse response filter having flat-passband for sensor read-out integrated circuit is proposed. In a current integrating filter, passband flatness degradation is inevitable due to *sinc*-like filtering characteristics. In this paper, by proposing a high order infinite impulse response filter architecture, flat-passband characteristic can be achieved. By implementing a filter architecture with a flat passband, the required sampling frequency can be lowered, which in turn can reduce power consumption. Moreover, the proposed high order infinite impulse response filter architecture has a high degree of freedom on adjusting input sample weights. The proposed integrated circuit is implemented in TSMC 65-nm CMOS process and operated on 1.2 V supply voltage.

Keywords: CMOS integrated circuit; current integrating; flat passband; infinite impulse response; sensor read-out integrated circuit

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Citation: Jo, S.-H. Low-Power Current Integrating Flat-Passband Infinite Impulse Response Filter for Sensor Read-Out Integrated Circuit in 65-nm CMOS Technology. *Electronics* **2023**, *12*, 1191. https://doi.org/10.3390/electronics12051191

Academic Editors: Fanyi Meng, Guangyin Feng and Kaiming Nie

Received: 12 January 2023
Revised: 22 February 2023
Accepted: 23 February 2023
Published: 1 March 2023

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1. Introduction

The analog filter adopted in existing integrated circuits has limited reconfigurability. That is, to change the filtering characteristics, sizes of passive components such as resistors or capacitors must be varied or the transconductance must be adjusted over a wide range [1–3]. On the other hand, current integrating filters have high reconfigurability, making them suitable for integrated circuits because their filtering characteristics can be changed by adjusting the ratio of sampling capacitances or clock frequencies [4–7]. However, current integrating filters cannot avoid flatness degradation in the passband because of their inherent *sinc* shaped frequency response, which causes signal-to-noise ratio (SNR) degradation and worsens the adjacent channel selectivity (ACS) [8,9].

There have been many attempts to reduce passband flatness degradation. Current integrating band-pass analog infinite impulse response (IIR) filters having inverse *sinc*-like frequency response have been proposed [10]. Through a cascade connection with a band-pass analog IIR filter, the *sinc* shaped frequency response can be compensated for. However, due to limitation of implementable filter coefficients of band-pass analog IIR filters, these filters cannot be applied for all shapes of frequency response. As a compensation method, digital inverse finite impulse response (FIR) filters using digital signal processing (DSP) on the digital back-end are suggested [11]. However, this approach requires additional power consumption and chip area.

Likewise, to achieve the flat-passband frequency response, high sampling frequency for low-pass analog IIR filter is adopted [12–14]. Even though an analog baseband filter is used, sampling frequency is in the range of several hundred MHz. If signal bandwidth is increased, sampling frequency would then increase several times. In other words, increased sampling frequency causes increased power consumption of clock generator and imposes a burden on the analog-to-digital converter (ADC). In this paper, as a solution to the flatness degradation of the current integrating analog filter, a low-pass analog IIR filter having a

flat passband is proposed; this filter does not require any compensation or high sampling clock frequency.

2. Current Integrating Analog IIR Filter Topology

2.1. Conventional Architecture

The conventional architecture for a current integrating analog IIR filter is shown in Figure 1 [5–7]. An operation diagram is presented in Table 1. Input signal is converted from voltage to current by the transconductance amplifier. When switch S_0 is ON, the input signal is integrated into capacitor C_{PR1} and C_{PHF} at a ratio α:$(1-\alpha)$. After that, the charges stored in C_{PR1} are read out and then discharged. However, the charges stored in C_{PH1} are not discharged. Therefore, C_{PHF} contains information of previous input signals, and the corresponding charges are transferred to C_{PR1} to form a filter having IIR characteristics. Its transfer function in the z-domain is expressed as

$$\begin{array}{l} H(z) = \frac{1-\alpha}{1-\alpha z^{-1}} \text{ where } \alpha = \frac{C_{HF}}{C_{HF}+C_R} \\ Assume\ C_{HF} = C_{PHF} = C_{NHF}\ and\ C_R = \{C_{PR1,PR2,and\ PR3}\} = \{C_{NR1,NR2,and\ NR3}\} \end{array} \quad (1)$$

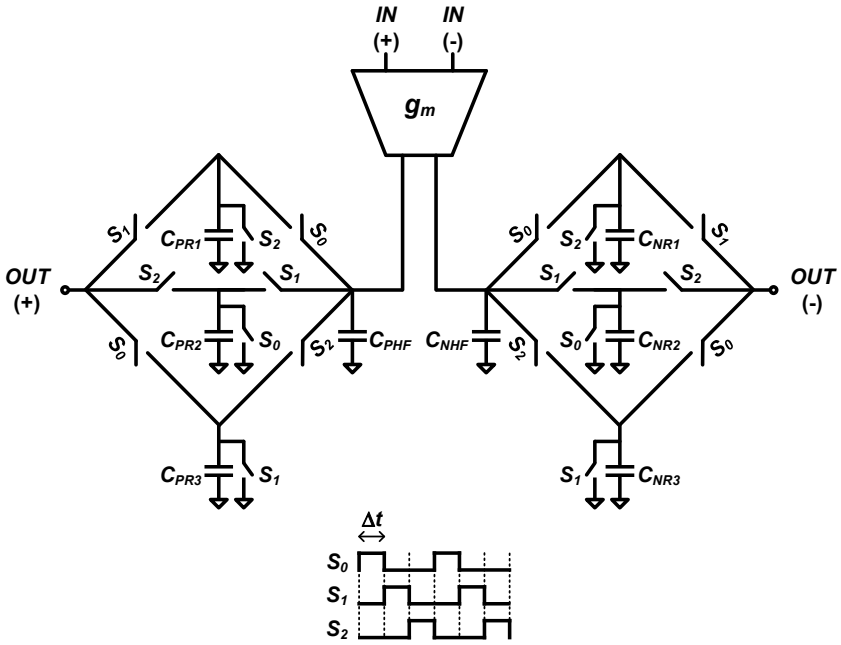

Figure 1. Conventional architecture of current integrating infinite impulse response filter.

Table 1. Operation diagram of conventional architecture. CS, RO, D and S stand for charge sampling, read−out, discharging, and sharing, respectively.

Operation Diagram		Clock State		
		S_0	S_1	S_2
Sampling capacitor on positive path	C_{PHF}	S	S	S
	C_{PR1}	CS	RO	D
	C_{PR2}	D	CS	RO
	C_{PR3}	RO	D	CS
Sampling capacitor on negative path	C_{NHF}	S	S	S
	C_{NR1}	CS	RO	D
	C_{NR2}	D	CS	RO
	C_{NR3}	RO	D	CS

Pole-zero plot and magnitude response are shown in Figure 2. Conventional current integrating analog IIR filter has only one pole [7], hence flat passband cannot be implemented. Since the pole is always located on the right-half real axis according to the capacitance ratio α, frequency response has a maximum magnitude at $f = 0$, and gradually decreases up to $f = 0.5 f_s$.

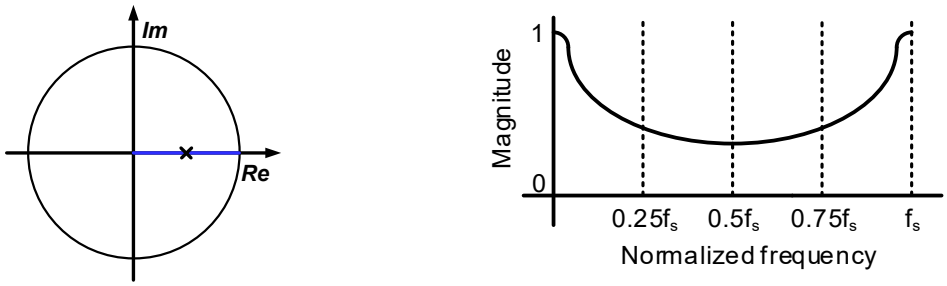

Figure 2. Conventional architecture (**a**) pole-zero plot and (**b**) magnitude response.

2.2. Proposed Architecture

The current integrating flat-passband analog high order IIR filter having two poles is proposed as shown in Figure 3. The operation diagram is presented in Table 2. Current input signal is utilized by adopting a transconductance amplifier. During the on-state of switches S_0, S_1, and S_2, input signal on positive path is stored in C_{PHF}, C_{PHS1}, and C_{PR1} at a ratio of α:β:γ. At the same time, input signal on negative path is stored in C_{NHF}, C_{NHS1}, and C_{NR1} at a ratio of α:β:γ. During the on-state of switch S_3, the charges in C_{PR1} are read out. Afterward, C_{PR1} is discharged during the on-state of switch S_4. On the other hand, input charges stored in C_{PHF} are not discharged. That is, previous input charges accumulate in non-discharged capacitor C_{PHF}, and then affect the next sampling operation. Hence, the once-delayed operation, z^{-1}, is implemented using the non-discharged capacitor C_{PHF}. Likewise, input charges stored in C_{PHS1} and C_{PHS2} are not discharged. Based on the differential architecture, both C_{PHS1} and C_{PHS1} operate at 50% duty cycle, that is, they operate in the on-state of switches S_0 or S_0'. In addition, they are alternately connected to positive and negative paths. Hence, accumulated input charges affect sampling operation once per two periods. Eventually, the plus-signed twice-delayed operation, z^{-2}, can be implemented. Transfer function of the proposed filter in the z-domain is given by

$$H(z) = \frac{\gamma}{1-\alpha z^{-1}+\beta z^{-2}}$$
$$\text{where } \alpha = \frac{C_{HF}}{C_{HF}+C_{HS}+C_R},\ \beta = \frac{C_{HS}}{C_{HF}+C_{HS}+C_R},\ \text{and } \gamma = \frac{C_R}{C_{HF}+C_{HS}+C_R} \quad (2)$$
$$\text{Assume } C_{HF} = C_{PHF} = C_{NHF},\ C_{HS} = \{C_{PHS1 \text{ and } PHS2}\} = \{C_{NHS1 \text{ and } NHS2}\},\ \text{and } C_R = \{C_{PR1,PR2,\text{and } PR3}\} = \{C_{NR1,NR2,\text{and } NR3}\}$$

As shown in Figure 4, instead of one pole locating on the right-half real axis in the conventional architecture, two poles are located on the right-half complex plane if α and β have a relation of $\alpha < 2\sqrt{\beta}$. The pole locations are expressed as

$$pole_{\{1 \text{ and } 2\}} = \left(\frac{\alpha}{2}, \pm\frac{\sqrt{|\alpha^2 - 4\beta|}}{2}\right) \quad (3)$$

Through adjustment of the pole locations, magnitude of frequency response can be equalized within a certain range. For implementation of flat passband, not a 3 dB cut-off frequency, but a 0.3 dB cut-off frequency is adopted where the magnitude difference compared to $f = 0$ is about 0.3 dB. This can be expressed as

$$\left||H(\omega)|_{f=0} - |H(\omega)|_{f=\text{cut-off}}\right| \leq 0.3\ dB \quad (4)$$

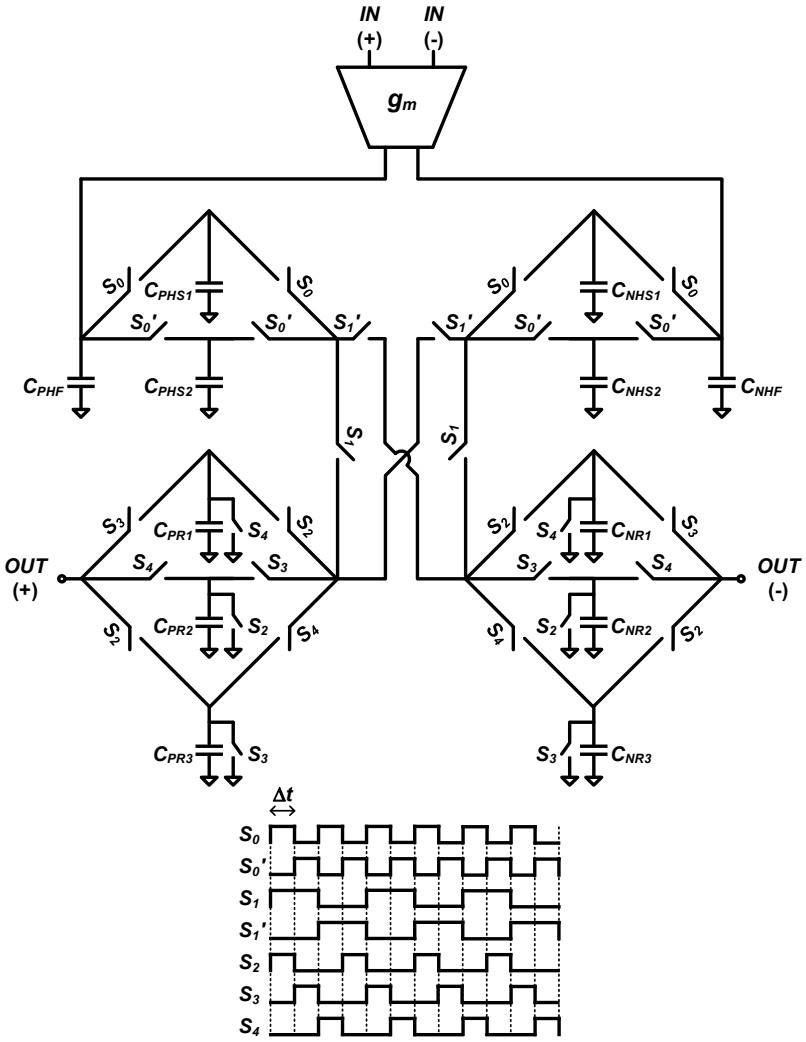

Figure 3. Proposed architecture of current integrating flat−passband infinite impulse response filter.

Table 2. Operation diagram of proposed architecture. CS, RO, D and S stand for charge sampling, read-out, discharging, and sharing, respectively.

Operation Diagram		Clock State						
		S_0	S_0'	S_1	S_1'	S_2	S_3	S_4
Sampling capacitor on positive path	C_{PHF}	S	S	-	-	-	-	-
	C_{PHS1}	S	-	-	-	-	-	-
	C_{PHS2}	-	S	-	-	-	-	-
	C_{PR1}	-	-	-	-	CS	RO	D
	C_{PR2}	-	-	-	-	D	CS	RO
	C_{PR3}	-	-	-	-	RO	D	CS
Sampling capacitor on negative path	C_{NHF}	S	S	-	-	-	-	-
	C_{NHS1}	S	-	-	-	-	-	-
	C_{NHS2}	-	S	-	-	-	-	-
	C_{NR1}	-	-	-	-	CS	RO	D
	C_{NR2}	-	-	-	-	D	CS	RO
	C_{NR3}	-	-	-	-	RO	D	CS

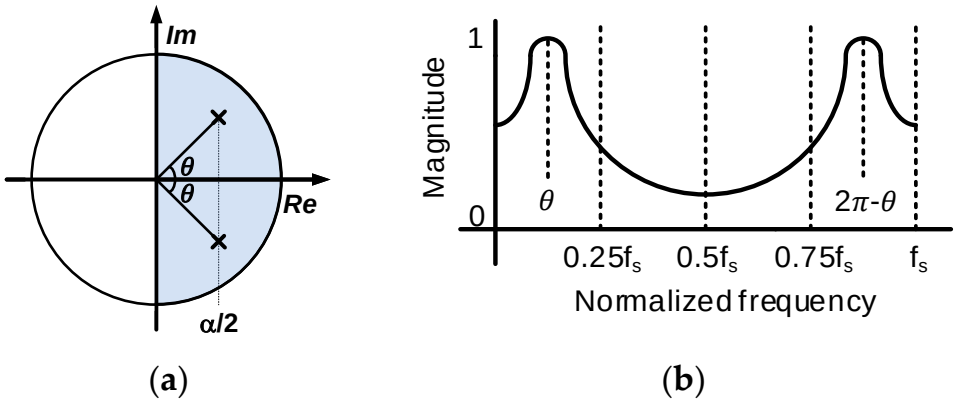

Figure 4. Proposed architecture (**a**) pole−zero plot and (**b**) magnitude response.

2.3. Transconductance Amplifier

The proposed architecture is operated on the basis of current integration. For this purpose, a fully differential transconductance amplifier (TA) [11] is employed; its schematic is shown in Figure 5. It contains a source-coupled differential-pair input stage that can provide high common-mode rejection. Furthermore, variation of DC operating point on output node has an effect on signal swing and causes linearity degradation. Thus, to minimize change of the output DC operating point, the common-mode feedback (CMFB) is adopted. Moreover, current mirrors having a size ratio of M boost their output currents M times. Transconductance can be expressed as

$$g_m = M\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{gs} - V_{th}) \tag{5}$$

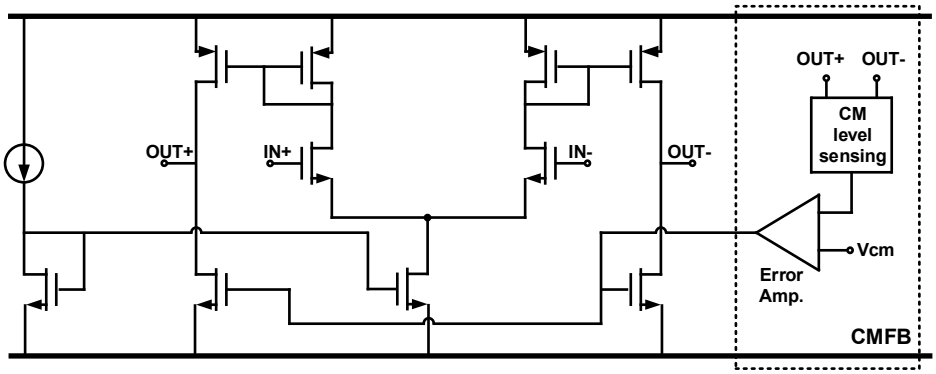

Figure 5. Schematic of transconductance amplifier.

3. Measurement Results

Frequency response of proposed architecture is shown in Figure 6. Black and red lines indicate simulated frequency responses of conventional and proposed architecture, respectively. Blue line indicates measured frequency response of proposed architecture. Sampling frequency was set to 20 MHz. To obtain the correct frequency response, the S21 scattering parameter was measured using a network analyzer. Passband degradation of approximately 1.8 dB at passband edge was obtained. Compared to existing analog filter, the current integrating filter did not have ripples in the passband. The proposed architecture had nulls at the integer multiples of the sampling frequency because of windowed integration [7]. The null depth had a finite value and, as the frequency increased, the null depth decreased. An important factor determining the null depth in the frequency response of the current integrating filter was the output impedance of the transconductance amplifier [5]. The output resistance of the transconductance amplifier was reduced by the influence of the parasitic resistance, which resulted in a decrease in null depth. A two-tone test was carried

out to measure the linearity of the proposed architecture. Two-tone signals at 9.5 MHz and 17.5 MHz were adopted, and IM3 power at 1.5 MHz was measured. Figure 7 shows IIP3 measured with sampling frequency of 20 MHz. The IIP3 was measured and found to be −6 dBm. Furthermore, the noise figure was measured and found to be approximately 40 dB at 1 MHz. Chip micrograph is shown in Figure 8. Proposed architecture was implemented using a TSMC 65-nm CMOS process and operated on 1.2 V supply voltage.

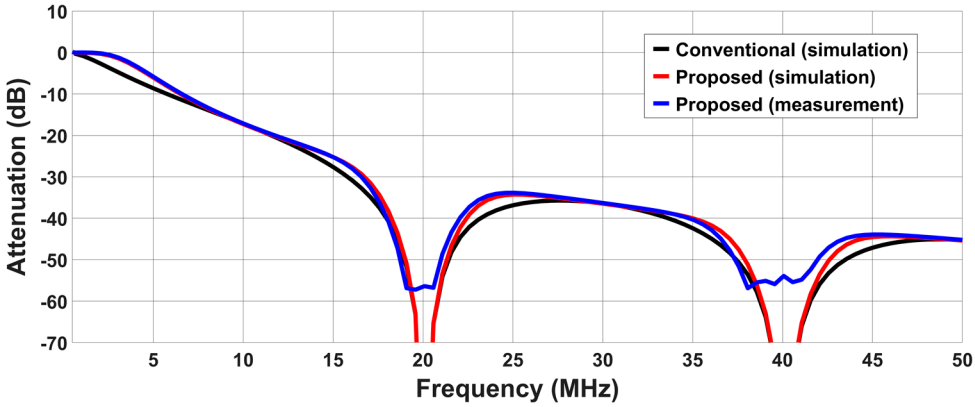

Figure 6. Measured frequency response of proposed architecture.

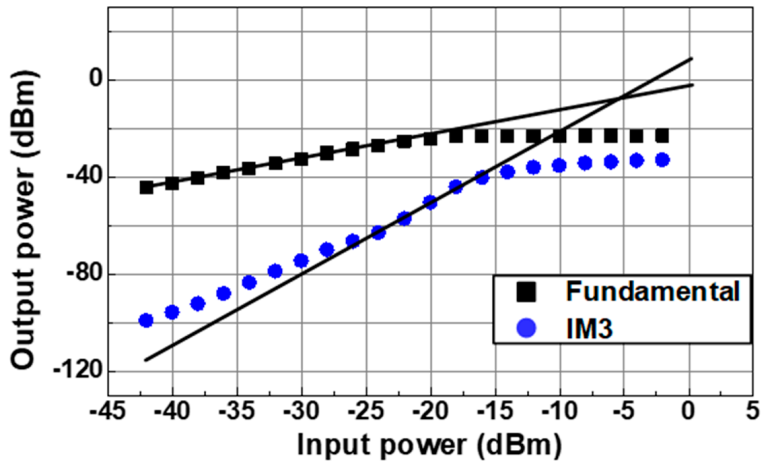

Figure 7. Measurement results of two−tone test.

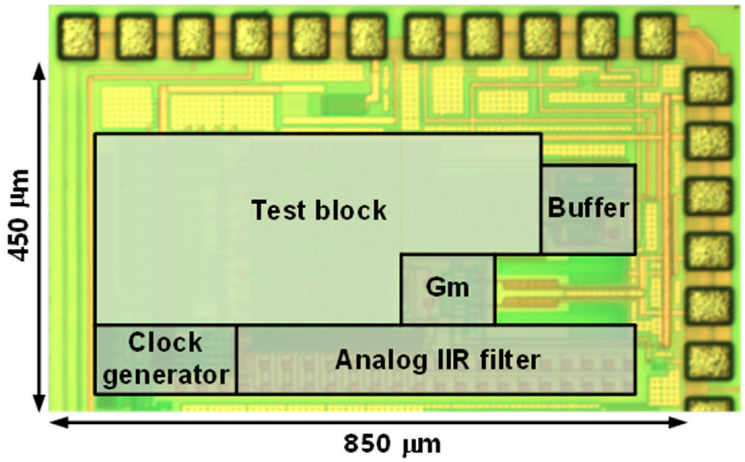

Figure 8. Chip micrograph.

4. Discussion

4.1. Performance Comparison

In this paper, in order to verify a high order infinite impulse response filter having flat-passband characteristics, a second order infinite impulse response filter was implemented. In particular, filter coefficients of $\alpha = 0.6$ and $\beta = 0.2$ are required to obtain flat-passband characteristics in the second order infinite impulse response filter. However, as shown in Equation (6), in the previous architecture, since filter coefficients α and β are defined as multiplication and addition among sampling capacitors, there are restrictions on determining coefficients α and β [12]. Thus, in the previous architecture, filter coefficients $\alpha = 0.6$ and $\beta = 0.2$ cannot be realized with any combination of sampling capacitors.

$$H(z) = \frac{\gamma}{1-\alpha z^{-1}+\beta z^{-2}}$$
$$\text{where } \alpha = \frac{C_{HF}}{C_{HF}+C_R} + \frac{C_{HS}}{C_{HS}+C_R},\ \beta = \frac{C_{HF}}{C_{HF}+C_R} \cdot \frac{C_{HS}}{C_{HS}+C_R},\ \textit{and}\ \gamma = \frac{C_R}{C_{HF}+C_R} \cdot \frac{C_{HS}}{C_{HS}+C_R} \quad (6)$$

On the other hand, as shown in Equation (2), in the proposed architecture, since the filter coefficients α and β are determined as the ratio among the sampling capacitors, it has a high degree of freedom in determining the filter coefficients. Therefore, filter coefficients $\alpha = 0.6$ and $\beta = 0.2$ for flat-passband characteristics can be implemented. However, it has a restriction that the sum of α and β cannot exceed 1.

In systems where current integrating filters are used, high sampling frequencies have been adopted [12–14]. In other words, when the sampling frequency increases, the signal bandwidth stretches, and thus the 3 dB cut-off frequency increases. Thus, the flatness degradation of the passband seemed to be mitigated somewhat by using a very high sampling frequency relative to the signal bandwidth. By adopting proposed flat-passband architecture, a sampling frequency can be reduced to several tens of MHz while maintaining signal bandwidth, which can lead to lower power consumption.

In addition, in the previous architecture, the order of the filter must be increased to increase the stop band attenuation, which has the disadvantage of reducing the signal bandwidth. However, if the cascade connection of proposed architecture is implemented or a higher order filter is implemented, the stop band attenuation can be increased while maintaining the signal bandwidth.

Furthermore, bandwidth-to-sampling frequency ratio (BSR) is defined as

$$BSR = \frac{Bandwidth\ [MHz]}{Sampling\ frequency\ [MHz]} \quad (7)$$

Bandwidth refers to the range of frequencies in a system within which the signal's magnitude is at least -3 dB of its maximum value. Design of power efficient manner can be distinguished by using the index of BSR. Proposed architecture shows the BSR of 0.19, which means high power efficiency compared to previous architectures. In the current integrating filter, most of the power is consumed in g_m-cell and clock generator. A clock generator with a high sampling frequency accounts for the largest portion of the system's power consumption. In particular, the power consumption of the clock generator is determined in proportion to the sampling frequency. In the proposed architecture, a current integrating filter with flat-passband characteristics is implemented while using a low sampling frequency, which enabled low-power operation. The performance comparisons are summarized in Table 3. Proposed architecture has a 3 dB bandwidth of about 3.8 MHz, and a sampling frequency of 20 MHz was used. Previous works have used sampling frequencies of hundreds of MHz to implement 3 dB bandwidths of several MHz. In addition, because the proposed architecture performs a non-decimation operation, it is free from aliasing issues. The proposed integrated circuit is fabricated in TSMC 65-nm CMOS technology and operates with 1.2 V supply voltage. The current consumption of gm-cell and clock generator is 0.25 mA and 0.04 mA, respectively. In particular, since the proposed

architecture implements a 3 dB bandwidth of several MHz while using a low sampling frequency, it shows low power consumption compared to previous works.

Table 3. Performance comparison between the proposed and the previous architectures.

	Proposed Architecture	**[12]**	**[13]**	**[14]**
Decimation	None	None	None	None
3 dB bandwidth [MHz]	3.8	0.4 to 30	1 to 9.9	0.49 to 13.3
Sampling frequency [MHz]	20	800	333	300
BSR	0.19	0.0005 to 0.0375	0.003 to 0.033	0.0016 to 0.044
Supply voltage [V]	1.2	1.2	0.9	1.8
Current consumption of g_m-cell [mA]	0.25	0.23	0.36	1.05
Current consumption of clock generator [mA]	0.04	1.4	0.66	1.33
Power [mW]	0.35	1.96	0.92	4.3
Technology	65-nm CMOS	65-nm CMOS	28-nm CMOS	180-nm CMOS

4.2. Related Application

Nowadays, sensor systems composed of multiple sensors of different types are widely used [15,16]. The sensor system consists of a sensor and a read-out circuit, and the read-out circuit consists of an amplifier and a filter as shown in Figure 9. In order to process multiple sensors in a readout circuit, a time-division multiplexing method using switching network is mainly adopted [17,18]. That is, one read-out circuit is utilized in common, and the type of sensor connected to the input terminal is changed through switching networks. Thus, in order to amplify and filter the output signals of multiple sensors of different types by using one common read-out circuit, a reconfigurable circuit architecture is required. The proposed filter having high reconfigurability can be usefully adopted for sensor systems. In addition, low power operation is possible by lowering the required sampling frequency through flat-passband implementation. Therefore, it is suitable for the multi-sensor system that is widely used in the internet of things (IoT) era.

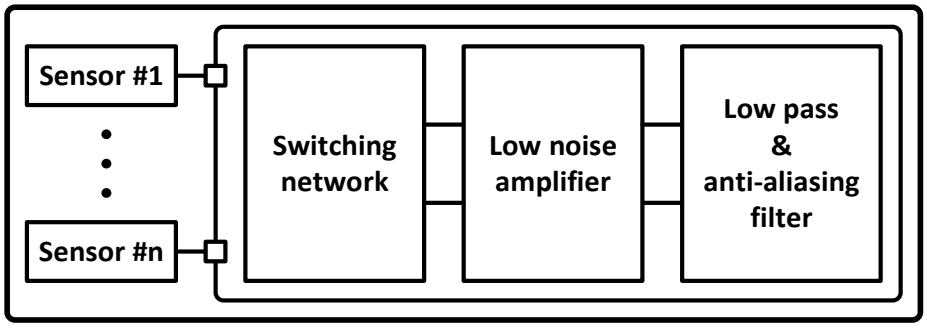

Figure 9. Multi-sensor read-out integrated circuit as an example application of proposed current integrating flat-passband infinite impulse response filter.

5. Conclusions

A low-power current integrating flat-passband analog infinite impulse response filter architecture is proposed. Even using a low sampling frequency, flat-passband characteristics can be obtained through the proposed architecture, and thus power consumption can be reduced. The current integrating filter is suitable for multi-sensor systems; using this filter,

sensor read-out integrated circuits having high reconfigurability could be implemented. The proposed integrated circuit was implemented in a TSMC 65-nm CMOS process.

Funding: This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT) (No. 2020R1F1A1076859).

Data Availability Statement: Not applicable.

Acknowledgments: The EDA Tool was supported by the IC Design Education Center, Korea.

Conflicts of Interest: The author declares no conflict of interest.

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