

Article

Grid-Forming Converter Overcurrent Limiting Strategy Based on Additional Current Loop

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Abstract: Compared with current source converters, voltage source converters (grid-forming converters) have better frequency support capabilities, voltage support capabilities, and regulation performance, thus they have broad application prospects. However, the grid-forming (GFM) converter has insufficient current control ability, and it easily causes problems such as overcurrent issues when a fault occurs. Thus, this insufficiency is one of the most important challenges the GFM converter is faced with. Aiming to solve the problems mentioned above, this paper proposes a control method of a GFM converter achieved with a low-pass filter structure and an additional current loop. The additional current loop controls the dq-axis current components by acting on the outer loop to generate appropriate phase and voltage amplitude reference. The low-pass filter structure is used to solve the system frequency stability problem caused by the inclusion of the additional current loop. On the premise of ensuring that the system frequency meets the grid-connection requirements, the proposed strategy rapidly limits the output current within the allowable range and guarantees expected voltage source characteristics of the converter during the fault period. Finally, the effectiveness and superiority of the proposed control strategy are verified by MATLAB/Simulink simulations.

Keywords: grid-forming converter; current limiting; low-pass filter; voltage support; frequency stabilization



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1. Introduction

Due to the growing needs of the development of energy strategy in the new era, building a new power system with new energy as the main body is an inevitable choice for China to achieve its goal of “dual carbon”. Most new energy equipment, such as wind power generators and photovoltaic cells, are connected to the grid through power electronic converters, and their grid-connected control methods can be divided into grid-following (GFL) and grid-forming (GFM) controls [1–4].

At present, GFL is a general technical means of grid-connected control of power electronic converters and uses a phase-locked loop to measure the phase of the grid voltage to achieve power regulation while connecting to the grid [5]. However, the control mode of GFL does not have the support and regulation of grid frequency and voltage [6], especially in transient cases. This lack of support and regulation is because the GFL performs as a current source and does not have the ability to support transient voltage.

It is generally accepted that GFM can actively control the frequency and voltage output of the converter, but GFM converters can cause large short-circuit currents during faults. Since the converter can only withstand 20~50% of the overcurrent [7,8], the large short-circuit current will cause the converter to be out of service due to device protection and may even cause serious equipment damage. Thus, for GFM converters, limiting the overcurrent rapidly has become one of the focuses of research.

At present, the overcurrent limiting strategies during short circuits of GFM converters mainly include current amplitude limiting [9–11], virtual impedance [12–15], and power reference changing [16,17]. Among them, current amplitude limiting does not have transient voltage support capability and needs to be synchronized through a phase-locked loop, which easily causes system oscillation instability in the case of a weak power grid [18,19]. The current limiting strategy based on virtual impedance changes the reference voltage according to the difference between the actual and set current values, which is equivalent to putting a power-consumption resistor in the line. According to the difference in the calculation methods of virtual impedance and current, the virtual impedance can be divided into linear virtual impedance [20,21] and nonlinear virtual impedance [22]. However, the calculation of virtual impedance relies on the voltage droop and loop parameters, and the accuracy of parameters cannot be guaranteed in actual operation. These limitations result in the current being inaccurately controlled. In addition, the virtual reactance will cause the short-circuit current to contain an attenuated DC component, which will affect the current control effect. Power reference changing cannot achieve accurate control of the current during the fault process, nor can it make full use of the converter overcurrent capability. Researchers [16] changed the rated power of the converter according to the degree of voltage dip and calculated the reactive and active power reference values based on the new power reference of the converter. On the one hand, the new power reference value does not make full use of the short-circuit capacity of the converter, thus the short-circuit current it provides is too conservative. On the other hand, the DC component at the beginning of the fault cannot be suppressed in time due to the slow response of the outer loop.

Aiming to solve the overcurrent problem of GFM converter in case of symmetrical faults, this paper proposes a current limiting strategy based on additional current loop combined with a low-pass filter structure. This strategy generates the phase and voltage amplitude that meet the current limiting requirements, through the additional current loop, and then suppresses the frequency fluctuation caused by the additional current loop through the low-pass filter structure. By this way, this strategy realizes the smooth control of active frequency during the fault. On the premise of ensuring that the system frequency meets the requirements, this control strategy makes full use of the short circuit capacity of the converter to achieve rapid control of current. At the same time, the voltage source characteristics of the converter during the fault period are maintained to provide stable voltage support for the system.

2. Proposed Current Limiting Strategy

The control structure of the GFM converter is shown in Figure 1.

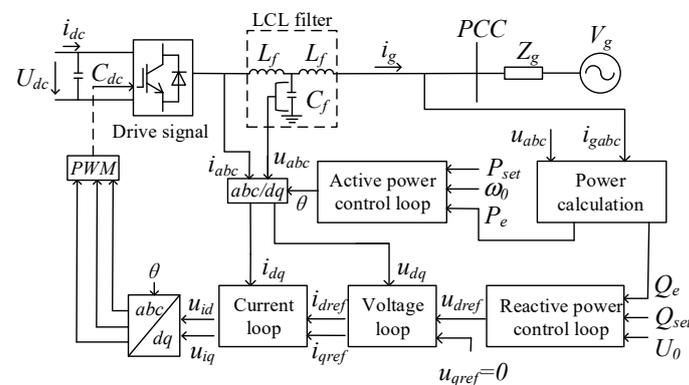


Figure 1. The main topology and control blocks of the GFM converter.

2.1. Active-Frequency Control Strategy

The virtual synchronous generator (VSG) control [23] is used for the active-frequency control link, and operating characteristics similar to synchronous generators are obtained by simulating the synchronous generator governor and rotor motion equation. This simulation can provide virtual inertia and synchronous power for the system.

During normal operation, the rotor equation of motion circuit in Figure 2 can be represented as,

$$J \frac{d^2\theta}{dt^2} = T^* - T_{em} - D_p(\omega - \omega_0) \tag{1}$$

where J represents the virtual inertia, T^* is the set value of the torque, T_{em} is the output torque, D_p represents the damping coefficient, and ω_0 is the reference angular velocity. T^* and T_{em} can be expressed as,

$$\begin{cases} T^* = \frac{P^*}{\omega_0} \\ T_{em} = \frac{P_e}{\omega_0} \end{cases} \tag{2}$$

where P^* is the reference value of active power generated by the virtual governor loop and can be calculated by the equation,

$$P^* = P_{ref} - k_p(\omega - \omega_0) \tag{3}$$

where k_p represents the active droop coefficient.

Substituting Equations (2) and (3) into Equation (1), we receive:

$$J \frac{d^2\theta}{dt^2} = T_0 - T_{em} - D(\omega - \omega_0) \tag{4}$$

where $T_0 = P_{ref}/\omega_0$, $D = D_p + k_p/\omega_0$, and D represents the equivalent damping.

Due to the addition of the first-order inertial delay link, VSG equivalently increases the inertia and damping of the converter. Due to this increase, the converter has good anti-interference ability, which can suppress the peak value when the frequency fluctuates but will affect the power tracking speed [24]. Therefore, the control feature of VSG is conducive to system's stability, but it is difficult for the converter to respond fast during the fault.

Therefore, an additional current loop is installed, and the active power reference is changed to improve the active's response time during the fault. Figure 2 shows a control block diagram that takes the fault characteristics into account.

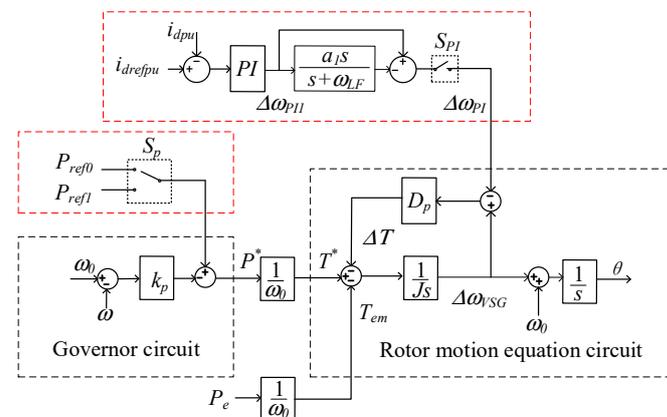


Figure 2. The improved control loop of GFM.

The additional current loop in the figure is used to reduce the damping, the active reference value is adjusted to be closer to the fault condition, and these two actions combine to accelerate the speed of the d-axis current control.

The active reference value is switched to Pref1 when a fault is detected and calculated from the d-axis current reference value during the fault as,

$$P_{ref1} = \frac{3}{2} i_{dref1} u_{dref} \tag{5}$$

where i_{dref1} is the d-axis current reference and u_{dref} is the d-axis voltage reference during the fault.

As demonstrated in Figure 2, the output of the additional current loop acts to decrease the input of the D_P during the fault, which is equivalent to weakening the damping. Therefore, the active loop response is improved. When the d-axis current i_{dpu} is unstable, the output of the additional current loop is not 0, thus the damping is weakened. Additionally, when the current is controlled at the set value of i_{drefpu} , the additional current loop input is 0, the angular frequency is stable at ω_0 , and the active power is stabilized at the given active reference of P_{ref1} , with $\Delta T = 0$.

The switching of the active power reference and the input of the additional current loop will cause the output of the active control to jump, resulting in large frequency fluctuations. To address this problem, apart from the additional current loop, a low-pass filter (Figure 3) is added to suppress large fluctuations of frequency in the initial switching and eliminate frequency static errors. In Figure 3, $\Delta\omega_{PI1}$ represents the output signal of the additional current loop, and $\Delta\omega_{PI}$ represents the output signal from the low-pass filter corresponding to $\Delta\omega_{PI1}$.

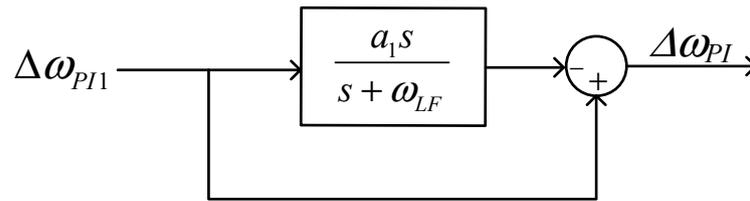


Figure 3. The structure of low-pass filter.

The transfer function of the filter link is,

$$G_{LF}(s) = \frac{(1 - a_1)s + \omega_{LF}}{s + \omega_{LF}} \tag{6}$$

According to the reference frequency of the grid, the bandwidth of the low-pass filter is designed to be 75 Hz, and the gain amplitude of the filter at the cutoff frequency can be expressed as,

$$20 \log_{10} |G_{LF}(s)| = -3 \tag{7}$$

Substituting Equation (6) into (7), we receive:

$$\omega_{LF} = 150\pi \sqrt{\frac{10^{-0.3} - (1 - a_1)^2}{1 - 10^{-0.3}}} \tag{8}$$

Figure 4 depicts the amplitude–frequency and phase–frequency characteristic curves for ω_{LF} as they alter with the value of a_1 .

According to the amplitude–frequency characteristic curve analysis, the amplitude drop is evident when the low frequency band $a_1 = 0.3$ and 1.7 , and the phase change is the smallest when $a_1 = 0.3$; thus, the filter parameters $a_1 = 0.3$ and $\omega_{LF} = 70.57$ Hz are chosen.

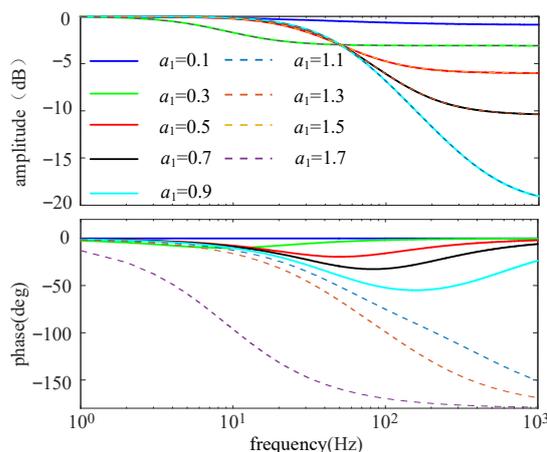


Figure 4. Amplitude and phase frequency characteristic curves of low-pass filter.

2.2. Reactive-Voltage Control Strategy

The reactive power reference is the voltage loop control target during normal operation, and its control structure is illustrated in Figure 5. The d-axis voltage reference u_{drefpu} is generated through the integral controller and the voltage feed-forward link to adjust the reactive power Q_{epu} to the reference value Q_{refpu} [25,26]. The d-axis voltage reference can be calculated by the following formulae.

$$\Delta Q_{pu} = k_q (U_{0pu} - U_{pu}) \tag{9}$$

$$u_{drefpu} = \left(\frac{k_{qi}}{s} \right) (Q_{refpu} + \Delta Q_{pu} - Q_{epu}) + U_{0pu} \tag{10}$$

$$u_{dref} = u_{drefpu} U_0 \tag{11}$$

where ΔQ_{pu} is the reactive power regulation obtained by simulating the generator’s excitation; k_q and k_{qi} are the generator voltage regulation coefficient and integration coefficient of integral controller; U_0 is the voltage reference; and U_{0pu} , U_{pu} , and Q_{refpu} are the unitary value of reference voltage, filter capacitor voltage, and reference reactive power, respectively.

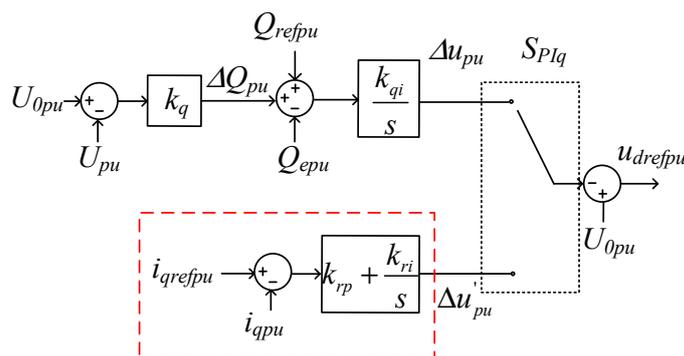


Figure 5. The improved control loop of reactive power.

During a fault, the voltage loop control target in the proposed strategy changes to the q -axis current setting value i_{qrefpu} , which cannot be realized by the original control structure.

Therefore, switching to an additional current loop allows the GFM converters to maintain the voltage source characteristics and meet the voltage support requirements, as shown in Figure 5.

The additional current loop in Figure 5 is used to obtain a voltage reference matching the q -axis reference current. When a fault is detected, the switches S_q and S_{PIq} are closed, and the d -axis reference voltage can be calculated by the following equation.

$$u_{drefpu} = \left(k_{rp} + \frac{k_{ri}}{s} \right) (i_{qrefpu} - i_{qpu}) + U_{0pu} \tag{12}$$

where k_{rp} and k_{ri} denote the proportion and integration coefficient of the additional current loop PI, respectively.

As illustrated in Figure 5, the system voltage is stable when the q -axis current stabilizes at the set value, and the additional current loop output stabilizes at a certain fixed value.

2.3. Selection of the dq-Axis Current Reference

According to China’s wind power grid-connected regulations [27], when grid voltage drops to $0.2\sim 0.9U_N$, the reactive current input must be $1.5(0.9 - U_s)I_N$ at least. Therefore, the dq -axis current reference during the fault can be expressed as follows.

$$i_{drefpu} = \begin{cases} i_{d0pu}, & (u_{pccpu} > 0.9) \\ \sqrt{1^2 - i_{qrefpu}^2}, & (0.2 \leq u_{pccpu} \leq 0.9) \end{cases} \tag{13}$$

$$i_{qrefpu} = \begin{cases} 0, & (u_{pccpu} > 0.9) \\ K_d(0.9 - u_{pccpu}), & (0.2 \leq u_{pccpu} \leq 0.9) \end{cases} \tag{14}$$

where i_{d0pu} is the reference value of the d -axis current before the fault, K_d is the reactive current gain coefficient (generally not less than 1.5 because this paper adopts d -axis voltage orientation), and u_{pccpu} is the voltage amplitude of point of common coupling (PCC).

The improved control structure of the GFM converter is shown in Figure 6.

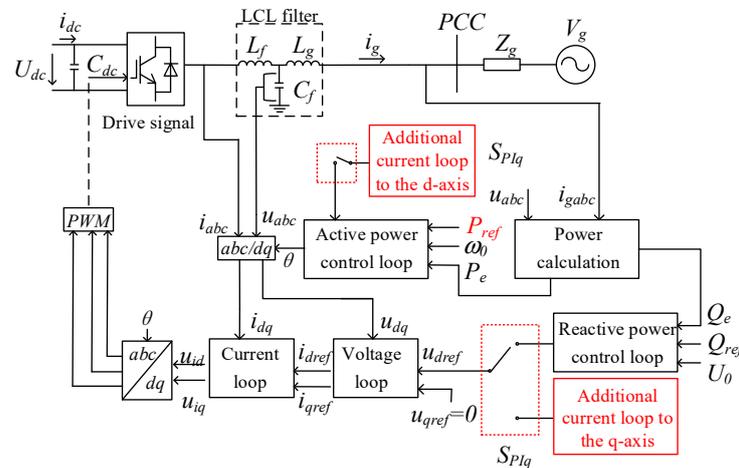


Figure 6. The improved topology and control blocks of the GFM converter.

3. Simulation Results

3.1. Test System Parameters

To test the performance of the proposed control strategy, a simulation was set up in Matlab/Simulink, and the corresponding system parameters are listed in Table 1. Power grid topology adopted in this paper can be seen in Appendix A. In this paper, a three-phase short circuit fault occurred in the system when $t = 0.3$ s, and the fault was removed when $t = 0.7$ s. The simulation duration was 1.2 s, and the overcurrent limit of the converter was set to 1.5 pu.

Table 1. Parameters of the simulated system.

| Symbol/Unit | Quantity |
|-----------------------|----------|
| f_0/Hz | 50 |
| U_0/V | 380 |
| V_{ac}/V | 800 |
| L_f/mH | 1.5 |
| $C_f/\mu\text{F}$ | 30 |
| L_g/H | 1 |
| R_L/Ω | 0.3 |
| L_L/mH | 0.4 |
| S_n/kVA | 15 |
| P_{ref0}/kW | 15 |
| Q_{ref}/kVar | 0 |

The following section will compare and analyze the overcurrent suppression effect and system characteristics of the converters under different control strategies.

3.2. Comparative Analysis between Additional Current Control and Power Reference Changing

Depending on the degree of voltage dip detected, the rated capacity of the converter is changed as [16],

$$S_{new} = u_{pccpu} S_n \quad (15)$$

The reactive and active power reference are calculated based on the new converter rated capacity and voltage dip and can be expressed as,

$$Q'_{refpu} = \begin{cases} 1 - u_{pccpu}, & (u_{pccpu} > 0.9) \\ 2S_{new}(1 - u_{pccpu}), & (0.5 \leq u_{pccpu} \leq 0.9) \\ S_{new}, & (u_{pccpu} < 0.5) \end{cases} \quad (16)$$

$$P'_{refpu} = \sqrt{S_{new}^2 - Q'_{refpu}^2} \quad (17)$$

Taking a grid voltage drop of 0.5 pu as an example, the reactive power reference can be calculated by Equation (16) as 0.5 pu, and the active reference is 0. Figures 7–9 illustrate the changes of electric quantities during the fault.

Figure 7 shows that during Δt_1 (0.08 s), the PCC voltage amplitude of power reference changing is greater than the proposed additional current control, corresponding to Figure 8, the higher PCC voltage amplitude needs more energy ($S_{P1P} + S_{Q1P} - S_{P1N}$) supplied by converters. However, the active and reactive power output of the converter during this period of increasing PCC voltage amplitude is much greater than the rated capacity, which may cause equipment damage. During the Δt_2 (0.32 s), the PCC voltage amplitude under the additional current control is higher because of the larger active output and can provide more energy ($S_{P2N} - S_{Q2P}$). When $t = 0.7$ s, the fault recovers, but the voltage recovery process of power reference changing is slow because of the big difference between the normal and fault operation state, resulting in power feedback. Furthermore, the trend of the power output curve in Figure 8 shows that the additional current control (red line) can provide stable power output for the system within 0.1 s after the fault due to its good dynamic response.

Figure 9 shows that the frequency deviation is smaller and more stable because the additional current control is faster and closer to the actual value during the fault period.

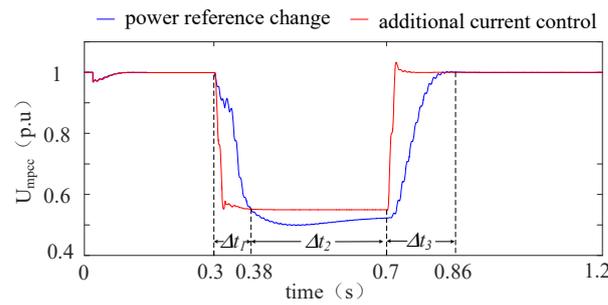


Figure 7. Comparison chart of PCC voltage amplitude.

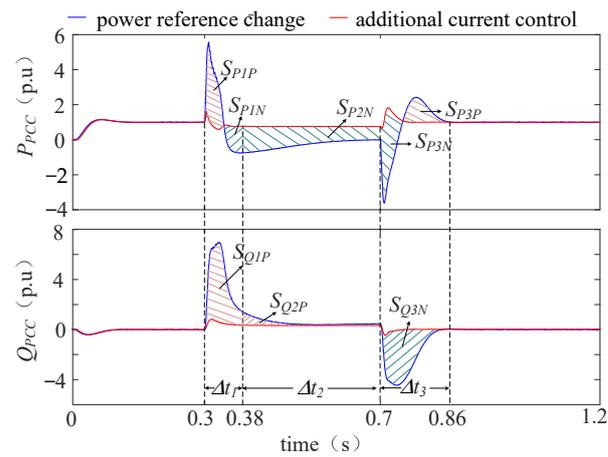


Figure 8. Comparison chart of output power.

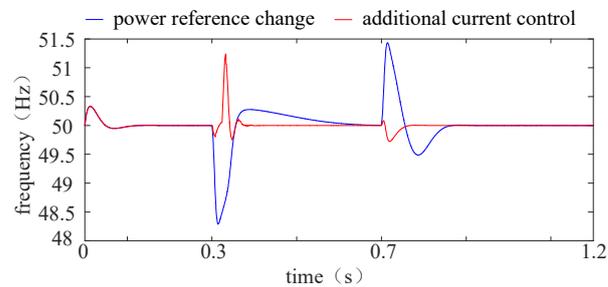


Figure 9. Comparison chart of frequency.

3.3. Comparative Analysis between Additional Current Control and Amplitude Limitation

Setting the current limiter directly after the voltage outer loop may cause system instability, thus the current reference used in current amplitude limitation is set by Equations (11) and (12). Thus, the converter is operated as a current source when the output current exceeds the limit. Taking a grid voltage drop of 0.2 pu as an example, the variation of each electrical quantity during the fault is found and is shown in the figure below.

Current amplitude limitation cannot control voltage effectively for its current source characteristic during faults. As seen in Figure 10, the voltage distortion under current amplitude limitation is serious, will increase the power loss and affect its fault ride-through capabilities, corresponding to Figure 11 (blue line), it can be seen that the converter export voltage during the fault can not be effectively controlled and be in a decreasing trend. According to the simulation of the proposed control strategy, the voltage waveform under fault is relatively stable, which can provide higher and more stable voltage support for PCC.

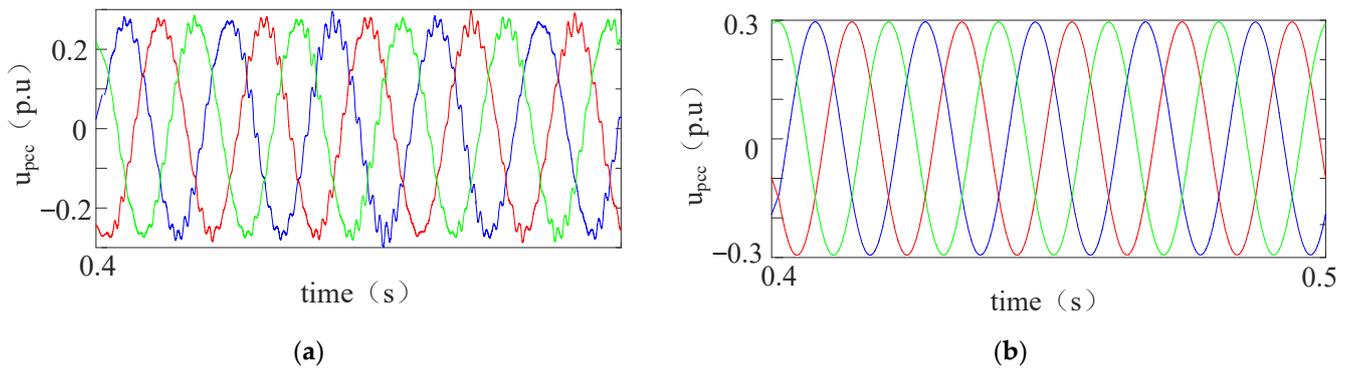


Figure 10. Comparison of PCC voltage: (a) PCC voltage under current amplitude limitation and (b) PCC voltage under additional current control.

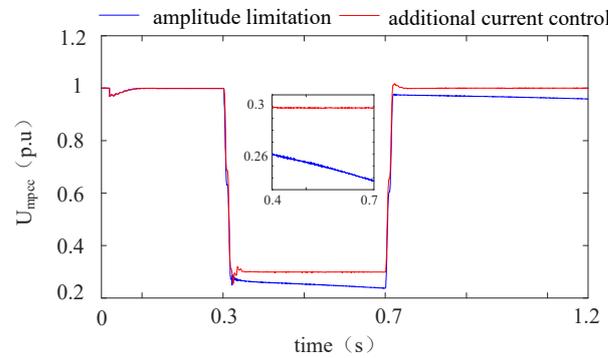


Figure 11. Comparison of PCC voltage amplitude under amplitude limitation and additional current control.

Another problem of the current amplitude limitation is the integral accumulation of outer voltage loop during fault. The system will become unstable if the current limiting is directly switched to the previous control mode. As illustrated in Figure 11, the voltage cannot recover to the set value.

3.4. Comparative Analysis between Additional Current Control and Virtual Impedance

Taking the virtual impedance design method in [21] as the reference, the output current and voltage results under the two control methods are found and are shown in Figures 12 and 13.

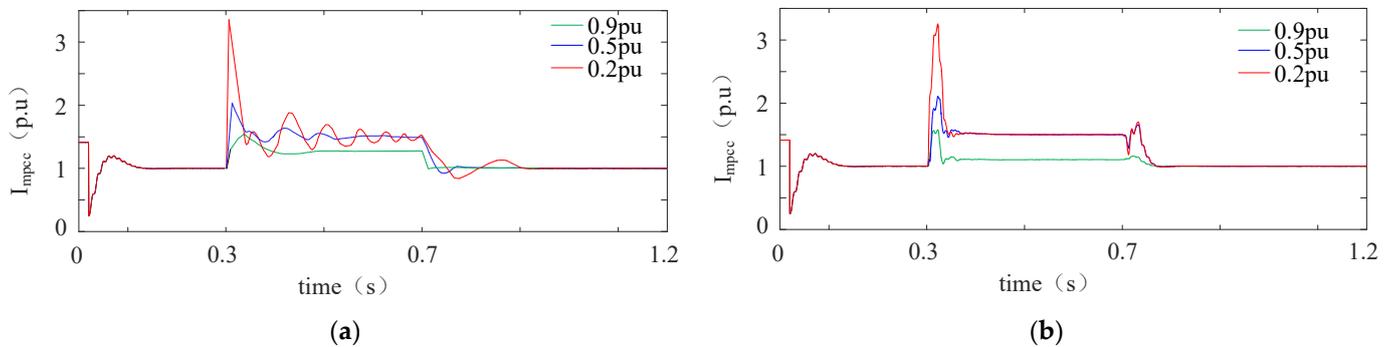


Figure 12. Comparison of output current amplitude: (a) output current amplitude under virtual impedance control and (b) output current amplitude under additional current control.

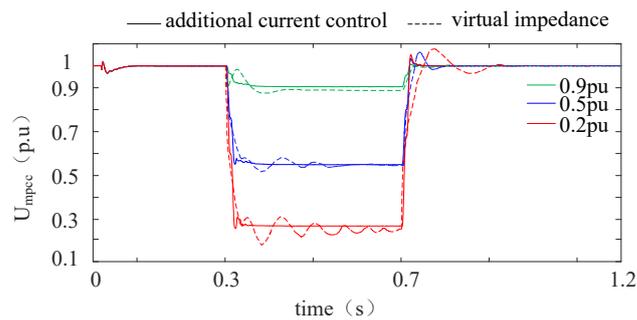


Figure 13. Comparison of PCC voltage amplitude under virtual impedance and additional current control.

In Figure 12a, the amplitude of output current under virtual impedance control fluctuates seriously with the increase of voltage sag, reducing the current response speed. When the grid voltage drops to 0.2 pu, the virtual impedance control stabilizes the current around the set value in 0.4 s after the fault. In addition, the output current of the converter fluctuates, resulting in an unstable voltage at the PCC (dotted line in Figure 13). Compared with the virtual impedance, the proposed additional current control can realize the rapid control of the current under different voltage sags, stabilize the current at the set value within 0.1 s, and provide stable voltage support for the grid.

3.5. Current Limitation Effect under Different Capacities

To further verify the effectiveness of the proposed strategy, the strategy is applied to different converter capacities to observe its control performance and the performance is shown in Figures 14–16. For comparison, the conventional control effect without current limiting strategy is shown in Figures 17 and 18.

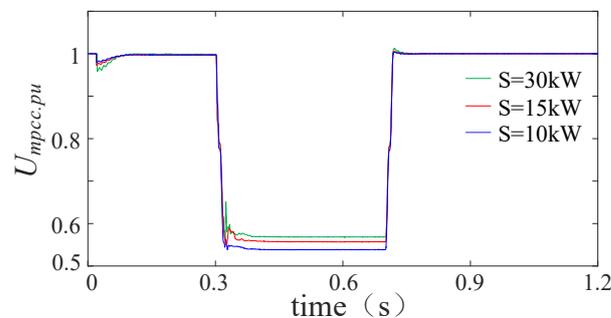


Figure 14. Voltage magnitude curve under additional current control at different capacities.

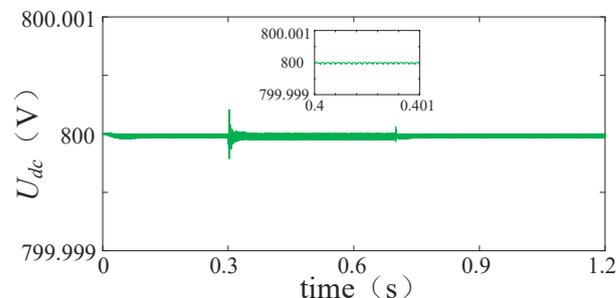


Figure 15. DC capacitor terminal voltage.

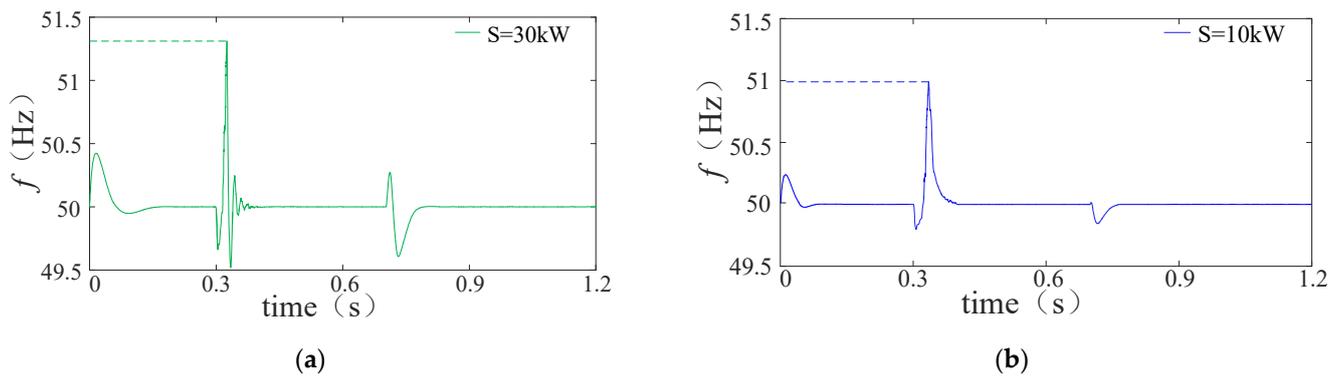


Figure 16. Frequency curve under additional current control: (a) converter capacity, $S_N = 30$ kW and (b) converter capacity, $S_N = 10$ kW.

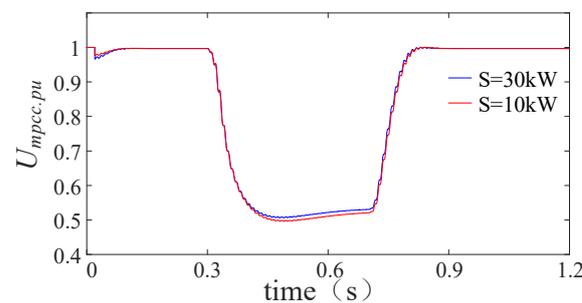


Figure 17. Voltage magnitude curve under conventional control at different capacities.

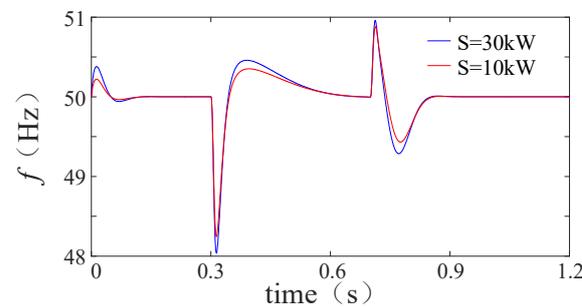


Figure 18. Frequency curve under conventional control at different capacities.

The voltage and frequency response curves in Figures 17 and 18 show that the conventional control is unable to change quickly and meet the output requirements of the converters during the fault scenarios. This inability is because the original control target remains unchanged. Thus, there will be a large frequency and voltage dip, thus the control cannot provide a smooth voltage support for the system.

From Figures 14–16, it can be shown that different capacity converters can be stabilized within 0.1 s under fault scenarios using the control method proposed in this paper. The proposed method has the following three main advantages compared with conventional control.

1. Fast response speed: the proposed control can achieve stability within 0.1 s after a fault.
2. The control method proposed in this paper can maintain the frequency deviation within 1.5 Hz compared to a frequency change of 2 Hz under a conventional controller.
3. The proposed control can promote voltage stabilization faster than a conventional controller and keep the voltage at a higher level. Hence, the proposed control can provide uninterrupted voltage support for the grid and facilitate fault recovery.

4. HIL Validation

To further verify the effectiveness of the proposed current limiting strategy, the strategy has been validated through hardware-in-the-loop experiments using an RTDS platform. The hardware set-up is shown in Figure 19. This research selected the Xilinx Virtex-6 series ML605 integrated development board. The research also used the Verilog HDL hardware description language to develop and implement the control strategy proposed in this paper under Xilinx ISE 14.7 integrated development environment. Finally, the modulation wave was generated by an FPGA board. The communication connection between the FPGA board and RTDS was established through an optical fiber.

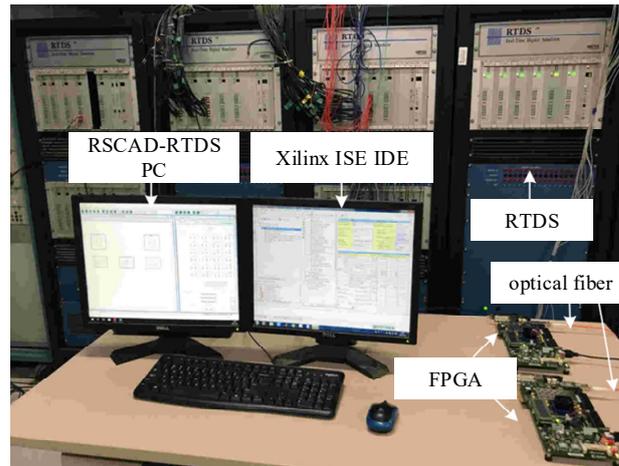


Figure 19. Configuration of the experimental platform.

The control effect after the application of the proposed strategy and under the conventional control are shown in Figures 20–25. The experimental results are in good agreement with the simulation that the proposed control has better stability during the fault and enables fault recovery.

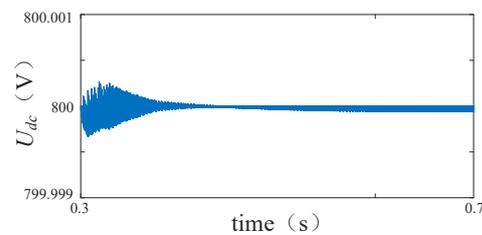


Figure 20. DC capacitor terminal voltage under conventional control.

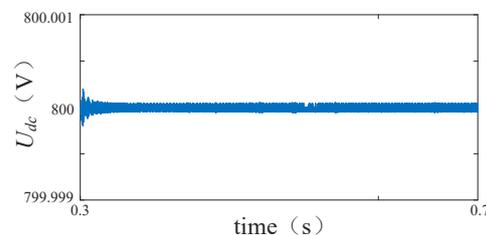


Figure 21. DC capacitor terminal voltage under additional current control.

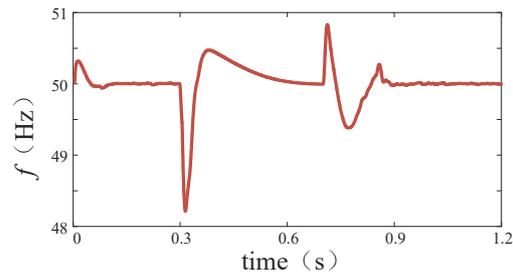


Figure 22. Frequency under conventional control.

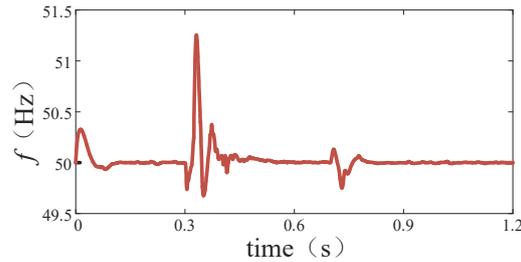
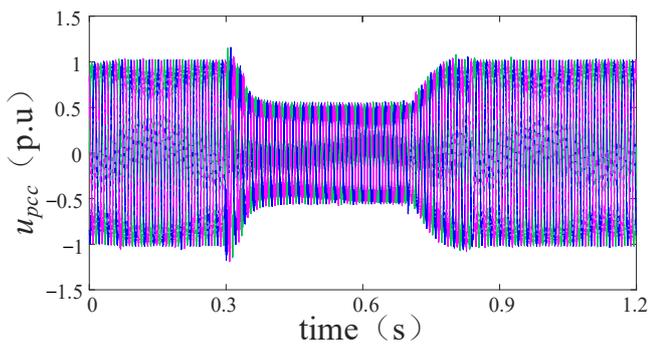
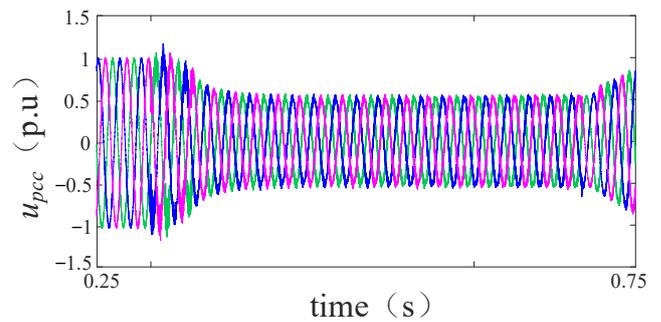


Figure 23. Frequency under additional current control.

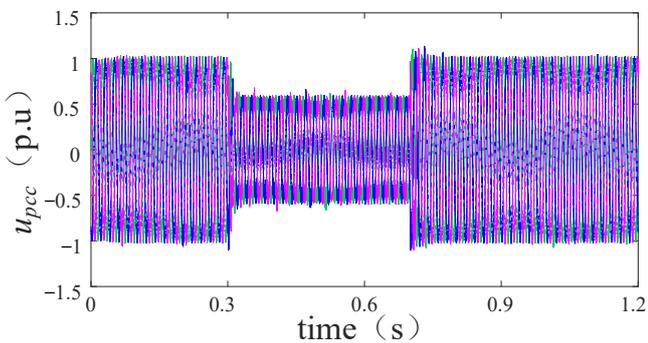


(a)

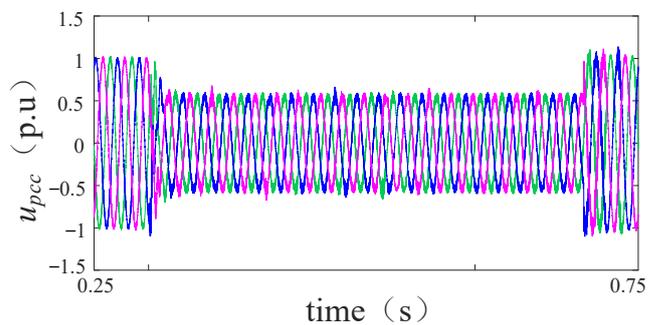


(b)

Figure 24. Voltage curve under conventional control: (a) voltage of the whole experiment and (b) voltage between $t = 0.25\text{--}0.75$ s after magnification.



(a)



(b)

Figure 25. Voltage curve under additional current control: (a) voltage of the whole experiment and (b) voltage between $t = 0.25\text{--}0.75$ s after magnification.

5. Conclusions

Aiming to solve the overcurrent caused by three-phase symmetrical faults, this paper proposed a current limiting method for GFM converter with low-pass filtering and additional current loop.

By adopting the proposed method, the decay rate of current is accelerated to reach the set value quickly. At the same time, this method ensures the voltage source characteristics of GFM and provides continuous and stable voltage support for the grid. The addition of low-pass filtering solves the problem of frequencies beyond the limit caused by the instantaneous input of the active additional current loop and smooths the frequency fluctuations. Furthermore, the proposed strategy makes full use of the capacity margin of the converter and provides voltage support during the fault period while ensuring the active transmission capacity to the greatest extent.

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Appendix A

In the above topology (Figure A1), nodes eight and nine are generator nodes. The distributed power supply is accessed by node 7 with a voltage level of 380 V and nodes 1–6 are load nodes. The parameters of two generators are shown in Table A1, and the parameters of lines and loads are shown in Table A2.

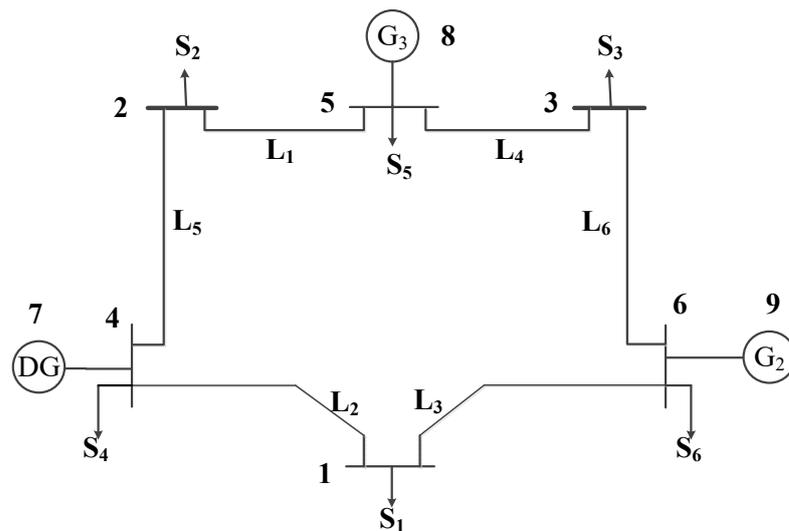


Figure A1. Power grid topology adopted in this paper.

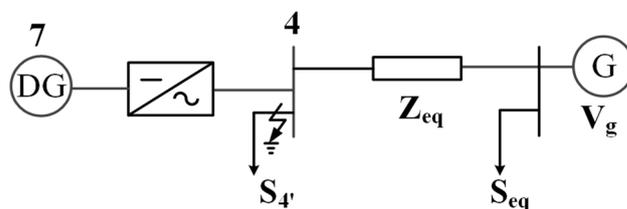
Table A1. Parameters of generators.

| | | |
|--------------|------------|-------|
| Generator G2 | S_n /kVA | 400 |
| | U_N /V | 380 |
| | f_N /Hz | 50 |
| | K_p | 0.045 |
| | J | 3.6 |
| | D_p | 0.41 |
| Generator G3 | S_n /kVA | 400 |
| | U_N /V | 380 |
| | f_N /Hz | 50 |
| | K_p | 0.045 |
| | J | 3.6 |
| | D_p | 0.41 |

Table A2. Parameters of the power grid topology.

| | R (Ω) | L (mH) |
|-------|------------------|----------|
| L_1 | 0.45 | 0.9 |
| L_2 | 0.62 | 1.24 |
| L_3 | 0.55 | 1.1 |
| L_4 | 0.25 | 0.5 |
| L_5 | 0.3 | 0.6 |
| L_6 | 0.35 | 0.7 |
| S_1 | 0.5 | |
| S_2 | 0.4 | |
| S_3 | 0.4 | |
| S_4 | 0.3 | |
| S_5 | 0.3 | |
| S_6 | 0.5 | |

The power grid can be regarded as a voltage source string impedance through network structure equivalence, and the circuit with the equivalent impedance is shown in Figure A2.

**Figure A2.** The circuit with power grid topological impedance equivalence.

In Figure A2, the equivalent impedance of the grid, $Z_{eq} = 0.3 + j0.3 \Omega$ and $S_{eq} = 0.4 \Omega$. To simulate the scenario of grid fault required in this paper, three-phase short-circuit grounding fault is set at bus four, and the drop degree of the equivalent voltage source is changed by setting different grounding resistance. When the grounding resistance is set to 0.075, 0.3, and 2.7 Ω , it corresponds to the scenario that the grid voltage drops to 0.2, 0.5, and 0.9 pu, respectively.

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