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Bifurcation Phenomena in Open-Loop DCM-Operated DC–DC Switching Converters Feeding Constant Power Loads

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Abstract: Constant power loading is an effect that appears in multiple-stage energy conversion systems with individually regulated switching power converters. In a two-stage system, an upstream or source converter drives one or more downstream or load converters. The downstream converters in a two-stage power conversion system are designed to provide the fastest transient response in stand-alone operation. Consequently, they behave as a constant power load (CPL) to the upstream converter within their control bandwidth. In the past, open-loop power converters feeding CPLs and operating in discontinuous conduction mode (DCM) were considered to be stable. In this paper, it is shown that these systems can undergo instabilities, which have been so far overlooked. First, numerical simulations from the switched model of an open-loop boost converter under DCM operation and loaded with a tightly regulated buck converter and the same converter loaded by an ideal CPL are presented to show that they exhibit similar nonlinear behavior and bifurcation phenomena. Then, the three elementary open-loop DC–DC converters operating in the DCM were considered and their bifurcation phenomena were revealed. It is shown that the period-doubling route to chaos in the DC–DC boost converter is interrupted by a sudden appearance of dangerous destructive dynamics due to the excessively unlimited load current in the CPL. For the buck converter, only the first period-doubling bifurcation is observed before the destructive behavior appears. The open-loop buck–boost converter under DCM and feeding a CPL is always unstable and exhibits no periodic orbit. Based on the observed phenomena, approximate discrete-time models were derived, which despite their simplicity, were seen to display the most-important and -essential features of the corresponding switching converters before destructive dynamics occurs.

Keywords: period-doubling; nonlinear circuits and systems; open-loop DC–DC converters

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1. Introduction

Cascaded DC–DC power converters appear in many engineering applications of power electronics such as electric vehicles and ships [1–5], microgrids [6–9], more electric power aircraft [10], and more electric ships [4], among others. In cascaded DC–DC converters, the first stage is called the source or the upstream converter, and the second stage is the load or the downstream converter. When the latter is controlled to maintain a tightly regulated output voltage on the load, it behaves as a constant power load (CPL) for the source converter [9–14]. For instance, in a microgrid with different voltage buses, if the downstream power electronics interface, which could be a grid-connected DC–AC inverter or a DC–DC converter, is tightly regulated, it will absorb constant power from the upstream DC–DC converter. The motor of an electric vehicle (EV) with tight velocity control and under constant torque operation will also absorb constant mechanical power from the three-phase DC–AC inverter, hence resulting in a CPL to the upstream DC–DC boost converter [14]. It is remarkable that the source converters in the previously mentioned

applications feed CPLs and that the number of these applications is increasing at an enormous rate.

A DC–DC converter comprises reactive elements such as inductors and capacitors and semiconductor devices such as transistors and diodes operating as periodically controlled switches that change their state when certain events take place. The common node between the transistor and the diode connects to an inductor. In most of the applications, continuous conduction mode (CCM) is employed. In this case, the inductor current never drops to zero. Yet, discontinuous conduction mode (DCM) can also be used for certain applications. In this case, the inductor current drops to zero and remains null until the end of the switching cycle. When a converter operates in DCM, it provides the potential advantages of better closed-loop stability with simple control and the reduced cost of the converter, among others advantages [15]. DCM typically occurs with a large inductor current ripple in a unidirectional converter operating at a light load. For instance, DCM is eventually encountered in a converter when its load is removed. In some applications, converters are deliberately designed to operate in DCM for all loading conditions. The DCM operation of elementary DC–DC converters is characterized by the fact that some switching instants are internally controlled even under open-loop operation. Indeed, the diode changes its conducting state when the inductor current becomes zero.

Generally, the mathematical model of cascaded DC–DC converters is high-dimensional, making their stability analysis challenging. The impedance criterion is a frequency domain technique widely used for the stability analysis of cascaded converters, after it was first proposed for predicting input filter interactions in DC–DC converters [16]. Later, the same criterion was applied for cascaded converters, leading to the definition of the minor loop gain consisting of the ratio between the output impedance Z_o of the load converter and the input impedance Z_i of the source or downstream converter. This minor loop Z_o/Z_i has since been widely used to assess the stability of cascaded converters.

In the theoretical treatment of the instabilities of the full-order system, several idealizations of the actual features of its behavior are possible. The choice of the idealization to be made and the parameters and the state variables to be omitted or simplified in the mathematical model depend on the specific problem and the kind of instability to be studied. The usual idealization of the load converter is to consider it as a CPL, leading naturally to a static equation for this stage, hence to a significant order reduction of the source converter model, but at the expense of an additional nonlinearity in the state equations. Indeed, in this kind of application, the whole system can be simplified as a DC–DC converter supplying a nonlinear CPL [9,14]. The effect of the different parameters of the source converter from the perspective of its stability can be, therefore, revealed using reduced-order models.

In reality, the steady-state regime of DC–DC converters is a periodic orbit, not an equilibrium point. The desired period of this periodic orbit is the same period of the external driving signal of the switches [17–19]. In the past, current-mode-controlled DC–DC converters have been a subject of intensive research studies (see [19] and the references therein), where it was shown using bifurcation theory that these systems are prone to exhibit a rich variety of complex dynamics and nonlinear behavior such as subharmonic and chaotic oscillations. The coexistence of different steady-state behaviors has been also shown to occur in these systems. Another type of bifurcation mainly attributed to the discontinuity of their Poincaré map models has been also demonstrated to take place in DC–DC converters. These discontinuity-induced phenomena are called border collision bifurcations [18]. In this type of bifurcation, the standard cascade period-doubling scenario is interrupted by a sudden jump to a different behavior due to the collision of the system trajectory or limit cycle with a border defining the limit of validity of the converter model.

Close to an operating point, CPLs exhibit a negative resistance behavior, leading to a high risk of instability [11,14,20,21]. A large number of different analysis attempts have been published for the converters feeding CPLs and operating in CCM, but only a few of these converters operating in DCM have been addressed. From the existing literature, it can be claimed that, with the exception of [22,23], the research and results that have been

published so far on the instability issues in DC–DC converters feeding CPLs considered the CCM operation. The available results on the stability analysis in [22,23] were based on averaged models, leading to inaccuracies in predicting the onset of instability in these systems in the parameter space. Indeed, it was concluded in [23] that the open-loop buck and boost converters operating in DCM are stable when they are loaded by CPLs. Using a nonlinear implicit discrete-time model [17,24–28], we show here that such claims about the stability of the buck and the boost converter are not accurate.

It is well known that closed-loop switching converters with both resistive loads and CPLs are prone to exhibit a large variety of complex dynamics and undesired instabilities [18,19,29–37]. The common denominator in all the past studies and research works was the consideration of a closed-loop converter either under VMC [17,26–28,38–41] or current mode control (CMC) [42–47]. In converters with a linear load, either resistive [17,26–28,38,40] or constant current [41] load, the piecewise linear state equations are employed for DC–DC converters to obtain the discrete-time model, and the stability analysis passes through solving the eigenvalues problem of the Jacobian matrix of this model, which can be obtained in closed-form. This is not directly applicable to DC–DC converters loaded by a CPL [30,31]. To effectively study instabilities in this case, ad hoc stability analysis techniques must be used. For instance, the piecewise linear approach can still be be employed to obtain their approximate discrete-time model and to perform the stability analysis of their periodic orbits, but after a careful linearization of the nonlinear model of the CPL [31].

For DC–DC converters with a resistive load operating in DCM and under a VMC feedback loop intending to regulate the output voltage, approximated discrete-time models were used in [38,39] to predict the onset of period-doubling bifurcation. The approximate discrete-time models were obtained by approximating the state transition matrices corresponding to each switch position of the converters. The same model can be obtained by discretizing the averaged model at the switching frequency rate. This is particularly useful when the state transition matrices are not available in closed-form, as when the load is nonlinear, such as a CPL. The model used in [38,39] was re-utilized in [48] to study the small signal behavior of a DC–DC converter. It is worth noting that, in the previous work, open-loop operated converters were not considered. Obviously, with a linear resistive load, the discrete-time model corresponding to an open-loop DC–DC converter is linear and always stable, and therefore, bifurcation phenomena cannot take place. The situation is different when the load is nonlinear, as the one considered in this study. In this case, the discrete-time model of the converter is nonlinear even under open-loop operation, and bifurcation phenomena can take place, as will be detailed later.

The main novelty in this paper is that the nonlinear behavior was observed in DC–DC converters operating in open-loop, i.e., with a duty cycle given in a fixed pattern and without any feedback loop. Apart from [49], which was our initial work on this topic, the literature reports no other work on nonlinear behavior such as period-doubling and bifurcation phenomena in open-loop-operated DC–DC converters. Indeed, an accurate implicit discrete-time modeling approach was proposed in [49], where the dynamics of the open-loop boost converter operating in DCM and feeding a CPL was explored in the parameter space, revealing the occurrence of period-doubling bifurcation when suitable parameters were varied. Following our previous work in [49] for the boost converter, we extended here our study to other elementary switching converters. The three open-loop elementary DC–DC converters feeding CPLs were considered and their stability analysis performed. Approximate explicit discrete-time models for the buck and the boost were also derived, allowing us to analytically perform the stability at the fast switching scale, predicting the onset of period-doubling and other bifurcations in the parametric space. The derived models, despite their simplicity, were to display the most-important and -essential features of the corresponding switching converters.

The rest of this paper is organized as follows: After this Introduction, in Section 2, the dynamical behavior of a DC–DC boost converter loaded by a CPL and operating in DCM is compared to the behavior of the same converter loaded by a tightly regulated buck

converter, putting in evidence the CPL effect of the latter. The experimental setup and some measurements are presented in Section 3, showing period-doubling bifurcation in an open-loop-DCM-operated boost converter with a CPL. The switched models of the three elementary DC–DC converters loaded by a CPL are given in Section 4, and the parametric space region where they operate in DCM is determined in Section 5 in tabular form. In Section 6, the average dynamics for DCM-operated power converters loaded by a CPL are given, and the expression of their equilibrium points, static voltage conversion gains, and stability boundary at the slow time scale (low-frequency) are determined. In Section 7, the period-doubling bifurcation of periodic orbits in open-loop-DCM-operated DC–DC converters feeding CPLs are shown to occur in these systems by using numerical simulations performed on the exact switched model implemented in the PSIM© software. The nonlinear dynamic behavior is addressed in Section 8, where the existence conditions and the stability and bifurcation analysis of the fundamental one-periodic orbit are presented, and different regions in the parameter space are determined for the open-loop boost and the buck converters. Finally, Section 9 summarizes the conclusions of this work.

2. Period-Doubling Bifurcation in an Open-Loop DCM-Operated Boost Converter Feeding a Tightly Regulated Buck Converter

The CPL effect was retaken here for a cascaded connection of two converters being the source converter operating in open-loop and under DCM and the load converter under a tight control of the output voltage. As an example, we considered here an open-loop boost converter loaded by a voltage-mode-controlled buck converter using a two-zero three-pole Type-III controller, as illustrated in Figure 1. Notice that, traditionally, converters with tight voltage control using a fixed frequency PWM are considered as a CPL [1,2]. Since the power delivered to the load is proportional to the squared voltage, if the voltage is tightly regulated, the instantaneous absorbed power will be practically constant. The values of the circuit parameters for the source converter and the load converters are depicted in Table 1. The chosen parameter values of the boost converter guarantee DCM operation. Those of the buck converter power stage and its operating duty cycle (output voltage) correspond to CCM. The parameter values of the Type-III voltage controller were chosen for an optimal response in terms of bandwidth and overshoot. For that, the gain of the controller was $\kappa = 0.6$, the two zeros' frequencies were 1 kHz and 8 kHz, and the two poles' frequency was 50 kHz both. The buck converter was loaded by a resistive load, whose resistance R_L was varied according to the power of the CPL ($P = v_{\text{ref}}^2/R_L$).

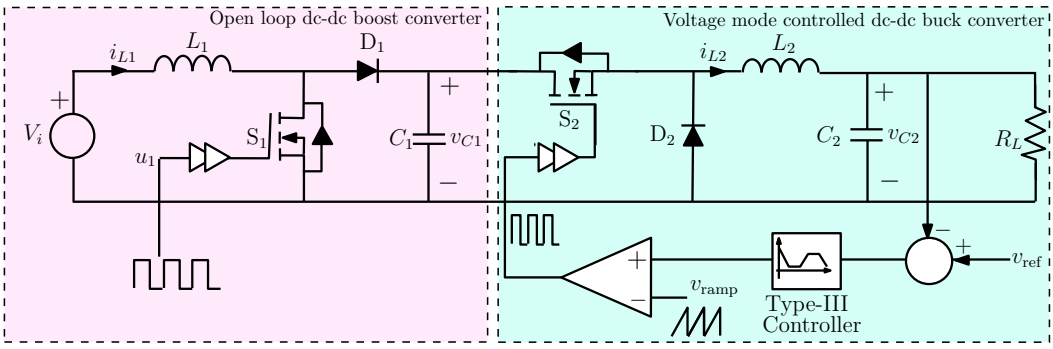
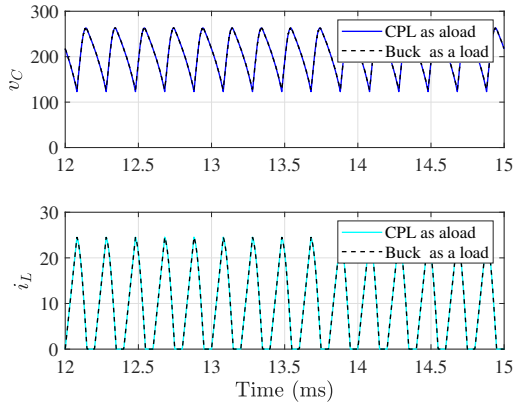


Figure 1. An open-loop boost converter loaded by a voltage-mode-controlled buck converter.

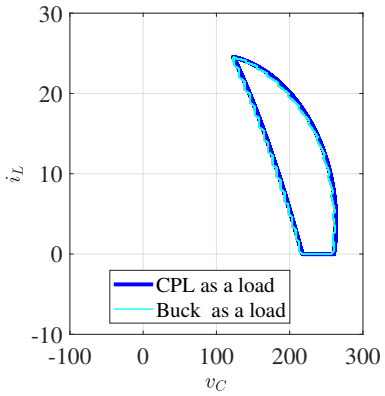
Figure 2 shows the behavior of an open-loop boost converter operating in DCM loaded, in the first case, by a tightly regulated buck converter with VMC and, in the second case, by an ideal CPL with the load power corresponding to a stable periodic regime and subharmonic oscillation in both cases. The agreement between the results depicted in Figure 2 was remarkable. Therefore, we continued our study by considering the load converter as an ideal CPL.

Table 1. Parameters used in the numerical simulations of the cascaded boost and buck converters.

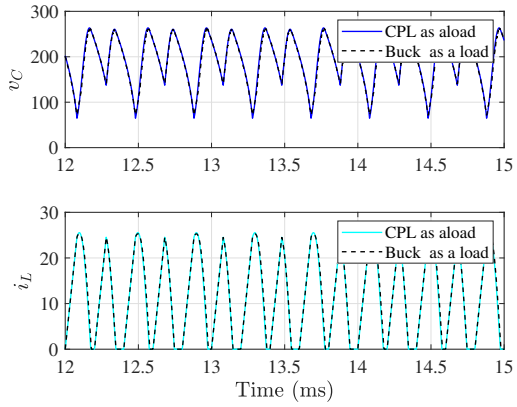
Source Converter (Boost)	**Load Converter (Buck)**
Input voltage, $V_i = 100$ V	Output voltage v_{ref} 48 V
Duty cycle, $D = \frac{1}{3}$	Load resistance R_L variable
Inductance, $L_1 = 326$ µH	Inductance $L_2 = 250$ µH
Capacitance, $C_1 = 4.5$ µF	Capacitance $C_2 = 47$ µF
Switching frequency $f_{s1} = 5$ kHz	Switching frequency $f_{s2} = 200$ kHz



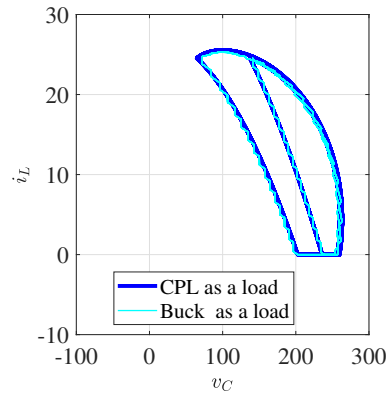
(**a**) $P = 800$ W.



(**b**) $P = 800$ W.



(**c**) $P = 900$ W.



(**d**) $P = 900$ W.

Figure 2. Behavior of an open−loop boost converter operating in DCM loaded by a tightly regulated buck converter and by an ideal CPL. (**a, b**) $P = 800$ W: stable periodic regime, (**c, d**) $P = 900$ W: subharmonic oscillation.

3. Experiments

An experimental prototype was used to observe some of the nonlinear phenomena considered in this study. A picture of the experimental setup is shown in Figure 3.

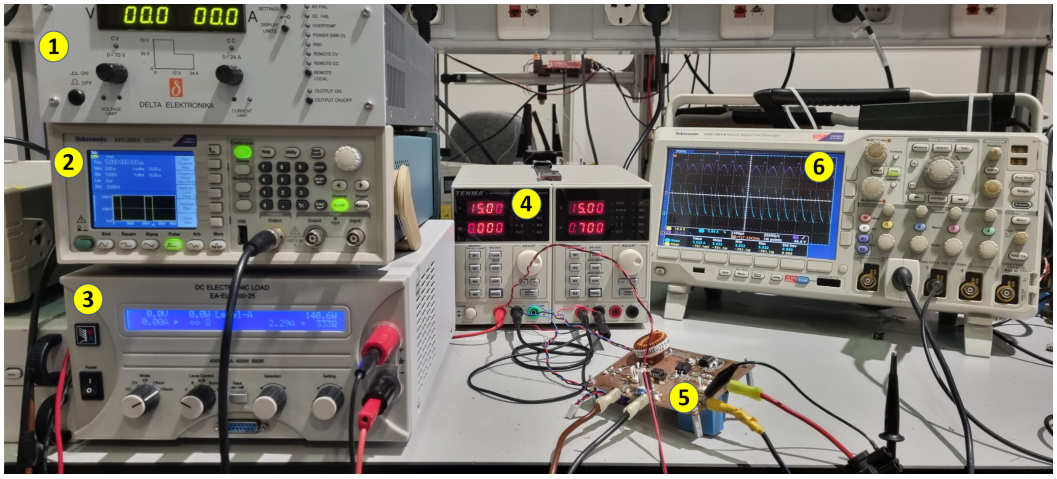


Figure 3. The experimental setup to observe period-doubling bifurcation in an open-loop boost converter with a CPL. ① Power supply, ② Function generator. ③ Electronic load. ④ Power supply. ⑤ Boost converter circuit. ⑥ Oscilloscope.

A dynamic load, ELEKTRO-AUTOMATIK EL3400-25, was used to emulate a CPL as a load for the converter. The nominal values of parameters were the same ones used in the theoretical study that will be presented. The switch was implemented using the IPB60R099CPA CoolMOS, and the used diode was STTH30R06CW (a Schottky diode). The inductor was fabricated using the Toroidal Magnetics Kool-mu core 2300HT-220-V-R with a nominal value of 200 μH. Its internal resistance was measured to be approximately 0.1 Ω. The output capacitor used consisted of a parallel connection of three film capacitors with a capacitance of 1.5 μF for each one, for a total capacitance of 4.5 μF. The driving square wave signal for the switch was provided by a function generator, Tektronix AFG2021. The switching frequency was fixed to 5 kHz, and its duty cycle was fixed to 0.22. The input voltage was fixed to 48 V. All the measurements were captured using a TEKTRONIX oscilloscope, MDO 3024.

Figure 4 shows the time domain waveforms and the state plane trajectories for two different values of the power. For $P = 28$ W, the system behavior was stable and periodic with the same period as the driving signal (Figure 4a,b). For $P = 30$ W, the converter exhibited subharmonic oscillation due to a period-doubling bifurcation (Figure 4c,d).

Remark 1. *Due to the danger of experimenting with a CPL because of the destructive dynamics associated with the small CPL voltage and, consequently, unlimited current, the values of the power used were deliberately chosen to be low in the experiments. However, the same phenomena take place for higher values of the power, but this could result in a* dangerous catastrophic destructive *behavior for the converter and also the electronic load emulating the CPL. Our main concern in this paper was to demonstrate that period-doubling bifurcation is possible in an open-loop-operated DC–DC converter when this is loaded by a CPL. Observe that, under complex dynamics, such as subharmonic oscillation and chaotic regimes, the ripple of the state variables becomes so large, that if the voltage of the CPL approaches low values, its current becomes very large, and vice versa, if the current approaches very small values, the voltage becomes very high. In both cases, once the current or the voltage reaches a certain value, the protections of the electronic load that we used to emulate the CPL are activated. With the protections activated, the dynamics of the system change, and some phenomena such as chaotic behavior would not be possible to detect.*

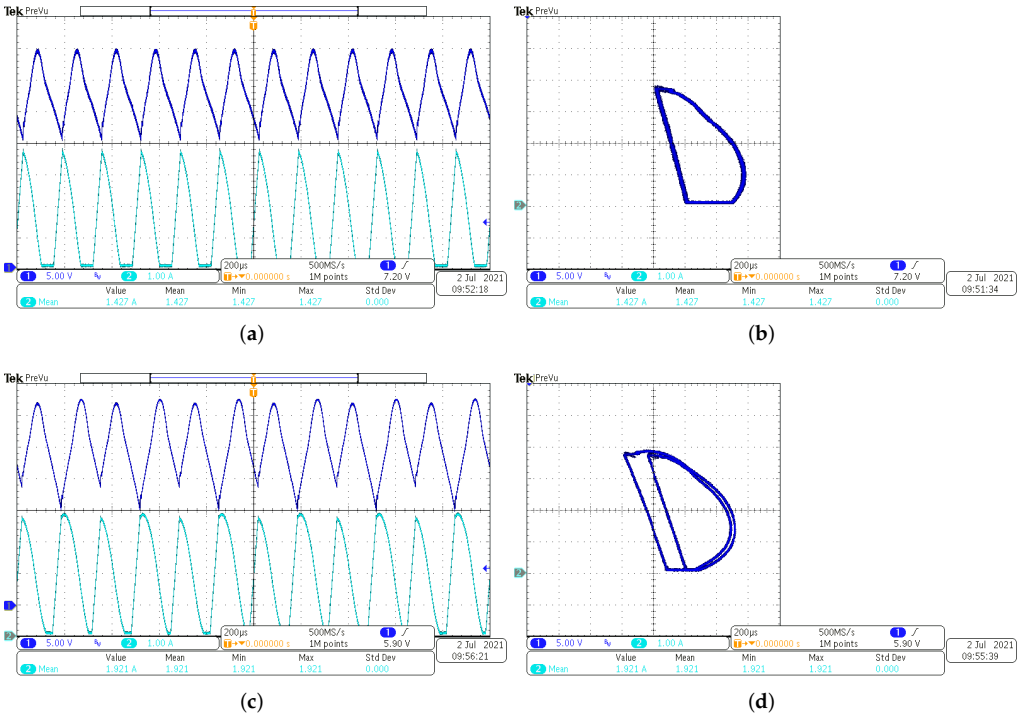


Figure 4. waveforms of an open-loop boost converter operating in DCM loaded by an ideal CPL. (**a,b**) $P = 28$ W: stable periodic regime, (**c,d**) $P = 30$ W: subharmonic oscillation due to period-doubling bifurcation.

4. Switched Model of Open-Loop Elementary DC–DC Switching Converters with a CPL

The theoretical study carried out in this paper corresponded to the elementary buck, boost, and buck–boost converters loaded by a CPL depicted in Figure 5. It was supposed that the switch Q of the converter is driven by a square wave periodic signal u with a period T (switching frequency $f_s = 1/T$) and a fixed duty cycle $D \in (0,1)$. Table 2 summarizes the state equations of three elementary converters with physical state variables and parameters, where v_C is the voltage across the capacitor, whose capacitance is C, i_L is the current through the inductor, whose inductance is L, V_i is the input voltage, and P is the CPL power.

Table 2. State equations for the three elementary converters with a CPL.

	Buck	**Boost**	**Buck–Boost**
$\frac{dv_C}{dt}$	$-\frac{P}{Cv_C} + \frac{i_L}{C}$	$-\frac{P}{Cv_C} + \frac{(1-u)i_L}{C}$	$-\frac{P}{Cv_C} + \frac{(1-u)i_L}{C}$
$\frac{di_L}{dt}$	$-\frac{v_C}{L} + \frac{uV_i}{L}$	$\frac{(u-1)v_C}{L} + \frac{V_i}{L}$	$\frac{(u-1)v_C}{L} + \frac{uV_i}{L}$

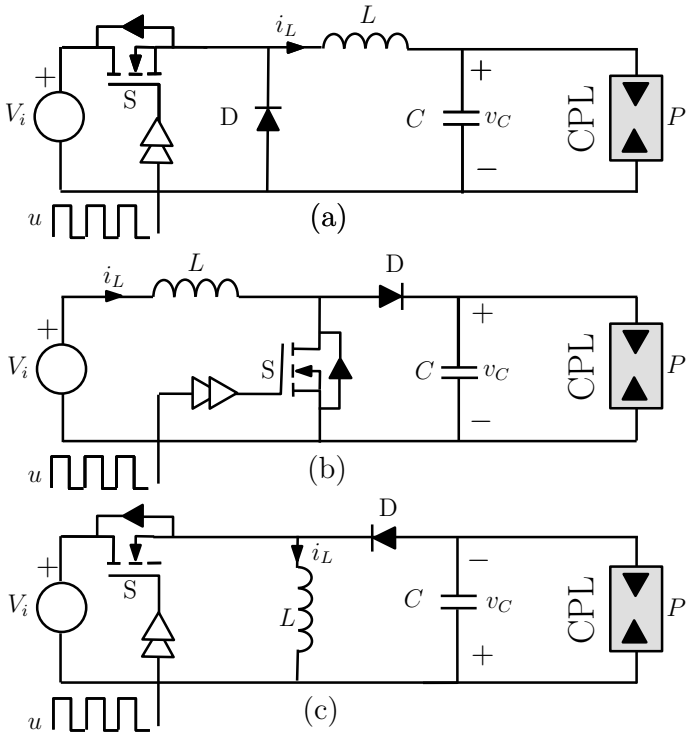


Figure 5. Elementary switching converters loaded by a CPL: (**a**) buck, (**b**) boost, and (**c**) buck–boost.

5. Parametric Space Region for DCM Operation

As in the resistive load case, the boundary between the CCM and DCM operation can be derived in terms of the switching period T, inductance value L, duty cycle D, and input voltage V_i. In the case of the CPL, the boundary also depends on the constant power P. The analysis reported in [50] (Chap. 5) was here adapted for the case of a CPL. In the boundary between CCM and DCM, the inductor current i_L of any elementary converter behaves in steady-state, as illustrated in Figure 6. Roughly speaking, the operation in DCM will eventually take place if either the ripple Δi_L is increased or the average inductor current I_L is decreased. The expression of I_L is given in Table 3 for the three elementary converters. At the boundary of CCM–DCM, one has $\Delta i_L = 2I_L = I_p$.

Table 3. Expressions for the steady-state value of the average inductor current I_L, the critical value P_{cri} of the power P, and the critical value K_{cri} of the dimensionless parameter K at the boundary of CCM–DCM for the three elementary DC–DC converters operating in DCM.

	Buck	**Boost**	**Buck–Boost**
I_L	$\frac{P}{DV_i}$	$\frac{P}{V_i}$	$\frac{P}{(1-D)V_i}$
P_{cri}	$\frac{V_i^2 D^2 T}{2L}(1-D)$	$\frac{V_i^2 DT}{2L}$	$\frac{V_i^2 D^2 T}{2L}$
K_{cri}	$D^2(1-D)$	D	D^2

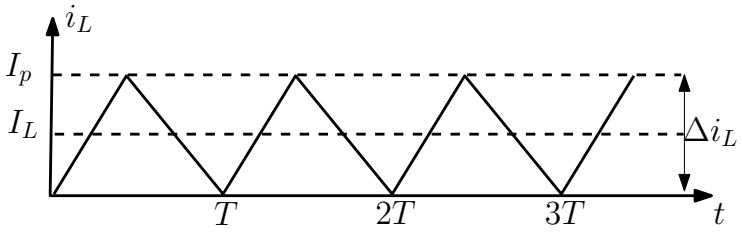


Figure 6. Steady-state inductor current i_L at the boundary of CCM–DCM for any elementary converter.

By particularizing the previous condition for the three elementary converters, the expressions shown in Table 3 for the critical value P_{cri} of the power P were obtained for the three elementary converters. The converter will work in DCM if $P < P_{\text{cri}}$. Let us define the dimensionless parameter $K = 2LP/(V_i^2 T)$. In terms of this dimensionless parameter, the CCM–DCM boundary conditions for the three elementary converters can be rewritten as $K = K_{\text{cri}}(D)$, where $K_{\text{cri}}(D)$ is given Table 3. Figure 7 shows the CCM–DCM boundary for the three elementary switching converters with a CPL in the dimensionless parameter space (D, K). For a specific value of D, if $K > K_{\text{cri}}(D)$, CCM takes place, and if $K < K_{\text{cri}}(D)$, DCM occurs.

It is worth noting that, for the buck converter, the maximum value of $K_{\text{cri}}(D)$ is $4/27$. This maximum value occurs for $D = 2/3$. Therefore, for this converter, the DCM operation will not take place for no value of D if $K > 4/27$. For the boost and the buck–boost converter, there will always exist an interval of the operating duty cycle D within which the DCM operation will theoretically take place if $K < 1$. This interval becomes wider if the value of the dimensionless parameter K decreases.

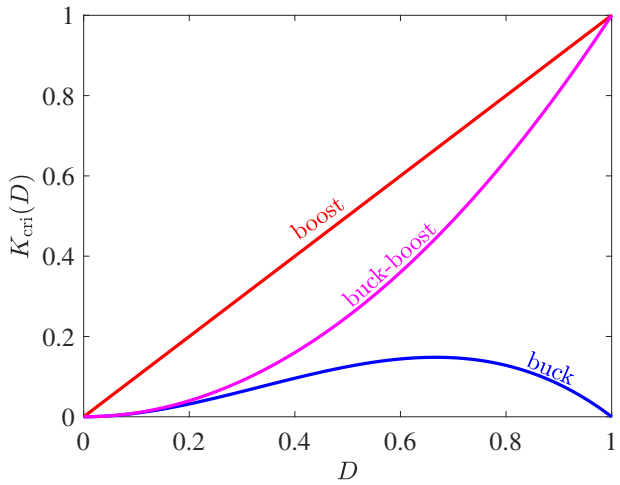


Figure 7. The critical value K_{cri} of K at the boundary CCM–DCM for elementary switching converters loaded by a CPL. For a specific value of D, if $K > K_{\text{cri}}(D)$, CCM takes place, and if $K < K_{\text{cri}}(D)$, DCM occurs.

6. Average Dynamics for DCM-Operated Power Converter with a CPL: Equilibrium Point, Static Voltage Conversion Gain, and Stability

6.1. Averaged Model

Under certain conditions, the dynamics of a DCM-operated converter can be accurately described by an averaged model. Let us assume that the capacitor voltage v_C ripple is sufficiently small during a switching cycle such that time dependence of the inductor current i_L can be considered linear: i_L goes from 0 to a certain peak value I_p during the time interval $(0, DT)$ (that for $u = 1$); after that, i_L drops to 0 during the time interval $(DT, (D + D')T)$ and remains 0 during the rest of the period with duration $(1 - D - D')T$ (Figure 8).

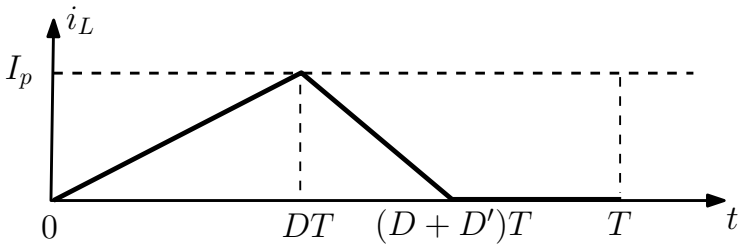


Figure 8. Sketch of the inductor current i_L waveform for any DCM-operated elementary converter.

From the expression of the inductor current time derivative di_L/dt in Table 2 with $u = 1$, the peak inductor current I_p was obtained, and from the same equation with $u = 0$, one obtain the expression of the ratio D'. These results are summarized in Table 4, and using them in the capacitor voltage derivative dv_C/dt (Table 2), in which i_L in the buck is substituted by its average $(D + D')I_p/2$ and $(1 - u)i_L$ in the boost and buck–boost is substituted by $D'I_p/2$, the following averaged models are obtained:

$$\frac{d\overline{v}_C}{dt} = \frac{P}{C\overline{v}_C}\left(\frac{V_i - \overline{v}_C}{V_i}\frac{D^2}{K} - 1\right) \quad \text{buck} \tag{1}$$

$$\frac{d\overline{v}_C}{dt} = \frac{P}{C\overline{v}_C}\left(\frac{\overline{v}_C}{\overline{v}_C - V_i}\frac{D^2}{K} - 1\right) \quad \text{boost} \tag{2}$$

$$\frac{d\overline{v}_C}{dt} = \frac{P}{C\overline{v}_C}\left(\frac{D^2}{K} - 1\right) \quad \text{buck–boost} \tag{3}$$

where the overline stands for averaging over one switching period, i.e., $\overline{v}_C(t) = \int_t^{t+T} v_C(\tau)d\tau$. It is worth noting that the previous models are nonlinear with respect to both the average state variable $\overline{v}_C$ and the duty cycle D. Note also that, in order, to guarantee the DCM operation, the condition $D + D' < 1$ must hold; thus, the value of K_{cri} in Table 3 can also be obtained from this condition with D' and $\overline{v}_C = V_C$ (steady-state) given in Table 4.

Table 4. Peak current I_P, ratio D', averaged voltage V_C, and conversion ratio $M(D, K)$ for the three converters with a CPL under DCM operation.

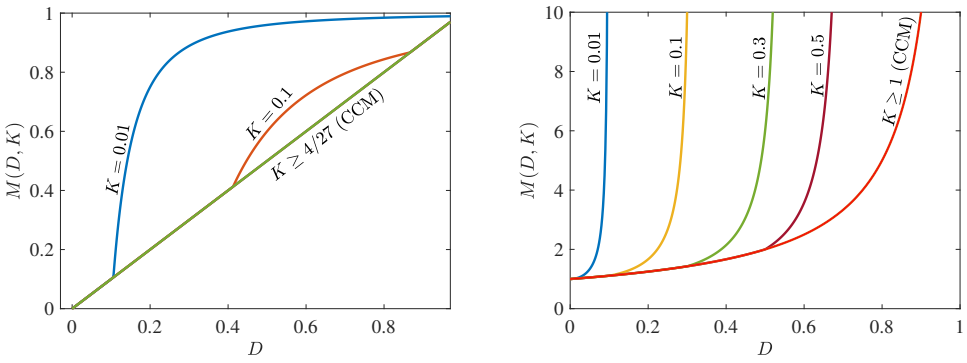
	Buck	**Boost**	**Buck–Boost**
I_P	$\frac{(V_i - V_C)DT}{L}$	$\frac{V_i DT}{L}$	$\frac{V_i DT}{L}$
D'	$\frac{(V_i - V_C)D}{V_C}$	$\frac{V_i D}{V_C - V_i}$	$\frac{V_i D}{V_C}$
V_C	$\frac{V_i(D^2 - K)}{D^2}$	$\frac{V_i K}{K - D^2}$	∄
$M(D, K)$	$\frac{D^2 - K}{D^2}$	$\frac{K}{K - D^2}$	∄

6.2. Equilibrium Points

In the case of existence, the equilibrium points can be obtained by making $d\overline{v}_C/dt = 0$ in the previous differential equations, hence obtaining the expressions of V_C shown in Table 4 for the buck and the boost converters, while no equilibrium exists for the DCM-operated buck–boost converter with a CPL. Note that, for the equilibrium point to exist in the buck and the boost converters, the conditions $K < D^2$ and $K > D^2$ must be fulfilled, respectively. Note also that $D^2 < D^2(1 - D)$, $\forall D \in (0, 1)$, and therefore, an equilibrium point always exists for the buck converter provided that it operates in DCM ($K < K_{\text{cri}} := D^2(1 - D)$).

6.3. Conversion Ratio

Under the existence conditions, the voltage conversion gain $M(D, K) := V_C/V_i$ for the DCM-operated buck and the boost converters with a CPL are given in Table 4. These conversion ratios are plotted in Figure 9 in terms of the duty cycle D for different values of K. It is worth noting that, at the boundary between CCM and DCM, the conversion ratios become the widely known load-independent voltage gains $M(D) = D$ and $M(D) = 1/(1 - D)$ for the buck and the boost converters, respectively.



(**a**) buck (**b**) boost

Figure 9. The conversion gain $M(D,K)$ for the buck and the boost converter for different values of dimensionless parameter K. The conversion gain for CCM is also shown for comparison.

As stated before, the DCM-operated open-loop buck–boost converter does not have an equilibrium point. Indeed, the solution of its averaged differential Equation (3) can be obtained in closed-form, and it confirms the previous statement. Let $z(t) = \frac{1}{2}C\overline{v}_C^2$, that is the averaged stored energy in the capacitor. Therefore, from (3), one obtains the following differential equation corresponding to the buck–boost converter in terms of z.

$$\frac{dz}{dt} = P\left(\frac{D^2}{K} - 1\right) \tag{4}$$

whose solution is as follows:

$$z(t) = z(0) + P\left(\frac{D^2}{K} - 1\right)t \tag{5}$$

Equivalently, in terms of the averaged value $\overline{v}_C$, one has

$$\overline{v}_C(t) = \sqrt{\overline{v}_C^2(0) + \frac{2P}{C}\left(\frac{D^2}{K} - 1\right)t} \tag{6}$$

Three different cases arise depending on D^2 and K. These are:

- $K < D^2$ (DCM operation): The response does not reach any equilibrium in steady-state. It is unbounded, and the system is unstable.
- $K = D^2$ (CCM–DCM boundary): The response is bounded, but presents an infinite number of equilibria depending on the initial condition $v_C(0)$. Indeed, in this case, one has $v_C(t) = v_C(0)\ \forall t$.
- $K > D^2$ (CCM operation): The response collapses at a certain time instant t_c given by

$$t_c = \frac{C\overline{v}_C^2(0)}{2PK(K - D^2)} \tag{7}$$

At this time instant, the voltage v_C across the CPL becomes zero and the current through it becomes infinite. For $t > t_c$, no real solution exists for the buck–boost converter averaged state equation. A similar treatment can be made for the buck and the boost converters under the conditions $V_i \gg \overline{v}_C$ and $V_i \ll \overline{v}_C$, respectively, but in general, the average state equations of these two converters cannot be integrated in closed-form.

Remark 2. *A so-called fast instability was reported in [20], where it was stated that, based on the system parameter values, the converter can go to instability very fast and it does not have enough time even to change the status of the switch. In that work, a resistive load was added in*

parallel with the CPL in the buck–boost converter for an equilibrium point to exist. In reality, this phenomenon takes place because either the initial condition is selected out of the basin of attraction of the equilibrium point or the latter does not exist, provoking a voltage collapse to zero and an infinite current through the CPL. In the experimental circuit, this dangerous catastrophic destructive dynamics may lead to the destruction of switching devices.

Remark 3. *The previous remark is based on the averaged model of the converters. In the real switched system, the ripple of the state variables either in periodic, subharmonic, or chaotic regimes may make voltage collapse to take place at a time instant smaller than* t_c.

6.4. Stability at the Low Frequency (Slow Scale)

To perform the stability analysis of the equilibrium point of the buck and the boost converters, let us define the error $e := \overline{v}_C - \overline{V}_C$. Therefore, from (1) and (2), one can write

$$\frac{de}{dt} = \varphi(\overline{v}_C) \tag{8}$$

where $\varphi(\overline{v}_C)$ is the following function:

$$\varphi(\overline{v}_C) = -\frac{P}{CV_i\overline{v}_C}\frac{D^2}{K} \quad \text{buck} \tag{9}$$

$$\varphi(\overline{v}_C) = -\frac{P}{C(\overline{v}_C - V_i)\overline{v}_C}\left(1 - \frac{D^2}{K}\right) \quad \text{boost} \tag{10}$$

Let us consider the Lyapunov function candidate $V = e^2/2$. Its time derivative is $dV/dt = ede/dt = \varphi(\overline{v}_C)e^2$. For the buck converter, $\varphi(\overline{v}_C)$ is always negative, and the equilibrium point is unconditionally stable since the time derivative of the Lyapunov function is negative in this case. For the boost converter, under the existence condition of the equilibrium point ($D^2 < K$) and if the condition $\overline{v}_C > V_i$ is guaranteed, $\varphi(\overline{v}_C)$ will be negative, and the error asymptotically vanishes in this case.

7. Period-Doubling Bifurcation of Periodic Orbits in Open-Loop-DCM-Operated DC–DC Converters Feeding CPLs

The fast scale dynamics in the switching period taking into account ripples in the state variables cannot be predicted by the averaging approach. In this section, the switched model is used for predicting period-doubling bifurcation in the open-loop-DCM-operated boost and the buck converters with CPLs.

7.1. The Boost Converter

To reveal the possible dynamical behaviors that can exhibit a DCM-operated boost converter with a CPL, a bifurcation diagram was computed using the *exact* switched model of the converter implemented in the PSIM© software. The result is represented in Figure 10. The used fixed parameter values are depicted in Table 5. The parameter P was taken as a bifurcation parameter, which varied in the range $(0.80, 0.96)$ kW. The sampled values of the capacitor voltage $v_C[n] := v_C(nT), n = 0, 1, 2\ldots$ are plotted versus the dimensionless parameter K. Clearly, it can be observed that, from an initial fundamental (one-periodic) orbit, a cascade of period-doubling bifurcations culminates in a chaotic regime. First, a stable two-periodic orbit is generated at a critical value of the power P, $P_{\text{flip}} \approx 847$ W, or equivalently, the dimensionless parameter K, $K_{\text{flip}} \approx 0.276$, and further variations of the bifurcation parameter P or equivalently K make this emerging orbit also unstable, and so on, finally producing chaotic dynamics. This phenomenon is the celebrated period-doubling bifurcation route to chaos encountered in many mathematical and physical systems. By increasing the bifurcation parameter P a bit further, a non-admissible dynamics, both from a mathematical and a practical point of view due to an unlimited CPL current, comes out. Indeed, the increasing size (interval for $v_C[n]$) of the chaotic attractor due

to further variation in the parameter produces the mentioned very high current in the load, and so, the dynamics makes no sense. A numerical integration, for instance with commercial software, would give incoherent results similar to the ones mentioned in Remark 1. The upper value of the bifurcation parameter was selected smaller than the one corresponding to any voltage collapse.

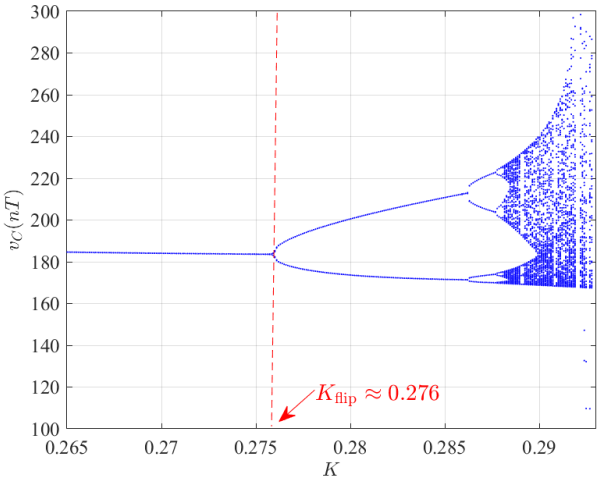


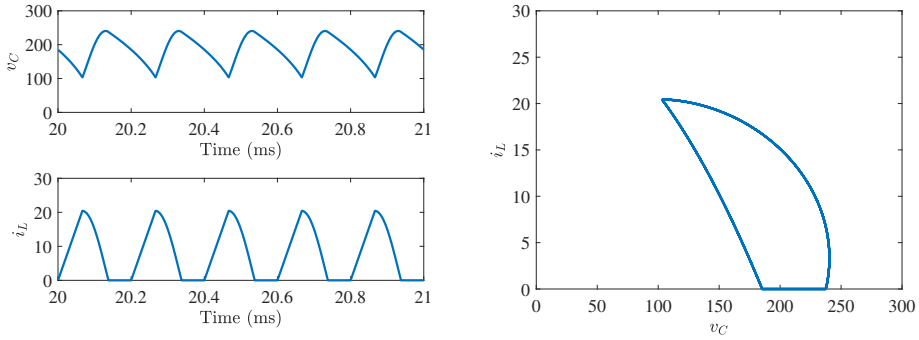
Figure 10. Bifurcation diagram of the DCM-operated boost converter with a CPL obtained using the PSIM© software.

Table 5. The used parameter values for the open-loop buck and boost converters loaded by a CPL.

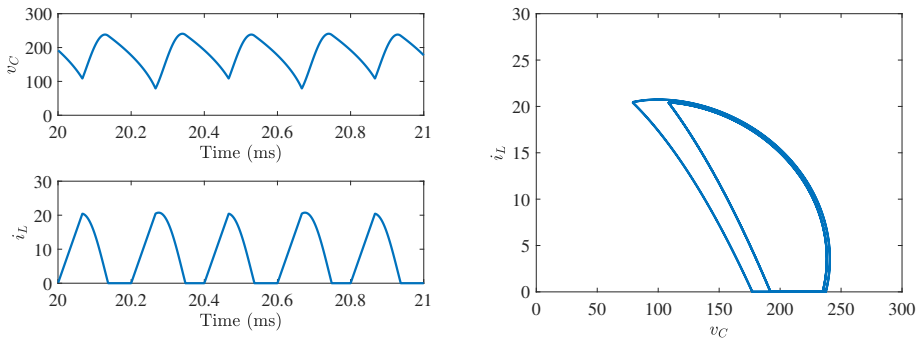
V_i	L	C	T	D
100 V	326 µH	4.5 µF	200 µs	$\frac{1}{3}$

As an important detail, it is worth mentioning that the route to chaos scenario corresponds to the classical period-doubling without border collision bifurcations, widely observed in switching converters [18,19], because the DCM operation is maintained for all the switching cycles even after bifurcations take place. In some cases, not shown here for the simplicity of presentation, it may happen that DCM is not accomplished for all the switching cycles in an arbitrary orbit. Obviously, this fact induces some deviation in the bifurcation diagram regarding the more standard patterns observed in Figure 10, due to discontinuity transitions associated with mixed CCM–DCM operation in a specific orbit.

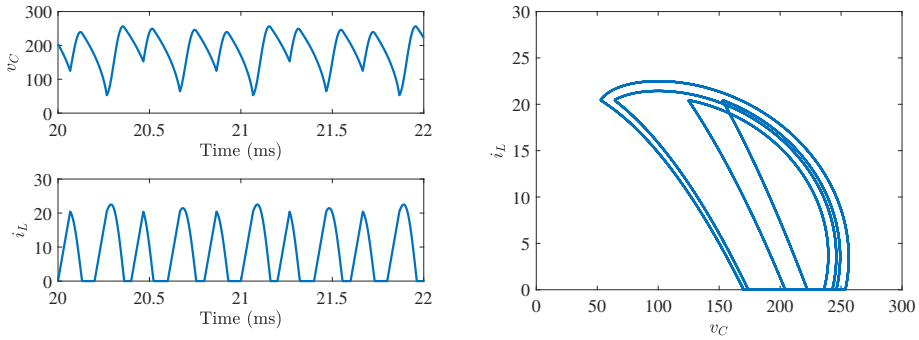
Representative time domain waveforms and state trajectories are represented in Figure 11. They were obtained using the same fixed parameters as in Figure 10 for different values of the dimensionless parameter K or, equivalently, power P. In this figure, orbits of different periodicity can be observed. The case of Figure 11a,b corresponds to a fundamental DCM one-periodic orbit. Figure 11c,d stand for the subharmonic oscillation with a periodicity of two produced; after that, the fundamental one-orbit loses its stability by a conventional smooth period-doubling bifurcation. The resulting DCM two-periodic orbit evolves such that it undergoes a period-doubling resulting in the DCM four-periodic orbit represented in Figure 11e,f. Finally, Figure 11g,h represent a DCM chaotic attractor.



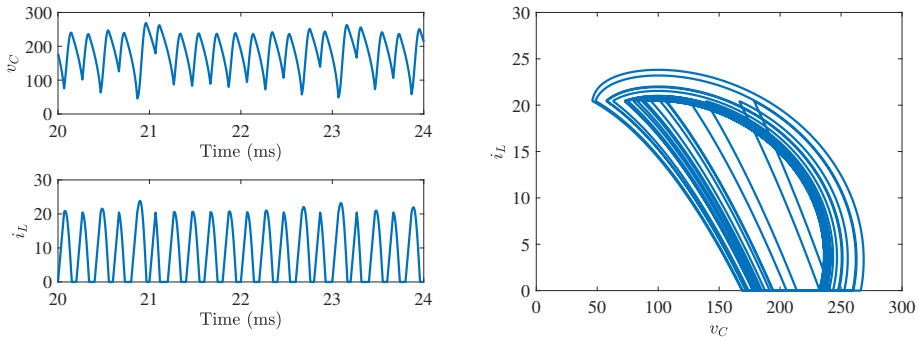
(**a**) $K = 0.2608$: T-periodic (**b**) $K = 0.2608$: 1-periodic



(**c**) $K = 0.2803$: $2T$-periodic (**d**) $K = 0.2803$: 2-periodic



(**e**) $K = 0.2875$: $4T$-periodic (**f**) $K = 0.2875$: 4-periodic



(**g**) $K = 0.2901$: chaotic (**h**) $K = 0.2901$: chaotic

Figure 11. Time domain waveforms of the capacitor voltage and the inductor current for different dynamical behaviors obtained from the switched model of an open-loop-DCM-operated boost converter implemented in the PSIM© software.

7.2. The Buck Converter

The region of DCM operation in the parametric space for the buck converter is much smaller than the one corresponding to the boost converter (Figure 7). The set of parameter values of Table 5 was also used here for the buck converter. A bifurcation diagram of the converter was computed using the PSIM© software. The result is shown in Figure 12. It was observed that the system only exhibited a first period-doubling bifurcation at a critical value $P_{\text{flip}} \approx 113$ W of the power P (equivalently, at a critical value $K_{\text{flip}} \approx 0.037$ of K) without the period-doubling cascade route to chaos. After that, the DCM two-periodic orbit emerged, and it existed for values of P lower than another critical value. By increasing P further, the *destructive unlimited* current phenomenon took place. The upper value of the bifurcation parameter was selected smaller than the value at which this phenomenon occurred $(K < 0.049)$ (equivalently, $P < 150$ W).

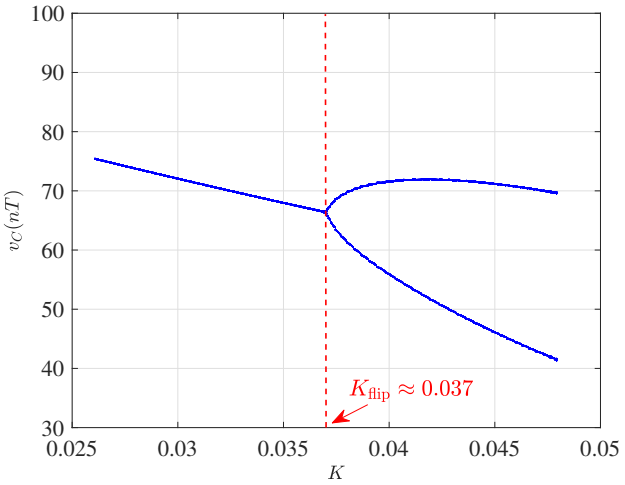


Figure 12. Bifurcation diagram of the DCM-operated buck converter with a CPL obtained using the PSIM© software.

8. Approximate Explicit 1D Discrete-Time Model and Fast-Scale Stability Limits

8.1. Boost Converter

8.1.1. Approximate Map

The discrete-time model of a switching converter is usually obtained by first obtaining the system response in the time domain and sampling it in synchronicity with the switching period. For switching converters with a CPL, an analytical expression for the system response is not available in continuous time for all sub-circuits. Therefore, here, we proceed in a different way. By performing a forward Euler discretization of the averaged model (2), one obtains the following discrete-time model for the open-loop-DCM-operated boost converter loaded by a CPL.

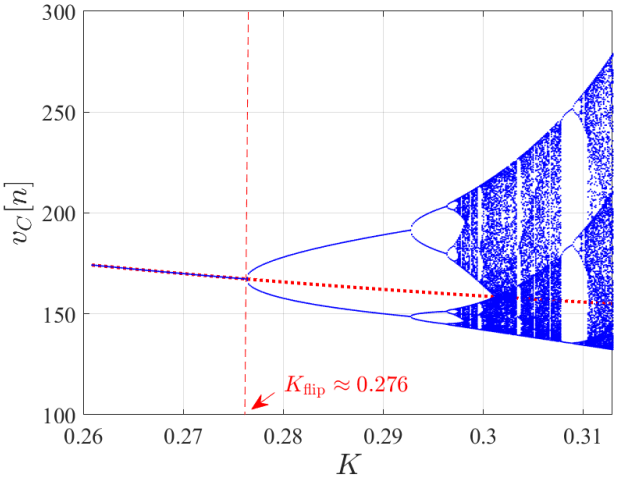
$$v_C[n+1] = f(v_C[n]) \tag{11}$$

where $f(v_C[n])$ is given by the following expression:

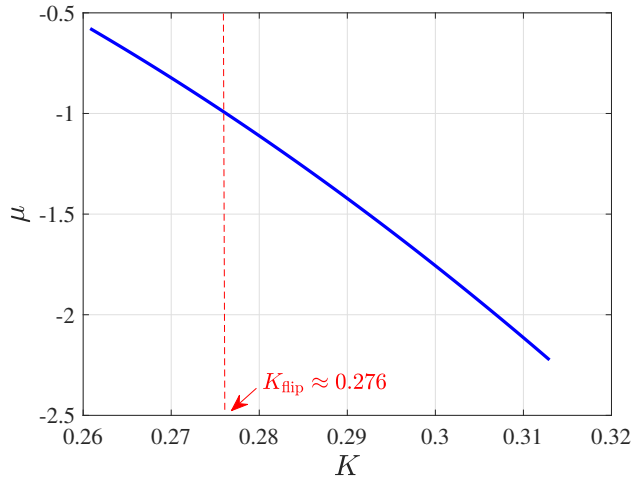
$$f(v_C[n]) = v_C[n] - \frac{PT}{C}\left(\frac{1}{v_C[n]} - \frac{1}{v_C[n] - V_i}\frac{D^2}{K}\right) \tag{12}$$

The model is only valid if the converter is effectively working in DCM, i.e., for $K < K_{\text{cri}}$. Otherwise, CCM will take place, and the model is no longer valid.

A bifurcation diagram obtained from the model in (12) by taking the parameter K as a bifurcation parameter is depicted in Figure 13a, where a cascade of period-doubling bifurcation was obtained and a good agreement can be observed with Figure 10.



(**a**)



(**b**)

Figure 13. (**a**) Bifurcation diagram of the open−loop-DCM-operated boost converter with a CPL obtained using the approximated discrete−time model. The evolution of the fixed point is also represented by the dotted line. (**b**) Characteristic multiplier μ.

8.1.2. Fixed Points and Their Stability

The fixed point of the map $f(\cdot)$ can be found by solving the equation $f(v_C[n]) - v_C[n] = 0$ for $v_C[n]$. In doing so, the expression of the fixed point is the same as the one obtained for the equilibrium point of the averaged mode, that is V_C in Table 4, for the boost converter. The evolution of fixed point is represented by the dotted line Figure 13a. Its stability status can be estimated by the characteristic multiplier, which is defined by

$$\mu = \frac{d}{dv_C[n]} f(v_C[n]) \Big|_{v_C[n]=V_C} \tag{13}$$

By applying (13) to (12), μ results:

$$\mu = 1 + \frac{PT}{C}\left(\frac{1}{V_C^2} - \frac{1}{(V_C - V_i)^2}\frac{D^2}{K}\right) \tag{14}$$

After some algebra, taking into account the value of V_C in Table 4, the characteristic multiplier for the boost can be expressed as

$$\mu = 1 - \frac{\left(K - D^2\right)^3 T^2}{2LCD^2K} \tag{15}$$

The behavior of the converter around a fixed point generally depends on whether the absolute value of the characteristic multiplier μ is greater or smaller than one. If it is smaller than one, the fixed point is an attractor, and if it is greater than one, it is a repellor. When μ crosses -1 as a parameter is varied, this possibly indicates a period-doubling bifurcation. In Figure 13b, the characteristic multiplier is plotted in terms of the bifurcation parameter. Observe that, at the first period-doubling bifurcation point, one has $\mu = -1$.

For this kind of map, the second iterate $f \circ f = f^{(2)}$ can also address a new period-doubling bifurcation if the parameter is further modified, and the same can occur for successive iterations of the map. This explains the period-doubling cascade observed in Figures 10 and 13a. Needless to say, the onset of instability can also be predicted by the pole of the discrete-time transfer function corresponding to the map $f(\cdot)$ [51]. Indeed, the characteristic multiplier coincides with the discrete-time pole.

8.1.3. Stability Boundaries in the Parametric Space

The period-doubling bifurcation boundary can be obtained by making $\mu = -1$; hence, from (14), the following condition in terms of the system parameters holds at this boundary:

$$\frac{V_i^2 D^2 T^2}{2LC(V_C - V_i)^2} - 2 - \frac{PT}{CV_C^2} = 0 \tag{16}$$

This is a very useful expression for delimiting the stability boundary in the parameter space at the fast-switching scale of the converter. Furthermore, from the third-degree K-polynomial in (15), the critical maximum value K_{flip} for guaranteeing the stability is

$$K_{\text{flip}} = \left(\frac{A}{3T} + \frac{4LC}{AT} + D\right) D \tag{17}$$

where A is a constant given by the following expression:

$$A = \sqrt[3]{6LC\left(9DT + \sqrt{(9DT)^2 - 48LC}\right)} \tag{18}$$

Accordingly, the corresponding maximum value P_{flip} of power P can be obtained from (17) and the expression of K in terms of P defined previously. For the parameter values considered in this study, the critical value of the dimensionless parameter K at the flip bifurcation point is $K_{\text{flip}} \approx 0.276$, and from this, the critical value of the power P is $P_{\text{flip}} \approx 847$ W, in remarkable agreement with the bifurcation diagrams represented in Figures 10 and 13a. In terms of the output capacitance, the closed-form expression obtained from (17) with $\mu = -1$ is simpler and can be written as follows:

$$C_{\text{flip}} = \frac{\left(2LP - TD^2V_i^2\right)^3}{8D^2L^2PV_i^4} \tag{19}$$

Figure 14 shows the regions of the dynamical behavior of the open-loop-DCM-operated boost converter with a CPL in the parametric plane (D, K). The DCM-operated converter is stable below the period-doubling boundary line. Increasing the capacitance C makes the stability region wider. In this case, the period-doubling bifurcation curve is monotonously increasing in terms of the duty cycle D.

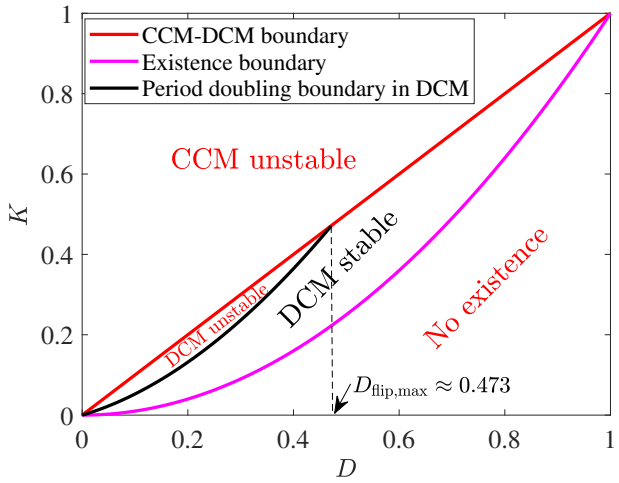


Figure 14. Regions of the dynamical behaviors of the open-loop-DCM-operated boost converter with a CPL in the plane (D, K) and the parameter values shown in Table 1.

Note that a maximum value $D_{\text{flip,max}}$ of the duty cycle D exists, above which period-doubling bifurcation cannot take place, since, in this case, $K_{\text{flip}} > K_{\text{cri}}$ and the converter will operate in CCM. The expression of $D_{\text{flip,max}}$ can be obtained in closed-form by solving the equation $K_{\text{flip}} - K_{\text{cri}} = 0$. Taking into account that $K_{\text{cri}} = D$ (see Table 3 for the boost converter), the following expression for $D_{\text{flip,max}}$ from (15), with $\mu = -1$, is obtained:

$$D_{\text{flip,max}} = 1 - \sqrt[3]{\frac{4LC}{T^2}} \tag{20}$$

Under the circuit parameters in Table 5, the value $D_{\text{flip,max}} = 0.473$ is obtained. This particular value of the duty cycle D is illustrated in Figure 14 as a vertical dashed line.

8.2. Buck Converter

8.2.1. Approximate Map

Following the same procedures as the ones followed for the boost converter, the map of the open-loop-DCM-operated buck converter is given by the following expression:

$$f(v_C[n]) = v_C[n] - \frac{PT}{CK}\left(\frac{K - D^2}{v_C[n]} + \frac{D^2}{V_i}\right) \tag{21}$$

8.2.2. Fixed Point and Its Stability

The expression of the fixed point is the same as in Table 3. Its stability can be determined by the characteristic multiplier, which can be expressed for the DCM-operated open-loop buck converter with a CPL as follows:

$$\mu = 1 - \frac{\left(TD^2\right)^2}{2LC(D^2 - K)} \tag{22}$$

The critical value of K at the border of instability ($\mu = -1$) is given by

$$K_{\text{flip}} = D^2\left(1 - \frac{T^2D^2}{4LC}\right) \tag{23}$$

With the parameter values of Table 5, the critical value K_{flip} of K at which period-doubling bifurcation takes place is $K_{\text{flip}} \approx 0.027$, corresponding to a critical value $P_{\text{flip}} \approx 83$ W of the power P. It is worth noting that this approximation of the critical bifurcation parameter value is smaller than the one obtained by the numerical simulations shown in

Figure 12 from the exact switched model. The discrepancy is attributed to the Euler approximation used to obtain the explicit discrete-time model from the averaged continuous-time model. Such an approximation is more accurate for the boost converter for which the capacitor voltage is piecewise linear than for the buck topology for which the capacitor voltage is piecewise quadratic. In terms of the output capacitance, the closed-form expression at the bifurcation boundary can be expressed as

$$C_{\text{flip}} = \frac{D^4 T^2}{4L(D^2 - K)} \tag{24}$$

8.2.3. Boundaries in the Parameter Space

The expression (23) is only valid if $0 < K_{\text{flip}} < K_{\text{cri}}$ for legitimately representing the period-doubling bifurcation boundary. This takes place for values of the duty cycle D within a certain interval $(D_{\text{flip,min}}, D_{\text{flip,max}})$. Solving the equations $K_{\text{flip}} - K_{\text{cri}} = 0$ and $K_{\text{flip}} = 0$ for the duty cycle D, the following expressions for $D_{\text{flip,min}}$ and $D_{\text{flip,max}}$ are obtained:

$$D_{\text{flip,min}} = \frac{4LC}{T^2}, \qquad D_{\text{flip,max}} = \sqrt{D_{\text{flip,min}}} \tag{25}$$

Figure 15 shows the regions of the dynamical behavior of the open-loop-DCM-operated buck converter with a CPL in the plane (D, K). If $D_{\text{flip,min}} < D < D_{\text{flip,max}}$, period-doubling bifurcation is expected to take place for $K_{\text{flip}} < K < K_{\text{cri}}$. The interval $(D_{\text{flip,min}}, D_{\text{flip,max}})$ is shown as a yellow strip in Figure 15.

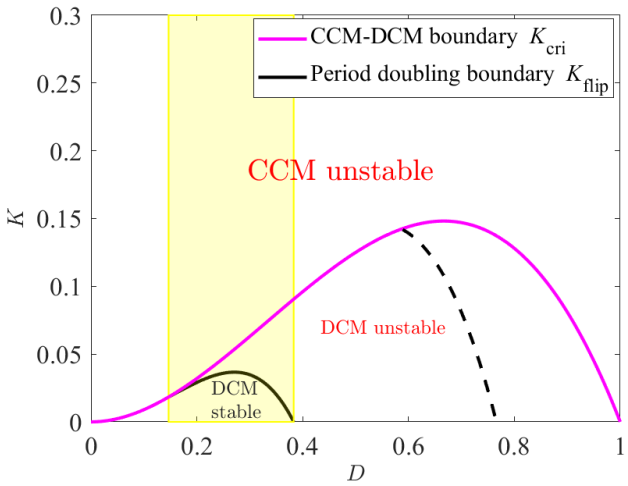


Figure 15. Regions of the dynamical behavior of the open-loop-DCM-operated buck converter with a CPL in the plane (D, K).

For $K_{\text{cri}} < K_{\text{flip}} < K$, it may happen that period-doubling bifurcation coexists with low-frequency oscillation ([52]), since, in this case, the converter will operate in CCM and an open-loop converter with a CPL operating in this mode is unstable at the slow scale. This will give rise to a mixed mode of operation in which, during some cycles, DCM will take place in the subharmonic regime, and during other cycles, CCM will occur, showing instability at the slow scale. If $D_{\text{flip,min}} < \sqrt{2LC}/T$, the expression of K_{flip} as a function of D presents a maximum $K_{\text{flip,max}}$ at $D = \sqrt{2LC}/T$. If $D_{\text{flip,min}} > \sqrt{2LC}/T$, the maximum value $K_{\text{flip,max}}$ is larger than K_{cri} and K_{flip} will be monotonously decreasing within the legitimate range of duty cycle D. This occurs if the capacitance C or inductance L are increased or the period T is decreased. The interval $(D_{\text{flip,min}}, D_{\text{flip,max}})$ moves to the right in this case. Figure 15 shows in the dashed line an example of such a monotonously decreasing K_{flip} curve for a relatively larger value of the capacitance ($C = 18\ \mu$F) than that shown in Table 5.

Note that, because $D < 1$, the expression of $D_{\text{flip,max}}$ is legitimate only if $2\sqrt{LC} < T$. In the opposite case, the interval of D within which period-doubling bifurcation may take place disappears. Therefore, a possible way to make the open-loop-DCM-operated converter be free from period-doubling bifurcation is to make $D_{\text{flip,max}}$ illegitimate, hence making $T < 2\sqrt{LC}$.

Finally, it is worth noting that a further accurate analysis based on an implicit discrete-time modeling [53], not shown here for simplicity, revealed that, while the approximate expressions for predicting period-doubling bifurcation boundary were quite accurate in the case of the boost converter, the ones corresponding to the buck converter presented a significant error. For instance, the exact value of $D_{\text{flip,max}}$ corresponding to the buck converter was larger than the one predicted by (25), and consequently, the exact theoretical width of the interval $(D_{\text{flip,min}}, D_{\text{flip,max}})$ was larger than the approximated one. Therefore, the analytical results presented in this section for the buck converter are only indicative.

9. Conclusions

In this work, we focused on studying the dynamics of open-loop DC–DC converters with CPLs operating in DCM. First, it was shown that a DCM-operated boost converter loaded by a tightly regulated voltage-mode-controlled buck converter may exhibit period-doubling bifurcation for certain values of the system parameters. The performed experimental measurements from a DCM-operated boost converter with a CPL showed that the system may exhibit practically the same behavior. Therefore, the work focused on the dynamics of the three elementary converters loaded by an ideal CPL. Numerical simulations from the switched model revealed that, for the boost converter, after the fundamental one-periodic orbit loses stability, a standard scenario of successive period-doubling leads to a chaotic attractor. Further variation of the bifurcation parameter may lead the system to exhibit *destructive* dynamics associated with low output voltage and, consequently, *unlimited* output load current. In the case of the buck converter, only the first period-doubling bifurcation was observed, and the *destructive* behavior due to *unlimited* output current interrupted the period-doubling cascade. Approximate discrete-time models were derived for the three elementary converters. The model of the boost converter was demonstrated to accurately predict the onset of the first period-doubling bifurcation for this converter. Concerning the approximate discrete-time model of the buck converter, the analytical results obtained from it were only indicative, and a more accurate numerical analysis is needed for predicting this bifurcation. It was also found that a fundamental periodic orbit does not exist in the case of the buck–boost converter. It is worth noting that, in the previous study, ideal circuit elements were considered. However, in a real circuit, parasitic elements such as the DC resistance of the inductor, the equivalent series resistance of the capacitor, the ON resistance and the OFF resistance of the transistor, and the forward-voltage diode could have an effect on the dynamic behavior of the converter. Namely, they can slightly modify the critical values of other more relevant circuit parameter values at the onset of period-doubling bifurcation and other complex behavior. However, the approximate discrete-time models with ideal circuit elements, despite their simplicity, were shown to display the most-important and -essential features of the corresponding switching converters.

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