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Study of Single Event Latch-Up Hardness for CMOS Devices with a Resistor in Front of DC-DC Converter

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Abstract: Bulk silicon Complementary Metal Oxide Semiconductor (CMOS) devices have distinct single event latch-up (SEL) problems in aerospace. Therefore, it is essential that CMOS devices are designed with appropriate circuit-level methods. Traditional resistor hardness satisfies the current aerospace trend of low cost, high performance, and miniaturization. Therefore conventional resistor hardness is often applied in circuit-level designs due to the reduction of latch-up current. In circuits containing a DC-DC buck converter, the resistor is connected to the back of the converter in the traditional method. However, the traditional method is unable to take devices out of the latch-up owing to the small resistance range. To solve this problem, the paper proposes an improved design for the resistor in front of the DC-DC buck converter. The proposed method enables the devices to exit the latch-up by increasing the resistance range according to the input characteristic of the DC-DC buck converter. The paper quantifies the range of the resistor through the parametric model containing the resistor and the DC-DC buck converter. Two CMOS devices are chosen for pulsed laser experiments, verifying that the proposed method increases the resistance ranges by 300% to 400% compared to the conventional method. It is also demonstrated that the proposed method exits the devices from latch-up within the resistor ranges. That is, the resistance ranges of 34 Ω~41 Ω and 51 Ω~56 Ω reduce the latch-up currents of the devices to below holding currents of 72.1 mA and 24.2 mA, respectively.

Keywords: CMOS devices; single event latch-up (SEL); single event effect (SEE); resistor; pulsed laser

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1. Introduction

Bulk silicon Complementary Metal Oxide Semiconductor (CMOS) devices are widely applied in satellite electronic systems owing to their low power consumption, high integration, and low production cost [1,2]. However, CMOS devices are often subject to collisions with high-energy protons and heavy ions from the cosmic space environment. Therefore, CMOS devices are susceptible to Single Event Effect (SEE) [3–6]. In particular, Single Event Latch-up (SEL), a special SEE, can alter devices' currents and even cause devices to burn up in severe cases [7–10]. From a circuit-level hardness perspective, SEL is generated by the conduction of parasitic PNP and NPN transistors inside the devices, creating low resistance paths between the devices' power supplies and grounds with resulting devices' current rise when the devices are exposed to the space radiation [11–14]. The hazard of SEL to CMOS devices is gradually increasing as commercial aerospace applications become more widespread [15,16]. Consequently, SEL hardness assurance has developed into an extremely significant challenge for CMOS devices in aerospace applications [17].

From a circuit-level hardness perspective, the devices will exit the SEL when the latch-up currents or latch-up voltages fall below the holding currents or voltages. To improve the SEL immunity of CMOS devices, three dominant research directions are proposed, respectively process-level hardness, layout-level hardness, and circuit-level

hardness [18–20]. Both process-level and layout-level designs enable the devices to be protected from SEL, while neither is applicable to commercial devices that have already been designed for production [21–23]. For the SEL problem in commercial CMOS devices, circuit-level designs are primarily adopted [24,25], which include power off-restart, constant current source, and cold backup. The power off-restart [26–28] adopts power disconnection to eliminate the latch-up of the devices. However, the approach will result in a functional interruption of the devices during power loss. The constant current source [29] keeps the devices' currents below the latch-up holding currents through a constant current source. The method is effective in increasing the latch-up hardness assurance of the devices, but it will limit the dynamic currents and affect the dynamic functionalities of the devices. The cold backup [30] uses a cold backup to set up multiple identical SEL-sensitive devices. If the current device occurs the latch-up, it will switch to the backup device to complete task requirements. The cold backup approach can effectively mitigate the latch-up hazard. However, it leads to the problem of manufacturing complex circuit structures and increased power consumption.

To address the above issues, a resistor in series behind a DC-DC buck converter (front of CMOS devices) is usually applied in conventional circuit-level hardness. In aerospace circuits, the satellite power supplies are 28 V and above, with the devices' voltages often at 5.5 V, 3.3 V and below. Therefore, to ensure that the devices are safely connected to the satellite power supplies, the DC-DC buck converter should be connected between the power supplies and the devices. In circuits containing a buck converter, a resistor is connected in series at the output of the DC-DC buck converter (i.e., the input of the devices). The resistor can effectively reduce latch-up current and latch-up harm by dividing voltages and limiting currents. Nevertheless, the dividing voltages of the resistor cannot exceed the normal operating voltage ranges of the devices, which will result in the resistor taking small ranges of values. The drawback will further cause the devices to fail to exit the latch-up. The more detailed deficiencies of the conventional resistor are described in depth in Section 2.1.

To overcome the limitation of the conventional resistor, the paper proposes an improved design with a resistor placed in front of the DC-DC buck converter. The design allows the devices to exit the latch-up by increasing the resistance range combined with the wider input voltage range of the DC-DC buck converter. The larger voltage input range of the converter indicates a wider resistance range. Since the latch-up current decreases as the resistance increases, therefore, the latch-up hazard of the devices becomes smaller with the higher resistance. When the latch-up current is reduced below the holding current, the devices will exit the latch-up. In order to quantify the range of the resistor that brings the devices out of the latch-up, the paper investigates the resistance calculation method by building a parametric model containing the resistor and the converter. After that, pulsed laser experiments will be implemented using two CMOS devices. As well, it is verified that the proposed method enables the devices to exit the latch-up within the resistance range.

The primary contributions of the paper are as follows:

(1) The proposed method addresses the prominent limitation of the traditional method. Conventional resistor hardness design only acts as a current limit for the latch-up, and does not allow the devices to exit the latch-up. The method proposed in the paper enables the device to exit the latch-up by combining the resistor in concert with the DC-DC buck converter.
(2) The method of taking the resistance is studied to improve the lack of mathematical analysis of the resistor in traditional latch-up hardness. The paper systematically analyzes the operating principle of the resistor in front of the DC-DC buck converter, establishes the corresponding parametric model, and proposes the method of taking the resistance. It has extremely valuable guidance for the proposed method in practical hardness assurance applications.
(3) The proposed method has the advantages of continuous operation with power, maintaining the dynamic functions of the devices, and occupying a smaller circuit design

area compared to power-off restart, constant current source, and cold backup in the circuit-level hardness methods. Furthermore, the proposed method is compatible with the current trend of low cost, high performance, and miniaturization in aerospace.

The paper is organized as follows: In Section 2, comparing the conventional method with the proposed method, it is demonstrated that the proposed method enables the device to exit the latch-up within the range of the resistor. As well, the range of resistance is quantified. In Section 3, to verify the SEL hardness performance of the proposed method, laser experiments are carried out. In Section 4, the paper discusses the resistive power consumption in the proposed method. Finally, a conclusion is given in Section 5.

2. Method

2.1. Inadequacy of Conventional Method

The section will provide comprehensive descriptions including the conventional resistor's connection, the principle of resistor operation, and the constraints of the traditional method. It focuses on the problem of the traditional method by elaborating on the latch-up hardness principle. Figure 1 is a schematic diagram of the circuit for a conventional resistor hardness design.

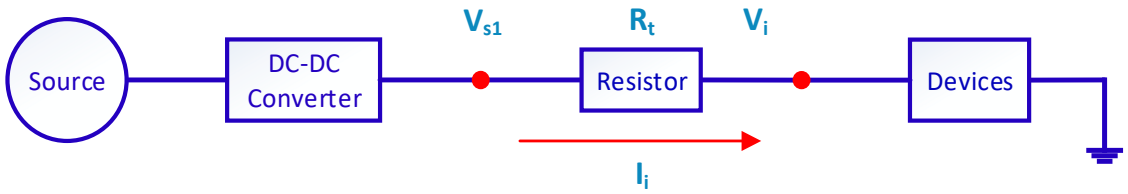

Figure 1. Schematic diagram of the circuit for a conventional resistor hardness design.

The R_t represents the resistor in the conventional method, which is connected at the output of the DC-DC buck converter. The V_{s1} denotes the output voltage of the converter. The V_i and I_i represent the voltage and current of the device, respectively. Thus, the is expressed as:

$$(V_{s1} - V_i) \cdot \frac{1}{R_t} = I_i \tag{1}$$

According to Equation (1), the resistor changes the device current by limiting the circuit current. The device current decreases as the resistance increases. It indicates that the higher the resistance, the lower the device's latch-up current. However, the increase in resistance is limited, since it will result in a reduced voltage of the device. When the device's voltage is below the normal voltage tolerance range, it will prevent the device from operating properly. Therefore, the resistor is subject to certain constraints in the actual latch-up hardness.

Based on the above resistive hardness principle in combination with the latch-up property, two constraints are derived [31–33]:

- Condition 1: The resistor does not affect the normal operation of the device. The operating voltage of the device should not exceed the normal voltage tolerance range. Otherwise the device cannot operate successfully. The voltage tolerance range is typical −10% to 10% of the rated voltage.
- Condition 2: Reduce the latch-up current to below the SEL holding current when the device is experiencing the latch-up [34–36]. According to the latch-up criterion, when the latch-up current drops below the latch-up maintenance point, the device will exit the latch-up state because the latch-up current cannot be maintained.

The traditional method of taking the resistance will be studied with respect to the constraints. As well, the range of resistance is researched to illustrate the latch-up hardness problem that exists with the conventional method. The 3.3 V CMOS process device is selected as the object of the study, i.e., V_{s1} = 3.3 V, then the voltage tolerance is −0.3 V~0.3 V.

The range of R_{t1} satisfying condition 1 in the conventional method is represented as:

$$0 \leq R_{t1} \leq \frac{V_{s1} - V_i}{I_i} \tag{2}$$

where $V_{s1} - V_i$ denotes the voltage tolerance. From Equation (2), it is known that R_{t1} has a harsh range of $0 \sim \frac{0.3}{I_i}$ Ω owing to its small voltage tolerance range.

The range of resistance R_{t2} fulfilling condition 2 in the conventional method is expressed as:

$$R_{t2} \geq \frac{V_{s1} - V_h}{I_l} \tag{3}$$

where V_h and I_l represent the latch-up holding voltage and latch-up current, respectively. As the resistor is required to meet both the normal operation and to make the device exit the latch-up, it is obtained that $R_{t2} \leq R \leq R_{t1}$. According to the test data of several devices, V_h is about 1.32 V~2.45 V, which means that $V_{s1} - V_h > V_{s1} - V_i$. Usually I_l is 2~3 times and more than I_i, as well as combined with the actual data, it is evident that $R_{t1} < R_{t2}$. It indicates that the conventional method does not allow the device to exit the latch-up.

To address the limitation of the conventional method, the paper proposes a latch-up hardness design with a resistor placed in front of the DC-DC buck converter. The details of the proposed method will be described in the next section.

2.2. The Proposed Method

The section describes in detail the connection method, operating principle, design advantages, parameter model and resistance-taking the method of the proposed method. Emphasis will be placed on the design advantages of the proposed method to allow the device to exit the latch-up and the discussion of the resistor-taking method by building a parametric model.

2.2.1. Take the Device out of the Latch-Up

Figure 2 depicts the schematic circuit diagram of the proposed hardness method. The resistor employed in the proposed method is named R_p, which is connected to the input of the DC-DC converter. V_{s2} indicates the supply voltage to which the converter is attached. V_d and I_d separately represent the input voltage and input current of the converter. Thus, R_p is given as:

$$(V_{s2} - V_d) \cdot \frac{1}{R_p} = I_d \tag{4}$$

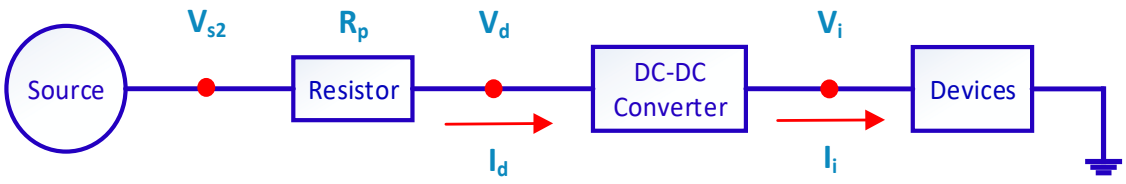

Figure 2. Schematic diagram of the connection of the resistor in the proposed method.

From Equation (4), it is obvious that the proposed method operates by varying the input current of the DC-DC converter to regulate the current of the device. The hardness mechanism of R_p is that R_p reduces the device current by limiting the input current of the converter. As well, the device current decreases as the input current is reduced. However, compared to conventional design, the advantage of the proposed approach is that the objective of exiting the device from latch-up will be achieved by increasing the voltage tolerance based on the wide input range of the DC-DC converter. The input voltage range of the DC-DC buck converter is more extensive than the device's voltage tolerance range, for example, the input range of LTM4644 converter is 2.4 V~14 V, which is much higher

than the 0.3 V voltage tolerance of the 3.3 V device. The effect of a larger voltage tolerance is to make a larger range of resistance that satisfies condition 1. Following the operating principle of R_p, it is known that a larger resistor makes the device latch-up current lower by further reducing the input current of the converter. When the device latch current falls below the latch-up holding current, the device will exit the latch-up.

2.2.2. Method of Taking the Resistance

To further investigate the proposed hardness method of taking the resistance that simultaneously meets conditions 1 and 2, a parametric model of the resistor placed at the input of the DC-DC buck converter is developed, as shown in Figure 3. The parametric model consists of supply voltage V_{s2}, resistor R_p, switch S, inductor L, capacitor C, diode D_i and feedback network. The feedback network is composed of resistors R_1 and R_2, an error amplifier and a duty ratio modulator. The function of the feedback network is to generate the duty cycle signal and control the state of the switch.

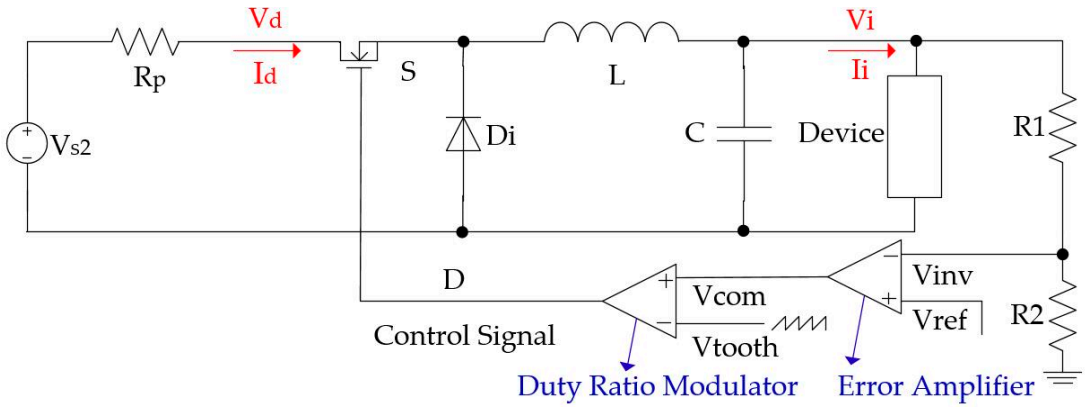

Figure 3. Parametric model of the resistor placed at the input of the DC-DC buck converter.

According to the I-V characteristic of R_p, R_p is represented as:

$$\frac{V_{s2} - V_d}{R_p} = I_d \tag{5}$$

where V_d and I_d denote the input voltage and input current of the DC-DC buck converter, respectively.

Following the DC-DC buck converter power conservation principle and duty cycle equation, it is known that:

$$V_d \cdot I_d = \frac{1}{\mu} \cdot V_i \cdot I_i \tag{6}$$

$$V_i = DV_d \tag{7}$$

where μ and D respectively denote the conversion efficiency and duty cycle of the converter. μ and D are related to the operating voltage and current of the converter which are available according to the datasheet or actual test values. Substituting Equations (6) and (7) into Equation (5) gives that:

$$-D^2 R_p I_i + D\mu V_{s2} - \mu V_i = 0 \tag{8}$$

From condition 1, the range of R_{p1} that satisfies the normal operation of the device is derived as:

$$R_{p1} \leq \frac{R_{eqn}(D\mu V_{s2} - \mu V_{ii})}{D^2 V_{ii}} \tag{9}$$

where R_{eqn} represents the equivalent resistance of the device in the normal state. V_{ii} indicates the minimum value of the device voltage V_i in the voltage tolerance range. For 3.3 V devices, V_{ii} is typically 3.0 V.

The boundary formula for the R_{p2} meeting condition 2 is given by:

$$R_{p2} \geq \frac{R_{eql}(D\mu V_{s2} - \mu V_h)}{D^2 V_i} \tag{10}$$

where R_{eql} signifies the equivalent resistance of the device in the latch-up state. In summary, the range of R_p that simultaneously satisfies the normal operation of the device and enables the device to exit the latch-up is:

$$R_{p1} \leq R_p \leq R_{p2} \tag{11}$$

3. Pulsed Laser Experiments

3.1. Experimental Setup and Devices Selection

To verify the latch-up hardness performance of the proposed method and the method of taking the resistance, pulsed laser experiments are carried out. The mechanism of SEL induced by pulsed laser experiments in CMOS devices is approximately the same as that of heavy ion experiments, both of which induce latch-up in CMOS devices by ionization of electron-hole pairs. However, the primary differences between pulsed laser experiments and heavy ion experiments are the small spot diameter and high resolution of the pulsed laser, which allows accurate simulation of SEE caused by individual high-energy particles in space [37,38]. In addition, the irradiation intensity and irradiation time of CMOS devices by the pulsed laser are precisely controllable [39]. The pulsed laser test setup adopts the self-researched equipment of the National Space Science Centre of the Chinese Academy of Sciences. Figure 4 shows a schematic diagram of the pulsed laser unit. The laser setup consists of the component laser generator, the optical path system, the 3D mobile table, the synchronization control system and the host computer [40–42]. Table 1 shows the main parameters of the laser equipment.

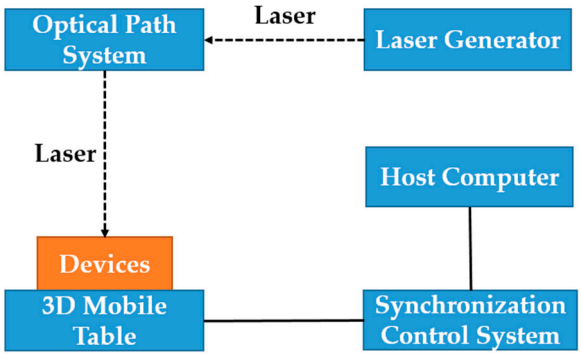

Figure 4. A schematic diagram of the pulsed laser equipment.

Table 1. The main parameters of the laser equipment.

Machine Type	Wavelength	Wideband	Frequency	Energy
Nd:YAG	1064 nm	25 ps	1~1k Hz	1.5 nJ

Based on the operating principle and parametric model analysis of the proposed method, it is shown that the method in the paper is generally applicable to latch-up sensitive devices. To verify the applicability of the proposed method, two CMOS chips, A3PE1500 and AD7472, are selected as the test objects for laser experiments. Table 2 summarizes the key parameters of the two subjects. The normal operating and latch-up holding currents for device 1 are 0.072 A and 0.088 A respectively; for device 2 the normal operating and latch-up holding currents are 0.022 A and 0.031 A accordingly.

Table 2. The key parameters of the two test subjects.

Device Number	Model	Operating Voltage	Operating Current
Device 1	A3PE1500	3.3 V	72 mA
Device 2	AD7472	3.3 V	22 mA
Device Number	**SEL Current**	**Holding Voltage**	**Holding Current**
Device 1	356.6 mA	2.1 V	88 mA
Device 2	97.3 mA	1.7 V	31 mA

The devices will be triggered to produce the SEL when a pulsed laser is an incident on the active regions inside the devices. To ensure that the laser energy is effectively injected into the active areas, the devices must be back-opened before laser experiments. Figure 5 illustrates the practical picture of the devices in the pulsed laser experiments. The diagram contains mainly the pulsed laser, the devices and the DC-DC buck converter. The input of the DC-DC buck converter is connected to the supply voltage, and the output is attached to the power supply of the devices.

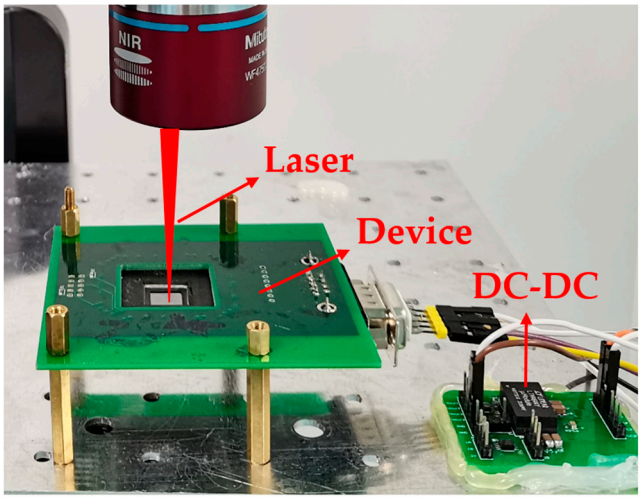

Figure 5. The practical picture of the devices in the pulsed laser experiments.

3.2. Experimental Method

The purposes of the experiments are to verify that the proposed method enables the devices to exit the latch-up as well as the resistor-taking method. To better illustrate the experimental results, comparative tests are designed in the paper for the conventional and experimental groups respectively. The resistor of the conventional group is connected to the output of the DC-DC buck converter, while the resistor of the experimental group is attached to the input of the DC-DC buck converter. Besides, the experimental manipulation is the same for both. The experimental operation is divided into three major steps, which are adjusting the position of the devices to be tested, testing the functions of the devices and changing the resistance.

- First, the devices are adjusted to a horizontal state by adjusting the 3D moving table to ensure that the laser energy is injected into the devices at the same depth.
- Then, with the circuit connected correctly, the power is turned on to test the functions of the devices. The voltages and currents of the devices in the initial state and the latch-up state in the two sets of experiments are detected and recorded respectively.
- Finally, by connecting different resistors, the electrical parameters of the devices in the initial state and in the latch-up state are recorded in both sets of experiments.

When the initial voltages of the devices exceed the voltage tolerance range, it means that the resistance is already the maximum value, and the experiment will end at this time. The following experimental results will be obtained by collating the relevant test data.

3.3. Experimental Results

3.3.1. Exiting the Devices from the Latch-Up by the Proposed Method

To demonstrate that the proposed method enables the devices to exit the latch by increasing the resistance range, the section first investigates the resistance range of the proposed method compared to the conventional design. Next, a comparative analysis is performed on the latch-up currents variation over the range of resistance values.

Figure 6 depicts the ranges of the resistance under the conventional method and the proposed design, respectively. Figure 6a shows a resistance range of 0 to 8.2 Ω in the conventional method within the normal operating voltage range of device 1. The proposed method, however, has a resistance range of 0 to 41 Ω. In comparison to the conventional method, the proposed method increases the resistance range by up to 400%. Figure 6b depicts the resistance ranges of 0~14 Ω and 0~56 Ω for the conventional method and the proposed method, respectively, in the operating voltage range of device 2. A 300% increase in resistance range can be achieved with the proposed design. It is concluded that the proposed design improves the resistance range by 300% to 400%.

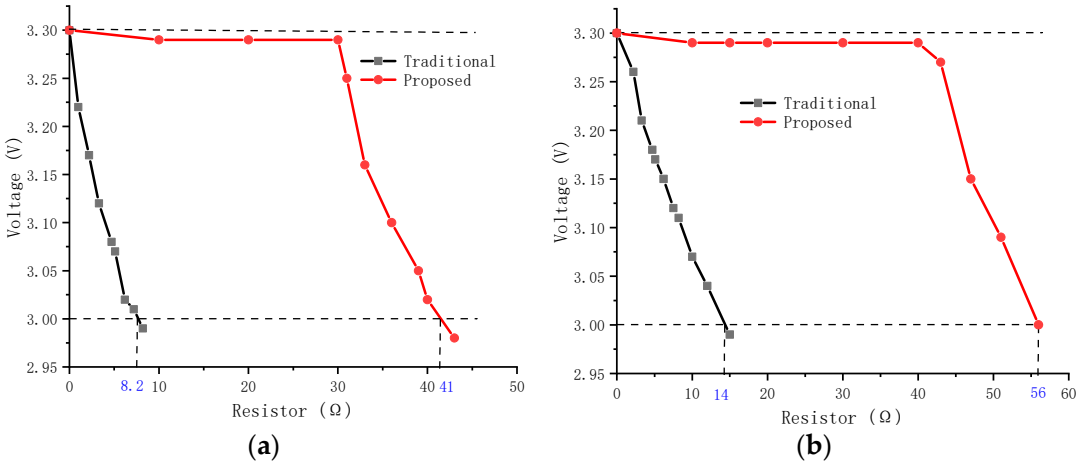

Figure 6. The ranges of the resistance under the conventional method and the proposed design, respectively. (**a**) Description of the ranges of the resistance in device 1; (**b**) Description of the ranges of the resistance in device 2.

The increase in the resistance range will further improve the latch-up hardness of devices. Under certain conditions, the resistor will make the devices drop out of the latch-up. Figure 7 shows the relationships between the resistor and the latch-up current of the two devices under two different methods. Figure 7a describes the conventional method of reducing the device 1 latch-up current to 134.7 mA at resistor maximum. Even so, the device 1 remains in an abnormal latch-up state. Nevertheless, the proposed method reduces the device current to below the latch-up holding current of 72.1 mA at a resistance of 34 Ω. Consequently, the proposed hardness design with resistances of 34 Ω and above will keep device 1 from latch-up. Figure 7b illustrates that the conventional method and the proposed design respectively reduce the device 2 latch-up current to 50.3 mA and 24.2 mA (below the holding current). However the proposed method improves the latch-up hardness of the device by making it latch-up-free under certain conditions because of the large resistance range.

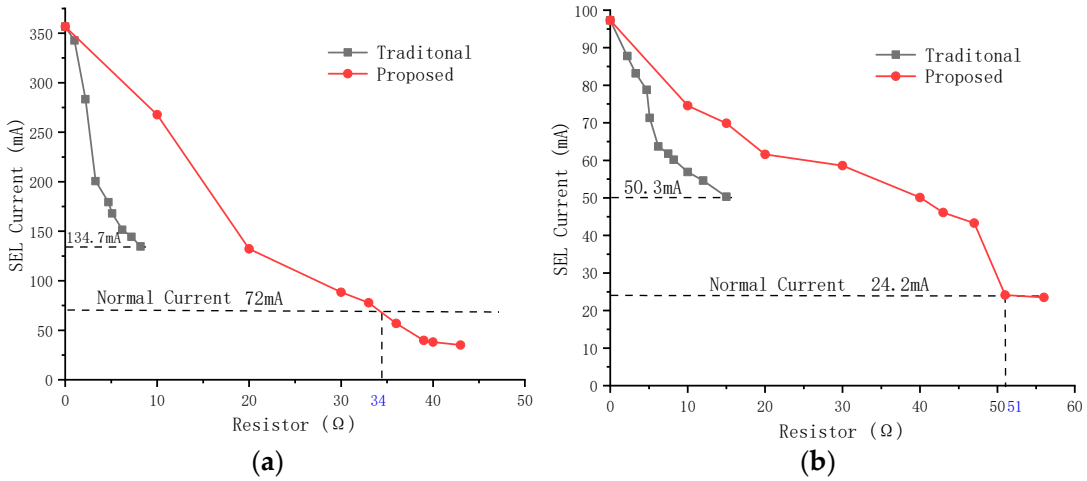

Figure 7. Graph of resistance versus latch-up current for two devices under two different methods. (**a**) Relationship between resistance and latch-up current of device 1; (**b**) Relationship between resistance and latch-up current of device 2.

3.3.2. Verification of the Resistance-Taking Method

To verify the resistance range of the proposed method, the main parameters of devices in Table 2 are substituted into Equations (4) and (11) respectively. The theoretical range of resistance is calculated to be 37 Ω~48 Ω and 53 Ω~62 Ω for device 1 and device 2 separately. Table 3 indicates the theoretical and actual ranges of resistance. According to the experimental results in Figure 6, it can be seen that R_{p1} of the two devices are 0 Ω~41 Ω and 0 Ω~56 Ω, respectively. According to the data in Figure 7, it is evident that R_{p2} of the two devices are 34 Ω and above, and 51 Ω and above, accordingly.

Table 3. The theoretical and actual ranges of resistance.

Devices	Type	R_{p1} (Ω)	R_{p2} (Ω)	$R_{p1} \cap R_{p2}$ (Ω)
Device 1	Theory Value	0~48	≥37	37~48
	Test Value	0~41	≥34	34~41
Device 2	Theory Value	0~62	≥53	53~62
	Test Value	0~56	≥51	51~56

It is noticed that the actual results of the resistance are smaller than the theoretical results. This phenomenon may be due to the capacitor and inductor of the converter having parasitic resistance in the actual circuit, resulting in an actual low resistance.

4. Discussion of Resistor Power Consumption

The issue with the proposed method is that it will cause an increase in the power consumption of the circuits, due to the increased resistance range compared to the traditional design. Figure 8 summarizes the power consumption data of the proposed resistor versus the conventional resistor in the devices. The power consumption of the resistor in the proposed method is about 0.11 W to 0.19 W, which is more than 50% higher than that of the conventional design.

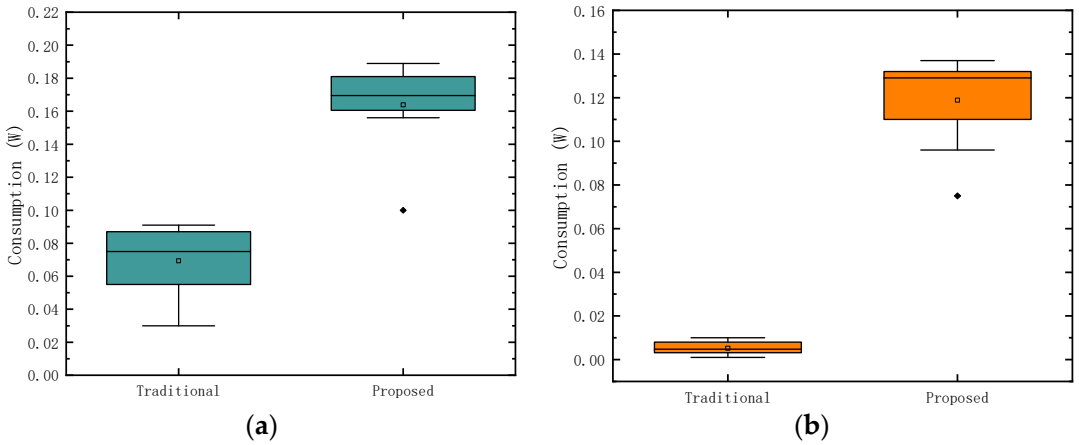

Figure 8. Description of the power consumption generated by the resistor in the two devices with two different methods. (**a**) Displays the power consumption generated by the resistor in device 1; (**b**) Introduction of the power consumption generated by the resistor in device 2.

To reduce the power consumption problem of the proposed method, the approach of reducing the converter input voltage is proposed. The minimum input voltage of the DC-DC buck converter is above the device voltage, i.e., V_{s2} > 3.3 V. Therefore, 6 V, 5 V, and 4.5 V supply voltages are chosen to explore the effect of voltage reduction on resistor power consumption. Figure 9 shows the resistive power consumption for the two devices with supply voltages of 6 V, 5 V, and 4.5 V, correspondingly. It is observed that the resistive power consumption reduces with decreasing supply voltage. Compared to the resistor power consumption with a supply voltage of 6 V, the resistor power consumption with a supply voltage of 4.5 V is reduced by more than 87% to about 0.06 W~0.08 W. Power consumption is acceptable in engineering.

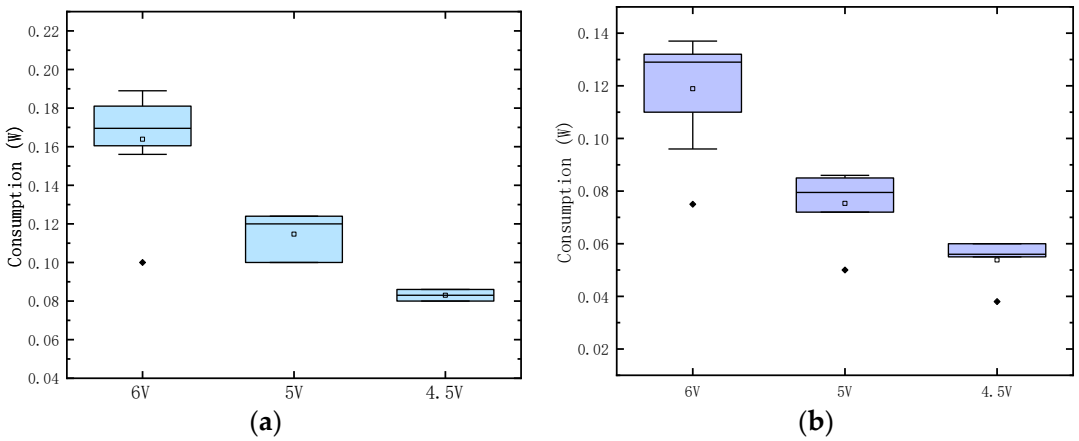

Figure 9. Power consumption of the resistor at 6 V, 5 V, and 4.5 V for the two devices separately. (**a**) The power consumption generated by the resistor in device 1; (**b**) The power consumption generated by the resistor in device 2.

5. Conclusions

The paper proposes a circuit-level SEL hardness design for a resistor in front of a DC-DC buck converter. The method improves the latch-up hardness performance by improving the resistance range compared to the conventional hardness design. The proposed method enables devices to exit the latch-up when the resistance takes the value of $R_{p2} \sim R_{p1}$. The proposed method is validated with the A3PE1500 and AD7472 CMOS devices to effectively increase the resistance range by 300% to 400%. It is also demonstrated that the resistor

enables devices to operate normally and exit the latch-up within the boundary range when devices are suffering from SEL.

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