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Observation of Large Threshold Voltage Shift Induced by Pre-applied Voltage to SiO_2 Gate Dielectric in Organic Field-Effect Transistors

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Abstract: Field-effect transistors based on organic semiconducting materials (OFETs) have unique advantages of intrinsically mechanical flexibility, simple preparation process, low manufacturing cost, and large-area preparation. Through the innovation of new material design and device structures, the performance of device parameters such as mobility, on–off current ratio, and the threshold voltage (V_{TH}) of OFETs continues to improve. However, the V_{TH} shift of OFETs has always been an important problem restricting their practical applications. In this work, we observe that the V_{TH} of polymer OFETs with the widely investigated device structure of a SiO_2 bottom-gate dielectric is noticeably shifted by pre-applying a large gate voltage. Such a shift in V_{TH} remains to a large extent, even after modifying the surface of the SiO_2 dielectric using a hexamethyldisilazane (HMDS) self-assembled monolayer. This behavior of V_{TH} can be ascribed to the charge trappings at the bulk of the SiO_2. In addition, the generality of this observation is further proven by using two other conjugated polymers including p-type PDPP3T and n-type PTzNDI-2FT, and a similar trend is obtained.

Keywords: organic field-effect transistor; threshold voltage shift; charge trapping; pre-applied voltage

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1. Introduction

With the rapid development of the Internet of Things (IOT), smart electronic devices such as automatic sweeping machines, intelligent monitoring, and other IOT products greatly facilitate everyone's daily life. To make these devices smarter and more convenient, there has been a flurry of research into wearable and flexible electronics. Organic semiconductor material-based field-effect transistors (OFETs) have attracted considerable attention due to their intrinsically bendable and stretchable flexibility, good biocompatibility, and the advantages of large-area fabrication through solution processing methods at low temperatures. Therefore, they hold great application potentials in the fields of health detection, physiological information processing, and flexible electronics [1–9].

In the last two decades, great efforts have been devoted to improving the device performances of OFETs, including the on–off current ratio [10–12], field-effect mobility [12–15], subthreshold swing [16–18], and threshold voltage (V_{TH}) [19–21]. Among the above parameters, V_{TH} is the key to determining whether the transistor works at the expected operation voltage. However, the capture and release of charge carriers by defects or traps in the devices typically lead to the V_{TH} shift. Trapped charges provide an additional electric field to the conduction channel, which directly alters the carrier concentration within the channel and, thus, critically affects the value of V_{TH} [22–24]. Furthermore, V_{TH} shifts in bias stress testing are considered to be one of the most important indicators to measure the stability of OFETs. A constant voltage is continuously applied to the gate electrode

of OFETs, and the time-dependent V_{TH} is compared in order to evaluate the stability of the transistor. The smaller the difference in V_{TH}, the better the stability of the device. This bias stress effect for OFETs is generally attributed to defects or charge traps at the interface between the dielectric and semiconductor [25–28]. This V_{TH} shift has detrimental impacts on the practical applications of OFETs.

On the other hand, the floating-gate strategy is an efficient way to precisely control V_{TH} and the consequent operation state for both traditional Si-based transistors and OFETs [29]. Usually, a floating-gate transistor differs from a field-effect transistor structure by the insertion of an additional floating-gate electrode into the dielectric. The floating gate is charged by a large external electric field. After the external electric field is removed, the charges stored in the floating gate attract or repel the carriers in the channel of the transistor, resulting in V_{TH} shifts. For the flash memory, the range of threshold voltage change is expected to be as large as possible, which means a wider memory window and facilitates the reading or writing process of stored information. High density, low power, and high speed are three important indicators in CMOS flash memory [30]. Organic non-volatile memory based on floating-gate structures has also been realized [31–33].

In this article, a bottom-gate bottom-contact OFET based on a Si/SiO_2 substrate is fabricated. When a bias voltage is pre-applied to the Si gate, an obvious shift in V_{TH} is observed, which can be attributed to the defects or traps at the bulk of the SiO_2 and is different from the stress bias effect and floating-gate transistors. This hypothesis is supported by the surface modification of SiO_2 gate dielectrics with a hexamethyldisilazane (HMDS) self-assembled monolayer (SAM), which is generally considered to be an efficient way to reduce defects or charge traps on the surface of SiO_2, and the V_{TH} shift still remains for the HMDS-modified transistors. In addition, the impact of semiconducting materials on such a phenomenon is excluded by fabricating OFETs using two other polymers including p-type PDPP3T and n-type PTzNDI-2FT, and similar trends are obtained.

2. Results and Discussion

Benefiting from their atomically flat surface, simplified processing procedure, and good insulation for low leakage current, heavily p-doped Si wafers with 300 nm thick thermally grown SiO_2 are widely utilized to fabricate back-gate OFETs [34–40]. Here, we use the same substrate with SiO_2 as the gate dielectric and doped Si as the back gate for the OFET, as shown in Figure 1. A p-type conjugated polymer, PffBT4T-2DT, is used as the organic semiconducting material. In order to minimize the contact resistance between the semiconductor and metal electrodes, a 2,3,4,5,6-pentafluorothiophenol (PFBT) SAM was functionalized onto Au electrodes before dynamic spin-coating with PffBT4T-2DT film [41,42].

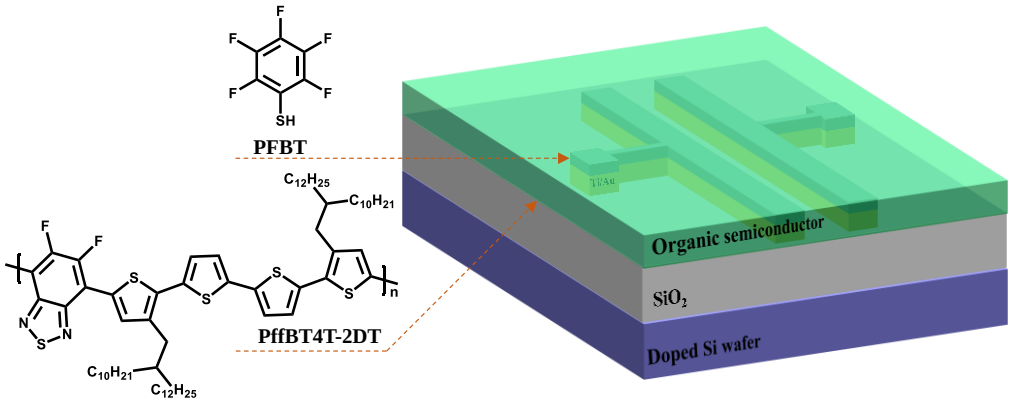

Figure 1. Chemical structures of PFBT (top) and PffBT4T-2DT (bottom) and schematic structure of the fabricated OFET.

The fabricated transistor shows a typical linear/saturation behavior, and a high on–off current ratio of 10^7 is achieved (Figure S1). In this saturation regime, drain current (I_{DS}) can be described using Equation (1):

$$I_{DS} = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS}-V_{TH})^2 \quad (1)$$

where μ represents the mobility of carriers and V_{GS} is the gate voltage. C_{OX} is the unit-area capacitance of the dielectric. W and L represent the width and length of the transistor channel. The intercept of the square root of I_{DS} is utilized to extract V_{TH}, and the value of −15.3 V is obtained for the PffBT4T-2DT transistor. We find that a pre-applied voltage to the Si gate has a remarkable influence on V_{TH}. For example, by pre-applying 100 V to the gate electrode for 10 s, V_{TH} shifts towards the positive direction compared to the initial state, and V_{TH} = 8.4 V is observed. On the other hand, we also apply a negative voltage of −100 V to the gate electrode. In this case, the transfer curve shifts to the negative direction, and V_{TH} moves to −37.1 V. The transfer curves at various pre-applied voltages are shown in Figure 2a, and the saturated mobility is almost independent of the pre-applied voltage (Figure S2). Figure 2b summarizes the relationship between the pre-applied voltage and the threshold voltage, and a near-linear relation is obtained. It is evident that, as the pre-applied gate voltage increases, the V_{TH} shift becomes clearer. The threshold voltage shift is 45 V by pre-applying a gate voltage of +100 V or −100 V, while this value is significantly enhanced to over 70 V by using the pre-applied voltage of −160 V. Interestingly, such a threshold voltage shift remains almost unchanged when pre-applying a constant gate voltage multiple times (Figure S3). Additionally, it is found that PFBT functionalization on Au electrodes has a negligible impact on such a phenomenon (Figure S4).

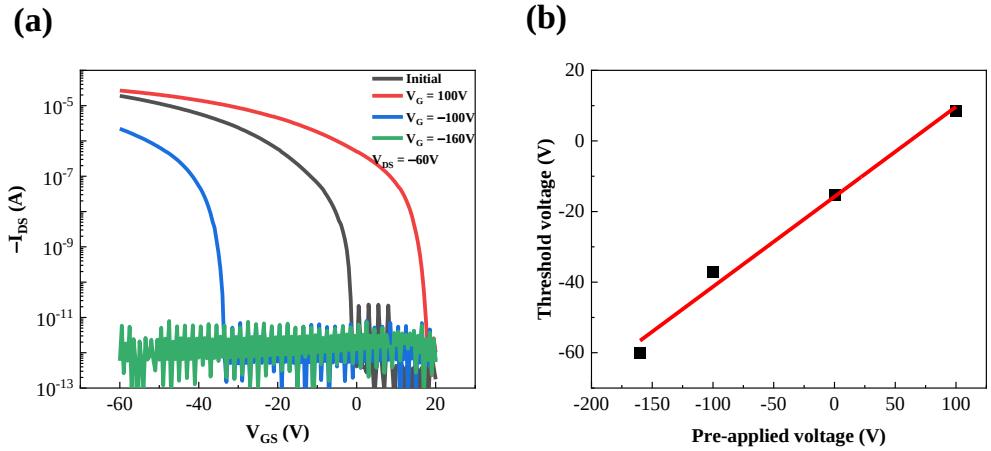

Figure 2. (**a**) Transfer curves at different pre-applied voltages to the gate electrode; (**b**) Threshold voltage shift as a function of pre-applied voltage to the gate electrode.

It has been widely reported that defects or traps at the interface between the organic semiconductor and the gate dielectric contribute to the shift of the transfer curve [43–45], and surface modification using HMDS SAM is an efficient method that helps reduce the defects of the SiO_2 surface and improves the performance of OFETs. Before spin-coating organic semiconductor thin films, the surface of the SiO_2 was exposed to an HMDS vapor for 3 min to passivate the surface [23,46]. It is evident that the HMDS modification of the SiO_2 surface efficiently reduces the density of trapping sites at the semiconductor/dielectric interface (Figure S5).

Under the same pre-applied gate voltage conditions mentioned above, the transfer curve of the device that is treated by HMDS is shown in Figure 3a. It is clear that there is still a large V_{TH} shift phenomenon, and a clear dependence on the pre-applied voltage remains (Figure 3b). Compared with the experimental results without HMDS modification,

the shift in threshold voltage (ΔV_{TH}) is slightly lower than that of HMDS-modified OFETs under the same pre-applied gate voltage (Figure 3c), which can be attributed to the reduced trapping sites at the interface between the organic semiconductor and SiO_2 dielectric, to a certain extent because of HMDS modification. Despite this, for HMDS treated devices, a pre-applied 100 V gate voltage still induces V_{TH} move up to 10.2 V (ΔV_{TH} = 20.45 V). Therefore, it can be concluded that the large V_{TH} shift we observed in this work did not originate from the interfacial trappings (bias stress effect), and the defects or trappings in the SiO_2 bulk might be the main contributor. Particularly, for the HMDS-treated transistor, the transfer curve was tested every 18 min after a voltage of −140 V was pre-applied to the gate electrode. The transfer curve slowly moved towards the initial position over time, as shown in Figure 3d. Although the large V_{TH} shift observed in this work does not belong to the bias stress effect, this time-dependent V_{TH} can still be described using the stretched exponential model [26,47] (Figure S6).

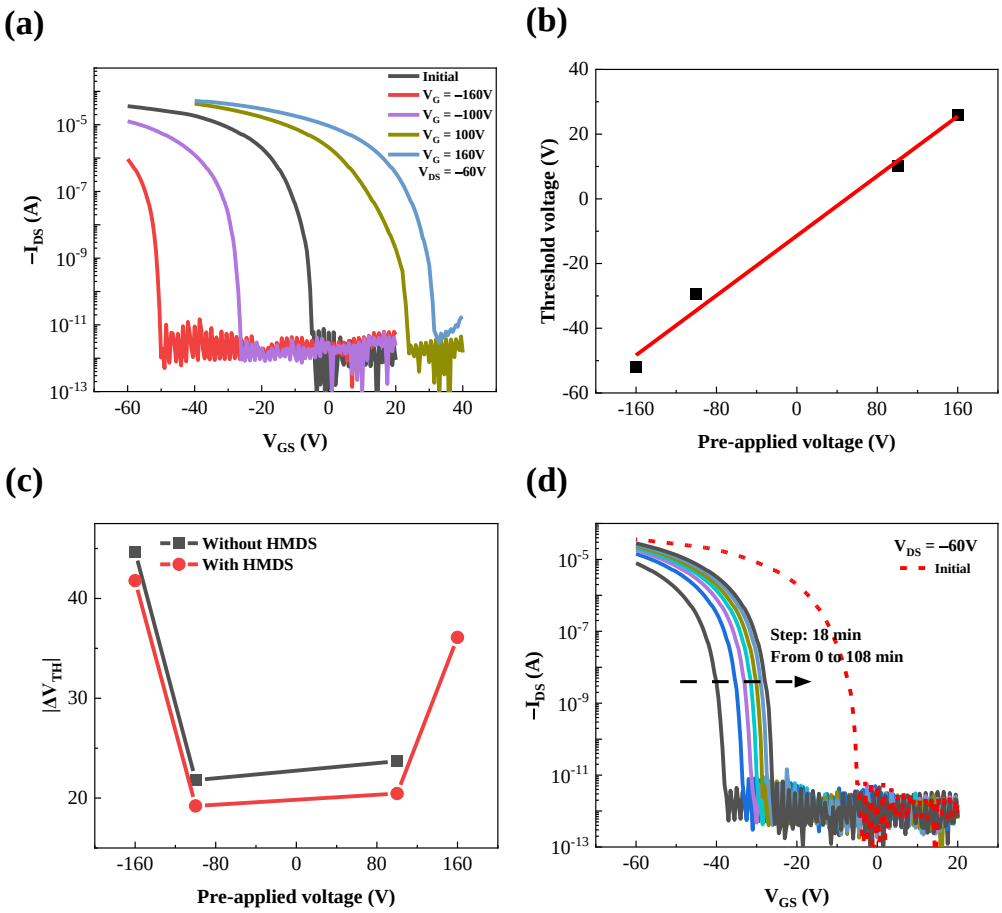

Figure 3. (**a**) Transfer curves of different pre-applied gate voltages after the device was treated with HMDS; (**b**) Threshold voltage shift as a function of pre-applied voltage to the gate electrode; (**c**) The relationship of ΔV_{TH} with pre-applied gate voltage with (red line) and without (black line) HMDS modification; (**d**) With a pre-applied −140 V gate voltage, the transfer curves of the HMDS-treated device with time.

Considering the above experimental results, the main reason for this phenomenon can be explained using Figure 4. When pre-applying a large positive gate voltage, electrons are injected from the source and drain electrodes into the gate dielectric [48]. After removing the pre-applied gate voltage, a certain portion of electrons are trapped in the bulk of the SiO_2. This process seems similar with floating-gate transistors, where the injected electrons "charge up" the dielectric. Those "charged up" electrons provide an additional electric field to the conduction channel, resulting in a large V_{TH} shift in the positive direction. As time

goes on, the trapped electrons are released to the channel slowly and gradually in the form of leakage current, causing the threshold voltage of the OFET to gradually recover over time, like the trend shown in Figure 3d. On the contrary, a negative pre-applied voltage leads to "injected" holes into the SiO_2 gate dielectric, trapped in the bulk of the dielectric after removal of the pre-applied gate voltage. These trapped holes repel the carriers within the conducting channel, causing V_{TH} shift in the negative direction.

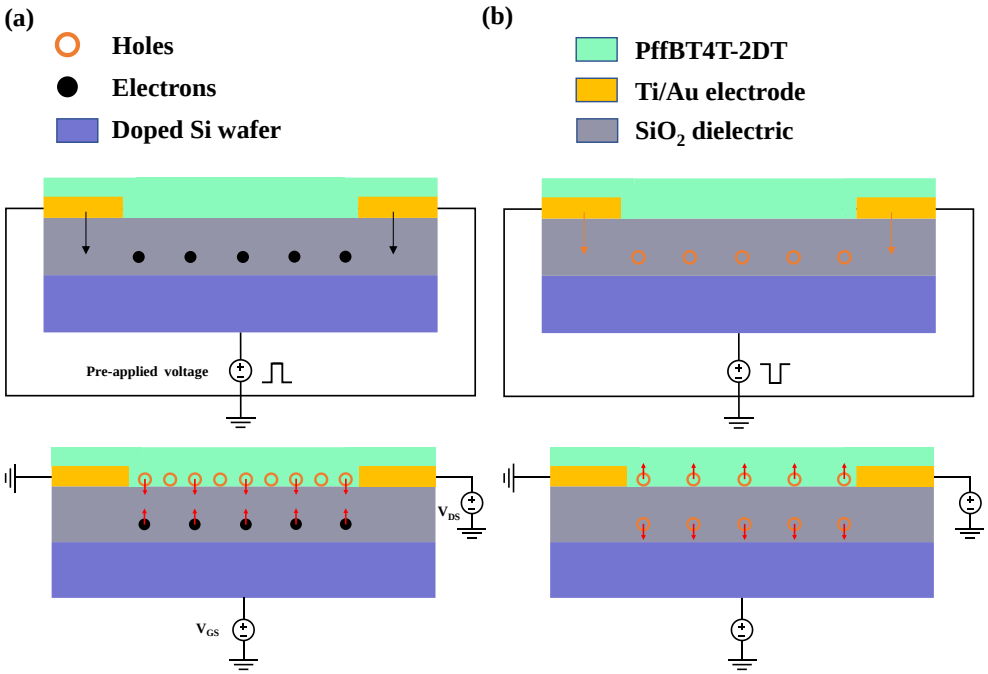

Figure 4. Operation model for shift threshold voltage: (**a**) pre-applied positive gate voltage and (**b**) negative voltage.

In addition, we also used other two conjugated polymers including p-type PDPP3T [49,50] and n-type PTzNDI-2FT to verify the generality of our observation of V_{TH} shift, where the surface of the SiO_2 dielectric is functionalized using HMDS SAM. Typical linear/saturation behaviors are observed for both transistors (Figures S5b and S7). The transfer curves of those two OFETs after pre-applied gate voltage are shown in Figure 5. It can be seen that, for both polymers, there still exists a large threshold voltage shift phenomenon after a pre-applied large gate electrode voltage, independent of semiconducting materials. For p-type PDPP3T, the pre-applied voltage of 140 V results in the V_{TH} shift from 4.8 V to 36.5 V, while the voltage of −140 V leads to V_{TH} = −19.4 V. In comparison, V_{TH} of n-type PTzNDI-2FT is shifted from 16.8 V to 46.1 V when pre-applying 140 V to the gate electrode, and moves to 7.4 V with the pre-applied voltage of −100 V. As explained in Figure 4, these behaviors should be ascribed to the charge trappings in the bulk of the 300 nm thick SiO_2 dielectric, which creates an additional electric field and critically affects the charge transport in the conduction channel.

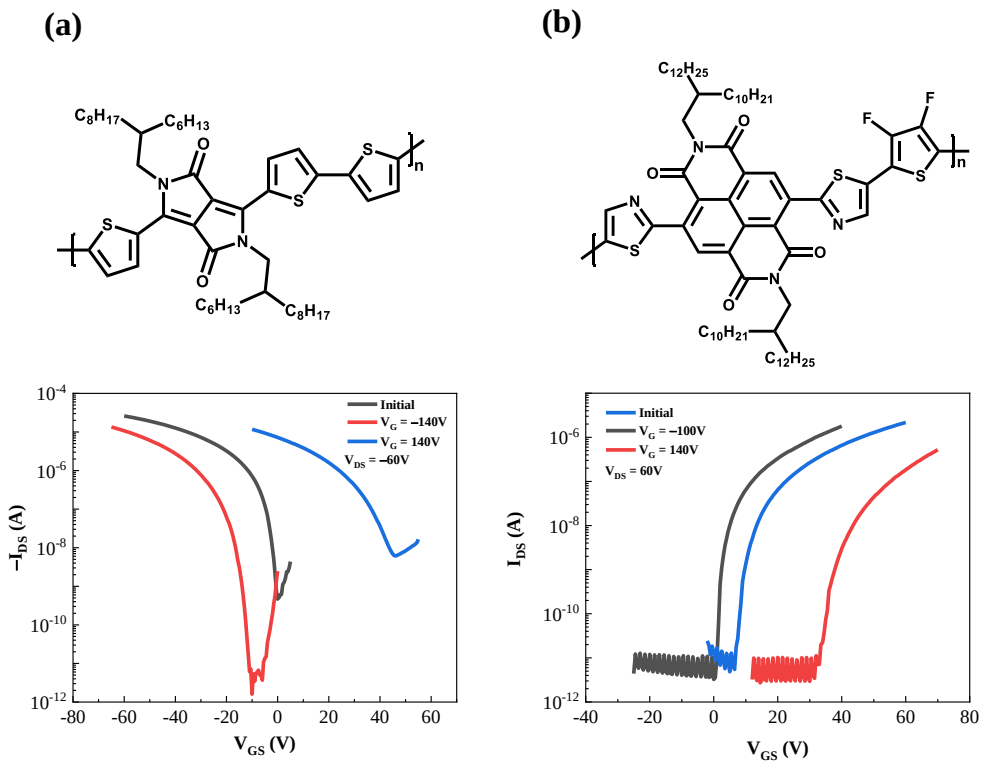

Figure 5. Chemical structures and transfer curves at different pre-applied gate voltages for (**a**) PDPP3T and (**b**) PTzNDI-2FT OFET.

3. Conclusions

In conclusion, we observe a large V_{TH} shift when pre-applying a voltage to the SiO_2 gate dielectric. Interestingly, such behavior remains even after surface modification of SiO_2 using HMDS SAM. It is assumed that the traps inside the SiO_2 bulk lead to the capture and release of electrons/holes under the condition of large pre-applied gate voltage, which affects the carrier concentration in the channel and causes the transistor threshold voltage to shift by about 80 V. This large V_{TH} shift induced by pre-applied gate voltage is further verified by using two other conjugated polymers. These results offer a new consideration for the design of OFETs and a new idea to further improve the stability of OFETs.

4. Experiments

Materials: PffBT4T-2DT was purchased from Nanjing Zhiyan Ltd. PDPP3T and PTzNDI-2FT were synthesized according to the literature [51,52].

PFBT modification: After activation by using oxygen plasma for 30 s, the Au electrodes were functionalized with PFBT SAM by immersing the cleaned substrates into 10 mM PFBT solution in ethanol for 6 h. After this, the device surface was cleaned twice with ethanol and blown dry under nitrogen.

HMDS modification: The substrate was placed in a vacuum chamber and heated up to 130 °C. Exposure to HMDS vapor was maintained for 3 min.

Transistor fabrication and characterization: The substrates for OFET fabrication were purchased from Tianjin Semiconductor Technology Research Institute Ltd., in which heavily p-type doped silicon with 300 nm thick thermally grown SiO_2 was used as back-gate electrodes and the dielectric layer. Source and drain electrodes were defined by photolithography to obtain a channel length of 10 um and channel width of 200 um. Titanium with a thickness of 5 nm and gold with a thickness of 30 nm were sequentially deposited on the substrate through electron beam evaporation as the source and drain electrodes of the OFETs. 5 nm thick titanium was used for enhancing the adhesion of gold electrodes to substrates. The Au electrodes were functionalized with PFBT modification. After the

PFBT SAM functionalization, the SiO_2 substrate was treated with HMDS modification to passivate the surface. Different organic semiconductor thin films were deposited by spin-coating at 1500 rpm for 60 s. After thin film deposition, the substrates were annealed at 100 °C for 30 min in a glovebox under a nitrogen atmosphere to remove the residual solvent. All electrical test results were measured using a Keithley-4200 Semiconductor Analyzer in a nitrogen atmosphere glovebox.

Supplementary Materials: The following supporting information can be downloaded at: https://www.mdpi.com/article/10.3390/electronics12030540/s1, Figure S1: The transfer (a) and output (b) curves of the PffBT4T-2DT transistor; Figure S2: (a) $I_{DS}{}^{0.5}$ vs V_{GS} plotting, where the data are from Figure 2 (a); (b) Saturation mobility at different pre-applied voltages.; Figure S3: (a) PffBT4T-2DT transistor transfer curves of −100 V and 100 V pre-applied voltage at the gate electrode for multiple times; (b) The transfer curves obtained by repeatedly pre-applied different voltages to the gate and drain electrodes simultaneously; Figure S4: Transfer curves of PffBT4T-2DT transistor without PFBT modification at different pre-applied voltages to the gate electrode. Figure S5: Hysteresis behaviors of PffBT4T-2DT (a) and PDPP3T (b) transistors before and after HMDS modification; Figure S6. (a) Pre-applied a −140 V gate voltage, the relationship of HMDS treated device transfer curve with time; (b) Fitting the threshold voltage over time after a pre-applied −140 voltage by stretched exponential model; Figure S7: Output curves of PTzNDI-2FT transistor.

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Data Availability Statement: The data presented in this study are available on request from the corresponding author.

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Conflicts of Interest: The authors declare no conflict of interest.

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