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DC-AC Converter with Dynamic Voltage Restoring Ability Based on Self-Regulated Phase Estimator-DQ Algorithm: Practical Modeling and Performance Evaluation

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Abstract: A self-regulated phase estimator (SRPE)-based DQ algorithm for a DC-AC converter with dynamic voltage restoring (DVR) ability is presented in this paper. When compared to the conventional phase-locked loop (PLL), the provided controller can significantly reduce phase distortions and low-order harmonics from the load voltage while attaining quicker dynamic response. Furthermore, the fundamental attribute of the load voltage allows the integrated DC-AC converter to operate at a consistent frequency eliminating frequency oscillations. The SRPE is utilized primarily in the DQ control theory as the reference voltage generator which can compensate for the grid voltage. SRPE has good band-pass filtering properties and a mathematically simple structure that can thoroughly attenuate voltage imbalance and has quick dynamic response. The SRPE has been made to be frequency-adaptive using a damping factor and robust grid frequency estimation. The SRPE can maintain the fundamental frequency at 50 Hz and keep the total harmonic distortions (THD) within the 5% limit even during grid disruptions. The DC-AC converter and SRPE-DQ's stability are thoroughly examined. The experiment is carried out to show the efficacy of the suggested complete control system. There are also comparative simulation studies to show the benefits of the suggested technique. The results reveal that the suggested approach can immediately identify and correct for any grid voltage imbalance while also assisting in maintaining the constant voltage at the load side despite voltage sag/swell and distortions.

Keywords: DC-AC converter; dynamic voltage restorer (DVR); load voltage compensation; DQ control theory; power quality; phase synchronization; phase-locked loop (PLL)

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1. Introduction

Power quality is crucial for the power electronic and system components including, inverter, converter, transformers, and utility grid to run smoothly [1,2]. Power quality deterioration can cause serious voltage fluctuations in numerous crucial power electric components that are frequently utilized in power industries. These unwanted fluctuations can also cause heat generation, components degradation, component tripping, and induce massive power losses. These variations typically manifest themselves in the power grid as voltage sag, voltage swell, and harmonic distortions. Several specific types of DC-AC converters are specialized custom power devices that have been created specifically to protect power electric components from such fluctuations in grid voltage [3,4]. A dynamic

voltage restorer (DVR) is one of them [5]. A DC-link voltage supply, a DC-AC converter, a transformer connected in series between the grid and the load, and some passive filters make up the basic configuration of DVR. The primary objective of these devices is to inject a compensation voltage at the point of common coupling (PCC) so that the voltage that feeds the load is unaffected by grid voltage changes. In other words, regardless of grid voltage fluctuations, the load voltage never changes.

The voltage variations must first be identified in order to construct a robust configuration of the DC-AC converter that performs the necessary operation. According to the IEEE Recommended Practice for Evaluating Electric Power System Compatibility with Electronic Process Equipment [6], voltage sag occurs when the grid voltage briefly drops from its nominal value. The short circuit faults in the grid, such as generation/load mismatch, unexpected load connections, component failure especially in the converter, and ground faults in the power system, are typically to blame for voltage sags. On the other hand, voltage swell occurs when the grid voltage briefly increases from its nominal range [6]. When a load is unexpectedly disconnected and large capacitors are turned on, voltage swell happens. The impact time of voltage sags and swells is very small, and it stays sometimes around 0.5 cycles to 1 min maximum. However, even in this small-time frame, it can cause massive disruptions in the grid network. As a result, it is highly required to detect these issues and compensate for the grid voltage very swiftly of these voltage variations. Voltage sag/swell detection is relatively simple. Nevertheless, it becomes highly challenging and difficult when frequency fluctuations along with voltage fluctuations occur in the grid network since these types of fluctuations contain high harmonic components. Thus, the total harmonic distortion (THD) can increase and cause serious consequences if the voltage compensation approach does not have the capability to effectively eliminate harmonics from the voltage.

The control scheme associated with the DC-AC converter/DVR determines how quickly the detection and compensation of the voltage/frequency fluctuation can be conducted. The quality of the load voltage is also influenced by the applied control strategy. There are two major obstacles that need to be overcome in order to increase power quality using a DC-AC converter/DVR. First, the control approach must be capable of accurately detecting the fluctuations in the grid voltage from its nominal amplitude/frequency by utilizing an accurate measurement of the grid voltage [7]. Moreover, it must be capable of separating the fundamental components of the grid voltage from the harmonically distorted components. In order to generate the required reference voltage, which is utilized to detect voltage fluctuations and filter harmonics components from the grid voltage, a sophisticated grid frequency-adaptive filtering scheme must be developed. Second, when reducing the THD of the load voltage, the control algorithm must be able to quickly track the reference voltage. This calls for the formulation of a reliable control strategy and algorithm that can quickly converge while also handling external disturbances and voltage fluctuations.

The researchers have developed a wide variety of control strategies for voltage compensation along with advanced DC-AC converter topologies in recent works of literature to address the necessary challenges and issues regarding voltage fluctuations in the grid network. Among these control techniques, the most popular and simplified control strategy is the conventional PI controller in the synchronous frame (SRF) or DQ control theory [8]. Although the implementation of SRF-PI is straightforward, the performance of this controller is highly dependent on the parameters of the PI (i.e., proportional gain and integral gain). This often requires manual tuning based on a trial-and-error approach. Additionally, various metaheuristics and other advanced optimization algorithms are utilized to accurately optimize the PI parameters. Nevertheless, it can add unwanted computational complexities to the system. Therefore, the performance of this controller is often not satisfactory, and it comprises a sluggish response and high overshoots. An SRF-Fuzzy controller is proposed by [9] to overcome the issues associated with conventional SRF-PI controllers in DVR. However, the absence of a systematic design process is the main issue of the fuzzy controller. Furthermore, like the PI controller, it also requires manual tuning of the member-

ship functions to optimize its performance. This issue was addressed by the SRF-adaptive neuro-fuzzy interference system-based (SRF-ANFIS) DVR proposed in [10]. This controller improved the performance of SRF-Fuzzy and the membership function was tuned using the adaptive neuro algorithm. However, it increases the converter's computation burden significantly since it utilized five layers of a neural network. An adaptive-SRF-based controller is proposed in [11] for the DVR application. Although the controller performs well and can compensate load voltage correctly under voltage sag/swell, it falters heavily under harmonically distorted grid voltage. An Energy Self-Recovery (ESR)-SRF controller-based DVR converter is proposed in [12] which uses a modified method of detecting grid voltage issues. However, the controller is designed, and its performance is validated only under various voltage sag conditions. Therefore, its applicability under voltage swell and voltage distortions is highly questionable.

As discussed earlier, the accurate generation of the reference voltage is a crucial part of the DC-AC converter/DVR control. Although it is very simple and straightforward to generate reference voltage in nominal conditions, control complexities may arise while dealing with the harmonically polluted grid voltage. Additionally, the frequency also oscillates close to the nominal value which makes it even more difficult to detect the anomalies. Several different approaches have been published in the literature to address this issue, including DQ control theory [8], DQ with artificial neural network [9,10], and PQ theory [13]. The DQ control has several benefits over other techniques, including its simplicity, speed, and reduced number of computations, all of which raise the likelihood that it will be put into practical use. The primary criterion that defines the efficacy of a DQ-based reference voltage generation is its capacity to deliver precise and efficient identification of the fundamental component. Nonetheless, more recently, the DQ control method has favored the use of conventional synchronization techniques, in particular a phase-locked loop (PLL) [9,10,12], and additional PI controllers for reference voltage generation. PLL technology has been frequently used in the DC-AC converter/DVR control literature to solve this problem. The PLL plays a significant role in DC-AC converter/DVR control. PLL is a kind of control mechanism that produces a phase angle that is proportional to the grid's voltage phase. A conventional PLL has a structure that includes feedback looping between a phase detector and a variable frequency oscillator. The grid voltage provided to the oscillator determines both its frequency and its phase, thus the name voltage-controlled oscillator (VCO). The oscillator produces a periodical waveform at a certain frequency, and the phase detector contrasts this output with the grid voltage waveform in order to maintain phase coherence. In order to maintain phase coherence between the output and the grid voltage, their frequencies must be similar. Conventional PLL has its own characteristics and limitations that may impact the performance of the DC-AC converter/DVR which includes the use of conventional low pass filter (LPF) with poor filtration ability, use of PI controllers, and inducing phase delay and distortions in the reference voltage.

A number of improved PLL are proposed in the literature to enhance the performance of the conventional PLL by replacing the LPF with other filters including adaptive notch filter (ANF) PLL [14], comb filter PLL [15], Kalman filter PLL [16], moving average filter (MAF) PLL [17], Savitzky-Golay filter (SGF) PLL [18], and second order generalized integrator (SOGI) PLL [19] are some examples. Nevertheless, each of these advanced filters-based PLLs has some common deficiencies which include complex trigonometric calculations and parametric sensitivity (i.e., filter order, signal-to-noise ratio, frame length). Considering these drawbacks, this manuscript proposed a self-regulated phase estimator (SRPE) for the DC-AC converter/DVR's synchronization operation that does not require any complex computations. Moreover, SRPE has an excellent transient response, high filtration ability, and does not introduce any phase delay in the output signal. SRPE has the following advantages over conventional PLL: (i) since SRPE is employed in a constant reference framework, no trigonometry computations are necessary, (ii) unlike traditional PLLs, SRPE does not contain a PID parameter, which has a slow reaction, large overshoots,

and necessitates manual tuning, (iii) it does not cause any phase difference or deviations in the output and (iv) compared to traditional low pass filters (LPF), which are often built into PLLs, SRPE offers better filtering capabilities.

The primary objectives of this manuscript can be listed as follows:

- Propose a DC-AC converter/DVR based on SRPE to improve the power quality of the grid.
- Propose SRPE and appropriately replace the use of PLL in DC-AC converter/DVR applications that eliminates the use of standard LPFs and PI controllers while addressing grid voltage issues such as voltage sag/swell, imbalance, and distortion.
- SRPE-based DC-AC converter/DVR is utilized to decrease structural complexity and computing cost while also improving power quality, transient responsiveness, and grid stability.
- Verify the proposed DC-AC converter/DVR's functionality by conducting proper simulation and laboratory experiments.

This paper is organized as follows: the problem formulation, the proposed SRPE controller of the DC-AC converter/DVR, and the implementation process of the proposed system are discussed in Section 2. Simulation results and discussion are presented in Section 3. Performance validation, experimental results, and discussion are presented in Section 4. Comparative analysis is presented in Section 5, Finally, Section 6 summarizes the conclusion drawn from the proposed study.

2. Methods

2.1. Problem Formulation

The considered DC-AC converter configuration is depicted in Figure 1. An accurate voltage reference signal is a major step in the operation of a DC-AC converter/DVR. It assists the converter to generate an appropriate voltage injection with a precise phase angle and frequency. Considering the generation of the voltage reference signal for three-phase systems, one of the most popular and simple ways is utilizing a conventional phase-locked loop (PLL) circuit. A simplified conventional PLL structure is shown in Figure 2. Conventional PLL performs relatively well when the grid condition is nominal. The PLL is built using a voltage-controlled oscillator (VCO), a loop filter, and a phase detector. The VCO produces a sinusoidal signal where the frequency nearly resembles the loop filter's center frequency. The loop filter reduces the input signal's high-frequency AC element in order to flatten the signal and smooth it down so that it is more similar to a DC signal. The phase detector produces a voltage based on the phase difference between two signals after comparing their phases. The output of the voltage-controlled oscillator and the reference input is multiplied. The Park and Clarke conversion is used to convert the *abc*-plane to the *dq*-plane. The voltages along the *dq*-plane are used to determine the phase angle. As the voltage in the *q*-plane (v_q) and the error in phase angle are directly proportional to each other, a PI compensator is used to ensure that the v_q is equivalent to zero. After the elimination of the phase angle estimate error is fixed, a reference voltage that is in phase lock with the source voltage may be generated.

The mathematical equations related to a conventional PLL can be realized by studying the transfer equations of three principal parts (i.e., loop filter, VCO, and phase detector). Firstly, the loop filter's transfer function can be demonstrated as follows:

$$F(s) = k_P \times \frac{k_i}{s} \tag{1}$$

Here, k_p is the proportional gain while k_i is the integral gain of the PI controller.

Secondly, by considering the VCO and phase detector gain as k_{VCO} and k_{PE}, correspondingly. The phase error of the PLL can be derived as follows:

$$E(s) = \frac{s}{s + k_{VCO}k_{PE}F(s)} \tag{2}$$

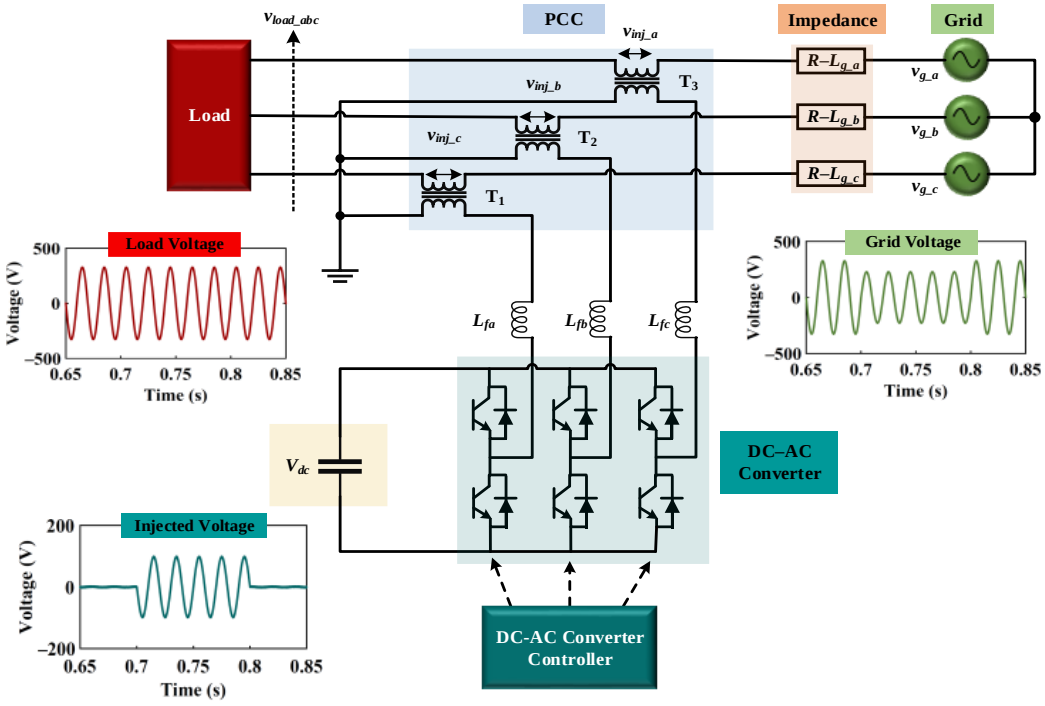


Figure 1. System structure of DC–AC converter integrated grid.

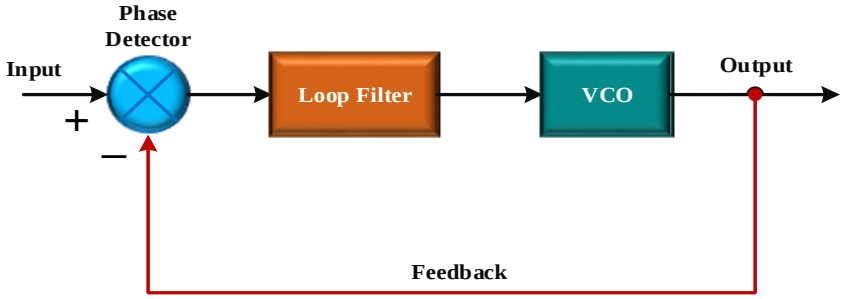


Figure 2. A simplified conventional PLL structure.

By putting the value of (1) into (2), the resultant value of the phase error becomes:

$$E(s) = \frac{s^2}{s^2 + k_{VCO}k_{PE}k_{P}s + k_{VCO}k_{PE}K_i} \tag{3}$$

A generalized second-order equation can be expressed as:

$$E(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{4}$$

Finally, while comparing (3) and (4), the following equations can be derived:

$$\omega_n = \sqrt{k_{VCO}k_i k_{PE}} \tag{5}$$

$$\zeta = \frac{k_P}{2}\sqrt{\frac{k_{VCO}k_{PE}}{k_i}} \tag{6}$$

The settling time of the PLL can be varied depending on the value of the undamped natural frequency (UNF), which results in faster synchronization. Generally, a high value for the UNF is selected, although mathematically it has to be relatively low to provide effective phase filtering. On the other hand, the damping factor affects the overshoot

of the PLL's response and thus, a trade-off between these two parameters is required to be considered in order to obtain the best result from the PLL. Another thing that can be observed from (5) and (6) is that the value of UNF and damping factor depends directly on the gains of the PI controller. This indicates that a fine-tuned PI controller is required to determine the best-optimized values for these two parameters. However, it often requires numerous trial-and-errors or sometimes the intervention of optimization algorithms that can increase the computational burden substantially. Therefore, in this manuscript, the use of PI controller along with the conventional LPF in the loop filter is avoided altogether since they are the two main causes of conventional PLL's performance deficiencies.

2.2. Proposed Solution

The proposed control mechanism used a self-regulating phase estimator (SRPE) mechanism in place of traditional PLLs. SRPE's main goal is to keep the grid voltage in sync with the reference phase of the system. The SRPE is used to obtain the phase data of the system. Figure 3 shows the SRPE control diagram.

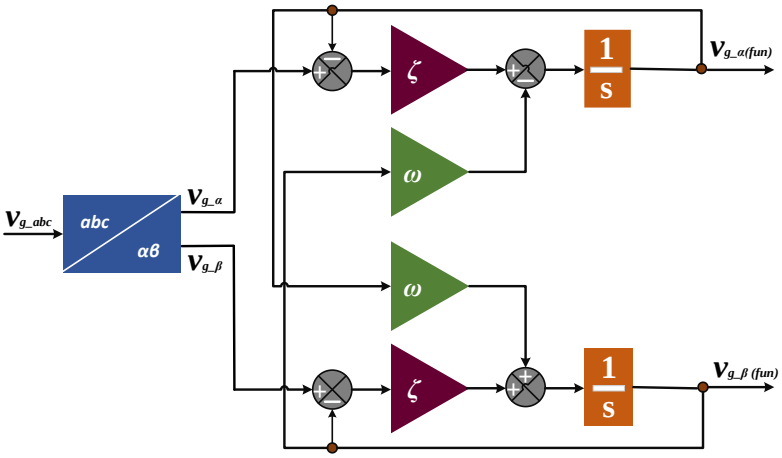


Figure 3. Control diagram of the proposed SRPE.

Understanding the basics of phase-locked loop (PLL) control in the synchronized reference framework is crucial to comprehending how SRPE works. The basic transfer function of the SRPE can be obtained from the synchronized reference framework's integration process and may be written in the following form:

$$V_{xy}(t) = e^{j\omega t} \int e^{-j\omega t} U_{xy}(t) dt \tag{7}$$

The instantaneous input signals before the integration are denoted by $U_{xy}(t)$ and the output signals after the integration are denoted by $V_{xy}(t)$. Utilizing the Laplace conversion, the transfer function in the s-domain may be obtained from (7) as described in the following:

$$H(s) = \frac{v_{g\_abc}(s)}{u_{g\_abc}(s)} = \frac{s + j\omega}{s^2 + \omega^2} \tag{8}$$

The damping factor (ζ) in (8), which is used to create the SRPE with a cut-off frequency of ω_c, results in the following new transfer function:

$$H(s) = \frac{\zeta\{(s + \zeta) + j\omega_c\}}{(s + \zeta)^2 + {\omega_c}^2} \tag{9}$$

By setting the damping factor (ζ) at $\omega = \omega_c$, the amplitude of the transfer function established in (9) will be transformed into a fixed number of 1. As a result, SRPE has no

phase difference at ω_c, as can be seen from the bode graph in Figure 4. The following is a representation of the outputs of (9), expressed in the $\alpha\beta$ domain:

$$v_{g\_\alpha}(s) = \frac{\zeta(s+\zeta)}{(s+\zeta)^2+{\omega_c}^2} u_{g\_\alpha}(s) - \frac{\zeta\omega_c}{(s+\zeta)^2+{\omega_c}^2} u_{g\_\beta}(s) \tag{10}$$

$$v_{g\_\beta}(s) = \frac{\zeta\omega_c}{(s+\zeta)^2+{\omega_c}^2} u_{g\_\alpha}(s) + \frac{\zeta(s+\zeta)}{(s+\zeta)^2+{\omega_c}^2} u_{g\_\beta}(s) \tag{11}$$

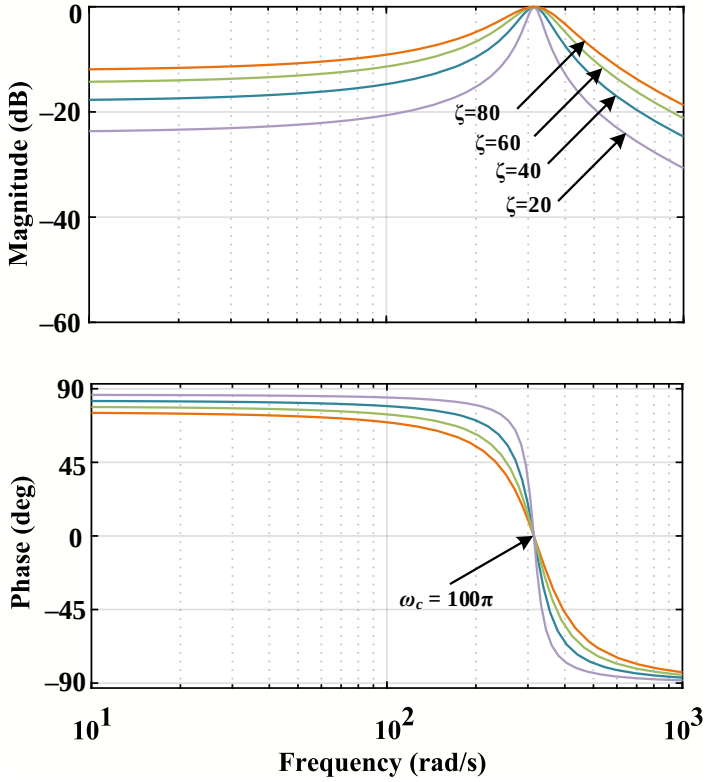


Figure 4. SRPE bode graphic for varying damping factors (ζ).

To understand the operation of the SRPE, generalized equations are presented above. Here, $u_{g\_\alpha\beta}$ represent the input signals and $v_{g\_\alpha\beta}$ represent the output signals in the $\alpha\beta$ domain.

Figure 5 demonstrates the dynamic reaction of the SRPE. It is evident that a smaller value of the damping factor (ζ) enhances the SRPE's sensitivity.

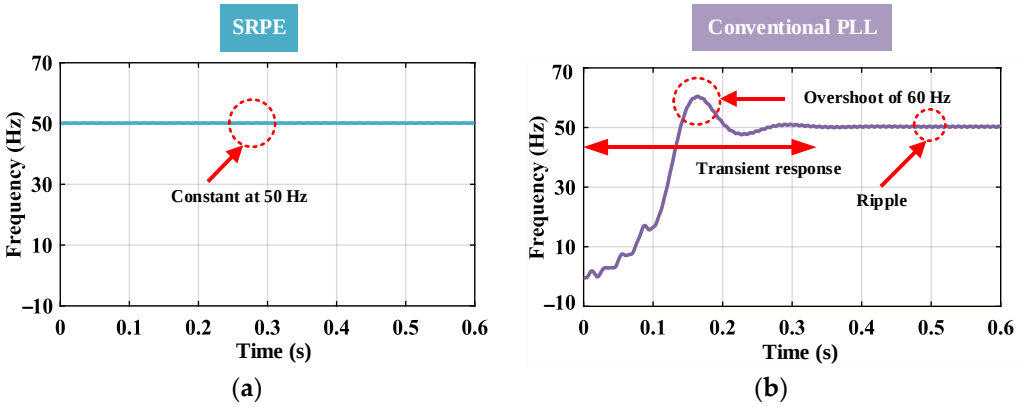


Figure 5. Frequency response in distorted grid condition (**a**) SRPE; (**b**) conventional PLL.

2.3. SRPE's Dynamic Reaction in Comparison to Traditional PLLs

By examining and contrasting the dynamic responses of SRPE and traditional PLL, it is possible to see how the SRPE is better than traditional PLL. The main distinction between SRPE and conventional PLL is how they operate. In contrast to conventional PLLs, which remove harmonic components from harmonically contaminated signals, the suggested SRPE extracts fundamental components. SRPE performs a two-step subtraction and addition after removing the fundamental component in order to produce the required signal. Instead, conventional PLL subtracts the required signal in a single step from the harmonically contaminated input. SRPE provides a number of benefits despite using a two-stage method as opposed to conventional PLL's one-stage operation. Figure 5 displays the frequency characteristics of the SRPE and conventional PLL when a frequency jump of +10 Hz is introduced in the grid voltage. The frequency response of the conventional PLL may be seen to have reached its steady state position after 0.35 s. Therefore, the conventional PLL required 0.35 s to attain the fundamental frequency. This lag results from the proportional–integral (PI) regulators and low-pass filters (LPF) used in conventional PLL, both of which have relatively slow reaction times. There is also a 60 Hz overshoot, which could impair the grid system's ability to function. Despite the fact that the frequency reaction achieved its steady state after 0.35 s, a closer look reveals that it still has a frequency ripple. Due to LPF's inadequate filtering capabilities, this ripple is present. Adjusting the order of the filter or using more sophisticated filters, such as the moving average, Weiner, Chebyshev, Kalman, and so forth may fix the problem. To handle increasingly challenging grid circumstances, these filters frequently need to be modified further since this procedure might create computational complications. Additionally, very complex mathematical computations are needed for these procedures. In contrast, the frequency responsiveness of SRPE is consistently constant irrespective of the presence of harmonic signal pollution. While this SRPE simply extracts the fundamental element, it does not need to be modified in any way depending on how severe the grid circumstances are. Due to this, SRPE has an additional functional benefit over traditional PLLs.

2.4. Reference Voltage Generation

Prior to initiating SRPE-based control, the grid voltages (v_{g_abc}) are Clarke transformed into $\alpha\beta$ elements $\left(v_{g\_\alpha\beta}\right)$. The matrix of transformations may be represented by:

$$\begin{bmatrix} v_{g\_\alpha} \\ v_{g\_\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{g\_a} \\ v_{g\_b} \\ v_{g\_c} \end{bmatrix} \tag{12}$$

In the event of an imbalanced grid voltage, it is possible to subdivide $v_{g\_\alpha\beta}$ into its fundamental ($v_{g\_\alpha\beta(fun)}$) and disrupted ($v_{g\_\alpha\beta(dis)}$) components. The breakdown may be grasped by considering:

$$\begin{bmatrix} v_{g\_\alpha} \\ v_{g\_\beta} \end{bmatrix} = \begin{bmatrix} v_{g\_\alpha(fun)} + v_{g\_\alpha(dis)} \\ v_{g\_\beta(fun)} + v_{g\_\beta(dis)} \end{bmatrix} \tag{13}$$

The generation of synchronization phases necessitates the presence of both fundamental elements in the $\alpha\beta$-plane. The SRPE technique is used to separate the fundamental elements. The SRPE technique is used to dampen the contorted grid voltage's harmonic content. That is why the phases of synchronization may now be derived with greater precision and accuracy. An example transfer function for SRPE after undergoing the Laplace transformation is given as follows:

$$\begin{bmatrix} v_{g\_\alpha(fun)}(s) \\ v_{g\_\beta(fun)}(s) \end{bmatrix} = \frac{\zeta}{s} \begin{bmatrix} v_{g\_\alpha}(s) - v_{g\_\alpha(fun)}(s) \\ v_{g\_\beta}(s) - v_{g\_\beta(fun)}(s) \end{bmatrix} + \frac{\omega_c}{s} \begin{bmatrix} -v_{g\_\beta(fun)}(s) \\ v_{g\_\alpha(fun)}(s) \end{bmatrix} \tag{14}$$

In this case, ω_c is the cut-off frequency and ζ is the damping factor. ζ's rating is roughly between 20 and 80, whereas ω_c's rating tracks the system's frequency. A rating of 20 is anticipated for ζ and 100π for ω_c in this endeavor.

With $v_{g\_\alpha(fun)}$ and $v_{g\_\beta(fun)}$, the synchronizing elements $\sin(\omega t)$ and $\cos(\omega t)$ can be achieved using following formula:

$$\begin{bmatrix}\sin(\omega t)\\ \cos(\omega t)\end{bmatrix} = \frac{1}{\sqrt{\left(v_{g\_\alpha(fun)}\right)^2 + \left(v_{g\_\beta(fun)}\right)^2}} \begin{bmatrix} v_{g\_\alpha(fun)}\\ -v_{g\_\beta(fun)}\end{bmatrix} \tag{15}$$

Using the frequency and phase data from SRPE, we can obtain the standard voltage signal (v_{std}) as shown in (16). Here, the gain of peak amplitude is achieved from the rated load voltage. The standard voltage signal needs to be in sync with the grid voltage at the point of common coupling (PCC).

$$\begin{bmatrix} v_{std\_a}\\ v_{std\_b}\\ v_{std\_c}\end{bmatrix} = V_{pk} \quad \begin{bmatrix}\sin(\omega t)\\ \sin\left(\omega t - \frac{2\pi}{3}\right)\\ \sin\left(\omega t + \frac{2\pi}{3}\right)\end{bmatrix} \tag{16}$$

$$\begin{bmatrix} v_{std\_\alpha}\\ v_{std\_\beta}\end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2}\\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2}\end{bmatrix} \begin{bmatrix} v_{std\_a}\\ v_{std\_b}\\ v_{std\_c}\end{bmatrix} \tag{17}$$

$$\begin{bmatrix} v_{std\_d}\\ v_{std\_q}\end{bmatrix} = \begin{bmatrix}\cos(\omega t) & \sin(\omega t)\\ -\sin(\omega t) & \cos(\omega t)\end{bmatrix} \begin{bmatrix} v_{std\_\alpha}\\ v_{std\_\beta}\end{bmatrix} \tag{18}$$

Afterward, the Clarke conversion matrices are employed to transform the standard voltage output from the *abc*-plane to the $\alpha\beta$-plane. Then, the SRPE is utilized as shown in (18) to establish synchronization phases and frequency, and the results of this latter step are then employed to create the standard voltage output in the *dq*-frames through the Park conversion matrices.

Moreover, the Formula (19) is used to convert the three-phase load voltages (v_{load_abc}), from the *abc*- to *dq*-frames, as shown in (20).

$$\begin{bmatrix} v_{load\_\alpha}\\ v_{load\_\beta}\end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2}\\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2}\end{bmatrix} \begin{bmatrix} v_{load\_a}\\ v_{load\_b}\\ v_{load\_c}\end{bmatrix} \tag{19}$$

$$\begin{bmatrix} v_{load\_d}\\ v_{load\_q}\end{bmatrix} = \begin{bmatrix}\cos(\omega t) & \sin(\omega t)\\ -\sin(\omega t) & \cos(\omega t)\end{bmatrix} \begin{bmatrix} v_{load\_\alpha}\\ v_{load\_\beta}\end{bmatrix} \tag{20}$$

After that, Formulas (21) and (22) is utilized to convert the three-phase grid voltage v_{g_abc}, from the *abc*-plane to the *dq*-frame.

$$\begin{bmatrix} v_{g\_\alpha}\\ v_{g\_\beta}\end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2}\\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2}\end{bmatrix} \begin{bmatrix} v_{g\_a}\\ v_{g\_b}\\ v_{g\_c}\end{bmatrix} \tag{21}$$

$$\begin{bmatrix} v_{g\_d}\\ v_{g\_q}\end{bmatrix} = \begin{bmatrix}\cos(\omega t) & \sin(\omega t)\\ -\sin(\omega t) & \cos(\omega t)\end{bmatrix} \begin{bmatrix} v_{g\_\alpha}\\ v_{g\_\beta}\end{bmatrix} \tag{22}$$

In the DC-AC converter/DVR control mechanism, the compensation technique utilized the contrasting method among the three signals which are the load voltages (v_{load_dq}), grid voltages (v_{g_dq}) and the standard voltages (v_{std_dq}) (all in *dq*-frame). Firstly, load voltages (v_{load_dq}) are compared with grid voltages (v_{g_d}) to obtain the real error voltage. Secondly, the standard voltages (v_{std_dq}) are compared with the grid voltages (v_{g_d}) to obtain the real reference voltages. Finally, the difference between real error voltages and real

reference voltages gives the compensating voltage waveform in *dq*-frame for the DC-AC converter/DVR.

$$v_{ref\_dq} = \left(v_{std\_dq} - v_{g\_dq}\right) - \left(v_{load\_dq} - v_{g\_dq}\right) \tag{23}$$

Then, the v_{ref_dq} is transformed into *abc*-plane as shown in (24) and (25). In order to provide precise gating signals for the DC-AC converter/DVR, these signals are fed into a pulse width modulation (PWM) voltage controller. The control diagram is depicted in Figure 6.

$$\begin{bmatrix} v_{ref\_\alpha} \\ v_{ref\_\beta} \end{bmatrix} = \begin{bmatrix} \sin(\omega t) & \cos(\omega t) \\ -\cos(\omega t) & \sin(\omega t) \end{bmatrix} \begin{bmatrix} v_{ref\_d} \\ v_{ref\_q} \end{bmatrix} \tag{24}$$

$$\begin{bmatrix} v_{ref\_a} \\ v_{ref\_b} \\ v_{ref\_c} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{ref\_\alpha} \\ v_{ref\_\beta} \end{bmatrix} \tag{25}$$

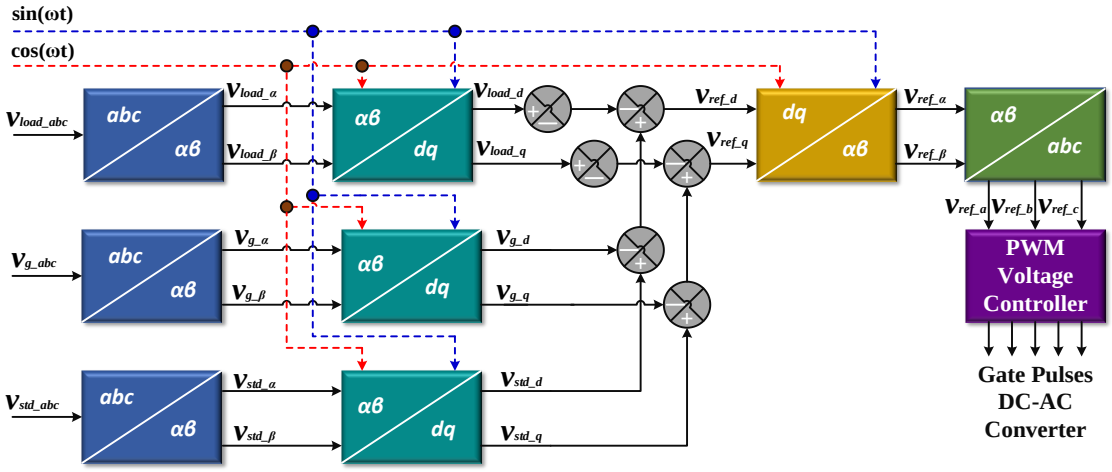


Figure 6. Control diagram of the proposed SRPE-DQ.

3. Simulation Results and Discussions

The SRPE control is designed for a DC-AC converter/DVR and its transient characteristic is evaluated in the MATLAB/Simulink platform (R2020b). The developed method is tested and utilized to compensate for the grid voltage disruptions. The DC-AC converter/DVR is developed for 326 V_{rms}/50 Hz to investigate the operation of the DC-AC converter/DVR. The three-phase signals are depicted in a Red-Green-Blue (RGB) color combination that represents phase a for red color, phase b for green color, and phase c for Blue color. Three-phase resistive load (80 Ω) has been utilized in the manuscript. A line impedance of (1 Ω^{-1} mH) is considered. The total power rating of the DC-AC converter is 11.5 kVA. To reduce the ripple generated by the DC-AC converter, a three-phase inductor (5 mH) is utilized. The sampling frequency of the system is 10 kHz. Different power quality issues are taken into consideration in a number of case studies.

3.1. Voltage Sag Compensation Using SRPE Mechanism

The output results for SRPE-DQ and traditional DQ in the course of supply voltage variations are depicted in Figure 7. Figure 7 shows the DC-AC converter/DVR's dynamic reaction when grid voltage drops by 30%. It can be noticed from the simulation results that the grid voltage magnitude decreased from 326 V to 228 V during 0.7 s to 0.8 s due to a three-phase to ground fault, which can be otherwise considered as a balanced sag [20]. As can be observed, there was no voltage injection from the DC-AC converter/DVR prior to the sag. The converter generates the necessary voltage in the course of the sag situation at the grid voltage and injects it in phase with the grid voltage into the PCC. This injection

prevents the voltage at the load side from being significantly impacted by the voltage sag. However, in the traditional DQ control mechanism, a conventional PLL circuit is utilized which could not perform like the proposed SRPE-DQ in the course of voltage sag. Since the phase and magnitude differences occur during the magnitude variation in the grid voltage, the conventional PLL could not track the phase information as precisely as SRPE. Therefore, the injected voltage contains a ripple that eventually affects the harmonic profile of the load side voltage. The total harmonic distortion (THD) of the load voltage is depicted in Figure 8. It can be noticed from Figure 8 that the THD is a little high in traditional DQ control as compared to SRPE-DQ control. Although inductors are utilized to reduce the ripple, however, it has very limited features.

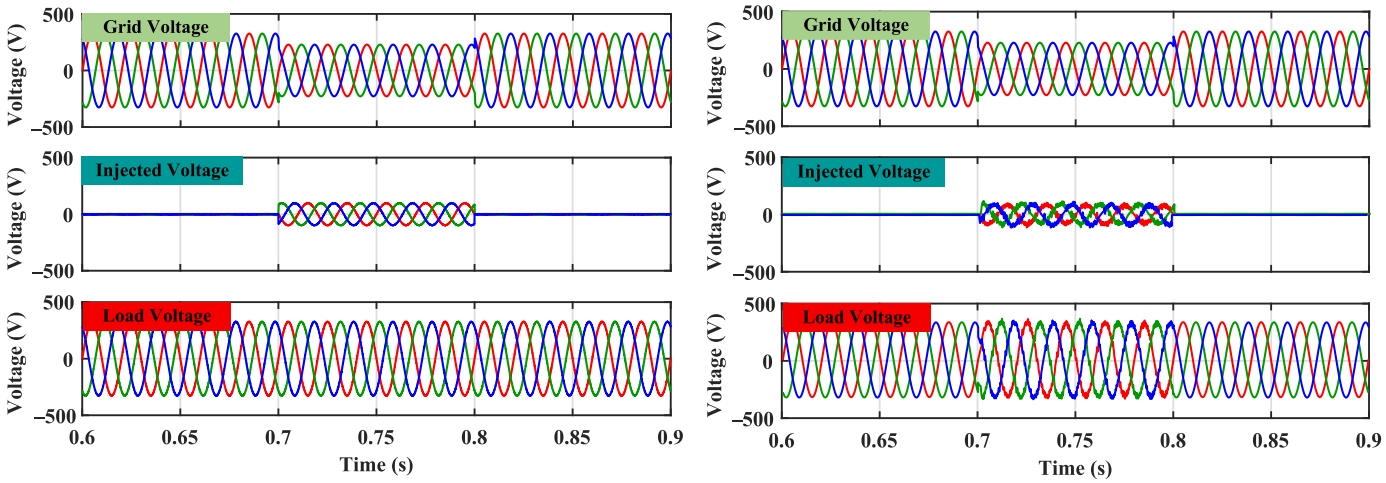


Figure 7. Simulated reaction of grid voltage in the course of voltage sag (v_{g_abc}), injected voltage (v_{inj_abc}), and load voltage (v_{load_abc}) (**a**) SRPE-DQ control; (**b**) traditional DQ control.

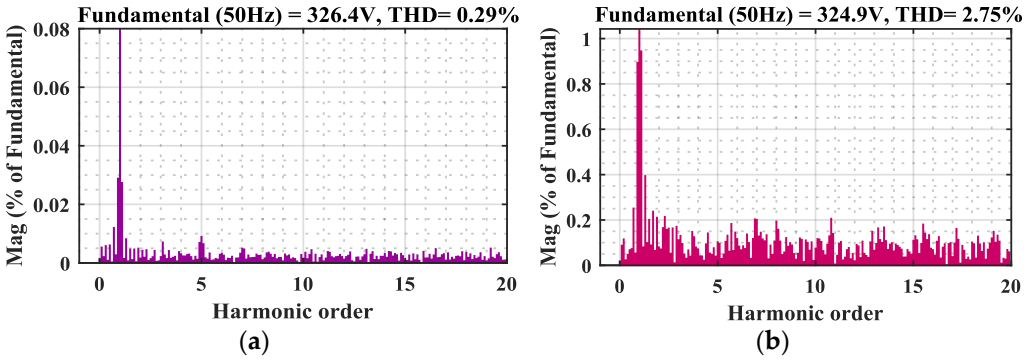


Figure 8. THD profile of load voltage during voltage sag (**a**) SRPE-DQ control; (**b**) traditional DQ control.

3.2. Voltage Swell Compensation Using SRPE Mechanism

The proposed SRPE-DQ algorithm is also evaluated during the voltage swell situation. It can be seen from Figure 9 that a 30% increase in grid voltage is introduced in the course of 0.7 s to 0.8 s. The voltage magnitude was increased from 326 V to 424 V. As can be seen from Figure 9, the DC-AC converter/DVR produces appropriate voltage during the voltage rise situation and inject it out of phase with the grid voltage into the PCC. Therefore, the load voltage was protected from this unfavorable condition. Although the traditional DQ control compensated for the grid voltage, the compensation was delayed by 0.009 s and the injected voltage contains ripples and consequently, the load voltage quality deteriorates.

The THD profile illustrated in Figure 10 reflects the performances and can be observed that the THD in traditional DQ is higher as compared to the SRPE-DQ control.

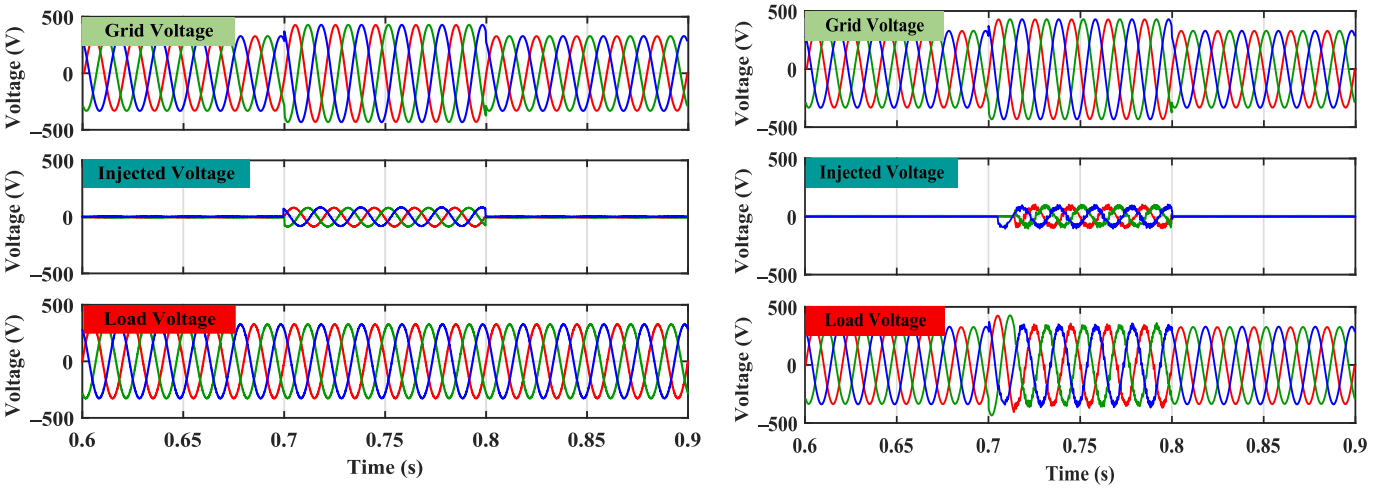


Figure 9. Simulated reaction of grid voltage in the course of voltage swell (v_{g_abc}), injected voltage (v_{inj_abc}), and load voltage (v_{load_abc}) (**a**) SRPE-DQ control; (**b**) traditional DQ control.

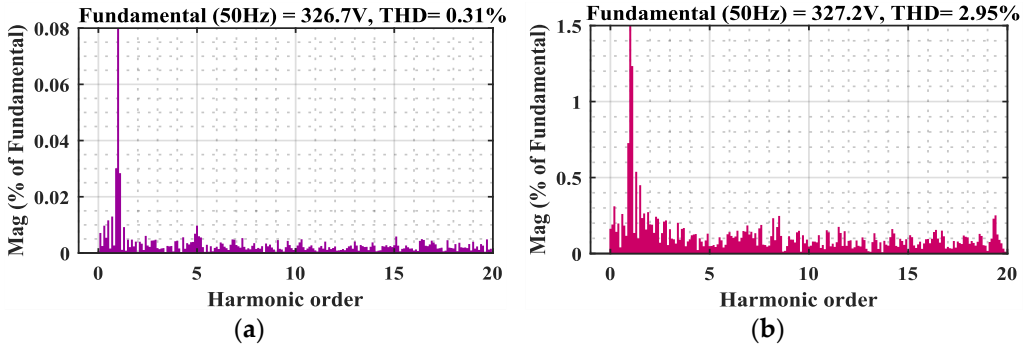


Figure 10. THD profile of load voltage during voltage swell (**a**) SRPE-DQ control; (**b**) traditional DQ control.

3.3. Voltage Harmonic Compensation Using SRPE Mechanism

The presence of harmonics in the load voltage profile can be detrimental to sensitive loads. In the course of 0.7 s to 0.8 s, voltage harmonic is introduced and the SRPE-based DC-AC converter/DVR successfully compensated for the grid voltage and maintained the load voltage profile at its rated value, which can be seen in Figure 11. The SRPE-DQ control tracks the phase precisely and generates the reference voltage which is later injected through the DC-AC converter/DVR. As can be observed from Figure 11, the conventional DQ could not compensate for the grid voltage immediately as compared to the SRPE-based converter. The traditional DQ control took 0.012 s to start injecting and can be observed clearly as some clear disturbances are present in the load voltage profile. The THD spectrum is presented in Figure 12, and it can be noticed that the THD is high in comparison to the SRPE-DQ control algorithm.

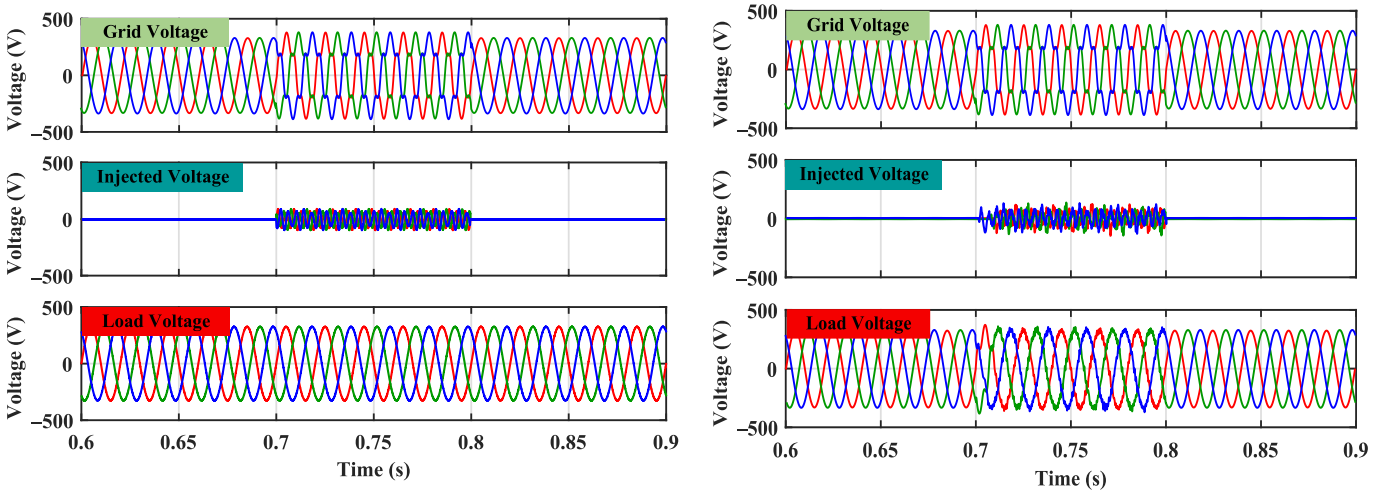


Figure 11. Simulated reaction of grid voltage in the course of voltage harmonic (v_{g_abc}), injected voltage (v_{inj_abc}), and load voltage (v_{load_abc}) (**a**) SRPE-DQ control; (**b**) traditional DQ control.

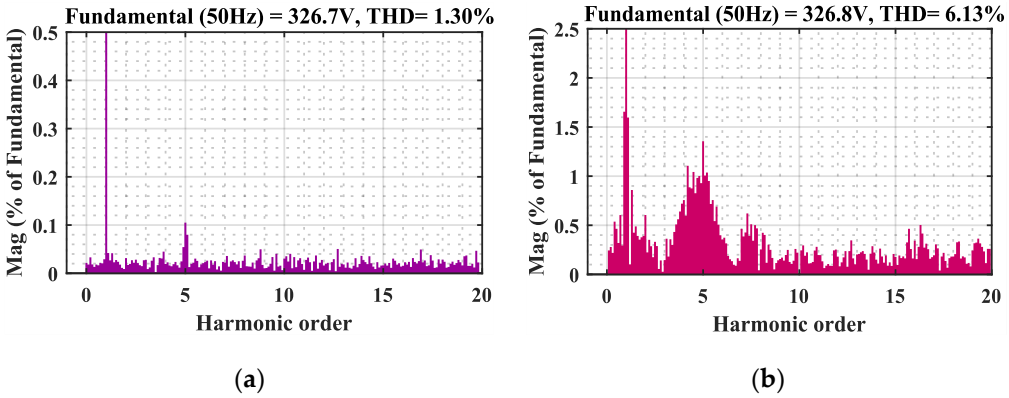


Figure 12. THD profile of load voltage during voltage harmonic (**a**) SRPE-DQ control; (**b**) traditional DQ control.

3.4. Voltage Unbalance Compensation Using SRPE Mechanism

Voltage unbalance can have an adverse effect on sensitive loads. An unbalance voltage was introduced on the grid side to evaluate the performance of the DC-AC converter/DVR. Figure 13 depicts the performance of both SRPE-DQ and traditional DQ, and it can be observed that the magnitude difference in grid-side voltage was compensated. However, due to the poor performance of the conventional PLL, the traditional DQ-based converter compensated the grid voltage with some trade-off, namely the presence of a high quantity ripple in the load side voltage, and consequently, the THD is high, which can be noticed in Figure 14.

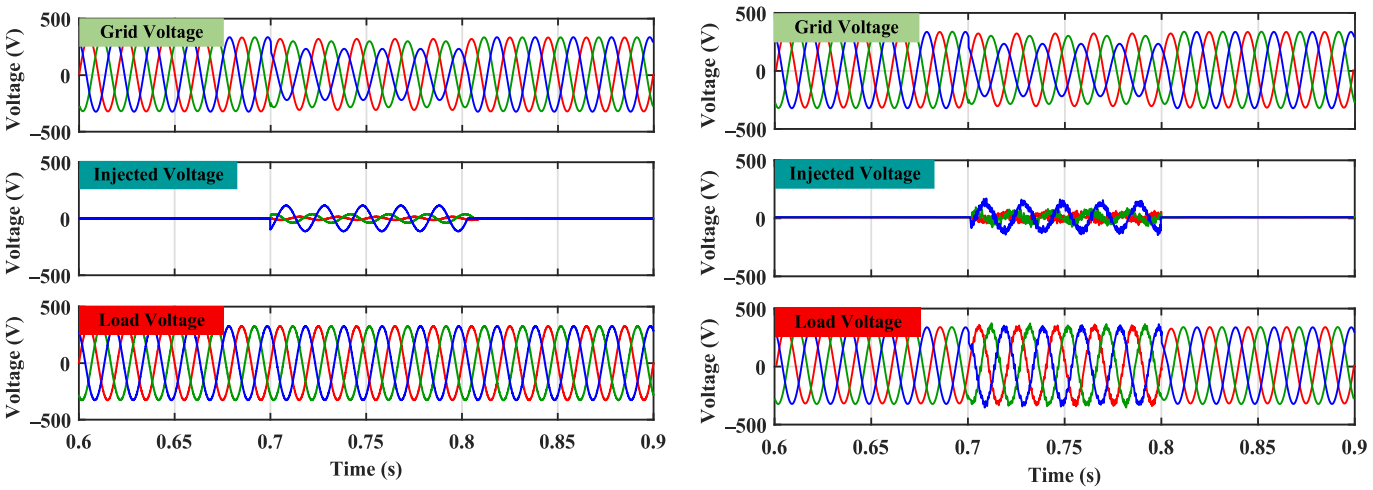


Figure 13. Simulated reaction of grid voltage in the course of voltage unbalance (v_{g_abc}), injected voltage (v_{inj_abc}), and load voltage (v_{load_abc}) (**a**) SRPE-DQ control; (**b**) traditional DQ control.

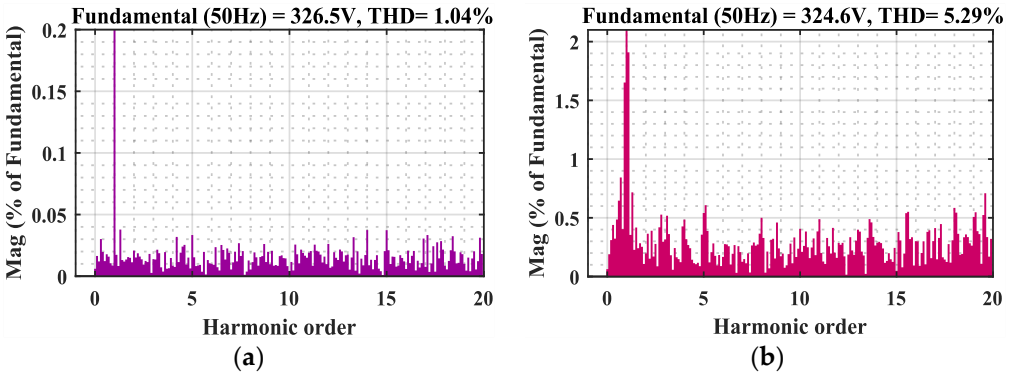


Figure 14. THD profile of load voltage during voltage unbalance (**a**) SRPE-DQ control; (**b**) traditional DQ control.

4. Experimental Validation and Results

The suggested control method has been implemented in a scale-down version which is 1.2 kW/100 V_{rms} (line to line), 50 Hz on the hardware setup that can be seen in Figure 15. The experimental specifications are tabulated in Table 1 [21]. Experimental investigations are carried out for dynamic situations to test the resilience of the suggested strategy. A three-phase programmable AC source was used to provide supply voltages (Chroma 61701). The SRPE-based DC-AC converter/DVR control techniques are implemented on a dSPACE 1104 model, which generates the appropriate gating signals for the DC-AC converter/DVR. In total, nine analog-to-digital (ADC) dSPACE blocks were utilized to measure the three-phase grid voltages, three-phase injected voltages, and three-phase load voltages. After the control processing in the SRPE-DQ controller, using six digital I/O blocks of dSPACE the pulses were generated and provided to the six switches of the DC-AC converter. The dSPACE was operating on a sampling time of 100 µs. The results of the experiments for both steady-state and dynamic circumstances are provided afterward.

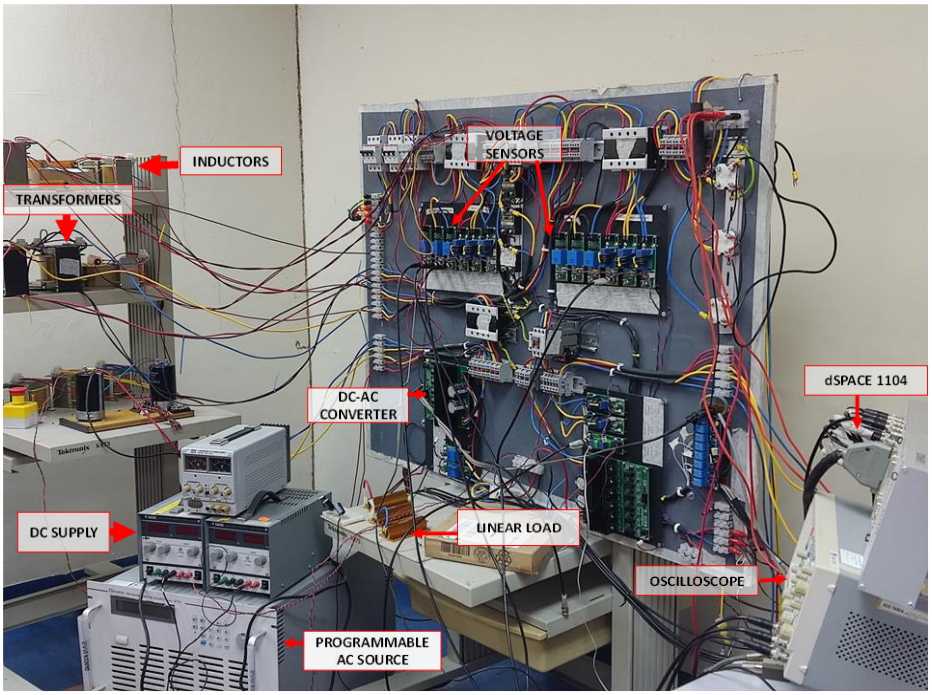


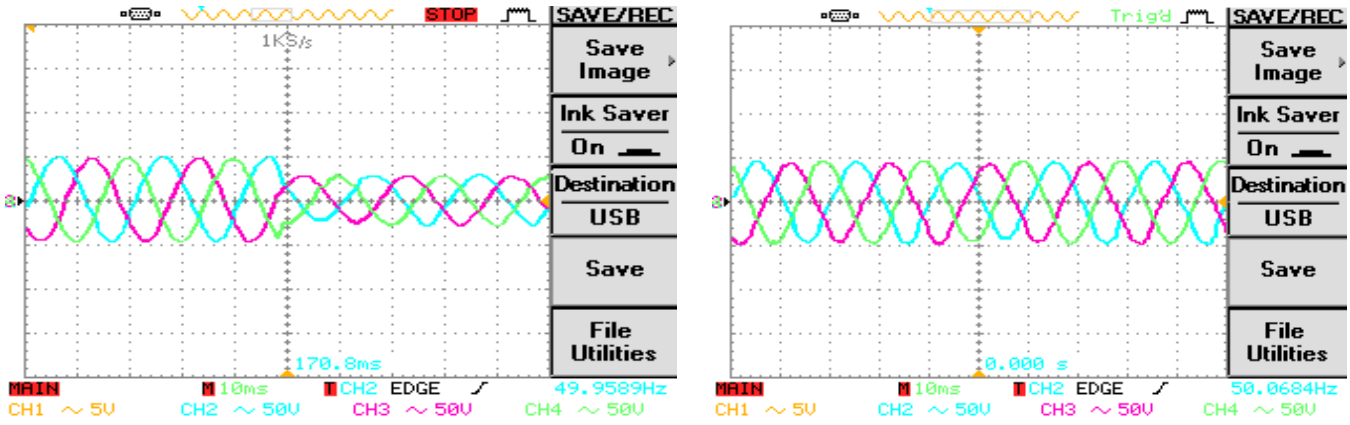
Figure 15. Experimental setup in the laboratory.

Table 1. Experimental setup parameters.

Specification	Value/Unit
Grid frequency	50 Hz
Line-to-line RMS voltage	100 V
AC load (R)	80 Ω
Line impedance (R-L_l)	(1 Ω^{-1} mH)
Active filter rating	1.2 kVA
Passive-filter (L_{fabc})	5 mH
Switching types	Infineon GP35B60PD
Switching frequency	10 kHz

4.1. Scenario 1: Voltage Sag Compensation Using SRPE Mechanism

In scenario 1, when the supply voltage drops due to a three-phase to-ground fault, which can be considered a balanced sag [20], the system's compensating performance is depicted in Figure 16. The supply voltage drops by 30%, and the load voltage is retained at a rated voltage of 100 V_{rms}. The load performance is undisrupted in the course of voltage sag. The converter produces the required voltage during the sag condition at the grid voltage and delivers it into the PCC in phase with the grid voltage. This injection restricts the voltage sag from having a substantial influence on the voltage at the load side.

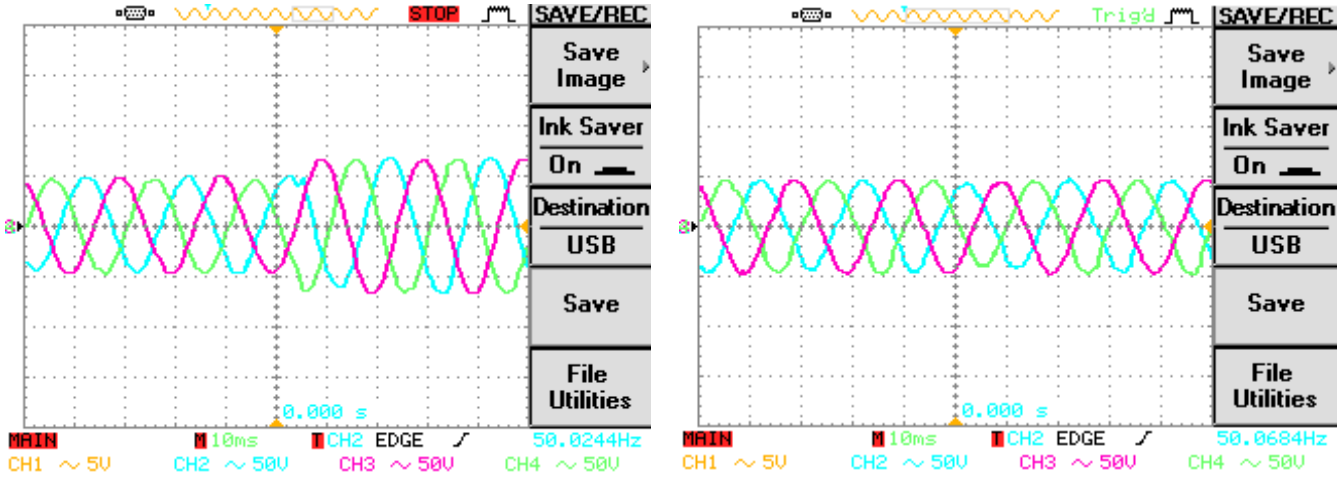


(**a**) (**b**)

Figure 16. Experimental results of the proposed SRPE-DQ-based DC-AC converter/DVR under voltage sag condition: (**a**) grid voltage; (**b**) load voltage.

4.2. Scenario 2: Voltage Swell Compensation Using SRPE Mechanism

Figure 17 displays the system's compensating performance during a 30% grid voltage swell. In this case, the SRPE control of the DC-AC converter/DVR tracks the phase of the supply voltage and injects the appropriate voltage out of phase with the PCC voltage and keeps the load voltages at their rated value.

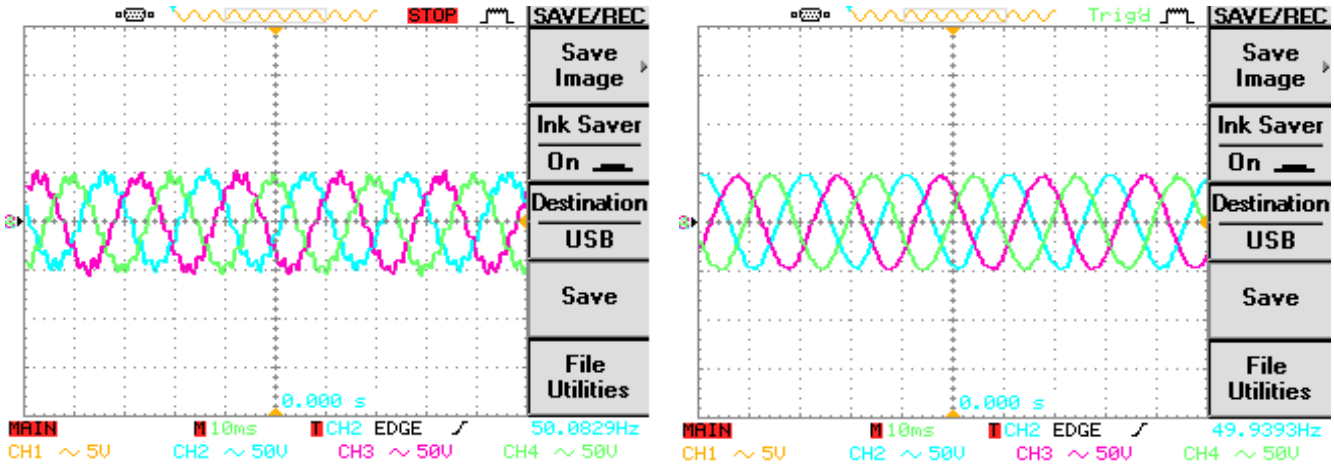


(**a**) (**b**)

Figure 17. Experimental results of the proposed SRPE-DQ-based DC-AC converter under voltage swell condition: (**a**) grid voltage; (**b**) load voltage.

4.3. Scenario 3: Voltage Harmonic Compensation Using SRPE Mechanism

For sensitive loads, the presence of harmonics in the load voltage profile may be harmful. The SRPE-based DC-AC converter/DVR effectively corrected for the grid voltage and kept the load voltage profile at its rated value throughout the introduction of the voltage harmonic, as shown in Figure 18. The reference voltage is created by the SRPE-DQ control, which also accurately records the phase, and afterward delivered via the DC-AC converter/DVR.

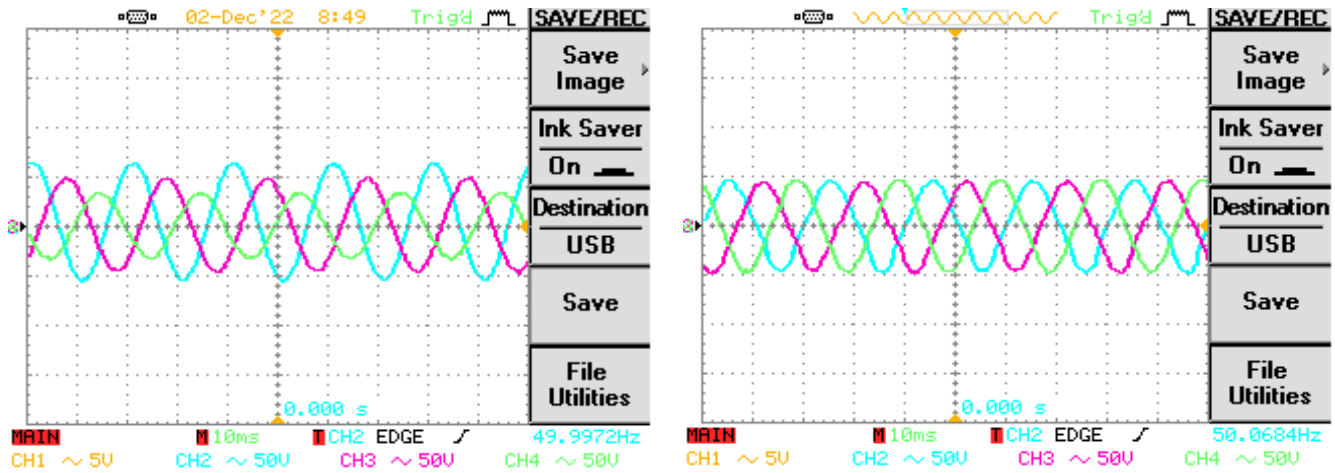


(**a**) (**b**)

Figure 18. Experimental results of the proposed SRPE-DQ-based DC-AC converter under voltage harmonic condition: (**a**) grid voltage; (**b**) load voltage.

4.4. Scenario 3: Voltage Unbalance Compensation Using SRPE Mechanism

Figure 19 depicts the system's performance while experiencing an imbalanced grid voltage. When there is an imbalanced voltage on the grid side, the three-phase grid voltage magnitudes are v_{g_a}= 100 V_{RMS}, v_{g_b} = 50 V_{rms}, and v_{g_c} = 120 V_{rms}. The load voltages are balanced and maintained at 100 V_{rms} throughout this imbalanced voltage sag, as illustrated in Figure 19.



(**a**) (**b**)

Figure 19. Experimental results of the proposed SRPE-DQ-based DC-AC converter under voltage unbalance condition: (**a**) grid voltage; (**b**) load voltage.

5. Comparative Analysis

The superiority and the robustness of the proposed SRPE-DQ-based DC-AC converter/DVR system are validated in this section by comparing it with other DC-AC converters/DVR and their controls. In [13], a DC-AC converter/DVR configuration with a dual p-q theory and instantaneous space phasor-based algorithm is proposed to compensate for the voltage-associated power quality issues. The proposed control performs voltage compensation with an energy-optimized feature. However, this control method needs conventional PLL and LPF for voltage compensation. Conventional PLL consists of LPF and PI controllers.

Although LPF is widely used in custom power devices, it has some significant issues such as average filtration ability, slow transient response, high noise components, and phase distortions [22]. Moreover, the PI controller has issues such as sluggish response to sudden disturbances, high overshoots, and manual tuning [23]. Another inherent drawback related to PI controllers is their inability to accurately track sinusoidal current references which leads to steady state error in the system [24]. Since the PLL in the above-mentioned configuration is used to perform the synchronization operation, this drawback of PI controllers can cause serious problems during grid disturbances. The conventional DQ control technique for voltage compensation was improvised in [25], utilizing additional PI controllers to generate accurate gate pulses injected by the DC-AC converter/DVR to compensate for the grid voltages. The study also utilized the conventional PLL along with additional PI controllers, which make the control system more complex, and unstable, since tuning PI controllers are not simple, especially during weak grid conditions. Another same approach was taken in [26], which consists of a conventional PLL for synchronization purposes and a PI controller to adjust the error voltage. Nonetheless, the THD in load voltage is moderate for voltage sag/swell conditions which are 3.24% and 3.44%, respectively, but the THD will be higher during grid voltage distortions. For SRPE-DQ, the THDs for sag, swell, harmonics, and unbalance are 0.29%, 0.31%, 1.30%, and 1.04%, respectively, and dynamic situations such as voltage harmonic and unbalanced grid conditions were not considered in the case studies of the abovementioned article. One more DQ-based DVR along with conventional PLL and LPF is utilized in [27]. Moreover, a DQ-based control is suggested in [28] to compensate for the grid voltage. Again, a conventional PLL control technique was utilized in the DQ control. Additionally, only voltage sag compensation was considered in the case studies and no experimental result was provided. The studies [9–12] were discussed in the introduction section, where it was discussed regarding the complexity of the control operation due to weight factor methods implementation. It can be observed from Table 2 that the majority of the research work utilized DQ control for reference voltage generation, which is the main scope of this proposed work. Finally, it can be observed from Table 2 that the proposed SRPE-DQ-based DC-AC converter/DVR has outperformed all DC-AC converters/DVRs. It also validates the theoretical hypothesis discussed in the previous section.

Table 2. Comparison among the state-of-the-art and the proposed model under several dynamic conditions.

Category	**[9]**	**[10]**	**[11]**	**[12]**	**[13]**	**[25]**	**[26]**	**[27]**	**[28]**	**Proposed**
Controller complexity	Complex	Complex	Simple	Simple	Simple	Simple	Complex	Simple	Simple	Simple
Grid sync	Conventional PLL	Conventional PLL	Conventional PLL	Not mentioned	Conventional PLL	Conventional PLL	Conventional PLL	Conventional PLL	Conventional PLL	SRPE
Harmonic robustness	×	×	×	×	√	×	×	×	×	√
Additional PI	Yes	No	No	Yes	No	Yes	Yes	Yes	No	No
Reference voltage generation method	DQ	DQ	DQ	PI	Dual-PQ	DQ	DQ	DQ	DQ	DQ
Weight factor method	Not applicable	ANFIS	Not applicable	Manual tuning	Not applicable	Not applicable	ANFIS	Manual tuning	Not applicable	Not applicable
Passive filter count	9	3	3	6	6	9	6	6	9	3
Low-pass filter	Yes	No	Yes	No	No	No	No	No	No	No
THD profile	Not mentioned	Not mentioned	Not mentioned	Not mentioned	Moderate	Good	Good	Moderate	Not mentioned	Excellent
Hardware validation	No	No	No	Yes	Yes	Yes	Yes	No	No	Yes

6. Conclusions

In this study, a self-regulated phase estimator (SRPE)-based DQ is implemented in DC-AC converter/DVR to improve the power quality of a system. The improved grid synchronization approach is provided to aid in the reference voltage generation for the DC-AC converter/DVR. To make the phase estimator adaptive to the grid frequency, a damping factor-based closed-loop control is introduced. The suggested phase estimator considerably reduces phase distortions while maintaining quick dynamic performance due to having the ability to generate a continuous fundamental output signal. This also contributes to maintaining a steady PWM switching frequency for the integrated DC-AC converter. The proposed grid-synchronized technique has been shown to be highly capable of extracting the fundamental component even in severely distorted grid conditions. The SRPE technique has been capable of maintaining fundamental frequency at 50 Hz during grid disruptions. The DC-AC converter/DVR's stability analyses are provided. The theoretical discoveries are validated experimentally under highly challenging grid voltage circumstances. The comparative simulation results show the superiority of the proposed SRPE-DQ control over the conventional DQ control theory. The results highlighted that the conventional DQ control can compensate for the grid voltage during voltage sag/swell conditions, however, during grid harmonic and unbalanced situations, it fails to perform efficiently with a THD of 6.13% and 5.29% which is much higher as compared to the proposed technique's THD of 1.04% and 1.30%, respectively. Moreover, the comparative analysis between the state-of-the-art and the proposed SRPE-DQ technique also reflects the dominance of the proposed technique by showing its harmonic robustness, minimum passive component count, and excellent THD profile. The experimental findings demonstrate that the suggested approach is extremely successful at maintaining the target load voltage stable when the grid voltage sags/swell, distortions, and imbalances occur. In experimental work, for safety purposes and due to the limitation of resources, the input source voltage was set to be 100 V_{rms} (line-to-line), which is supplied by a programmable AC source. Although the SRPE controller performs effectively for the DC-AC converter under the grid voltage variations until now no proper optimization has been designed for the damping factor value, which may restrict the improvisation of the controller. A future study might examine using the suggested DC-AC converter/DVR control mechanism to improve the power quality of grid-connected and/or islanded microgrids.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

E	$E(s)$	phase error of the PLL
F	$F(s)$	loop filter's transfer function for PLL
K	k_p	proportional gain of the PI controller for PLL
	k_i	integral gain of the PI controller for PLL
	k_{PE}	phase detector gain for PLL
	k_{VCO}	voltage-controlled oscillator gain for PLL
U	U_{xy}	instantaneous input signals for synchronous reference framework
	$u_{g\_\alpha\beta}$	input signals in the $\alpha\beta$ domain for SRPE
	V_{xy}	instantaneous output signals for synchronous reference framework
V	v_{g_abc}	three-phase grid voltages
	v_{g_dq}	grid voltages in dq-frame
	$v_{g\_\alpha\beta}$	grid voltages in $\alpha\beta$-frame
	$v_{g\_\alpha\beta(fun)}$	fundamental components of grid voltages in $\alpha\beta$-frame
	$v_{g\_\alpha\beta(dis)}$	disrupted components of grid voltages in $\alpha\beta$-frame
	v_{std}	generated three-phase standard voltage signals
	v_{std_dq}	generated three-phase standard voltage signals in dq-frame
	v_{load_dq}	load voltages in dq-frame
	v_{inj_abc}	DC-AC converter/DVR's three-phase injected voltages
Greek and others	ζ	damping factor for SRPE
	ω_c	cut-off frequency for SRPE
	$\sin(\omega t)$	synchronizing elements generated by SRPE
	$\cos(\omega t)$	synchronizing elements generated by SRPE

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